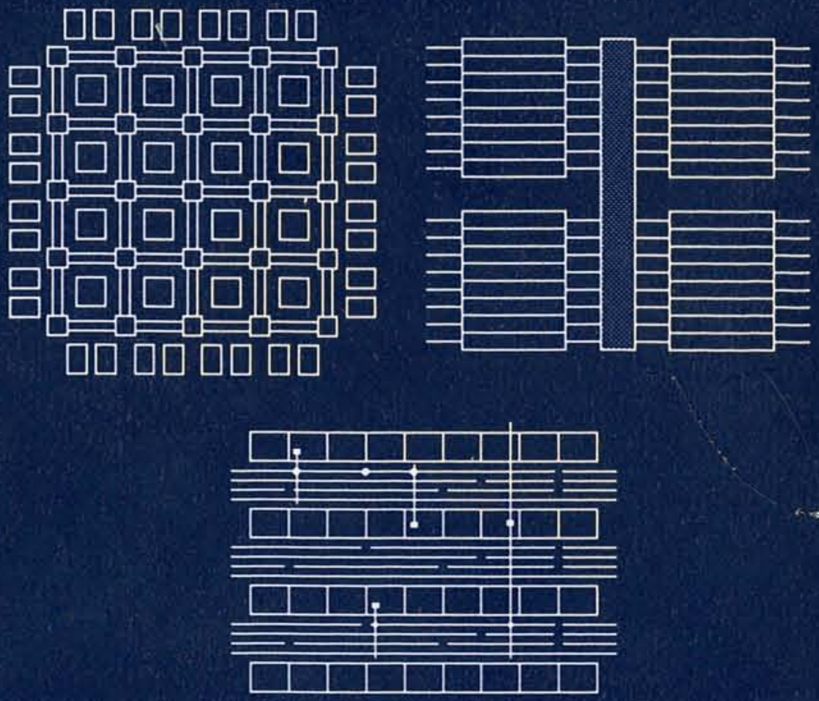
FIELD-PROGRAMMABLE GATE ARRAY TECHNOLOGY



edited by

Stephen M. Trimberger

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Stephen M.
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The Technical Staff o
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Robert H

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nets and paths with maximum delay values. These constraints can be provided as annotation in the schematic or in a separate design constraints file.

Manual intervention in FPGA partitioning can take the form of a CLBMAP, a schematic-level constraint that forces the partitioner to accept a user-defined mapping for part of the logic. The CLBMAP is a cell in the library that a designer connects in parallel with the logic it is mapping. The CLBMAP represents no logic, but its connections are used to guide the partitioner to implement the mapped logic in a single CLB. A designer can go further, designing in terms of CLBs with their programming.

The XACT Design Editor (XDE) (figure 2.4.6) is an interactive graphical editor similar in concept to MPGA wiring editors. XDE contains both the logical and physical descriptions of the design. Users modify both descriptions simultaneously as they design the circuit. A designer can use XDE to pre-place and route CLBs or to do post-placement and routing fixup. XDE can also be used as a complete design system, allowing a designer to map the logic manually onto the device. XDE can accept a netlist as input, or a design can be created and implemented completely in XDE.

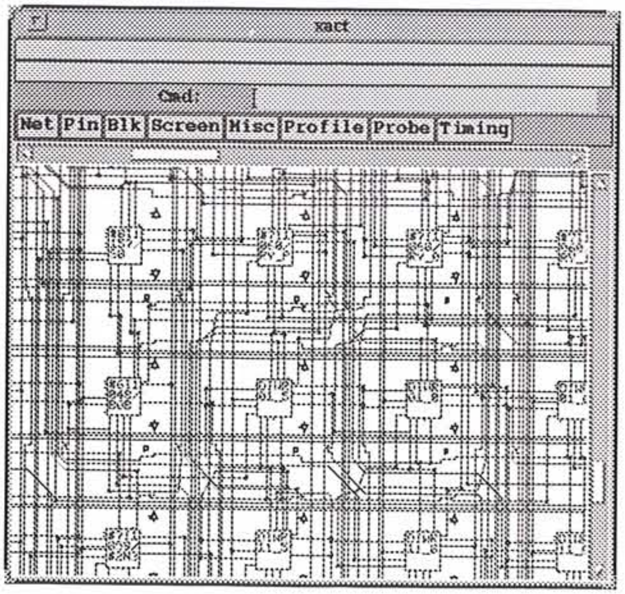

Figure 2.4.6. XDE Screen.

XDE includes the checking and editing functions required for manual design, including a design rules checker, a timing verifier and a router. XDE allows a designer to turn on or off individual pips in the interconnect, to set the functionality of function tables, and to control the functions in CLBs and IOBs.

XDE provides the front-end interface to the c
simple modifications of the design. It includes
internal signals routed out to unused pads to al
for debugging a design. The probe modificatio
version of the design that is then loaded into th
probe points separately from the base design, so
prototype debugging is complete.

2.5. The Future

FPGAs are similar to MPGAs in many respects,
that a researcher can draw upon to apply in thi
architecture is large and relatively unexplored,
research. These unexplored areas may eventuall
terms of density and performance. Since softwa
software questions will opened or re-opened by I

Programming Technology

The CPLD-style array architectures, built with
cannot be scaled beyond thousands of gates of
quadratically, as does static power consumptio
capacity EPROM devices show significantly
devices, as well as massive power requireme
consumption requires a multi-level logic org
architectures described in this chapter. EPROM
built in large arrays, so they become inefficient in
to extend EPROM-based architectures to large
section into a straightforward memory array, an
FPGA, basically building an SRAM FPGA with

Large antifuse-programmed devices rely on v
themselves. A single ten-thousand-gate antifu
million antifuses. Although only a few percent v
architecture relies on those few percent being
FPGA will fail to program correctly, and must b
fail to program is not a serious issue with sma
dollars and programming yield is above 99 per
cost hundreds of dollars and the programming yi
that customers will accept discarding 20% of
antifuse manufacture limits the size of antifuse-b

SRAM-programmed devices have none of thes
technology improvements and have very low po
with very high quality and fully tested at the facto