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Boubezari et al.

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(54) **METHOD FOR TESTABILITY ANALYSIS AND TEST POINT INSERTION AT THE RT-LEVEL OF A HARDWARE DEVELOPMENT LANGUAGE (HDL) SPECIFICATION**

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(58) **Field of Search** 716/18, 4

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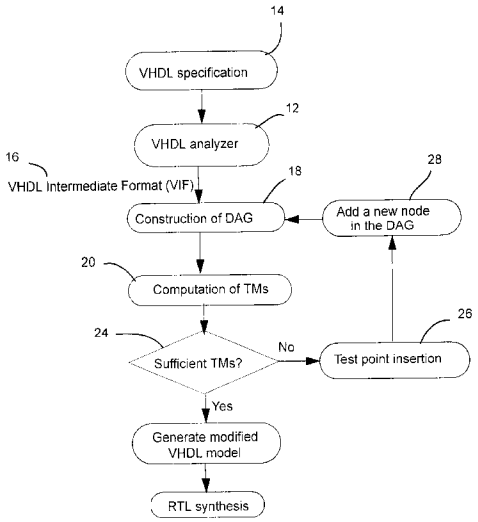
(57) **ABSTRACT**

A method is provided for producing a synthesizable RT-Level specification, having a testability enhancement from a starting RT-Level specification representative of a circuit to be designed, for input to a synthesis tool to generate a gate-level circuit. The method includes the steps of performing a testability analysis on a Directed Acyclic Graph by computing and propagating Testability Measures forward and backward through VHDL statements, identifying the bits of each signal and/or variable, and adding test point statements into the specification at the RT-Level to improve testability of the circuit to be designed. The computation of Controllability and Observability method is purely functional, and does not subsume the knowledge of a gate-level implementation of the circuit being analyzed.

36 Claims, 7 Drawing Sheets



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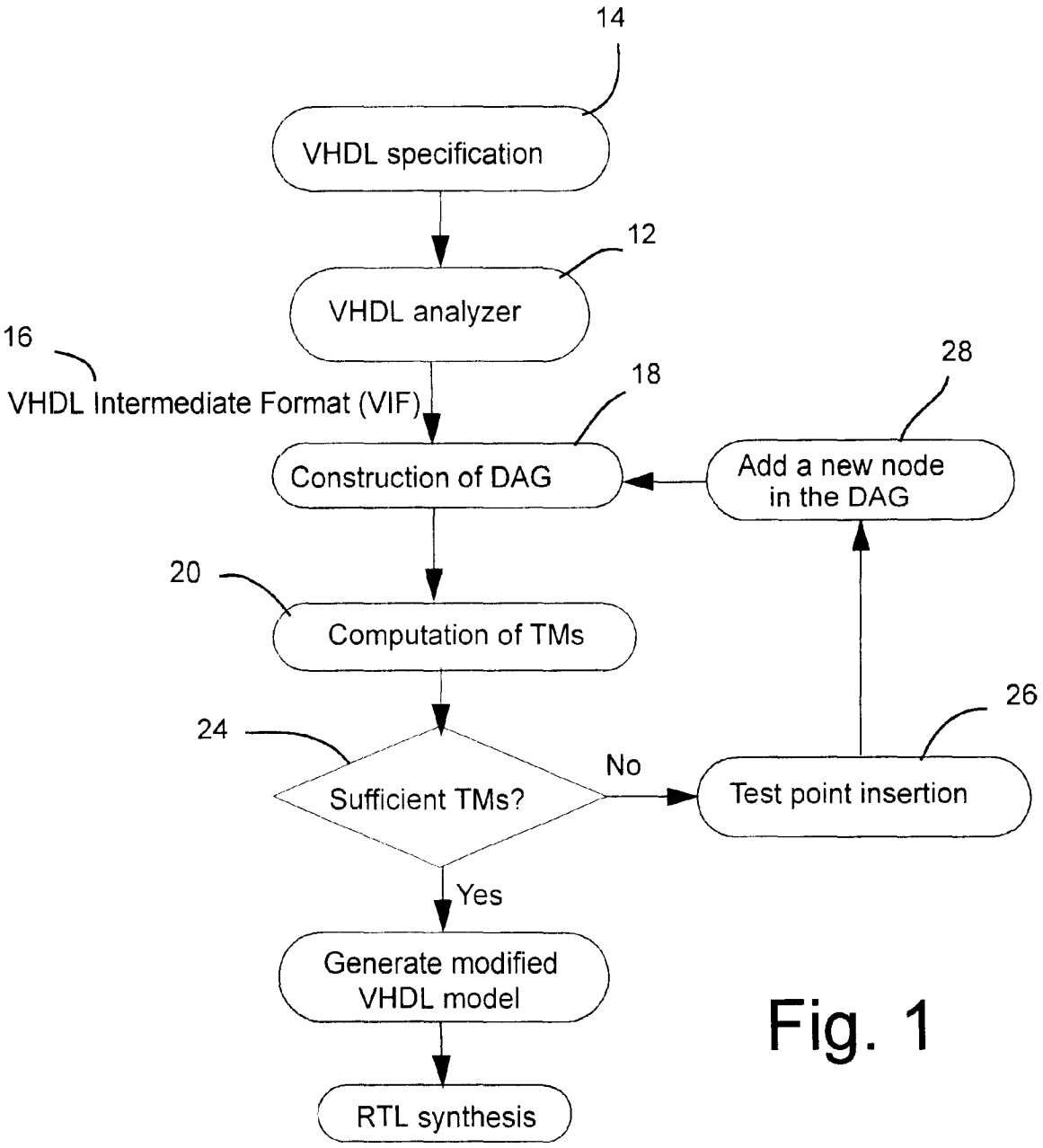

Fig. 1

```
entity MOORE is              -- Moore machine
  port(X, CLOCK: in BIT;
       Z: out BIT);
end;
architecture BEHAV of MOORE is
  type STATE_TYPE is (S0, S1, S2, S3);
       signal  CURRENT_STATE,  NEXT_STATE:
STATE_TYPE;
begin
  -- Process to hold combinational logic
  COMBIN: process(CURRENT_STATE, X)
  begin
    case CURRENT_STATE is
      when S0 =>
        Z <= '0';
        if X = '0' then
          NEXT_STATE <= S0;
        else
          NEXT_STATE <= S2;
        end if;
      when S1 =>
        Z <= '1';
        if X = '0' then
          NEXT_STATE <= S0;
        else
          NEXT_STATE <= S2;
      when S2 =>
        Z <= '1';
        if X = '0' then
          NEXT_STATE <= S2;
        else
          NEXT_STATE <= S3;
        end if;
      when S3 =>
        Z <= '0';
        if X = '0' then
          NEXT_STATE <= S3;
        else
          NEXT_STATE <= S1;
        end if;
    end case;
end process COMBIN;
-- Process to hold synchronous elements (flip-
flops)
  SYNCH: process
  begin
    wait until CLOCK = '1';
    CURRENT_STATE <= NEXT_STATE;
  end process SYNCH;
end BEHAV;
```

Fig. 2

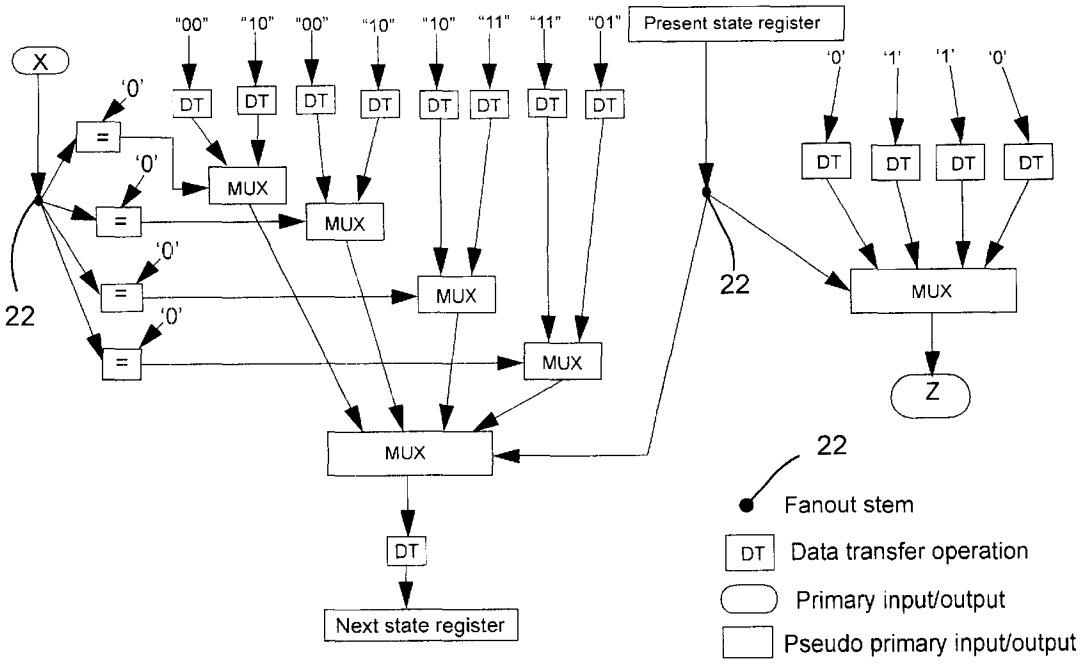

Fig. 3

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