

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

In re U.S. Patent No. 6,947,882	Trial No.	IPR 2012-00041
Application No.:		
Filed: Sept. 24, 1999		
Issued: Sept. 20, 2005	Atty. Dkt. No.	007121.00005
Inventors: Frederic Reblewski Olivier Lepape Jean Barbier		
Patent Owner: Mentor Graphics Corporation		
For: REGIONALLY TIME MULTIPLEXED EMULATION SYSTEM		

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PRELIMINARY RESPONSE BY PATENT OWNER
UNDER 37 C.F.R. § 42.107

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Patent Owner Mentor Graphics Corporation (hereafter “Patent Owner”) hereby respectfully submits this Preliminary Response to the Petition seeking *inter partes* review in this matter. This filing is timely under 35 U.S.C. § 313 and 37 C.F.R. § 42.107, as it is being filed within three months of the September 28, 2012 mailing date of the Notice granting the Petition a filing date of September 26, 2012.

A trial should not be instituted in this matter as none of the references relied upon by Petitioner in its Petition gives rise to a reasonable likelihood of Petitioner prevailing with respect to a challenged claim of the U.S. Patent No. 6,947,882 (the ‘882 patent), either alone or in any combination with each other.

I. There Is No Reasonable Likelihood of Petitioner Prevailing As To A Challenged Claim of the ‘882 Patent

“The Director may not authorize an *inter partes* review to be instituted unless the Director determines that the information presented in the petition filed under section 311 . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged” 35 U.S.C. § 314(a). As discussed below, all the anticipation rejections proposed in the Petition are deficient for failing to set forth each and every feature arranged as recited by the respective claims of the ‘882 Patent, and thus do not establish a *prima facie* case of anticipation.

Further, all the obviousness rejections proposed in the Petition lack articulated reasoning with a rational underpinning to support a legal conclusion of obviousness. *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). Indeed, the Petition barely provides

“mere conclusory statement[s]” (*id.*) that the claims are obvious, let alone provide cogent reasoning as to why a person of ordinary skill in the art would modify or combine the cited documents in the manner recited by the respective claims of the ’882 Patent. *See, e.g.*, Petition at 13-14: “At a minimum, these claims would have been obvious to a person of ordinary skill in the art in view of [cited document].”

For at least these reasons, the Petition does not show a reasonable likelihood of prevailing with respect to even a single one of the challenged claims, and *inter partes* review should not be instituted.

A. Technology Background

The ’882 patent concerns emulation systems for emulating integrated electrical circuit designs. As described in the Background section of the patent, “[a] circuit design to be emulated is ‘realized’ on the emulation system by compiling a ‘formal’ description of the circuit design, and mapping the circuit design onto the logic elements (LEs) of the FPGAs [field programmable gate arrays] and the routing chips.” ’882 patent (SYNOPSISYS 1001) at 1:17-20.

Time multiplexing of multiple logical signals onto a single pin is a technique that had previously been used to reduce the number of interconnects required between FPGA chips and routing chips of the emulation system, including input/output pins on the chips. The challenged claims of the ’882 patent are directed to emulation systems that overcome shortcomings in the known emulation systems employing time multiplexing of signals.

In particular, the known systems were constrained by virtue of the clocking architectures they employed. Systems such as the “Virtual Wires” system described in the Babb et al. article discussed in the Background section of the ’882 patent employed a single clock globally distributed throughout the system and used for both clocking the user design (emulation clock) and routing the signals over the

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