Sterne Kessler Goldstein Fox
ATTORNEYS AT LAW

Intellectual Ventures Management, LLC
v.
Xilinx, Inc.

IPR2012-00023

DEMONSTRATIVES OF PETITIONER
Intellectual Ventures Management, LLC

Hearing: November 7, 2013

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'609 Patent Claim 1

1. A capacitor in an integrated circuit ("IC") comprising:

a core capacitor portion having a first plurality of conductive elements electrically connected to and forming a first part of a first node of the capacitor formed in a first conductive layer of the IC and a second plurality of conductive elements electrically connected to and forming a first part of a second node of the capacitor formed in the first conductive layer, the first plurality of conductive elements alternating with the second plurality of conductive elements in the first conductive layer, and a third plurality of conductive elements electrically connected to and forming a second part of the first node formed in a second conductive layer adjacent to the first conductive layer, at least portions of some of the second plurality of conductive elements overlying and vertically coupling to at least portions of some of the third plurality of conductive elements;

a shield capacitor portion having a fourth plurality of conductive elements formed in at least the first conductive layer of the IC, the second conductive layer of the IC, a third conductive layer of the IC, and a fourth conductive layer of the IC, the first conductive layer and the second conductive layer each being between the third conductive layer and the fourth conductive layer, the shield capacitor portion being electrically connected to and forming a second part of the second node of the capacitor and surrounding the first plurality of conductive elements and the third plurality of conductive elements; and

a reference shield electrically connected to a reference node of the IC other than the second node of the capacitor, the shield capacitor portion being disposed between the reference shield and the core capacitor portion.

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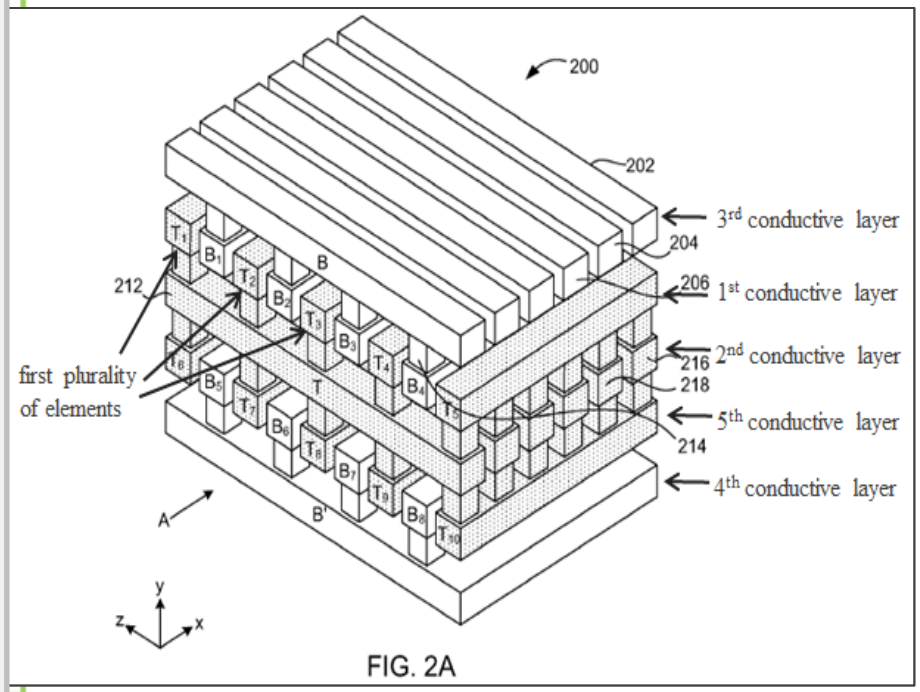

FIG. 2A

Petition, at p. 5 (annotated FIG. 2A from '609 Patent)

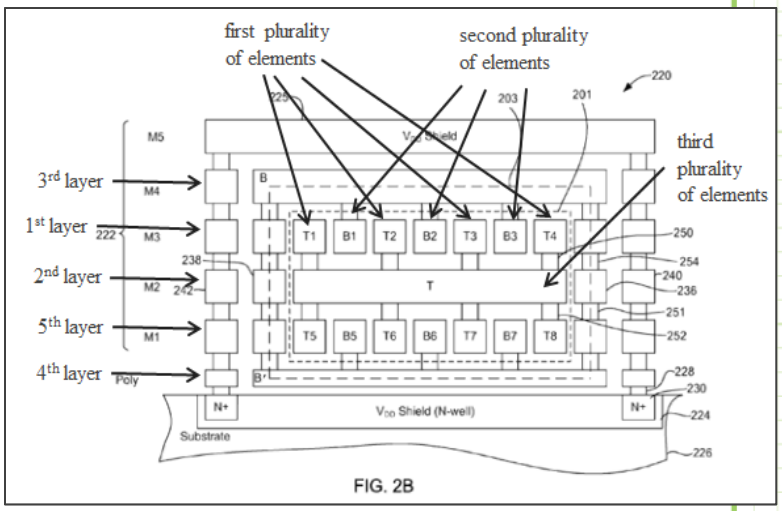

FIG. 2B

Petition, at p. 5 (annotated FIG. 2B from '609 Patent)

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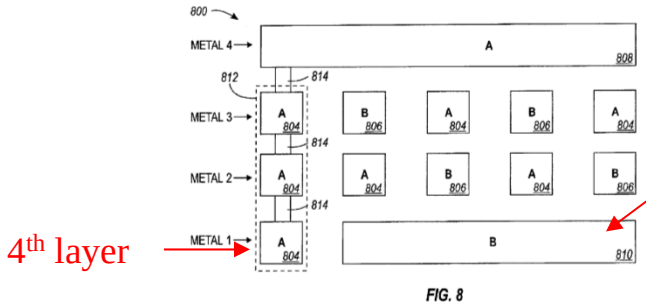
Forming the fourth conductive layer out of poly would have been obvious

2. The capacitor of claim 1 wherein the third conductive layer is a metal layer of the IC and the fourth conductive layer is a poly layer of the IC, the shield capacitor portion including a first node shield plate formed in the metal layer from a plurality of metal stripes and a second node shield plate formed in the poly layer.



Paul, FIG. 8 (annotated)

Pet. Reply at 2

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3 4

FIG. 3B is a cross-section of the capacitor of FIG. 3A.
FIG. 4 is a cross-section of a capacitor with increased spacing to the additional shielding layers.
FIG. 5 is a block diagram of a capacitor with extended fingers.
FIG. 6 is a block diagram of a capacitor with extended fingers.
FIG. 7A is a block diagram of a capacitor array with common inner-terminal fingers.
FIG. 7B is a cross-section of a capacitor in the array of FIG. 7A.
FIG. 7C is an electrical schematic diagram of the capacitor array of FIG. 7A.
FIG. 8A is a block diagram of an array terminating capacitor with terminated fingers at one end of a capacitor array.
FIG. 8B is a block diagram of an array terminating capacitor with extended fingers at one end of a capacitor array.
FIG. 9A is a block diagram of an array terminating capacitor with extended fingers at one end of a capacitor array, the extended fingers coupled to a common terminal.
FIG. 9B is a block diagram of an array terminating capacitor at one end of a capacitor array, the capacitor having fingers connected via a secondary finger extending perpendicular to the fingers.

DETAILED DESCRIPTION OF THE INVENTION

A description of preferred embodiments of the invention follows.

It is increasingly desirable to minimize the power consumption of electronic circuits. One means of reducing power consumption is to reduce the size of capacitors used in the circuits, thus representing signals with smaller charge quantities. In this case it is desirable to produce capacitors with very small values, while retaining good matching and well-controlled ratios. While the unit-capacitor matching method discussed above is well-suited to large capacitor values, it is less effective when the desired unit capacitor requires a small number of fingers and L_f approaching the process's minimum dimensions. In this case the end effects become more significant, resulting in poor matching, less-predictable capacitance, and greater overall capacitance variation batch-to-batch. MIM capacitor designs which provide very small capacitance values with good matching, well-controlled ratios, and small batch-to-batch variability would therefore be desirable.

In many circuit designs it is desirable to minimize the so-called "parasitic" capacitance between capacitor terminals and other circuit nodes. Parasitic capacitance to circuit commons ("ground") can cause increased circuit noise and reduced circuit speed. Parasitic capacitance to other circuit nodes can give rise to errors due to noise and un-intended signal coupling. It would therefore be desirable to provide a MIM capacitor design with minimized capacitance to ground and with shielding from other circuit nodes.

Embodiments of the present invention provide MIM capacitors with each of the desirable properties just enumerated. The first feature of this invention provides near-elimination of parasitic capacitance and near-perfect shielding at one capacitor terminal.

This embodiment is explained with the aid of FIGS. 2A and 2B. Consider first the interdigitated MIM capacitor 200 depicted in FIG. 2A. Here, first terminal 21 extends to a plurality of fingers 27, the outermost of which are extended and wrapped around the lower corners of these extensions are identified as 29. Further, two additional layers of metal are 23 and 24, covering the finished area in section along II-II' in FIG. 2D shows plates 23, 24 more clearly. They are electrical terminal 21 by vias, such as vias 29, the area shown.

The effect of these new features is to encircle terminal 22, including fingers 28 in both horizontal and vertical directions provide shielding in the vertical direction gers and other elements of terminal 2 shielding. This terminal 22 is provided shielding from both ground and other 22 has capacitance almost entirely to te ne-capacitance to any other circuit no terminal. 22 comprises [illegible] de rasitic rectangular capacitor area in FIG This shielding of one capacitor plate (22 here termed "self-shielding." In many c capacitor plate needs to have good shield capacitance: the self-shielding design satisfies these requirements.

For a given area, the capacitor 200 provides slightly higher capacitance tha FIGS. 1A and 1B, due to the added verti of plates 23 and 24 as well as the extra cuits 25 and 26. However, the dependen design parameters N_f and L_f, as expl remains valid. The three capacitance va C_f have different values due to the revis

For applications in which capacitor 1 be shielded, two additional metal layers in FIGS. 3A and 3B, to provide the need 3A, the entirety of FIG. 2A is repeated minals 31 and 32, corresponding to 21 and 34, corresponding to 23 and 24, are 36 is surrounded by a shield "wall" 37, and covered top and bottom by shield plates 35 and 36. A cross section along line C-C', as shown in FIG. 3B, shows the structure of the "wall" 37 and shield plates 35 and 36 relative to the capacitor 30. The vertical "wall" 37 is constructed of metal lines 39 in the three metal layers used by capacitor 30, plus rows of vias such as 38 connecting these lines and the top and bottom plates 35 and 36. This wall is penetrated by only one metal layer, carrying the connections to terminals 31 and 32 which are visible in FIG. 3A.

As an alternative to the use of a metal layer as shown in FIG. 3B (which may be needed for interconnect purposes) the bottom shield plate 36 can be implemented with a poly-silicon or diffusion layer. The minimum number of metal layers required to implement the fully-shielded capacitor of FIGS. 3A and 3B is nine layer.

With 37 and plates 35 and 36 provide effective shielding of terminal 31 from external circuit nodes. As a side effect, however, they add parasitic capacitance from terminal 31, and also a slight parasitic capacitance from terminal 32, to the shield, which is usually at ground potential. In contrast, the shielding of terminal 22 in FIGS. 2A and 2B is provided by terminal 21 itself (self-shielding) and adds no parasitic capacitance to terminal 22. Thus the added shielding for terminal 31 represents a compromise.

If additional metal layers, together with their inter-metal dielectric layers, are available, this added parasitic capacitance can be reduced. FIG. 4 shows cross sections (analogous to FIG. 3B) of such a structure. The use, mentioned above, of

"As an alternative to the use of a metal layer as shown in FIG. 3B (which may be needed for interconnect purposes) the bottom shield plate 36 can be implemented with a poly-silicon or diffusion layer."

Anthony, 4:49-52

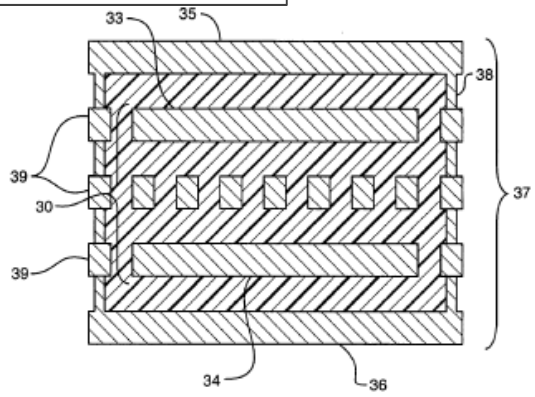

FIG. 3B

Anthony, FIG. 3B

Pet. Reply at 2-3 & 4-5

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