MORGAN T. JOHNSON

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PROFESSIONAL EXPERIENCE

Advanced Inquiry Systems Inc. – Hillsboro, Oregon **2002 – Present**

AISI is a venture funded, high tech startup based on my patented technologies covering full wafer, single touch down testing of chips. Full wafer contactors called Wafer Translators have recently met key milestones and are moving to production with a focus on NAND, NOR and DRAM full wafer, single touchdown test. Additionally, technologies for contacting flip-chip wafers (CPUs, GPUs and SoCs are examples) are progressing and will be shipping by early 2013

Morgan Johnson Technology – Portland, Oregon **2000 – 2001**

Informal Partnership with *SanDisk*, worked with head test engineers and managers, developed a full wafer contactor for use in wafer-level-burn-in and test for NAND memory wafers. This technology formed the basis for AISI.

Prototype Solutions (Phase II) – Beaverton, Oregon **1997 – 1999**

Developed a technology put forth in a 1994 DARPA proposal. One-hour turn laser personalized ceramic substrates were achieved. Laser scribing of isolated wires directly in thick-film gold over filled vias on a multilayer co-fired ceramic substrate was developed.

Prototype Solutions (Phase I) – Beaverton, Oregon **1994 – 1996**

Co-founded and served as Chief Technology Officer to develop and bring to market laser programmed, removable wiring to market as chip prototyping.

- **Contract with DRC (Design Research Corporation)** for a U.S. Navy Project requiring:
  - **Design and build** a moderate cost, near IR laser system to customize MCM scale and on-chip metal, multi-layer interconnect. The system laser spot delivery accuracy of +/- 1/10th micron “on-the-fly” was achieved.
  - **Innovation:** *Stacking, pressure connected, ceramic and organic substrates* - with memory, FPGA and DSP packaged and bare die. This stack was topped with a laser programmed wiring plate to interconnect all die with one-day turn, no tooling, no soldering and no substrate modification. *(All goals were met with exception of DSP die which could not be obtained).*
- **DARPA Contract:**
  - **Innovation:** *Laser programmed, removable multi-layer thin-film wiring* - Must connect a minimum of 2,048 pins with random net lists (accomplished).

Routing must be 100% with any net list (accomplished). It must take less than one hour to route and laser program (final, typical time was 20 min.).

- **Innovation:** *Inexpensive 100% open and short tester* - Must be accomplished in one hour. Tester did 100% test & reporting in 2 minutes for substrates up to 2,048 pins. Tester cost $3,200.
- **Innovation**: *Laser system for under $100,000* - (actual cost $92,000). System routinely programmed copper and gold thin-film metallization on break-link wiring plates with organic dielectrics. These 68mm square substrates had two or three metal layers with BCB or polyimide dielectrics.
- **Innovation**: *8 Ceramic plates and a wiring plate pressure connected* – Stack contained over 80,000 pressures connected lapped gold pads. Contract required the stack to be assembled and disassembled 200 times without degradation of signals. Proof cycles took one entire day and passed.
- **Innovation*: 3D-i**, a patented, solder ball based stacking board-to-board connectors* - Co-invented, patented and developed with Dave Ekstrom, a unique low cost board to board connector that enables board stacking with high connection numbers between several boards. Test structure design used over 34,000 solder solid core solder balls, which were reflowed in one operation. 3D-I patent has issued.

Morgan Johnson Technology – Portland, Oregon **1989 – 1993**

- **Formalized Partnership:** *Mentor Graphics* – formed with MJTech to develop removable laser programmed wiring for use in conjunction with FPGAs to build low cost, quick-turn chip emulators.
- **Formalized Partnership:** *TriQuint Semiconductor* – formed with MJTech to develop one-day turn custom GaAs ASIC chips. They supplied desk and lab space on their site, phone service, clerical service and FAB.

Morgan Johnson Technology – Palo Alto, California **1988 – 1989**

- Continued a version of single mask programmed arrays. In one project for Adaptec networking chip set development turned a gate array design 8 times in 8 days prior to a critical industry conference and show proving how fast development and in-system debug could be accomplished.

Innovation: *laser programmed, removable wiring* - for quick-turn MCMs and PCBs.

LaserPath Corporation – Sunnyvale, California **1983 – 1987**

Founder and Chief Technology Officer**.** *A venture funded high tech startup based on my inventions and patents. Investors included Eugene Kliener of Kliener, Perkins, Caulfield, Byre, General Electric Venture Capital, Crosspoint Ventures, and James D. Wolfenson.* Laser Programmed, “Same Day” and five business day delivery of custom chips when universal current practice was 12 weeks committed and about 16 to 24 weeks actual.

- **FORMAL PARTNERSHIP: General Electric Corporation** adopted the chip process as their corporate standard for internal development of electronics world wide and issues a press release to that effect.
- **FORMAL PARTNERSHIP: General Electric Semiconductor** contracted as our foundry and manufactured our wafers that were the Gate Arrays we laser customized.
- **Innovation:** *Laser programmable semicustom gate arrays* **–** done at the wafer level, with same functionality as masked programmed chips, same gate and logic structure, same I/O cell options, same chip package options. This was the first commercial application of laser based random logic creation. *Formed Partnership with General Electric* – GE agreed to act as foundry for LaserPath wafers in return for rights to use the technology company-wide for any project needing custom chip.
- **Innovation:** *Single Mask Programming of Custom Chips* – Metal 1, Via, Metal 2 and Pad Mask were replaced in customization with a single "Break-Mask". Allowed an entire wafer to be customized with one mask. Photo masks were being delivered in three weeks when the project was undertaken – we were able to reduce photo mask delivery to 8 hours without a time premium.
- **Three Patents:** issued (one Canadian) covering laser and single mask programmed chips, MCMs and PCBs.
- LaserPath had twice the design wins in its first year as any previous custom chip supplier. 200 custom chip designs were each delivered in 5 business days – *only one was late (1/2 of one percent) versus typical industry practice of 25 to 30% late.* Customers included Intel, IBM, Compaq, Hughes, Honeywell, and Rockwell, 11 groups inside AT&T, Bell Labs, General Electric, Adaptec, Xerox and RCA.

Hewlett Packard – Corvallis, Oregon **1980 – 1982**

Joint Project, HP-41C Handhelds. HP's 41C product line could not be easily used "in-the-field" by surveyors, contractors, field researchers and other professionals requiring printing and weather protection.

- **Innovation:** *Conversion Kit and Case* – Converted separate parts into unified, robust portable system with printer and storage for accessories and supplies. Shown in HP's booth at the Consumer Electronics Show in Las Vegas. Officially endorsed by HP Corvallis for use with any elements of the 41C product line**.** Sold by HP's largest distributor, Government Marketing Services from 1980 – 1984**.** Manufactured and assembled by MJDesign.

Cray Computer – Boulder Colorado **1980 – 1981**

Funded research to develop Laser Programmed MCMs for Cray II Scientific Super Computer System.

- **Innovation:** *Laser programmed PCBs* – that could be customized on-site, as needed using existing laser trim systems – Cray anticipated 1,400 designs per machine on common unprogrammed format.

- **Innovation:** *Laser Programmable MCM structures* - 2 mil lines/spaces, plated 2 mil post vias on Al heat sink carrier, wire bonded bare die ECL, one Gig clock – developed jointly with PakTel, San Diego, CA.
- **Innovation**: *Laser Programmed ECL On-Chip Wiring* – initial development of laser link blowing patterns to program ECL logic, route signals and deliver power and ground. First look at on-chip metal link blowing with ESI Model 80 Laser Memory Repair System.

Morgan Johnson Design – Denver, Colorado **1977 – 1979**

High Tech Consulting.

- Designed science education products with focus on energy use issues.
- **Innovation:** *Invented laser programmed interconnect* – June, 1978 – applications at PCB, hybrid, MCM, single chip package and on-chip metallization levels.
- **Innovation:** *3D-laser programmable circuit structures* – with 2D-laser access. Designs had the capability to route signal, ground and voltage creating virtual coax wiring.

PATENTS

I have 36 issued patents, about 12 patents pending, about 9 foreign patents pending and over 30 patents in draft as of September 2012.

EDUCATION

B.S. Graphics, University of Oregon, Eugene, OR, 1960-63 & 65.
Industrial Design, Art Center College of Design, Pasadena, CA, 1964.