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Brennan

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(54) **SHIELDED PLANAR CAPACITOR**

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(52) **U.S. Cl.** **361/306.1**; 361/306.3; 361/321.2; 361/308.1; 361/311; 361/313
(58) **Field of Search** 361/306.1, 306.3, 361/308.1, 309, 311, 373, 321.1, 321.2, 321.6, 301.2, 303, 328, 330, 525

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(57) **ABSTRACT**

A shielded planar capacitor structure (202) is discussed, formed within a Faraday cage (210) in an integrated circuit device (200). The capacitor structure (202) reduces parasitic capacitances within the integrated circuit device (200). The capacitor (202) comprises a capacitor stack (102) formed between a first and second metal layers (230,232) of the integrated circuit. The capacitor stack (102) has a first conductive layer formed from a third metal layer (106) disposed between the first and second metal layers (230,232) of the integrated circuit, a dielectric isolation layer (110) disposed upon the first conductive layer (106); and a second conductive layer (112) disposed upon the dielectric isolation layer (110) and overlying the first conductive layer (106). The structure (202) further has a first and second isolation layers (104,114) disposed upon opposite sides of the capacitor stack (102). The Faraday cage (210) is formed between the first and second metal layers (230,232) of the integrated circuit (200), comprising a first and second shield layers (402,414) each having a plurality of mutually electrically conductive spaced apart traces (404). The first and second isolation layers (404,414) and the capacitor stack (102,434) are sandwiched between the first and second shield layers (402,414). Conductive elements (432) are distributed around the periphery of the capacitor stack (102,434) and the first and second isolation layers (404,412). The conductive traces (424) of the first shield layer (402) are connected to the conductive traces (424) of the second shield layer (414) through the conductive elements (432).
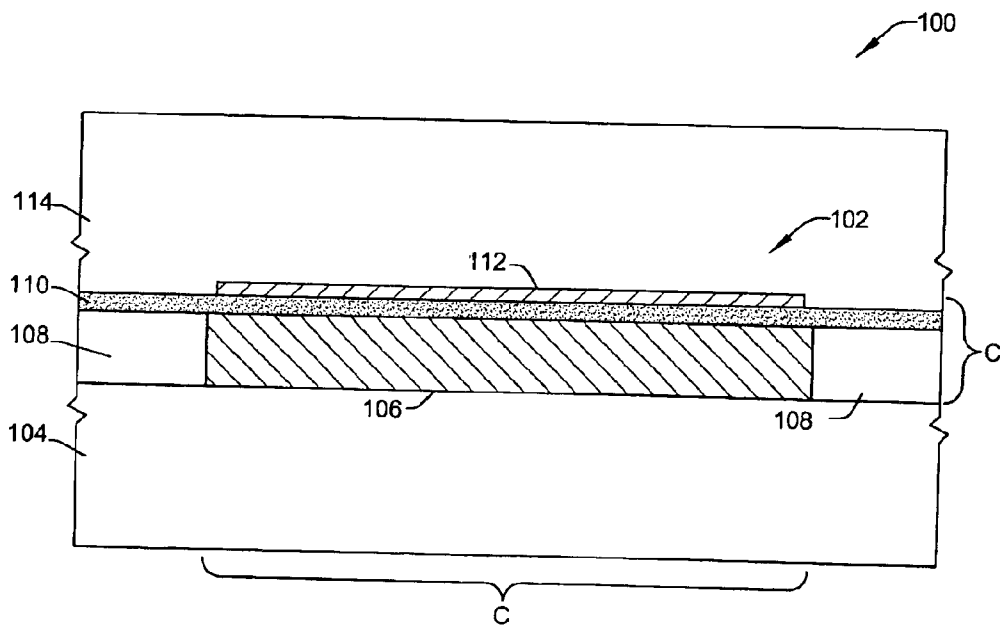
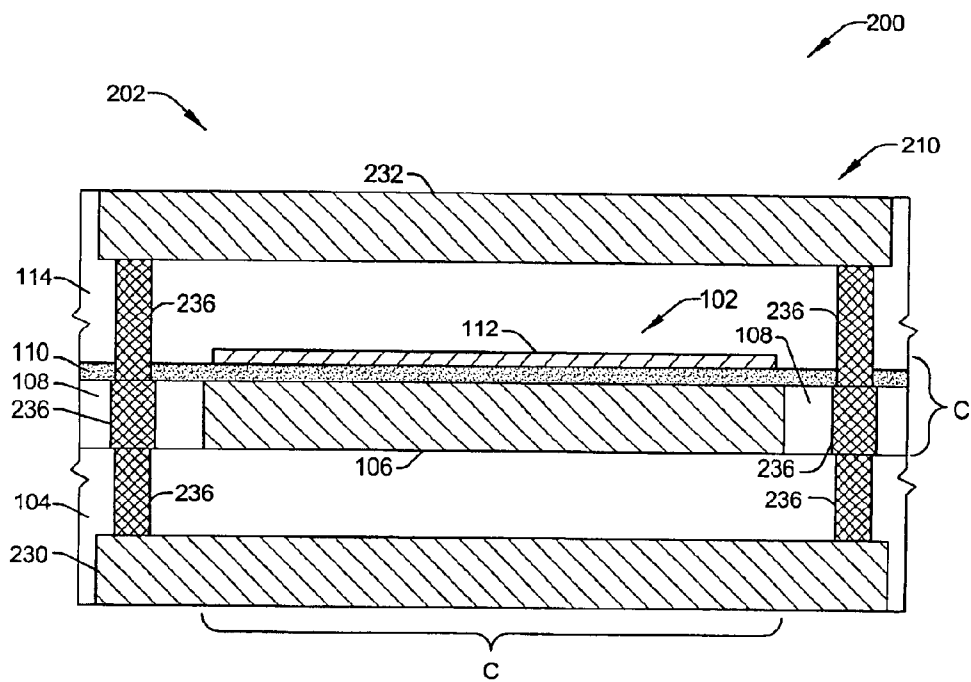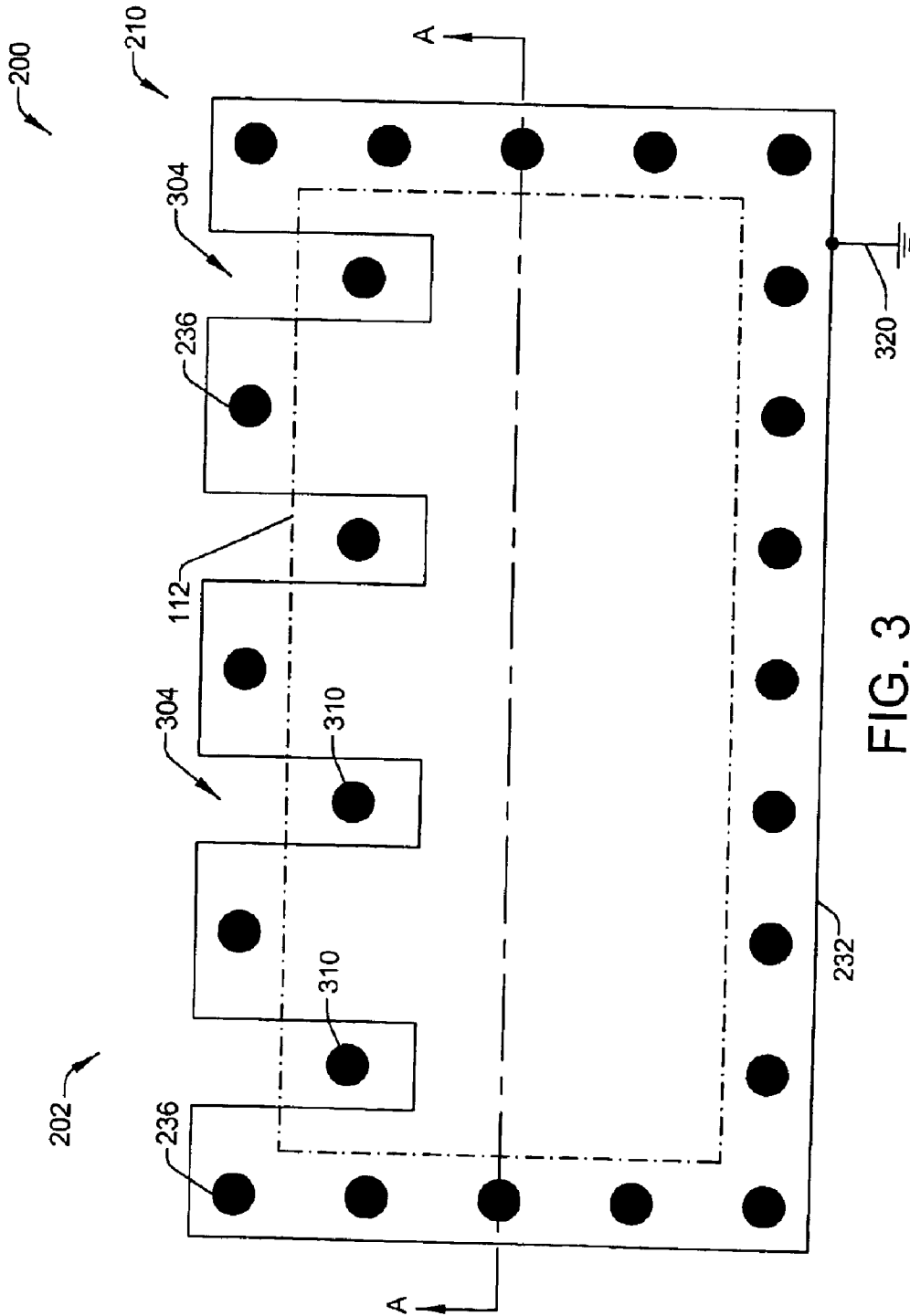**32 Claims, 5 Drawing Sheets**
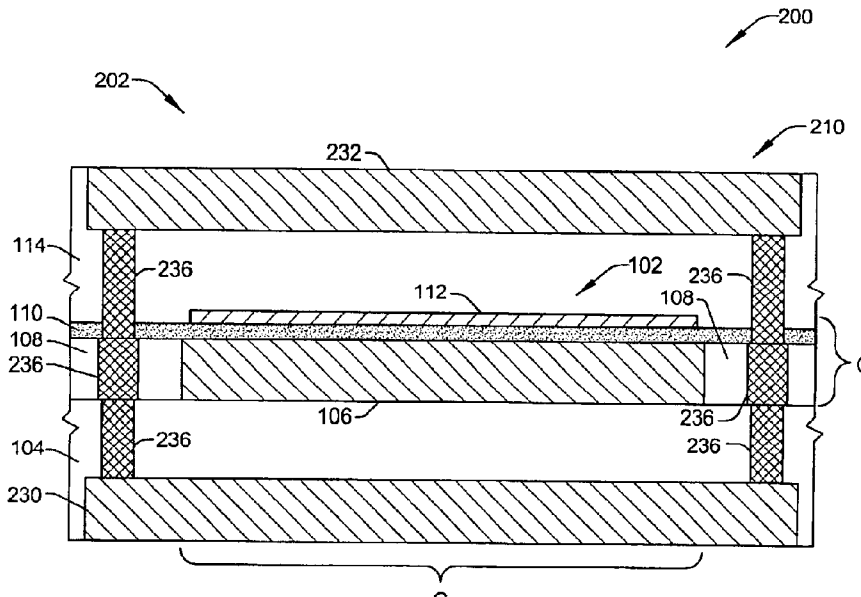
FIG. 1

FIG. 2

FIG. 3

FIG. 4

DOCKET ALARM
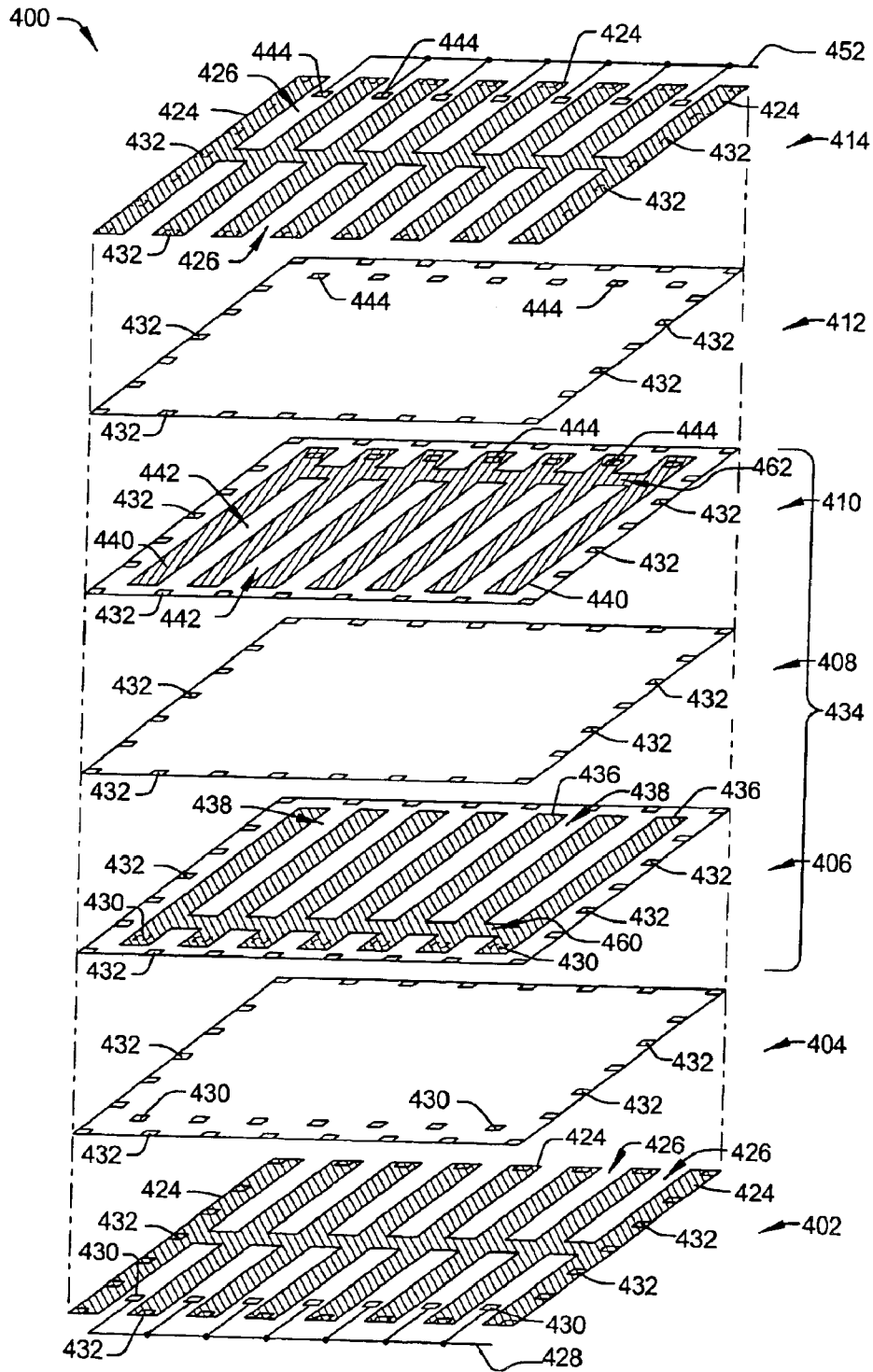
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