SHIELDING FOR INTEGRATED CAPACITORS

RELATED APPLICATIONS

[0001] This patent application is being concurrently filed with commonly owned U.S. Patent Application entitled INTEGRATED CAPACITOR WITH TARTAN CROSS SECTION by Patrick J. Quinn; and with commonly owned U.S. Patent Application entitled INTEGRATED CAPACITOR WITH INTERLINKED LATERAL FINS by Patrick J. Quinn; and with commonly owned U.S. Patent Application entitled INTEGRATED CAPACITOR WITH CABLED PLATES by Patrick J. Quinn; and with commonly owned U.S. Patent Application entitled INTEGRATED CAPACITOR WITH ARRAY OF CROSSES by Patrick J. Quinn; and with commonly owned U.S. Patent Application entitled INTEGRATED CAPACITOR WITH ALTERNATING LAYERED SEGMENTS by Jan L. de Jong et al., the disclosures of which are each hereby incorporated by reference in their entireties for all purposes.

FIELD OF THE INVENTION

[0002] The present invention relates to capacitors formed in integrated circuits ("ICs") commonly referred to as integrated capacitors.

BACKGROUND

[0003] Methods of fabricating ICs typically include a front-end sequence of processing, in which various electrical devices such as transistors are formed in a semiconductor substrate, and a back-end sequence of processing, generally including forming alternating layers of dielectric material and patterned conductive material (typically metal) with conductive vias or other techniques being used to interconnect the metal layers to form a three-dimensional wiring structure that connects electrical devices to other electrical devices and to terminals of the IC.

[0004] Capacitors are used in IC systems for a variety of purposes. In many instances, it is desirable to incorporate (integrate) a capacitor in the IC chip. A simple approach is to form two conductive plates with an intervening dielectric; however, this consumes a relatively large area for the capacitance obtained. One technique for increasing the capacitance of a given area is to use multiple conductive plates, each

conductive plate separated from the proximate plate(s) by dielectric. Further techniques use conducting strips, also called conductive lines, conductive fingers, or conductive traces, that are alternately connected to the first and second capacitor terminals (nodes). Sidewall coupling between the conductive strips provides capacitance. Layers of conducting strips, either offset or arranged in vertical congruency, can be added to further increase the capacitance of an integrated capacitor structure.

[0005] One capacitor has a number of conductive strips in successive layers connected to the first node alternating with an equal number of conductive strips connected to the second node of the integrated capacitor. The conductive strips are offset a half cell on successive layers, so that a conductive strip connected to the first node has conductive strips connected to the second node above and on both sides of it. Providing an equal number of conductive strips in a layer for each node balances the coupling of each node to the substrate, which is desirable in some applications, but undesirable in others, such as switching applications where it is desirable to have less coupling at one node. In order to reduce coupling to the substrate, a thick layer of silicon dioxide is used between the substrate and the first layer of conductive strips. This may be difficult to integrate in a standard CMOS fabrication sequence and might require additional steps to be added to the standard process flow. The overlapping parallel conductive strips are connected at their ends using buss strips that consume additional surface area.

[0006] Another approach to providing an integrated capacitor is to have conductive strips in a layer connected to alternate nodes of the capacitor with overlapping conductive strips connected to the same node. This forms essentially a curtain of conductive strips and interconnecting vias connected to the first node of the capacitor with adjacent curtains of conductive strips and interconnecting vias connected to the second node. Overlapping conductive strips connected to the same node avoids the lost surface area associated with buss strips; however, inter-layer capacitance is reduced because the upper strip is connected to the same node as the lower strip. This effect is somewhat obviated because, as critical dimensions shrink, inter-strip capacitance becomes more dominant than inter-layer capacitance. In other words, the

dielectric layer separation between successive metal layers becomes increasingly greater than the dielectric separation between conductive strips with decreasing critical dimension.

[0007] Conventional integrated capacitors are often susceptible to electronic noise, which can affect the performance of the IC. In some applications, such as a filter capacitor application where one of the capacitor nodes (typically the bottom node) is connected to ground or to a power supply voltage, some degree of noise is often tolerable. However, in other applications, such as when the capacitor is used in a signal path (i.e., as a coupling capacitor or a switched capacitor), noise coupling can seriously degrade the performance of the circuit. Noise coupled onto a capacitor are particularly problematic when very low analog voltages are coupled through the capacitor, especially in a system on a chip, which often produce more electrical noise than other types of ICs, such as a memory chip. Thus, integrated capacitors providing better noise immunity are desired for used low-noise applications on an IC.

SUMMARY

[0008] A capacitor in an integrated circuit ("IC") includes a core capacitor portion having a first plurality of conductive elements electrically connected to and forming part of a first node of the capacitor formed in a first conductive layer of the IC and a second plurality of conductive elements electrically connected to and forming part of a second node of the capacitor formed in the first conductive layer. The first plurality of conductive elements alternates with the second plurality of conductive elements in the first conductive layer. A third plurality of conductive elements electrically connected to and forming part of the first node is formed in a second conductive layer adjacent to the first conductive layer, at least portions of some of the second plurality of conductive elements overlying and vertically coupling to at least portions of some of the third plurality of conductive elements. The capacitor also includes a shield capacitor portion having a fourth plurality of conductive elements formed in at least the first conductive layer of the IC, the second conductive layer of the IC, a third conductive layer of the IC, and a fourth conductive layer. The first and second conductive layers are between the third and fourth conductive layers. The shield

capacitor portion is electrically connected to and forms part of the second node of the capacitor and surrounds the first and third pluralities of conductive elements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Accompanying drawing(s) show exemplary embodiment(s) in accordance with one or more aspects of the invention; however, the accompanying drawing(s) should not be taken to limit the invention to the embodiment(s) shown, but are for explanation and understanding only.

[0010] FIG. 1 is a circuit diagram of a circuit using capacitors according to embodiments of the invention.

[0011] FIG. 2A is an isometric view of a portion of a shielded integrated capacitor suitable for use in embodiments of the present invention.

[0012] FIG. 2B is a side view of a integrated capacitor 220 in accordance with FIG. 2A.

[0013] FIG. 2C is a side view of the integrated capacitor according to FIG. 2A with a ground shield according to an embodiment.

[0014] FIG. 2D is a side view of the integrated capacitor according to FIG. 2A with an alternative ground shield according to another embodiment.

[0015] FIG. 3A is a side view of an integrated capacitor with a bottom node shield according to an alternative embodiment.

[0016] FIG. 3B is a partial cutaway plan view of the M5 and M4 layers showing a portion of the ground plate and underlying bottom node shield plate of FIG. 3A.

[0017] FIG. 4A is side view of an integrated capacitor with a bottom node shield according to yet another alternative embodiment.

[0018] FIG. 4B is a cross section of a shielded integrated thin-dielectric capacitor in an IC according to another embodiment.

[0019] FIG. 5 is a plan view of an FPGA incorporating an integrated capacitor according to an embodiment.

DETAILED DESCRIPTION

[0020] FIG. 1 is a circuit diagram of a circuit 100 using capacitors 102, 104

according to embodiments of the invention. The top node 108 of capacitor 104 is switchable to be connected to or disconnected from a high-impedance input 114 of amplifier 116. The top node 106 of the feedback capacitor 102 is also connected to the high-impedance input 114 of the amplifier 116 while the bottom node 110 is connected to output 118 of the amplifier 116. The feedback capacitor 102 is switchably shorted by closing switch 119. The coupling capacitor 104 has a top node 108 shielded by a bottom node shield 120 that essentially surrounds the top node 108 with conductive structures electrically connected to the bottom node and reduces parasitic capacitive coupling of the top node 108 to other nodes of the circuit 100. Connection to the top node 108 is made through a gap in the bottom node shield 120. Although the bottom node shield is shown as being contiguous, in some embodiments the bottom node shield is made up of several conductive elements, such as metal filaments, metal vias, and polysilicon or silicide plates or strips, to form a conductive cage around the top node, shielding the top node from electronic noise and from coupling to other nodes of the IC. In some embodiments, the bottom node shield contributes to the overall capacitance of the integrated capacitor by coupling to the top node. Note that a capacitor is generally thought of as a two terminal device, and the "top" and "bottom" nodes as described herein generally correspond to these two terminals of the capacitor. Thus, the structures described below may be thought of as connecting (e.g., electrically) to one or the other node, or forming portions or parts of a node. A node is not separate from the capacitive structures connected to it, but those structures may form portions of a node.

[0021] The feedback capacitor 102 has a top node 110 shielded by a bottom node shield 122, and by an optional reference shield 124. The reference shield 124 is connected to a relatively stable reference voltage present in the IC, such as analog ground, digital ground, or V_{DD}. The reference shield 124 essentially surrounds the bottom node shield 120 and shields the bottom node from substantially coupling to more than one voltage reference (e.g., the bottom node couples to V_{DD} or ground, but not both). In other embodiments, a reference shield partially surrounds a bottom node shield. The reference shield has a gap allowing electrical contact to be made to the bottom node, as described above.

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