IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *inter partes* review of: U.S. Patent 7,994,609 to Quinn Filed: Herewith For: **SHIELDING FOR INTEGRATED CAPACITORS**	Atty. Docket: 3059.701IPR0

Declaration of Morgan Johnson
in Support of Petition for *Inter Partes* Review of U.S. Patent No. 7,994,609

I, Morgan Johnson, declare as follows:

1. I have been retained by Sterne, Kessler, Goldstein, and Fox PLLC on behalf of Intellectual Ventures Management, LLC ("Intellectual Ventures Management") for the above-captioned *inter partes* review proceeding. I understand that this proceeding involves U.S. Patent No. 7,994,609 ("the '609 Patent") entitled "Shielding for Integrated Capacitors," and that the '609 Patent is currently assigned to Xilinx, Inc.

2. I have reviewed and am familiar with the specification of the '609 Patent filed on November 21, 2008 and issued on August 9, 2011. A copy of the '609 Patent is provided as IVM 1001. I will cite to the specification using the following format: ('609 Patent, 1:1-10). This example citation points to the '609 patent specification at column 1, lines 1-10.

3. I have reviewed and am familiar with U.S. Patent No. 6,737,698 to Paul *et al.* (hereinafter "Paul"), U.S. Patent No. 7,439,570 to Anthony (hereinafter "Anthony"), U.S. Patent No. 7,286,071 to Hsueh *et al.* (hereinafter "Hsueh"), U.S. Patent No. 6,903,918 to Brennan (hereinafter "Brennan"), U.S. Patent No. 7,238,981 to Marotta (hereinafter "Marotta"), and U.S. Patent Application Publication No. 2008/0128857 to Bi (hereinafter "Bi").

4. I am familiar with the technology at issue as of the November 21, 2008 filing date of the '609 Patent.

5. I have been asked to provide my technical review, analysis, insights, and opinions regarding the above-noted references that form the basis for the grounds of rejection set forth in the Petition for *Inter Partes* Review of the '609 Patent.

I. Qualifications

6. I have more than 29 years of experience in the electronic interconnect and semiconductor industries.

7. I earned a Bachelor of Science degree in Graphics from the University of Oregon. My studies included subjects in advanced mathematics related to

geodesic domes. I also attended The Art Center College of Design in Pasadena, California, where I majored in Industrial Design.

8. I currently serve as Chief Scientist at Advanced Inquiry Systems, Inc. (AISI), a company that I founded in 2003. As Chief Scientist, my research focuses on tools and interfaces for full-wafer testing of products such as NAND and NOR flash, Dynamic Random Access Memory (DRAM), and certain logic devices. My research is additionally driven by the semiconductor industry's demand for highly-parallel wafer testing of System-on-Chips (SOCs), such as processors for mobile devices. Through my research, AISI has implemented a device that achieves contact with up to 500,000 pads per wafer during tests. AISI was founded on my patented work in this area and benefits from over 30 issued patents.

9. I co-founded Prototype Solutions Corporation in 1994, a company focused on using advanced interconnect and packaging technology to provide quick-turn prototypes and hardware emulation using programmable logic devices such as Field Programmable Gate Arrays (FPGAs). The technology is used to prototype highly-complex Central Processing Units (CPUs), Graphic Processing Units (GPUs), System on Chips (SOCs), and Application Specific Integrated Circuits (ASICs).

10. I founded LaserPath Corp. in 1983. Laserpath was a semiconductor company focused on laser programmable semiconductor gate arrays. The foundation of this technology was based on my inventions and patents. LaserPath achieved over 200 design wins in the first 9 months of sales—setting a record. LaserPath's technology included Gate Arrays programmed with a laser in a ceramic package, tested, and delivered to customer in as little as two hours and more typically within 5 business days. This rapid Gate Array turnaround time and large number of design wins drastically shifted the ASIC business from a 12-week delivery to a new standard of 3- week delivery.

11. From 1981 to 1982, I researched controlled impedance, instant turn-around circuit boards for the Cray 2 computer system. My research was funded by Cray Computer Corporation—Boulder, Colorado Team. This research was the genesis for my later-developed technology that evolved into LaserPath.

12. In addition to my semiconductor industry experience, I am an inventor on 36 U.S. patents related to interconnects, high-speed connectors, and semiconductors.

13. My *Curriculum Vitae* is attached as IVM 1012, which contains further details on my education, experience, publications, patents, and other qualifications

to render an expert opinion. My work on this case is being billed at a rate of $300.00 per hour, with reimbursement for actual expenses. My compensation is not contingent upon the outcome of this *inter partes* review.

II. My Understanding of Obviousness

14. It is my understanding that a claimed invention is unpatentable if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

15. It is my understanding that "obviousness" is a question of law based on underlying factual issues including the content of the prior art and the level of skill in the art. I understand that for a single reference or a combination of references to anticipate the claimed invention, a person of ordinary skill in the art must have been able to arrive at the claims by altering or combining the applied references.

16. I also understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when considering the prior art. I understand this test should not be rigidly applied, but that the test can be important to avoid such hindsight.

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