

## MORGAN T. JOHNSON

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### PROFESSIONAL EXPERIENCE

**Advanced Inquiry Systems Inc. – Hillsboro, Oregon** **2002 – Present**

**AISI** is a venture funded, high tech startup based on Morgan Johnson patented technologies covering full wafer, single touch down testing and burn-in of chips.

AISI has attracted over \$30M in investments from, among others, INTEL Capital, Applied Materials, KLA Tencor, and Olympic Venture Partners.

Full wafer interposer contactors called Wafer Translators have recently met key milestones and are moving to production with focus on NAND, NOR and DRAM full wafer, single touchdown test. Additionally, interposer technologies for contacting flip-chip wafers (CPUs, GPUs and SoCs are examples) are progressing and will be shipping by Q2, 2014

AISI has about 35 issued patents. Morgan Johnson is, on all but one, a named inventor. Additionally, AISI has royalty free, permanent licenses to several additional patents by Mr. Johnson

Over 20 new Johnson patent filings extend the technology to Wafer Level Chip Scale Packaging and include a break through wafer probe technology that yields true package part test results from unsingulated die on the wafer. AISI formed a JDA with Intel for the development of semiconductor test methods and equipment. Intel Capital is an investor in four rounds of venture capital financing.

These full wafer interposers reside and connect between the die on the wafer and the Contactor connected to the wafer tester. These interposers contact up to 13,000 die on a wafer simultaneously. They can have up to 110,000 contacts, all touching the wafer die and the contactor while connected to the tester. These contactors are trademarked Translated Wafer™

Morgan Johnson enjoys a faculty appointment as Adjunct Professor in the Electrical Engineering School at Portland State University, Portland Oregon. Mr. Johnson has been a guest lecturer at the Jet Propulsion Laboratory (JPL) in Pasadena, California.

#### SOME OF MORGAN JOHNSON'S MORE RECENT AISI PATENTS:

**8,476,630 July 2013 Methods** of adding pads and one or more interconnect layers to the passivated topside of a wafer including connections to at least a portion of the integrated circuit pads thereon

**8,461,024 June 2013 Methods and apparatus** for thinning, testing and singulating a semiconductor wafer

**8,405,414 Mar 2013 Wafer testing systems and associated methods** of use and manufacture

**8,362,797 Jan. 2013 Maintaining a wafer/wafer translator pair** in an attached state free of a gasket disposed therebetween

**8,088,634 Jan. 2013** Methods of adding pads and one or more interconnect layers to the passivated topside of a wafer including connections to at least a portion of the integrated circuit pads thereon

**8,076,216 Dec, 2011** Methods and apparatus for thinning, testing and singulating a semiconductor wafer

**7,960,986 June 2011** Methods and apparatus for multi-modal wafer testing

### **Morgan Johnson Technology – Portland, Oregon**

**2000 – 2001**

Informal Partnership with *SanDisk*, worked with head test engineers and managers, developed a full wafer interposer contactor for use in wafer-level-burn-in and test for NAND memory wafers. This technology formed the basis for AISI.

### **Prototype Solutions (Phase II) – Beaverton, Oregon**

**1997 – 1999**

Developed a technology put forth in a 1994 DARPA proposal. One-hour turn laser personalized ceramic substrates were achieved. Laser scribing of isolated wires directly in thick-film gold over filled vias on a multilayer co-fired ceramic substrate was developed.

**NOTE: This work yielded US Patent 6,878,901 LASER MICROMACHINING AND ELECTRICAL STRUCTURES FORMED THEREBY – INVENTOR Morgan Johnson – April 2005**

#### ○ **HEWLETT PACKARD Printer Division (at their request)**

- **DELIVERABLE I:** *Design for an interposer* containing numerous FPGAs that could emulate a custom ASIC and an interface to a second board that contains all chips to make up a printer controller except those on the interposer – the assembly to be able to run at virtually full system speed to support firmware and software development.
- **DELIVERABLE II: A three board stack:**
  - **Top board** containing all components except the ASIC emulation elements and with 3,200 pressure connect interface pads to the:
  - **Middle Interposer board** containing four laser programmable, auto routable interconnect layers, 10,000 through hole vias and 300,000 two layer blind vias to connect the FPGAs on the Bottom board to each other and to the components on the Top board. This interposer has 3,200 pads point up to the top board and 3,200 pads point down to the Bottom board
  - **Bottom board** packages 8 FPGAs with 3,200 interface pads

**NOTE:** The auto routing worked perfectly and the laser programmed both sides of the middle interposer with great success and perfect yield on the second try.

## XILINX – Programmable Device Division:

**NOTE:** Working with Bob Conn, a senior technical staff member, Johnson developed a series of designs for high die count; bare die interposer packages over a period of two years. Johnson made numerous trips to Xilinx headquarters from Portland, Oregon

Bob wanted to bring die close enough together to obviate the need for controlled impedance signal paths. This required the longest signal to be below  $\frac{1}{4}$  wave length or about 3.7 inches. Die to die signal capacitance had to be below 2 pico farads.

These goals were achieved in the Phase III design. The Phase III design fit into a 4.1 inch cube but could still export 85 watts per die. Die to die distance was at a three dimensional minimum.

The fabrication of the Cube required only standard ceramic methods and design rules

Thermal management was via embedded heat pipes - somewhat exotic then but in every notebook PC today.

Bob Conn wanted a compute cube that could operate at Super Computer Benchmark performance but cost only a few thousand dollars. High I/O band width, a feature of all super computers, was addressed by the design and appeared to be adequate to sustain high benchmark performance.

Additionally we discussed the fact that the cube could act as a 2,048 pin, non-blocking cross bar switch for voice and data switching centers where it would replace several 72 inch high fully populated racks and use 1/1000 the power and operate at 20 times the data rate.

- **DELIVERABLE Phase 0:** *A series of design speculations for consideration*
  - **DELIVERABLE Phase I:** *An 8 FPGA chip interposer with the ability to stack with at least three additional 8 FPGA chip interposers to form a 24 FPGA die package. The stack provided a thermal path per-die that could remove up to 60 watts. Average signal path length was 6.8 inches*
  - **DELIVERABLE Phase II:** *An 8 FPGA chip interposer with the ability to stack with at least five additional 8 FPGA chip interposers to form a 48 FPGA die package. The stack provided a thermal path per-die that could remove up to 65 watts. Average signal path length was 5.2 inches*
  - **DELIVERABLE Phase III:** *A 12 FPGA chip interposer with the ability to stack with at least even additional 12 FPGA chip interposers to form a 96 FPGA die package. The stack provided a thermal path per-die that could remove up to 85 watts. Worst case signal path length was 3.2 inches – Phase III hardware fits into a 4 inch cube*
- **DARPA Contract – Prototype Solutions** competed for and won a large DARPA contract aimed at producing quick turn, multi die interposers that could be stacked and interconnected to form a variety of electronics assemblies. The contract was for \$1.5M (back when that was real money)

- **THE NAVAL SURFACE WEAPONS LAB** provided project oversight, benchmark result approval, progress reporting and arbitration of contract and technical issues.
- **Certification of 100% completion** of all contract goals and deliverables was given by the NSWL to Prototype Solutions
  - **1. DARPA DELIVERABLE & Innovation:** *Laser programmed, removable multi-layer thin-film wiring* - Must connect a minimum of 2,048 pins with random net lists (accomplished). Routing must be 100% with any net list (accomplished). It must take less than one hour, be completely automatic to route and laser program any net list (final, typical time was 20 min.).
 

**NOTE:** the above technologies yielded **US Patent 5,937,515 entitled CONFIGURABLE CIRCUIT FABRICATION METHOD** – Inventor Morgan Johnson - August 1999
  - **2. DARPA DELIVERABLE & Innovation:** *Inexpensive 100% open and short tester* - Must be accomplished in one hour. Tester did 100% test & reporting in 2 minutes for substrates up to 2,048 pins. Tester cost \$3,200. The tester was the first known fully automatic opens and shorts tester that did not use capacitive “golden standard” routs to infer opens or shorts but instead sent signals to and from an array of FPGAs that were connected to the wiring plate being tested. In a 2,048 pin laser programmed wiring plate 1 line would broadcast and 2,047 pins would listen. The entire netlist of the plate could be derived and compare with the desired net list with error reporting and short location and open location coordinates being delivered.
  - **3. DARPA DELIVERABLE & Innovation:** *Two layer autorouters* – The autorouter ran on an ordinary PC and was capable of routing 1,024 nets with 100% completion 100% of the time. The code routed all nets in less than 1 second. It remains the fastest autorouters of record and never required a second pass with altered rules or eased constraints
  - **4. DARPA DELIVERABLE & Innovation:** *Laser trigger map* capable of extracting laser firing points from the completed autorouters result and feeding the laser firing coordinates to the laser system. This was completely integrated with the laser positioning system which brought each laser trigger point into place when the laser was fired.
  - **5. DARPA DELIVERABLE & Innovation:** *Laser system for under \$100,000* - (actual cost \$92,000). System routinely programmed copper and gold thin-film metallization on break-link interposer wiring plates with organic dielectrics. These 68mm square substrates had two or three metal layers with BCB or polyimide dielectrics.
  - **6. DARPA DELIVERABLE & Innovation:** *8 Ceramic plates and a wiring plate pressure connected* – Stack contained over 80,000 pressures connected lapped gold pads. DARPA contract required the stack to be assembled and disassembled 200 times without degradation of function or signals. Proof cycles took one entire 18 hour day and passed 100 continuity tests after each disassembly and reassembly cycle.

- **7. DARPA DELIVERABLE & Innovation:** *3D-i, a patented, solder ball based stacking board-to-board connectors* - Co-invented, patented and developed with Dave Ekstrom, a unique low cost board to board connector that enables interposer board stacking with high connection numbers between several interposer boards. Test structure design used over 34,000 solder solid core solder balls, which were reflowed in one operation. 3D-I patent has issued. The patent includes invention and methods of producing multi chip interposers that are themselves interconnected to package large numbers of die in a single package assembly

**NOTE:** The above technologies and experiments yielded **US Patent 6,443,990 entitled MULTIPLE BOARD PACKAG EMPLOYING SOLDER BALLS AND FABRICATION METHOD AND APPRATUS-** Inventor Morgan Johnson – March 2000

- **SYNOPSYS – Logic Automation Division:**

- **1. DELIVERABLE & Innovation:** *Laser programmed, removable interposer and associated chip package to allow quick turn installation of chips into their in-circuit co-simulation system*
- **2. DELIVERABLE & Innovation:** *Hardware Simulation chip emulation module and add-in board for add-in to PCs and work stations and ad-in board for previous hardware simulation boxes*
- **3. DELIVERABLE & Innovation:** *High bandwidth flat cable system for connection of the FPGA Modules to the standard Hardware Modeler standard product, The cable system had a laser programmable Paddle board with a snap-in laser programmable interposer to re-identify the chips for interface to the test and simulation instruments*

**Prototype Solutions (Phase I) – Beaverton, Oregon**

**1994 – 1996**

Co-founded and served as Chief Technology Officer to develop and bring to market laser programmed, removable wiring to market as chip prototyping.

- **Contract with DRC (Design Research Corporation)** for a U.S. Navy Project requiring the following deliverables:
  - **DRC DELIVERABLE 1:** Design and build a moderate cost, near IR laser system to customize multi-die packaging including Multi Chip Module (MCM) stacking interposer wiring, passives specific interposers containing capacitors, resistors, inductors and certain laser adjustable versions of each, and pure wiring interposers called “wiring plates”. Optionally, certain on-chip metal, multi-layer interconnect could be customized System laser spot delivery accuracy of +/- 1/10<sup>th</sup> micron “on-the-fly” was achieved and 3<sup>rd</sup> party verified. The laser system had a green wave length kit installed as well.

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