IPR2012-0023
Exhibit XLNX-2007
Curriculum Vitae of
Richard A. Blanchard, Ph.D.

Expertise

- MOS and Bipolar Device Tech.
- Semiconductor Device Physics
- Microchip Fabrication & Analysis
- Electronic Systems
- Electrical & Electronic Failures
- ESD & EOS Failures
- Assembly & Packages
- CMOS, DMOS & BiCMOS Tech.
- Power IC's & Power Electronics
- Printed Circuit Board Mfg.
- Printable Electronics, including LEDs
- Semiconductor Process & Control
- Patents & Trade Secrets

Employment History

From: 1991, 2008-
To: Present

Blanchard Associates
Mountain View, CA
Position: *2008-Present: Industry Consultant and Expert Witness*
Blanchard Associates specializes in working with both start-ups and established companies in the development of new products as well as intellectual property. His projects have included the development of improved low voltage and high voltage MOS-gated devices and the development of printable electronics such as LEDs and discrete transistors. This work has included the identification of patentable material and work to protect this material. He is also an Exclusive Expert for SVEWG.

From: 1998
To: 2007

Silicon Valley Expert Witness Group, Inc.
Mountain View, CA
Position: *Exclusive Expert and Consultant*
Silicon Valley Expert Witness Group, Inc. (SVEWG) is a high technology, "Silicon Valley" consulting company specializing in expert witness litigation support and

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technology consulting. SVEWG has an extensive roster of world-class technology experts used in the defense and promotion of intellectual property rights and other litigation disputes. SVEWG Principals offer extensive in-house technology, legal and business expertise and have direct access to senior litigation and technology consultants worldwide.

From: 1991 **Failure Analysis Associates, Inc. (Now named "Exponent")**
To: 1998 Menlo Park, CA
Position: *Principal Engineer & Division Manager*
Responsible for the Electrical/Electronic Division of Failure Analysis Associates providing consulting services to the electrical and electronics industry. Specific duties include:

- Semiconductor devices. Failure analysis and reverse engineering of solid-state electronic components and circuits. Semiconductor processing and semiconductor process equipment. Semiconductor manufacturing and process control.
- Failure analysis of electric and electronic systems, subsystems, and components, including causes of electrical fires
- Reliability modeling and lifetime prediction of electrical and electronic systems and subsystems
- Automotive electronics. Design of discrete devices and integrated circuits
- Power Electronics. Power MOS and Smart Power Technologies

From: 1987 **IXYS Corporation**
To: 1991 San Jose, CA
Position: *Senior Vice President*
Responsible for the development of IC products. Established an in-house CAD capability. Recruited an IC design team and coordinated the definition and development of IXYS ICs. Identified, qualified and monitored the IC foundries that manufactured these circuits. Set up testing capability at IXYS. Coordinated

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assembly on IC's. Worked on various MOSFET and IGBT device, test, and assembly problems.

From: 1982 **Siliconix, Inc.**
To: 1987 Santa Clara, CA
Position: *Vice President, Engineering*
Other titles held at Siliconix, Inc. were Engineering Manager (1982-1983) and Director (1983-1984). Responsible for the development of advanced process technology and the design of both discrete devices (JFETs, lateral and vertical DMOS transistors) and integrated circuits (low and high voltage CMOS, D/CMOS and bipolar-JFET). Personally responsible for many key innovations and inventions in power MOS and D/CMOS IC technology and their assembly and test requirements. He submitted approximately 20 patent disclosures while employed at Siliconix, Inc. He holds the two key "trench FET" patents, of which he is the sole inventor.

From: 1976 **Supertex, Inc.**
To: 1982 Sunnyvale, CA
Position: *Founder and Vice President, MOS Power Products*
Responsible for investigation of new semiconductor devices and new technologies. In charge of Power MOS device research, design and development. His work lead to the design and development of both the discrete power MOS device family and the high voltage IC (HVIC) family sold by Supertex, Inc. Responsible for an in-house assembly area as well as engineering aspects of power MOS and HVIC testing.

From: 1976 **Cognition, Inc.**
To: 1978 Mountain View, CA
Position: *Founder and Consulting Engineer*
Responsible for developing the process technology for fabricating monolithic silicon pressure sensors. A process line was established for the manufacture of piezoresistive pressure sensors, including the precision etching of thin silicon diaphragms.

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From: 1974 **Foothill College**
To: 1978 Los Altos Hills, CA
Position: *Associate Professor, Assistant Division Chairman, Engineering & Technology Division*
Accomplishments included developing the curriculum for the Semiconductor Technology Program, and establishing a small processing facility for teaching students the fundamentals of semiconductor technology. Supervised approximately 60 instructors in the evening and off-campus programs.

From: 1974 **Independent Consultant**
To: 1976 Los Altos Hills, CA
Duties: Consultant to the semiconductor industry, including court appointed "Special Master" in the Fairchild Semiconductor Corporation v. National Semiconductor Corporation Isoplanar patent suit.

From: 1970 **Fairchild Semiconductor**
To: 1974 Mountain View, CA
Position: *Senior Engineer, Department Manager*
Responsible for the fabrication of the integrated circuits in the Polaroid SX-70 camera. Technologies directly related to this work include standard bipolar technology, bipolar- MOS technology, silicon gate technology and flip-chip assembly technology.

Patents

Patent No.	Date Issued	Title
8,330,213	12/11/2012	Power Semiconductor Devices, Methods, and Structures with Embedded Dielectric Layers Containing Permanent Charges
8,330,217	12/11/2012	Devices, Methods, and Systems with MOS-Gated Trench-to-Trench Lateral, Current Flow
8,133,768	03/13/2012	Method of Manufacturing a Light Emitting Photovoltaic or Other Electronic Apparatus and System
8,049,271	11/01/2011	Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Formation of Floating Islands
7,989,293	08/02/2011	Trench Device Structure and Fabrication

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7,825,492	11/02/2010	Isolated Vertical Power Device Structure with Both N-Doped and P-Doped Trenches
7,745,885	06/29/2010	High Voltage Power MOSFET Having Low On-Resistance
7,736,976	06/15/2010	Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands
7,705,397	04/27/2010	Devices, Methods, and Systems with MOS-Gated Trench-to-Trench Lateral Current Flow
7,704,842	04/27/2010	Lateral High-Voltage Transistor with Vertically-Extended Voltage-Equalized Drift Region
7,586,165	09/08/2009	Microelectromechanical Systems (MEMS) Device Including a Superlattice
7,586,148	09/08/2009	Power Semiconductor Device Having a Voltage Sustaining Region that Includes Doped Columns Formed by Terraced Trenches
7,557,394	07/07/2009	High-Voltage Transistor Fabrication with Trench Etching Technique
7,544,544	06/09/2009	Low Capacitance Two-Terminal Barrier Controlled TVS Diodes
7,535,041	05/19/2009	Method for Making a Semiconductor Device Including Regions of Band-Engineered Semiconductor Superlattice to Reduce Device-On Resistance
7,531,850	05/12/2009	Semiconductor Device Including a Memory Cell with a Negative Differential Resistance (NDR) Device
7,531,829	05/12/2009	Semiconductor Device Including Regions of Band-Engineered Semiconductor Superlattice to Reduce Device-On Resistance
7,504,305	03/17/2009	Technique for Forming the Deep Doped Regions in Superjunction Devices
7,473,966	01/06/2009	Oxide-Bypassed Lateral High Voltage Structures and Methods
7,442,584	10/28/2008	Isolated Vertical Power Device Structure with Both N-Doped and P-Doped Trenches
7,411,249	08/12/2008	Lateral High-Voltage Transistor with Vertically-Extended Voltage-Equalized Drift Region
7,397,097	07/08/2008	Integrated Released Beam Layer Structure Fabricated in Trenches and Manufacturing Method Thereof
7,339,252	03/04/2008	Semiconductor Having Thick Dielectric Regions
7,304,347	12/04/2007	Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench

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