

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTELLECTUAL VENTURES MANAGEMENT, LLC  
Petitioner

v.

XILINX, INC.  
Patent Owner

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Case IPR2012-00023  
Patent 7,994,609 B2

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Before SALLY C. MEDLEY, KARL D. EASTHOM, and  
JUSTIN T. ARBES, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
*35 U.S.C. § 318(a) and 37 C.F.R. § 42.73*

## I. BACKGROUND

Petitioner, Intellectual Ventures Management, LLC (“IVM”), filed a Petition to institute an *inter partes* review of claims 1–19 of U.S. Patent No. 7,994,609 B2 (“the ’609 Patent”), owned by Xilinx, Inc. Paper 3 (“Pet.”). *See* 35 U.S.C. § 311. As set forth in this Final Written Decision, *see* 35 U.S.C. § 318(a), based on the record presented, IVM has shown “by a preponderance of the evidence,” 35 U.S.C. § 316(e), that claims 1–19 of the ’609 Patent are unpatentable under 35 U.S.C. § 103(a). In addition, Xilinx has failed to show that proposed amended claims are patentable under 35 U.S.C. § 103(a). *See* Paper 17 (“Mot. to Amend”).

After IVM filed its Petition, Xilinx filed a Preliminary Response opposing the institution of the *inter partes* review. Paper 9 (“Prelim. Resp.”). The Board granted the Petition, concluding that IVM’s Petition demonstrated a reasonable likelihood that claims 1–19 are unpatentable under 35 U.S.C. § 103(a) for obviousness, and instituted trial. Paper 11 (“Inst. Dec.”).

After the Institution Decision, Xilinx filed a Response. Paper 15 (“PO Resp.”). Xilinx also filed a Motion to Amend, contingent upon the Board ultimately determining that challenged claims 1–19 are unpatentable. *See* Paper 17 (“Mot. to Amend”). IVM then filed a Petitioner Reply to Xilinx’s Response, maintaining that the challenged claims are unpatentable. Paper 22 (“Pet. Reply”). IVM also filed an Opposition to Xilinx’s Motion to Amend, Paper 21 (“Opp.”), and Xilinx filed a Patent Owner Reply to the Opposition, Paper 24 (“PO Reply”). Both parties requested an oral hearing, which occurred on November 7, 2013. A transcript of the oral hearing appears in the record. Paper 33 (“Tr.”).

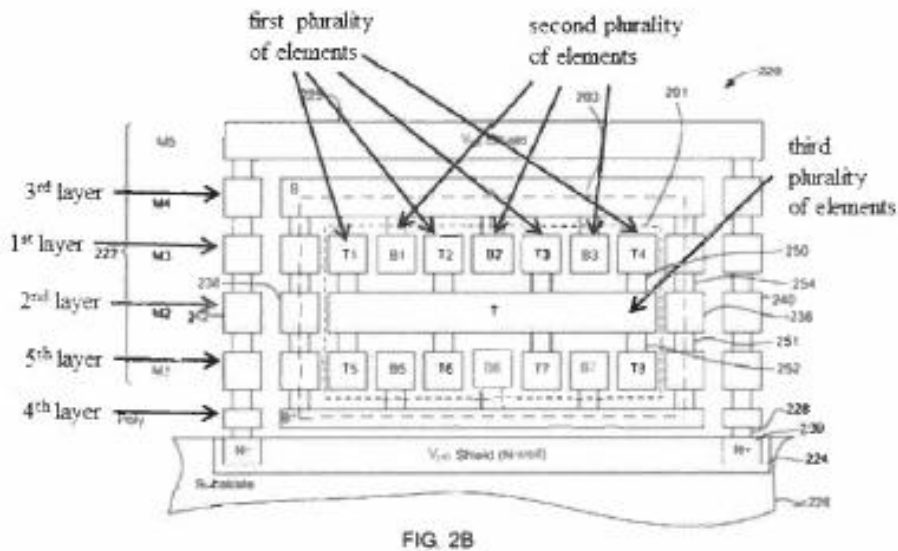
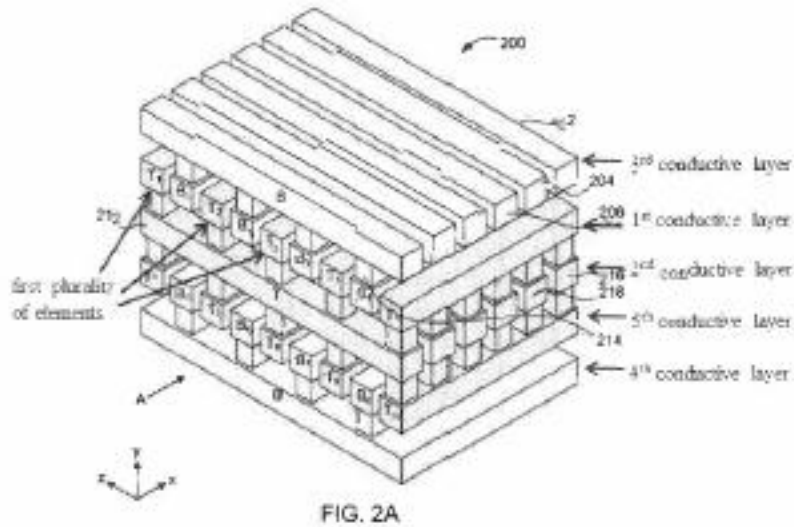
In its Response—i.e., in “response to the [P]etition [and] addressing any ground for unpatentability not already denied,” 37 C.F.R. § 42.120—Xilinx argues that claims 2, 8, 9, 18, and 19, “are valid.” PO Resp. 5. Xilinx does not argue that

claims 1, 3–7, and 10–17 are patentable. Claims 2, 8, and 9 depend from independent claim 1, and claim 19 depends from independent claim 18. Therefore, as Xilinx acknowledged during the oral hearing, Xilinx concedes that claims 1, 3–7, and 10–17 are unpatentable based on the applicable grounds listed in the Institution Decision. Tr. 48, ll. 5–9; *accord* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012) (“The [patent owner] response should identify all the involved claims that are believed to be patentable and state the basis for that belief.”); Inst. Dec. 13 (determining that IVM’s Petition “sufficiently demonstrates a reasonable likelihood that claims 1–19 are unpatentable based on Grounds 1–6”).

#### *A. The '609 Patent*

The '609 Patent describes a shielded capacitor in an integrated circuit (IC) having a core capacitor portion that includes multiple layers of conductive elements. Shields, including a shield capacitor portion and a capacitor reference shield, surround the core capacitor portion. The shield capacitor portion includes multiple conductive elements in different metal layers. According to claim 1, the shield capacitor portion forms part of a capacitor node and lies partially between the reference shield and the core capacitor portion. The shields reduce electronic noise. *See* Ex. 1001, col. 2, l. 40 – col. 3, l. 3; col. 5, ll. 1–4; col. 6, ll. 24–31; Abstract.

To identify disclosed structure that corresponds to certain elements recited in claims 1 and 2, IVM annotates Figures 2A and 2B from the '609 Patent, which are reproduced below:



IVM's annotated figures above show a centrally located core capacitor, including a first (T1, T2) and second (B1, B2) plurality of node elements, numbered conductive layers, one capacitor node (B, B', B1-B5), the other capacitor node (T, T1-T5), and shields. *See* Pet. 4-5.

With respect to independent claim 1 (which follows), layer T corresponds to a second part of a first capacitor node, layers B and B' correspond to a shield capacitor portion and a second part of a second capacitor node, and the  $V_{DD}$  shield corresponds to a reference shield.

### *B. Exemplary Claims*

Claims 1 and 2 are reformatted and annotated with bracketed information added to claim 1 to help illustrate example structure and with limitations at issue in claim 2 emphasized, as follows:

1. A capacitor in an integrated circuit (“IC”) comprising:
  - a core capacitor portion having a first plurality of conductive elements [*see* T1, T2] electrically connected to and forming a first part of a first node of the capacitor formed in a first conductive layer of the IC and a second plurality of conductive elements [*see* B1, B2] electrically connected to and forming a first part of a second node of the capacitor formed in the first conductive layer,
  - the first plurality of conductive elements alternating with the second plurality of conductive elements in the first conductive layer, and a third plurality of conductive elements [*see* T] electrically connected to and forming a second part of the first node formed in a second conductive layer adjacent to the first conductive layer, at least portions of some of the second plurality of conductive elements overlying and vertically coupling to at least portions of some of the third plurality of conductive elements;
  - a shield capacitor portion [*see* B, B'] having a fourth plurality of conductive elements formed in at least the first conductive layer of the IC, the second conductive layer of the IC, a third conductive layer of the IC, and a fourth conductive layer of the IC, the first conductive layer and the second conductive layer each being between the third conductive layer and the fourth conductive layer, the shield capacitor portion being electrically connected to and forming a second part of the second node of the capacitor and surrounding the first plurality of conductive elements and the third plurality of conductive elements; and
  - a reference shield [*see*  $V_{DD}$  Shield] electrically connected to a reference node of the IC other than the second node of the capacitor,

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