

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2002/0053728 A1**

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(43) **Pub. Date:**

May 9, 2002

(54) **PANEL STACKING OF BGA DEVICES TO FORM THREE-DIMENSIONAL MODULES**

(52) **U.S. Cl.** **257/686; 438/109**

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(57) **ABSTRACT**

A chip stack comprising at least one base layer including a base substrate having a first conductive pattern disposed thereon. The chip stack further comprises at least one interconnect frame having a second conductive pattern disposed thereon which is electrically connected to the first conductive pattern of the base layer. Also included in the chip stack are at least two integrated circuit chip packages. The integrated circuit chip packages may each be electrically connected to the first conductive pattern of the base layer such that one of the integrated circuit chip packages is at least partially circumvented by the interconnect frame. Alternatively, one of the integrated circuit chip packages may be electrically connected to the first conductive pattern, with the remaining integrated circuit chip package being attached to the base substrate and at least partially circumvented by the interconnect frame such that the circumvented integrated circuit chip package and the second conductive pattern of the interconnect frame collectively define a composite footprint for the chip stack. A transposer layer may be included as a portion of each chip stack, with the transposer layer including a third conductive pattern specifically configured to provide a CSP-TSOP interface.

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(21) **Appl. No.:** **10/017,553**

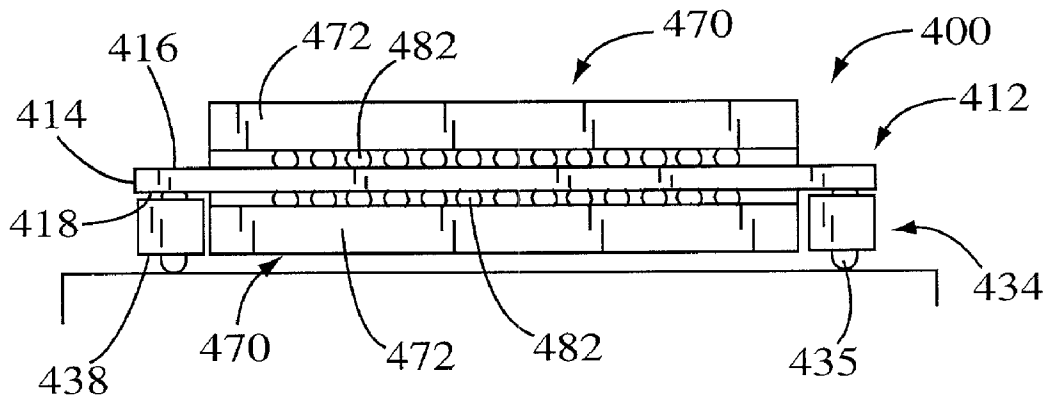
(22) **Filed:** **Dec. 14, 2001**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/598,343, filed on Jun. 21, 2000.

Publication Classification

(51) **Int. Cl.⁷** **H01L 23/02; H05K 1/00; H01R 12/00; H01L 21/50; H01L 21/48; H01L 21/44**



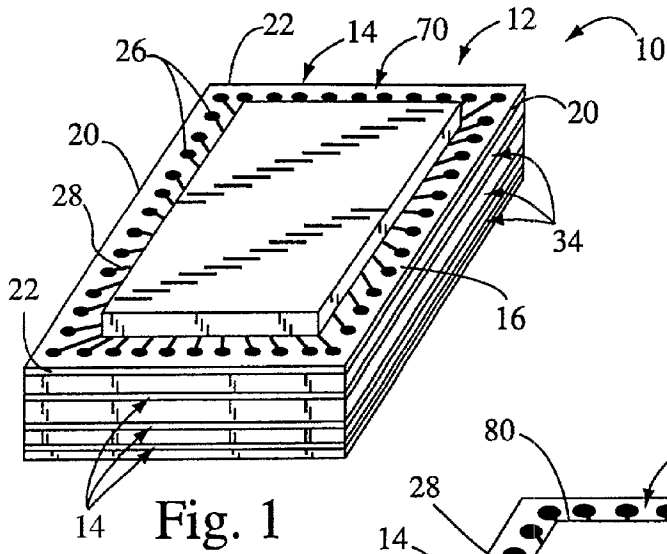


Fig. 1

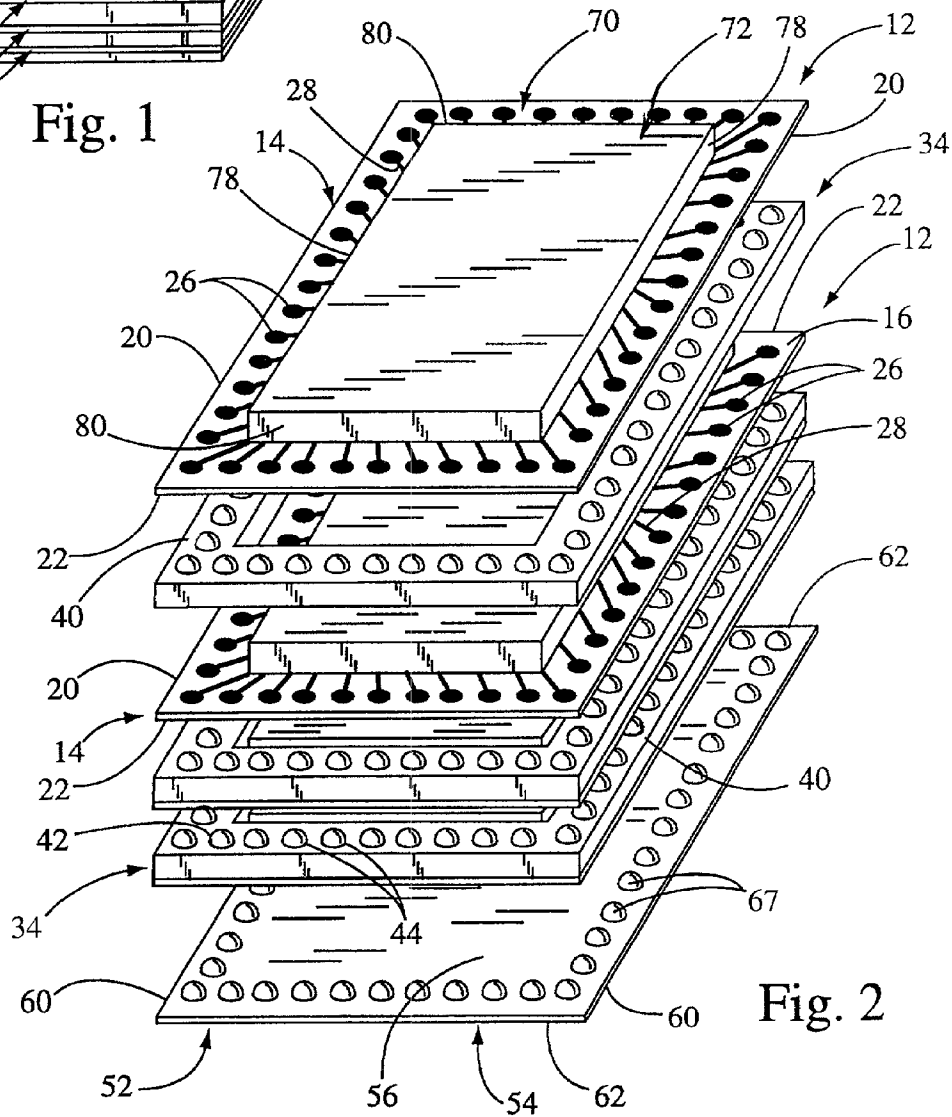


Fig. 2

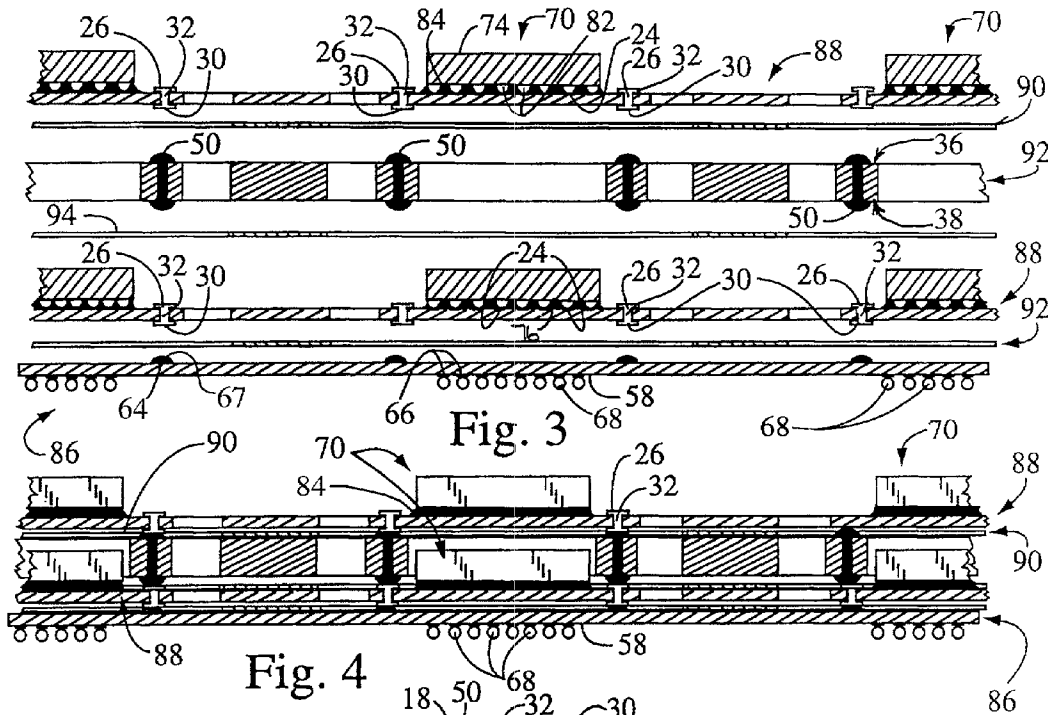


Fig. 4a

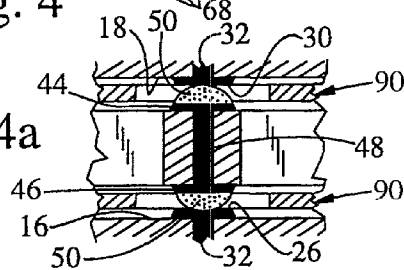


Fig. 5

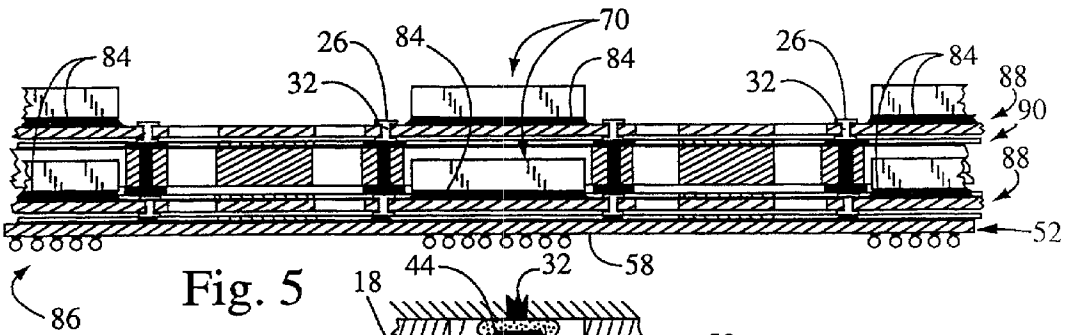
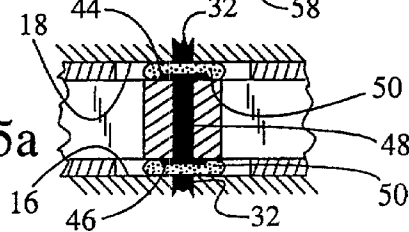


Fig. 5a



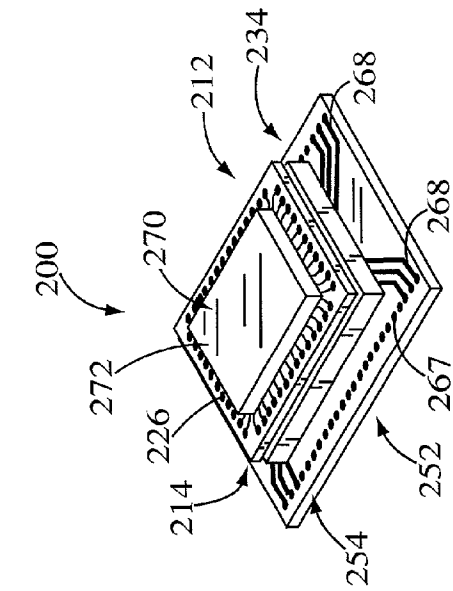


Fig. 6

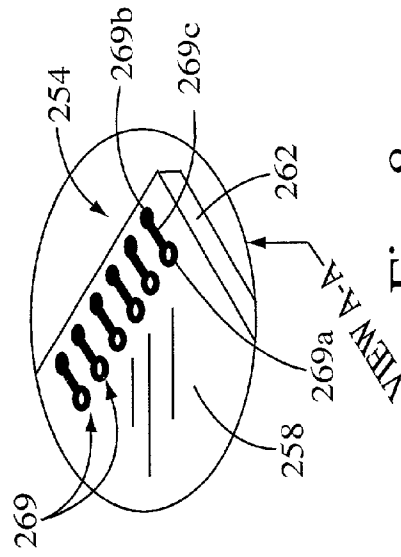


Fig. 8

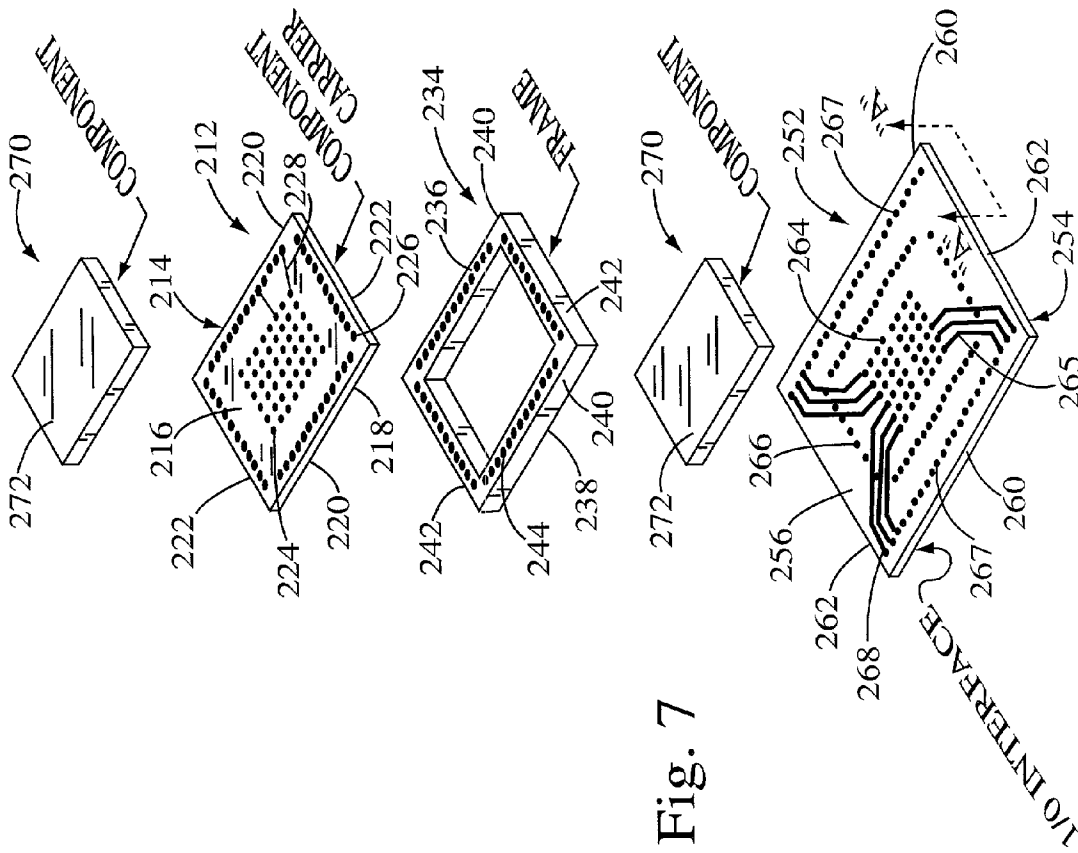


Fig. 7

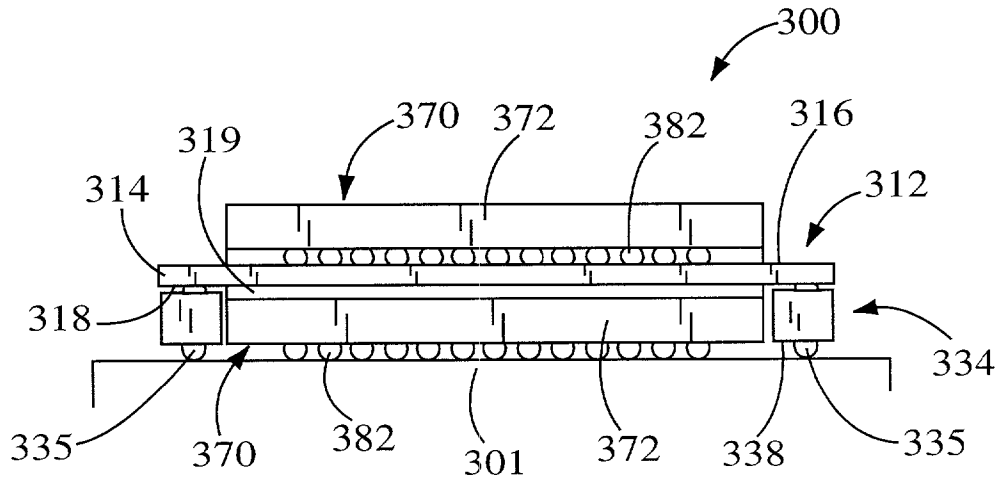


Fig. 9

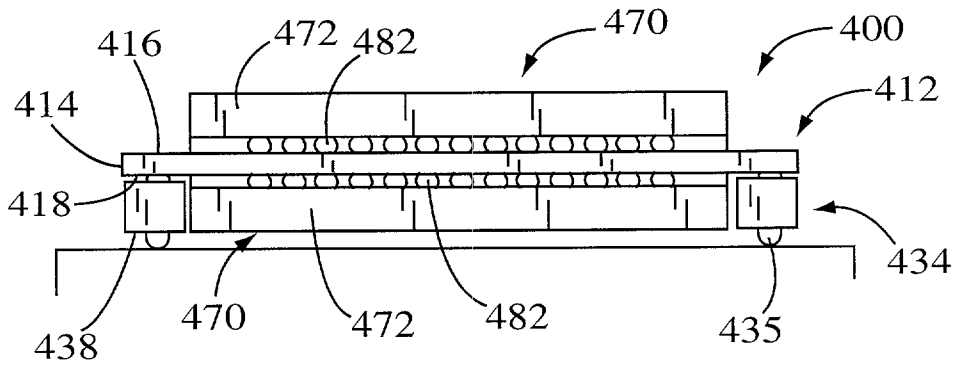


Fig. 10

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