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Siniaguine

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(54) **CLOCK DISTRIBUTION NETWORKS AND CONDUCTIVE LINES IN SEMICONDUCTOR INTEGRATED CIRCUITS**

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(52) **U.S. Cl.** **438/107**; 438/108; 438/110; 257/723; 257/777
(58) **Field of Search** 327/295, 296, 327/297, 298, 299; 257/690, 698, 723, 777; 438/107, 108, 110

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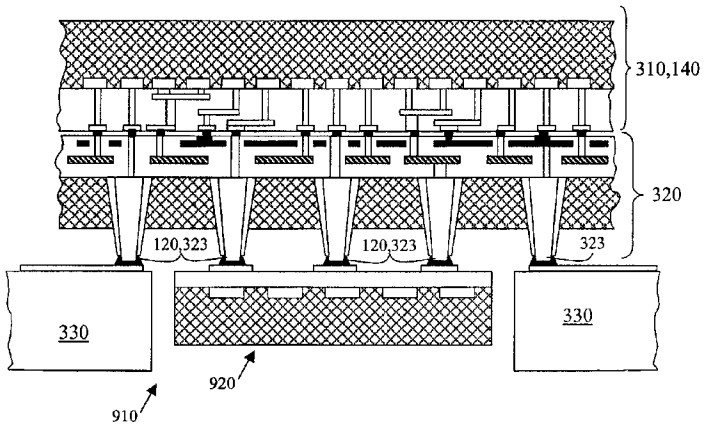
(57) **ABSTRACT**

A clock distribution network **(110)** is formed on a semiconductor interposer **(320)** which is a semiconductor integrated circuit. An input terminal **(120)** of the clock distribution network is formed on one side of the interposer, and output terminals **(130)** of the clock distribution network are formed on the opposite side of the interposer. The interposer has a through hole **(360)**, and the clock distribution network includes a conductive feature going through the through hole. The side of the interposer which has the output terminals **(130)** is bonded to a second integrated circuit **(310)** containing circuitry clocked by the clock distribution network. The other side of the interposer is bonded to a third integrated circuit or a wiring substrate **(330)**. The interposer contains a ground structure, or ground structures **(390, 510)**, that shield circuitry from the clock distribution network. Conductive lines **(150)** in an integrated circuit are formed in trenches **(610)** in a semiconductor substrate.

21 Claims, 15 Drawing Sheets



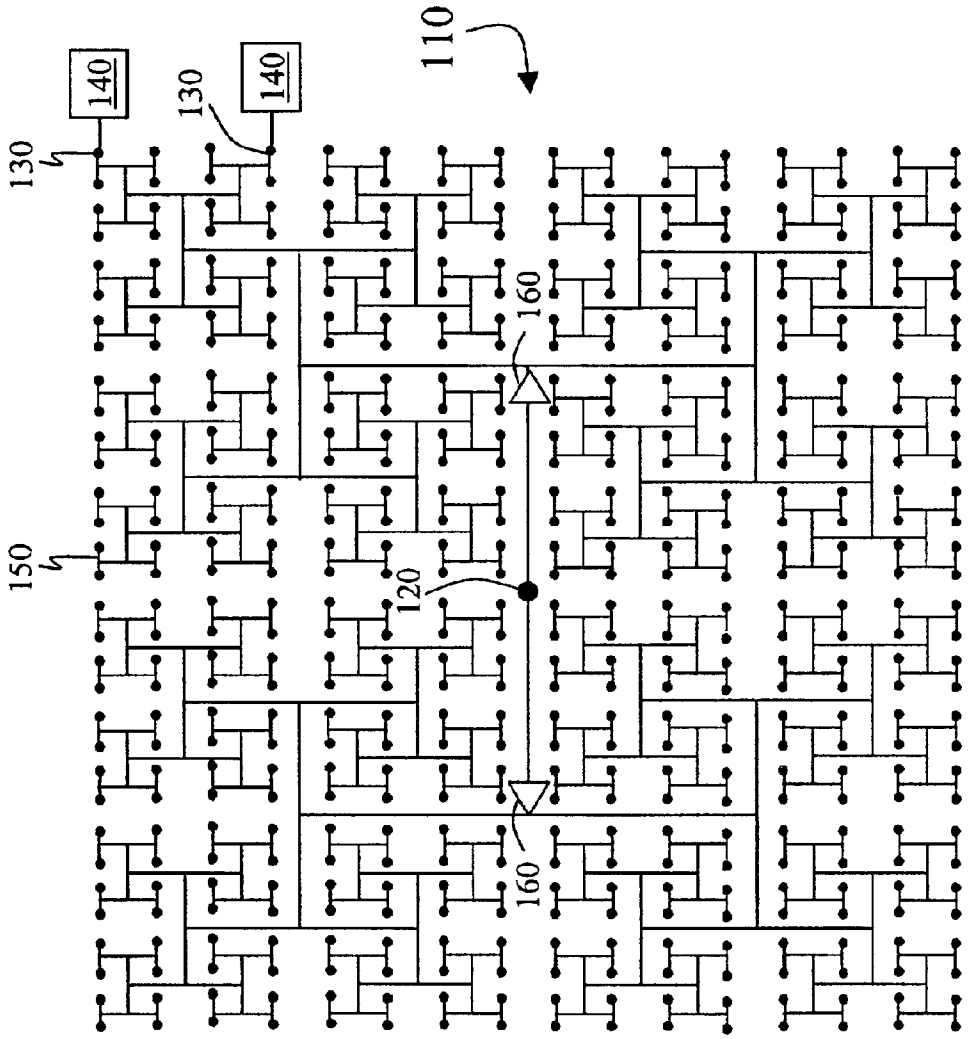


FIG. 1 PRIOR ART

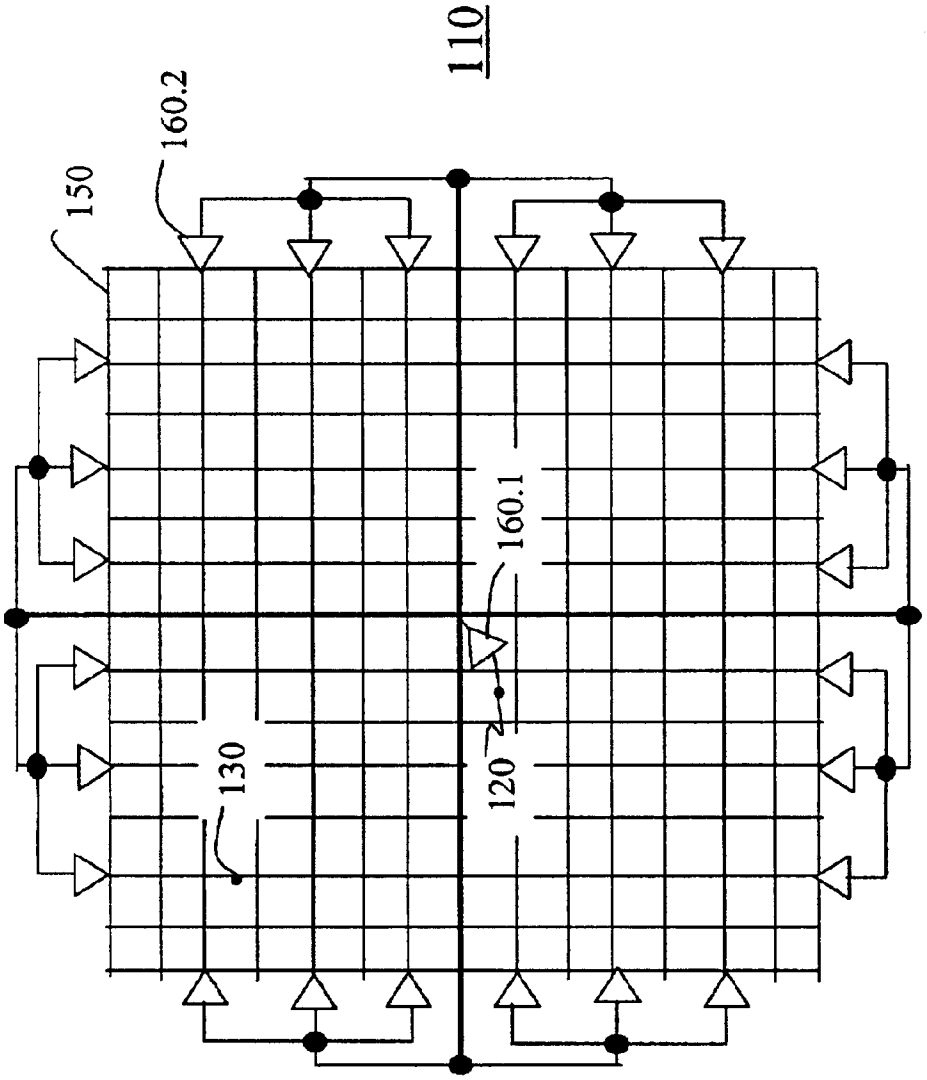


FIG. 2 PRIOR ART

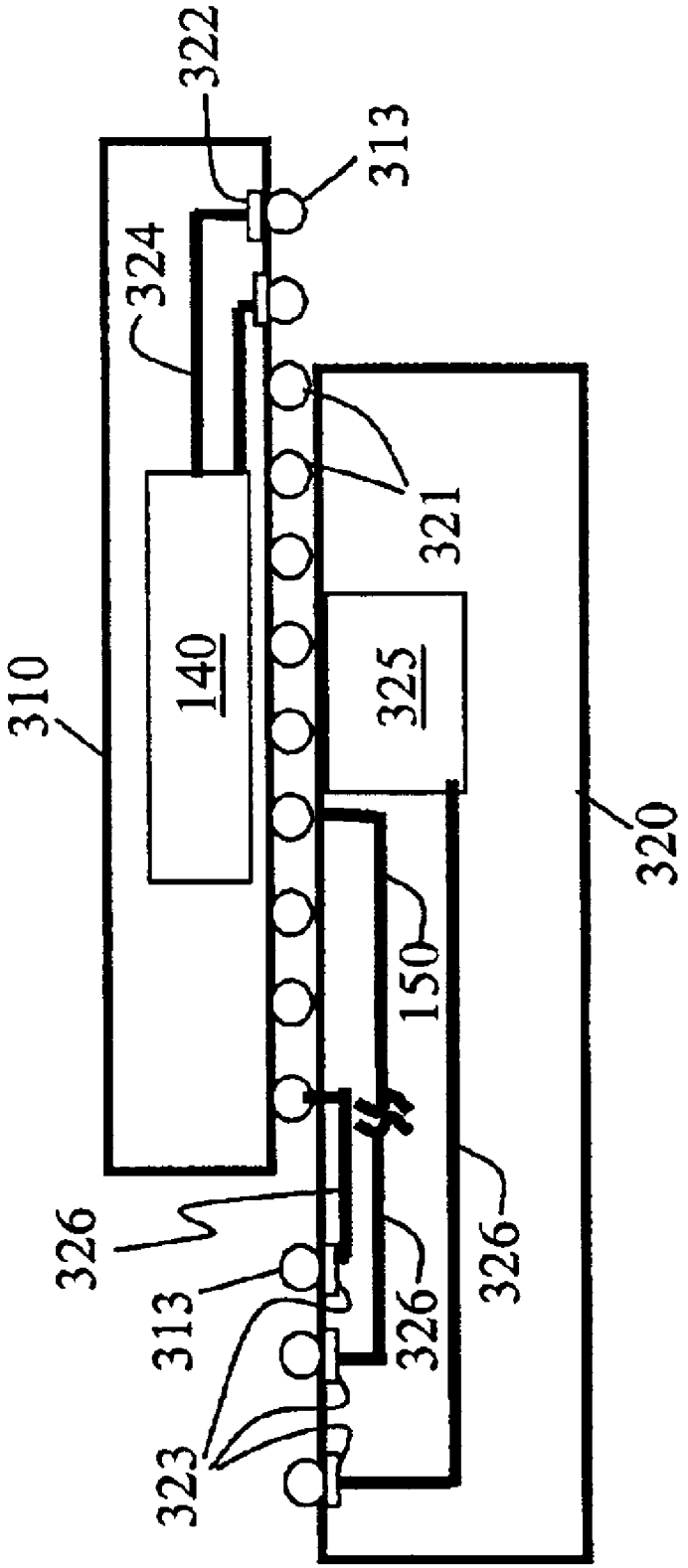


FIG. 3 PRIOR ART

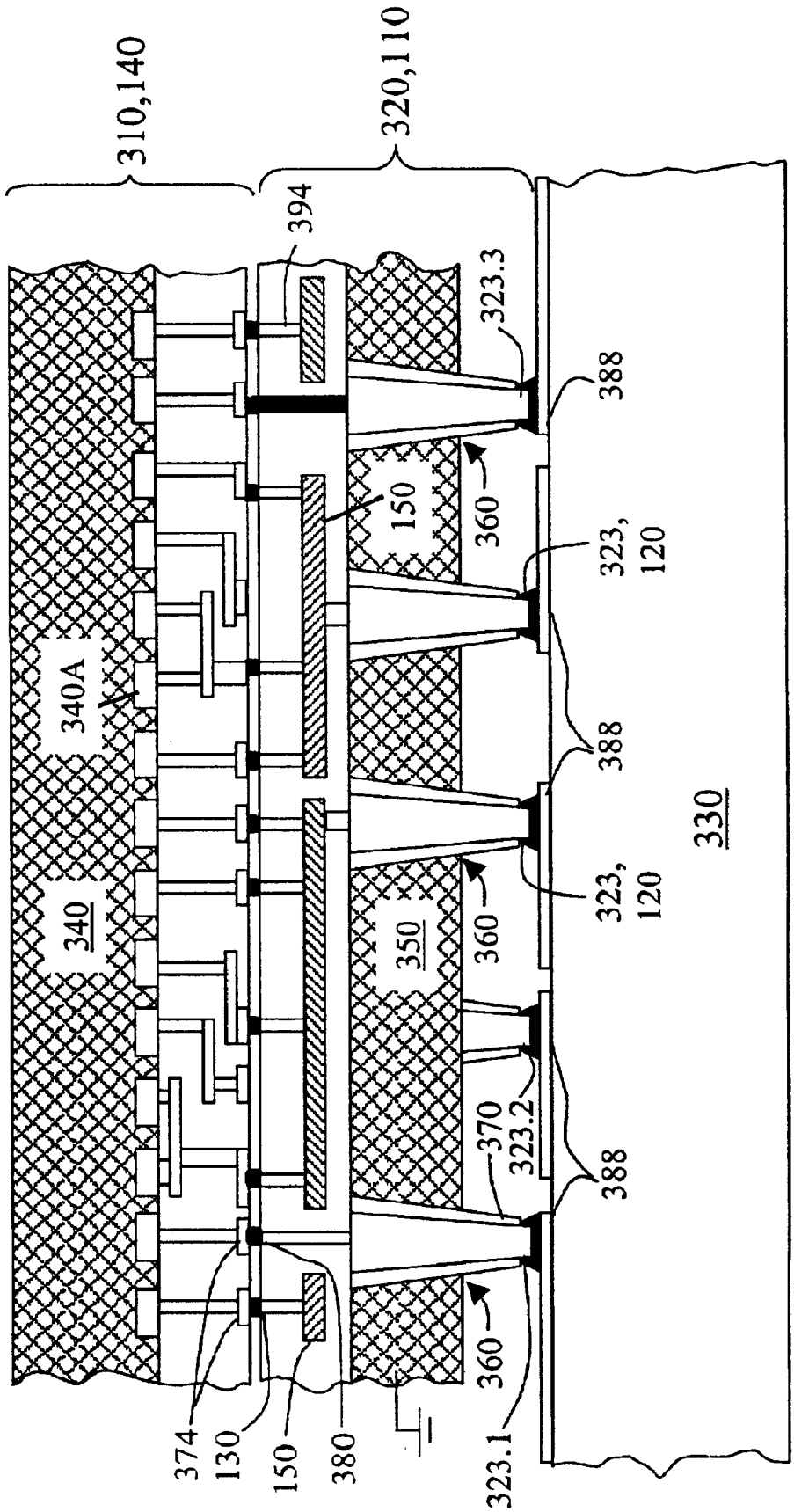


FIG. 4

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