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[54] **MICROELECTRONIC COMPONENT WITH RIGID INTERPOSER**

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[51] **Int. Cl.**[6] **H01L 23/48**; H01L 23/06; H01L 23/52

[52] **U.S. Cl.** **257/696**; 257/693; 257/778; 257/705

[58] **Field of Search** 257/669, 737, 257/738, 693, 696, 783, 48, 668, 778, 688, 705, 700, 695

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,303,393	2/1967	Hymes .	
3,952,404	4/1976	Matunami	29/589
4,893,172	1/1990	Matsumoto et al.	257/669
5,067,007	11/1991	Kanji et al.	257/696
5,148,265	9/1992	Khandros et al.	257/668
5,148,266	9/1992	Khandros et al.	257/668
5,152,695	10/1992	Grabbe et al.	439/71
5,173,055	12/1992	Grabbe	439/66
5,433,822	7/1995	Mimura et al.	257/737
5,518,964	5/1996	DiStefano et al.	438/113
5,659,952	8/1997	Kovac et al.	257/668
5,763,939	6/1998	Yamashita	257/668
5,763,941	6/1998	Fjelstad	257/669

OTHER PUBLICATIONS

IMB Technical Disclosure Bulletin, "Chip Column Package Structure", vol. 40 No. 08 Aug. 1997. p 117 (257/696).

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[57] **ABSTRACT**

A microelectronic component for mounting a rigid substrate, such as a hybrid circuit to a rigid support substrate, such as a printed circuit board. The microelectronic component includes a rigid interposer which may have a chip mounted on its first surface; a pattern of contacts on the rigid interposer; a flexible interposer overlying the second surface of the rigid interposer; a pattern of terminals on the flexible interposer; flexible leads; and solder coated copper balls mounted on the flexible interposer. The microelectronic component may have a socket assembly mounted on the first surface of the rigid interposer. The microelectronic component may be mounted on a rigid support substrate.

48 Claims, 1 Drawing Sheet

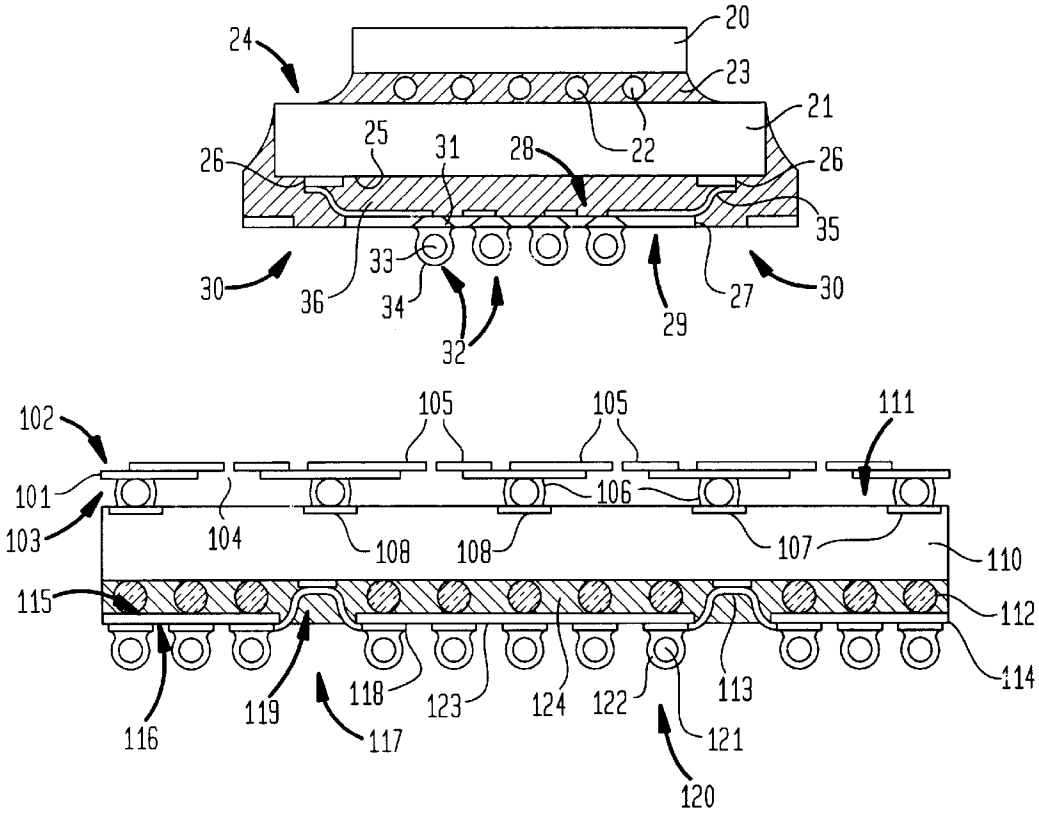


FIG. 1

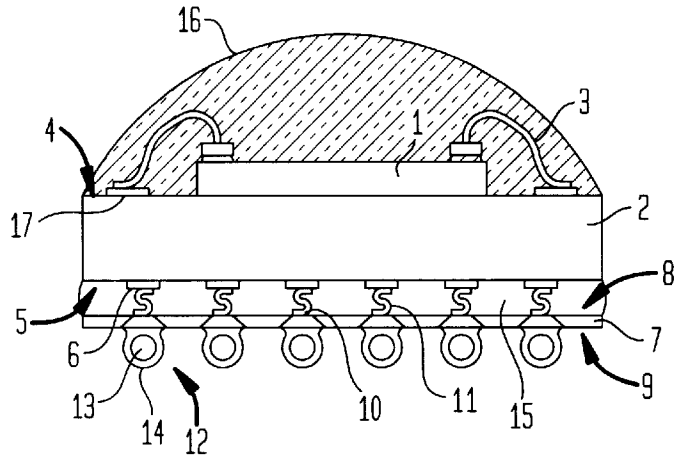


FIG. 2

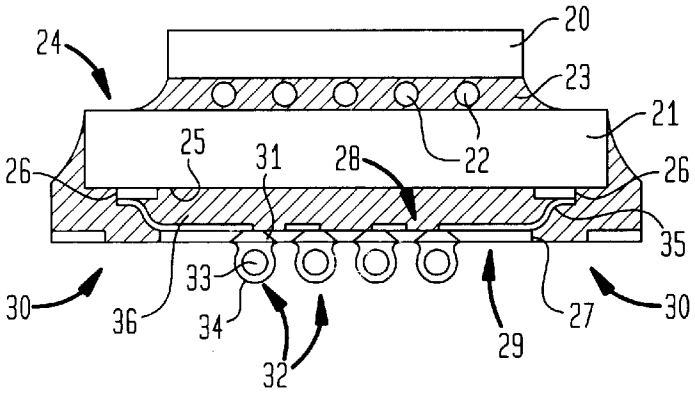
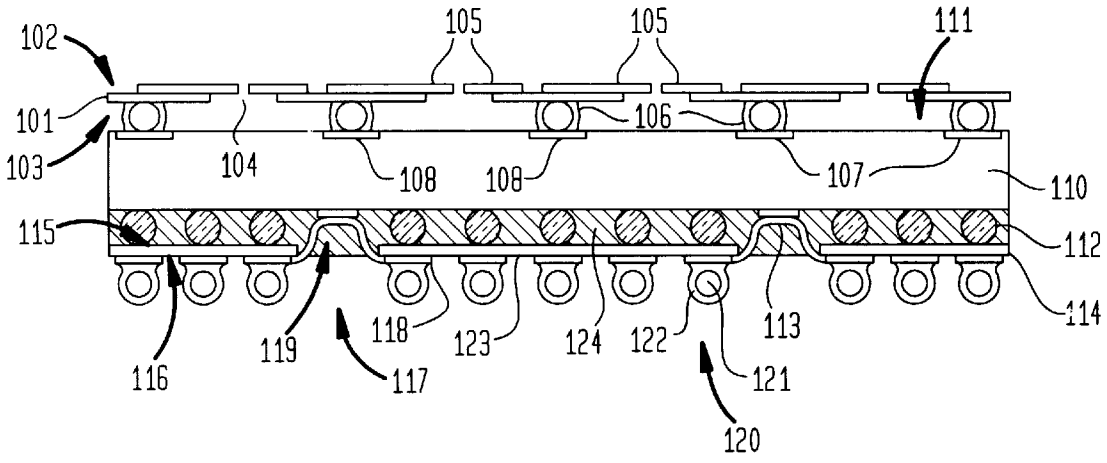


FIG. 3



MICROELECTRONIC COMPONENT WITH RIGID INTERPOSER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the art of electronic packaging, and more specifically to components useful for mounting and/or testing semiconductor chips and related electronic components. The present invention also relates to semiconductor chip assemblies and electronic devices incorporating such components.

2. Description of the Related Art

Modern electronic devices utilize semiconductor components, commonly referred to as "integrated circuits" which incorporate numerous electronic elements. These chips are mounted on substrates that physically support the chips and electrically interconnect each chip with other elements of the circuit. The substrate may be part of a discrete chip package, such as a single chip module or a multi-chip module, or may be a circuit board. The chip module or circuit board is typically incorporated into a large circuit. An interconnection between the chip and the chip module is commonly referred to as a "first level" assembly or chip interconnection. An interconnection between the chip module and a printed circuit board or card is commonly referred to as a "second level" interconnection. In "chip on board" packaging, the chip is mounted directly on the printed circuit board. This type is interconnection has been referred to as a "1½ level" interconnection.

One relatively common packaging scheme is called a "hybrid circuit". A hybrid circuit typically contains a semiconductor chip that has been mounted and electrically interconnected to a circuit that has been formed on a thin layer of a rigid ceramic material. The method used to electrically interconnected the chip to the circuit is generally any of the methods that are known for use in first level bonding, such as wire bonding, tab bonding and flip chip bonding. In some cases it is desirable to mount and electrically interconnect the hybrid circuit to a printed circuit board. Solder is typically used to form the interconnection. It is difficult, however, to rework a hybrid circuit that has been soldered to a printed circuit board. In order to rework the assembly, the hybrid circuit must be removed from the printed circuit board. When the hybrid circuit is separated from the printed circuit board, part of the solder mass is removed from the contacts on the hybrid circuit. Non-uniform partial solder masses remain on the hybrid circuit contacts, the printed circuit board or both. When the hybrid circuit is resoldered to the printed circuit board, the non-uniform partial solder masses can cause short circuits and alignment problems.

Another problem associated with the assembly process is testing. In a typical assembly process, each hybrid circuit is tested before it is soldered to a printed circuit board. Testing involves clamping the hybrid circuit to a socket to engage the solder balls of the hybrid circuit with the test contacts of the test assembly. When the solder balls are engaged with the test contacts, the solder tends to creep and to deform, especially if the hybrid circuit is equipped with high-lead solder. The testing process, like the rework process, can lead to short circuit and alignment problems. To overcome these problems, it is desirable to use solid core solder balls to interconnect the ceramic substrate to a printed circuit board.

In U.S. Pat. No. 3,303,393, which issued on Feb. 7, 1967, Hymes et al. disclose a semiconductor chip assembly with flip-chip connections which incorporates copper core solder balls. One solid core solder ball is provided between each contact on the chip and each contact pad on the substrate. Although these connections work well for small devices, with larger devices, the rigid connections provided by the solid core solder balls tend to crack at the soldered junctions between the balls and the opposing surfaces. Warpage or distortion of the chip or substrate, furthermore, make it difficult to engage all of the solid core solder balls between the chip and substrate simultaneously, or to engage all of the solid core solder balls between the chip and a test fixture. Although it is desirable to use solid core solder balls to interconnect a hybrid circuit to a printed circuit board, such an interconnection would be subject to similar problems.

The electrical power that is dissipated when a microelectronic device is in operation tends to heat up that device. When the device is no longer in operation, it tends to cool down. Over a period of time, the device tends to undergo a number of heating up and cooling down cycles as the device is repeatedly turned on and off. These cycles, which cause an associated expansion and contraction of the device, are commonly referred to as "thermal cycling".

A device in which a hybrid circuit is bonded to a printed circuit board using solid core solder balls would be subject to substantial strain, caused by thermal cycling, during operation of the device. Electrical power dissipated within the hybrid circuit during operation would tend to heat up the hybrid circuit and, to a lesser extent, the printed circuit board. The temperature of the hybrid circuit, therefore, and, to a lesser extent, the printed circuit board would rise each time the device is turned on and fall each time the device is turned off. Since the hybrid circuit and the printed circuit board are normally constructed from different materials having different coefficients of thermal expansion, the hybrid circuit and printed circuit board would normally expand and contract by different amounts. This is commonly referred to as a "thermal mismatch". The thermal mismatch causes the electrical contacts on the hybrid circuit to move relative to the electrical contact pads on the printed circuit board as the temperature of the hybrid circuit and printed circuit board change. The relative movement would deform the electrical interconnections between the hybrid circuit and the printed circuit board and place them under mechanical stress. Since these stresses would be applied repeatedly with repeated operation of the device, they would cause breakage of the electrical interconnections. Thermal cycling stresses may occur even where the hybrid circuit and printed circuit board are formed from like materials having similar coefficients of thermal expansion. This is because the temperature of the hybrid circuit may increase more rapidly than the temperature of the printed circuit board when power is first applied to the hybrid circuit. Unfortunately, solid core solder balls are neither flexible nor strong enough to withstand the strain generated by differential rates of thermal expansion.

Commonly assigned U.S. Pat. Nos. 5,148,265; 5,148,266; 5,518,964; and 5,659,952; and patent application Ser. No. 08/365,747, filed on Dec. 29,1994, the specifications of which are incorporated by reference herein, provide substantial solutions to the problems of thermal stresses and component testing. Nonetheless, still further improvement is desirable.

SUMMARY OF THE INVENTION

One aspect of the present invention provides a flexible chip carrier. The flexible chip carrier of this aspect of the present invention includes a rigid interposer having first and

second surfaces. The rigid interposer is preferably adapted to mount and electrically connect a semiconductor chip onto the first surface of the rigid interposer. An interconnection between the rigid interposer and a semiconductor chip is a "first level" interconnection. The rigid interposer may be adapted to interconnect a semiconductor chip using any of the known methods of creating "first level" interconnections. Some conventional "first level" interconnection methods include wire bonding, tape-automated bonding and flip-chip bonding. The second surface contains a plurality of contacts disposed in a pattern. The area encompassed by the contacts is defined as a "contact pattern area". The rigid interposer is preferably a thin, sheet-like layer material. The rigid interposer may be composed of any rigid dielectric material. Preferred rigid dielectric materials include ceramic materials, such as alumina, beryllia, silicon carbide, aluminum nitride, forsterite, mullite, and glass-ceramics; composite materials, such as polyester/fiberglass, polyimide/fiberglass, and epoxy/fiberglass; and silicon. More preferred rigid dielectric materials are the ceramic materials listed above. The preferred ceramic material is alumina. On preferred embodiments, the rigid interposer contains an electrical circuit. Although the coefficient of thermal expansion, hereinafter "CTE", of the rigid interposer is generally greater than the CTE of a semiconductor chip and generally less than the CTE of an epoxy-polyimide printed circuit board, the CTE of the rigid interposer may be roughly equal to the CTE of the semiconductor chip. This is because other sub-components of the present invention, specifically the flexible interposer and/or the optional compliant layer can compensation for the CTE mismatch between chip and the rigid interposer and the CTE mismatch between the rigid interposer and the flexible interposer.

The flexible chip carrier also includes a flexible interposer that overlies the second surface of the rigid interposer. The flexible interposer has a top surface that faces toward the second surface of the rigid interposer, and a bottom surface that does not. The flexible interposer preferably is a thin, flexible sheet of a polymeric material such as polyimide, a fluoropolymer, a thermoplastic polymer or an elastomer. In preferred embodiments, the flexible interposer contains an electrical circuit. The flexible interposer may have one or more apertures, extending from the top surface of the flexible interposer to the bottom surface.

A plurality of electrically conductive terminals is disposed on the flexible interposer in a pattern on at least one surface selected from the group consisting of the top surface and the bottom surface. In preferred embodiments, either all of the terminals disposed on the top surface or all of the terminals are disposed on the bottom surface of the flexible interposer. At least some of the terminals, and preferably most or all of the terminals, are disposed within the area of the flexible interposer overlying the contact pattern area on the rigid interposer. Generally, each terminal is associated with one contact on the rigid interposer.

The flexible chip carrier also includes a plurality of electrically conductive leads connecting at least some of the contacts on the rigid interposer with at least some of the terminals on the flexible interposer. Each lead has a contact end connected to the associated contact on the rigid interposer and a terminal end connected to the associated terminal on the flexible interposer. The leads and the flexible interposer are constructed and arranged so that the contacts ends of the leads are moveable relative to the terminals at least to the extent required to compensate for differential thermal expansion between the components. The interconnection between the contacts on the rigid interposer and the terminals on the flexible interposer is a second "first level" interconnection. The leads are preferably flexible so that the terminals are moveable with respect to the contacts to accommodate movement caused by differential thermal expansion.

The flexible interposer is flexible to facilitate movement of the contact ends of the leads relative to the terminals and thus to contribute to the ability of the chip carrier to withstand thermal cycling. Each flexible lead may extend through an aperture in the flexible interposer. The flexible leads may be formed integrally with the terminals on the flexible interposer, or else may be separately formed fine wires. Preferably, the leads are curved to provide increased flexibility. The leads may be generally S-shaped. Each lead may be formed from a ribbon of conductive materials having oppositely-directed major surfaces, the ribbon being curved in directions normal to its major surfaces to form a curved configuration of the lead In a preferred embodiment, the lead is S-shaped.

Some preferred arrangements of leads connecting the contacts to the terminals include a "fan-in", "fan-out", "fan-in/fan-out", and area array. In a "fan-in" arrangement, the contacts on the rigid interposer are typically disposed on the periphery of the rigid interposer. The terminals are generally disposed inside the region that overlies the region bounded by the contacts on the rigid interposer. The leads connecting the terminals to the associated contacts fan inwardly. In a "fan-out" arrangement, the contacts on the rigid interposer are again generally disposed on the periphery of the rigid interposer, and the terminals on the flexible interposer are generally disposed in a region that is outside the region that overlies the region bounded by the contacts. The leads connecting the terminals to the associated contacts fan outwardly. In a "fan-in/fan-out" arrangement, some terminals on the flexible interposer are disposed inside the region bounded by the contacts and some are disposed outside the region. Some leads, therefore, fan-in and some fan-out. The rigid interposer contacts typically are disposed in single rows and columns on the second surface and the leads are interdigitated. By the term "interdigitated", it is meant that fan-in and fan-out leads are interspersed with one another. The preferred interdigitated fan-in/fan-out arrangement is where each lead that is adjacent to a fan-in lead is a fan-out lead and each lead that is adjacent to a fan-out lead is a fan-in lead. In an "area array" arrangement, the contacts on the rigid interposer may be disposed on the periphery of the rigid interposer or may be disposed in a so called area array, i.e., a grid like pattern covering all or a substantial portion of the bottom surface of the rigid interposer. For the leads to be in an area array arrangement, however, the terminals on the flexible interposer must be disposed in area array.

The flexible chip carrier further includes a plurality of joining units, each-including a solid core which is preferably spherical. Each joining unit is disposed on the bottom surface of the flexible interposer, is electrically interconnected to one terminal, and extends downwardly from such terminal. If any terminals are disposed on the bottom surface of the flexible interposer, one of said joining units is preferably disposed directly on each of such terminals. The solid cores are preferably electrically conductive. Preferably, the solid cores are made from copper or nickel.

The flexible chip carrier also includes a unit bonding material. The unit bonding material extends between the terminal and the solid core. Preferably, the unit bonding material is standard lead/tin solder and is provided as a part of the joining unit, as a coating extending over the solid core.

The unit bonding material may be used to bond the flexible chip carrier to a printed circuit board or another support substrate.

The flexible chip carrier may also include a compliant layer covering the flexible leads in whole or in part. The compliant layer comprises a dielectric material having a low modulus of elasticity, such as an elastomeric material. Preferred elastomeric materials include silicones, flexiblized epoxies, and thermoplastics. Silicone elastomers are particularly preferred. The dielectric material may be provided in the form of a layer, with holes in the layer aligned with the terminals on the flexible interposer. In preferred embodiments, the compliant layer is formed in at least a two step process. The first step involves dispensing a controlled amount of a thixotropic or non-slumping silicone elastomer on a portion, but not all, of the bottom surface of the rigid interposer and/or a portion, but not all, of the first surface of the flexible interposer, to create a compliant spacer. The compliant spacer controls the separation between the rigid interposer and the flexible interposer. The second step involves dispensing a second silicone elastomer over the thixotropic or non-slumping silicone elastomer. Compliant spacers and their use in microelectronic assemblies is more fully described in commonly assigned, U.S. Pat. No. 5,659,952, the specification of which is hereby incorporated by reference.

One aspect of the present invention provides a semiconductor chip assembly. The semiconductor chip assembly of the present invention includes the flexible chip carrier described above and at least one semiconductor chip that has been connected to the first surface of the rigid interposer of the flexible chip carrier. The semiconductor chip assembly of the present invention may contain a plurality of semiconductor chips.

If the semiconductor chip assembly contains a plurality of chips, each chip is mounted on and electrically interconnected to the rigid interposer of the flexible chip carrier. Such assemblies may be referred to as multichip modules. Such a multichip module may, for example, comprise a monolithic microwave integrated circuit and a high frequency digital integrated circuit on one rigid interposer that is part of a flexible chip carrier. If both of these high frequency elements are on one rigid interposer, the high frequency elements of the circuit can be isolated from the lower frequency elements. In another embodiment, an integrated circuit in the form of a central processing unit, sometimes referred to as a "cpu", and one or more memory chips may be mounted on a rigid interposer of the present flexible chip carrier to form a semiconductor chip assembly of the present invention. Such an assembly would also be a multichip module.

Preferred methods of connecting the one or more semiconductor chips to the flexible chip carrier include wirebonding, flip chip bonding and tab bonding, with wire bonding and flip chip bonding being more preferred. If the semiconductor chip is to be wire bonded, the rigid interposer should have as plurality of electrically conductive pads disposed in a ring-like pattern. The chip is secured to the first surface of the rigid interposer at the center of the ring-like pattern, so that the contact pads on the rigid interposer surround the chip. The chip is mounted on the first surface of the rigid interposer. The chip is mounted on the rigid interposer in a face-up disposition, with the back surface of the chip confronting the first surface of the rigid interposer, and with the front surface of the chip facing upwardly, away from the rigid interposer so that the electrical contacts on the front surface of the chip are exposed. Fine wires are connected between the electrical contacts on the front surface of the chip and the contact pads on the first surface of the rigid interposer. These wires extend outwardly from the chip to the surrounding contact pads on the first surface of the rigid interposer.

If the semiconductor chip is to be connected to the rigid interposer using flip chip technology, the electrical contacts on the front surface of the chip are provided with bumps of solder. The first surface of the rigid interposer should include a plurality of contact pads arranged in an array corresponding to the array of electrical contacts on the chip. The chip, with the solder bumps, is inverted so that its front surface faces towards the first surface of the rigid interposer, with each electrical contact and solder bump on the chip being positioned on the appropriate contact pad on the first surface of the rigid interposer. The assembly is then heated so as to liquefy the solder and, upon resolidification of the solder, bond each contact on the chip to the confronting contact pad on the first surface of the rigid interposer.

The semiconductor chip assembly of the present invention has at least two "first level" interconnections in the flexible chip carrier. The first "first level" interconnection is the interconnection between the semiconductor chip and the rigid interposer and second "first level" interconnection is the interconnection between the rigid interposer and the flexible interposer.

Another aspect of the present invention provides a test assembly for semiconductor chips. Current semiconductor chip manufacturing techniques do not result in 100% yields, some chips, therefore, will be defective. Often, the defect can not be detected until the chip is operated under power in a test fixture or in an actual assembly. A single bad chip can make a larger assembly, which may include other chips or other valuable components, worthless, or can require painstaking procedures to extricate the bad chip from the assembly. The chips and the mounting components used in a semiconductor chip assembly should, therefor, permit testing of the chips and replacement of the chips before the chips are fused to a substrate.

Semiconductor chips can be tested in the test assembly of the present invention. The test assembly of this aspect of the present invention includes the flexible chip carrier as described above. The test assembly further includes a sheet socket assembly or connector. Preferred sheet socket assemblies and connectors are those described in commonly assigned U.S. Pat. No. 5,615,824; U.S. Pat. No. 5,632,631; U.S. patent application Ser. No. 08/254,991, filed on Jun. 7, 1994; and U.S. patent application Ser. No. 08/862,151, filed on May 22, 1997, the specifications of which are incorporated by reference herein.

In preferred embodiments, the sheet socket component or connector includes a planar or sheet like dielectric body having first and second major surfaces and also having a plurality of holes open to the first major surface. The second major surface faces toward the first surface of the rigid interposer of the flexible chip carrier. The holes are disposed in an array corresponding to an array of bumped leads on a semiconductor chip or microelectronic device which is to be tested. The sheet socket assembly further includes an array of resilient contacts secured to the first major surface of the dielectric body in registration with the holes so that each such resilient contact extends over one hole. Each resilient contact is adapted such that it can resiliently engage a bumped lead that has been inserted into the associated hole. The sheet socket assembly also includes a plurality of socket terminals electrically connected to these resilient contacts.

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