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(12) **United States Patent**
Alexander et al.

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(54) **INTERPOSER PROVIDING LOW-INDUCTANCE DECOUPLING CAPACITANCE FOR A PACKAGED INTEGRATED CIRCUIT**

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* cited by examiner

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 139 days.

(57) **ABSTRACT**

Structures that provide decoupling capacitance to packaged IC devices with reduced capacitor and via parasitic inductance. A capacitive interposer structure is physically interposed between the packaged IC and the PCB, thus eliminating the leads and vias that traverse the PCB in known structures. A capacitive interposer is mounted to a PCB and the packaged IC is mounted on the interposer. The interposer has an array of lands on an upper surface, to which the packaged IC is coupled, and an array of terminals on a lower surface, which are coupled to the PCB. Electrically conductive vias interconnect each land with an associated terminal on the opposite surface of the interposer. Within the interposer, layers of a conductive material alternate with layers of a dielectric material, thus forming parallel plate capacitors between adjacent dielectric layers. Each conductive layer is either electrically coupled to, or is electrically isolated from, each via.

(21) Appl. No.: **10/313,482**

(22) Filed: **Dec. 6, 2002**

(51) **Int. Cl.**⁷ **H01L 23/48**; H01L 23/34

(52) **U.S. Cl.** **257/678**; 257/738; 257/774; 257/777; 257/780; 257/737; 257/713; 257/722; 257/690; 257/691; 257/698; 257/699; 257/784

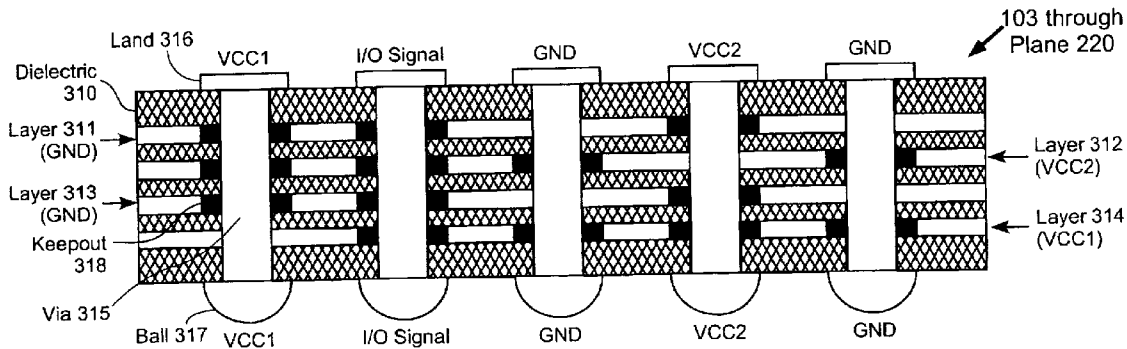
(58) **Field of Search** 257/738, 774, 257/777, 780, 737, 713, 722, 784, 690, 691, 698, 699

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53 Claims, 7 Drawing Sheets



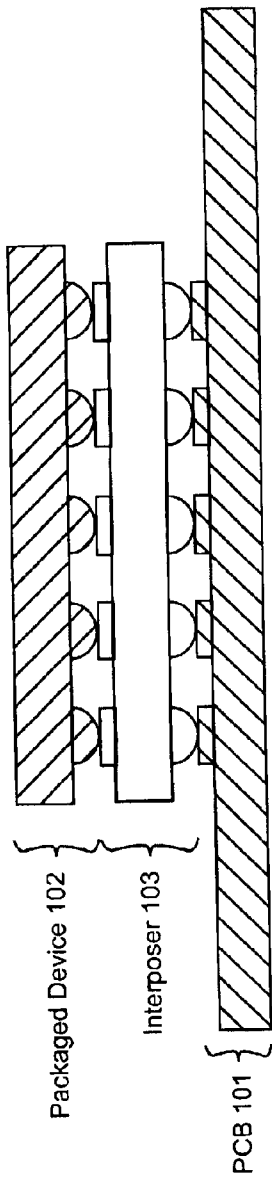


FIG. 1

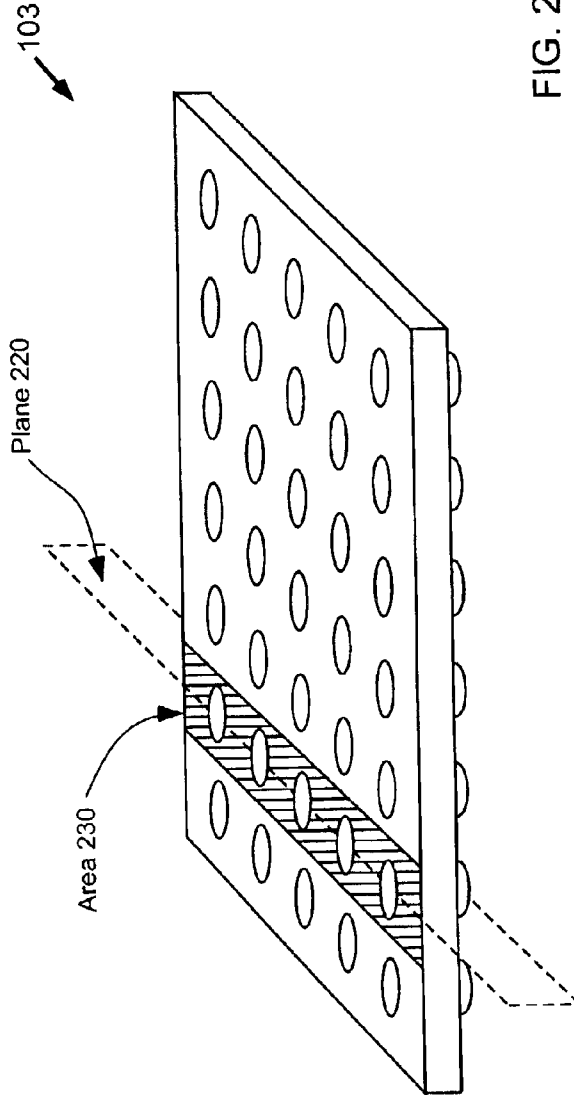


FIG. 2

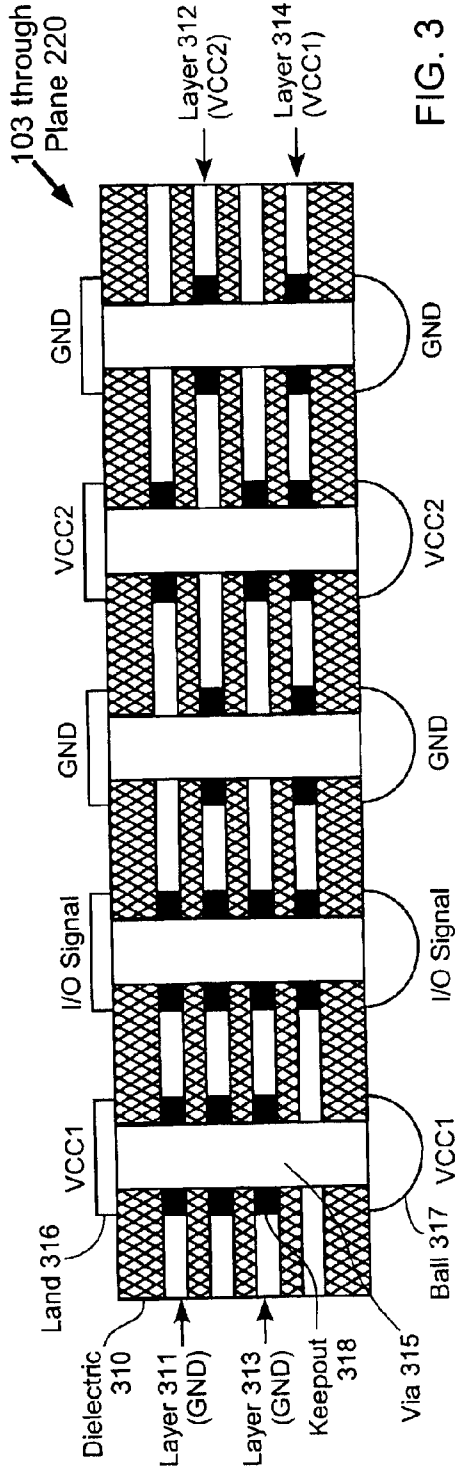


FIG. 3

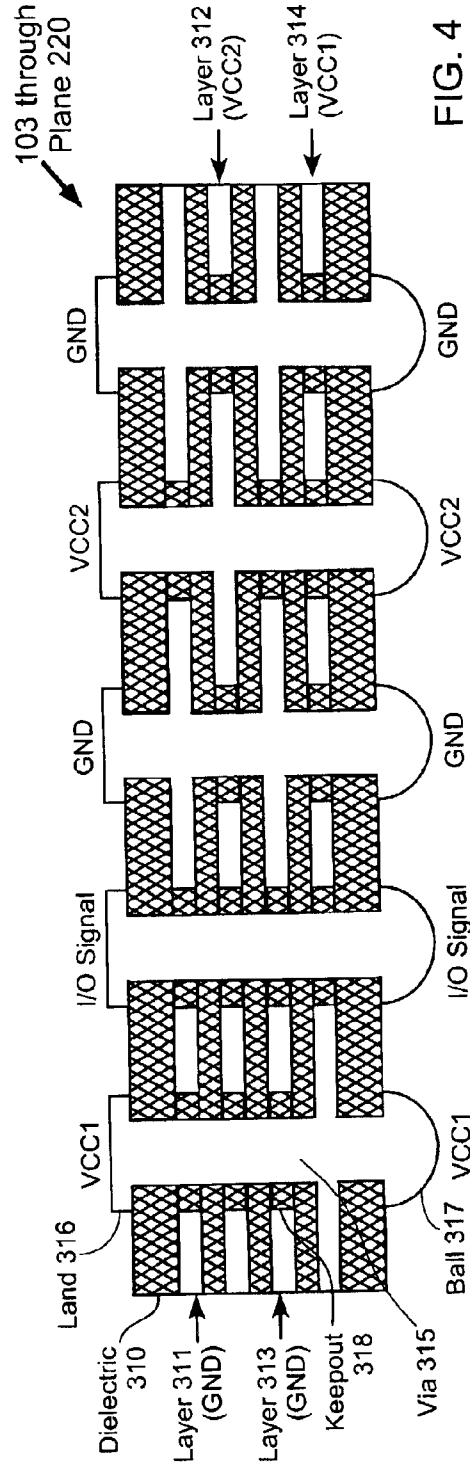
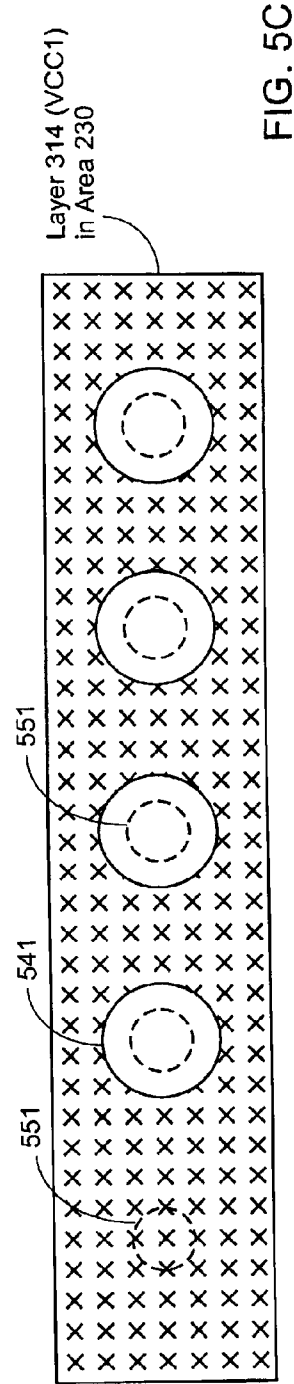
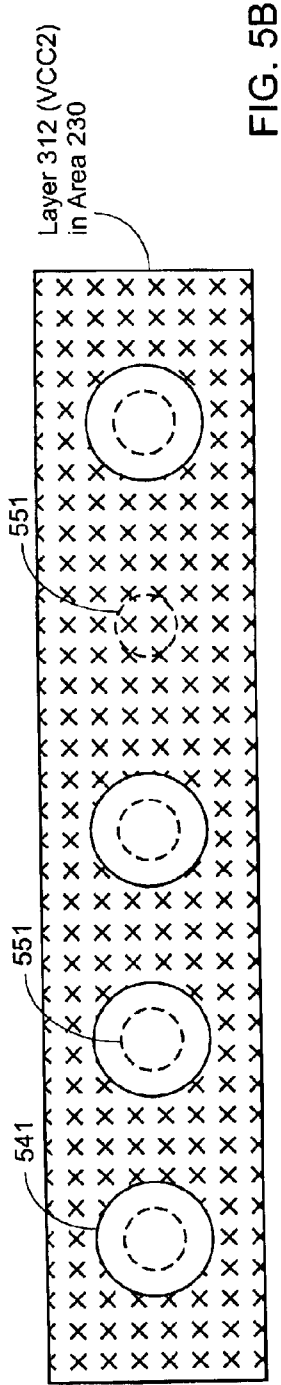
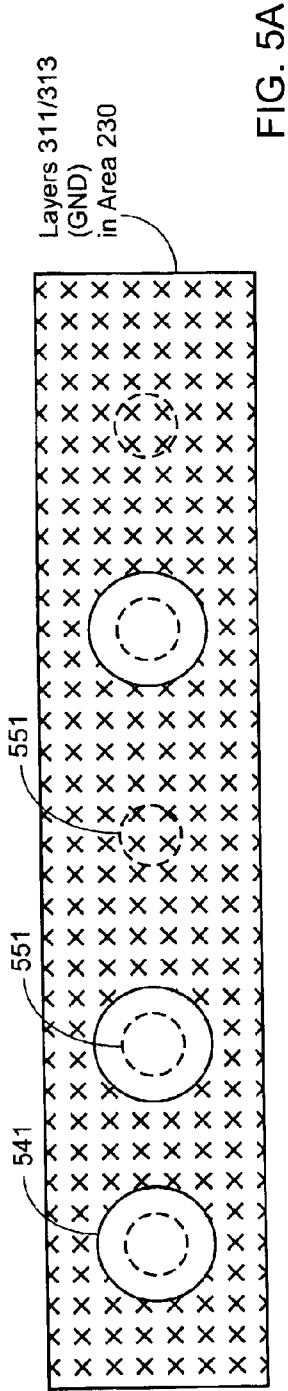


FIG. 4



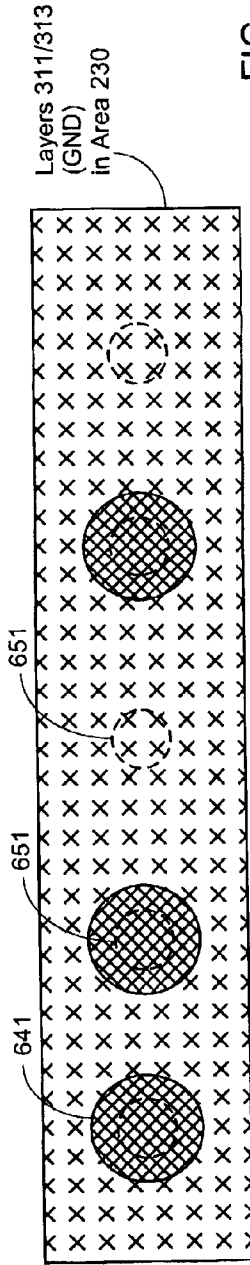


FIG. 6A

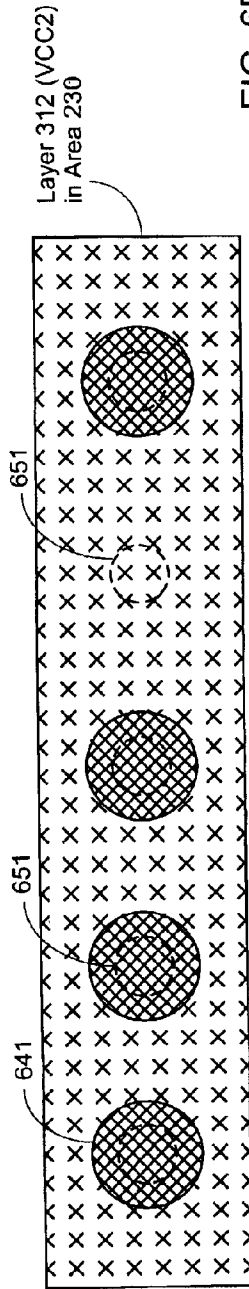


FIG. 6B

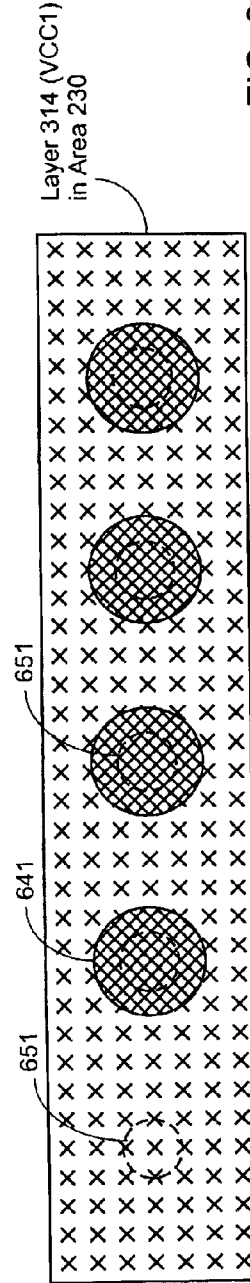


FIG. 6C

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