

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTELLECTUAL VENTURES MANAGEMENT, LLC  
Petitioner

v.

XILINX, INC.  
Patent Owner

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Case IPR2012-00018  
Patent 7,566,960

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**DECLARATION OF MORGAN T. JOHNSON IN SUPPORT OF  
PETITIONER'S OPPOSITION TO PATENT OWNER'S MOTION TO  
AMEND**

IVM 1012  
IPR2012-00018

I, Morgan T. Johnson, declare as follows:

1. I have been retained by Intellectual Ventures Management, LLC (“IVM”) to provide declaratory evidence in *inter partes* review of U.S. Patent No. 7,566,960 to Robert O. Conn (“the ‘960 Patent”), which is assigned to Xilinx, Inc.

2. I have reviewed and am familiar with the specification and the claims of the ‘960 Patent filed on October 31, 2003.

3. I have reviewed and am familiar with the following references: U.S. Patent No. 6,730,540 to Siniaguine (“Siniaguine”; IVM 1004); U.S. Patent No. 6,469,908 to Patel et al. (“Patel”; IVM 1005); U.S. Patent No. 6,970,362 to Chakravorty (“Chakravorty ‘362”; IVM 1007); U.S. Patent No. 6,423,570 to Ma et al. (“Ma”; IVM 1008); U.S. Patent No. 6,891,258 to Alexander et al. (“Alexander”; IVM 1016); U.S. Patent No. 6,319,829 to Pasco et al. (“Pasco”; IVM 1017); and U.S. Patent No. 6,002,168 to Bellaar et al. (“Bellaar”; IVM 1018). I will cite to these references using the following format: (IVM 1004, 1:1-10). This example citation points to the Siniaguine specification at column 1, lines 1-10.

4. I am familiar with and am a practitioner of the technology at issue and the state of the art at the time the application leading to the ‘960 Patent was filed. The filing date of the ‘960 Patent was October 31, 2003. Based on the

technologies disclosed in the '960 Patent, I believe that one of ordinary skill in the art would have a B.S. degree in Electrical Engineering or equivalent training, as well as 3-5 years of experience in the field of electronics packaging and interconnect design.

5. I have been asked to provide my technical review, analysis, insights and opinions regarding the above-noted references.

### **Qualifications**

6. I have more than 29 years of experience in the electronic interconnect and semiconductor industries.

7. I earned a Bachelor of Science degree in Graphics from the University of Oregon. My studies included subjects in advanced mathematics related to geodesic domes. I also attended The Art Center College of Design in Pasadena, California, where I majored in Industrial Design.

8. I currently serve as Chief Scientist at Advanced Inquiry Systems, Inc. (AIS), a company that I founded in 2002. As Chief Scientist, my research focuses on tools and interfaces for full-wafer testing of products such as NAND and NOR flash, Dynamic Random Access Memory (DRAM) and certain logic

devices. My research is additionally driven by the semiconductor industry's demand for highly-parallel wafer testing of System-on-Chips (SOCs), such as processors for mobile devices. Through my research, AISI has implemented a device that achieves contact with up to 500,000 pads per wafer during tests. AISI was founded on my patented work in this area and benefits from over 30 issued patents.

9. I co-founded Prototype Solutions Corporation in 1994, a company focused on using advanced interconnect and packaging technology to provide quick-turn prototypes and hardware emulation using programmable logic devices such as Field Programmable Gate Arrays (FPGAs). The technology is used to prototype highly-complex Central Processing Units (CPUs), Graphic Processing Units (GPUs), System on Chips (SOCs) and Application Specific Integrated Circuits (ASICs).

10. I founded LaserPath Corp. in 1983. LaserPath was a semiconductor company focused on laser programmable semiconductor gate arrays. The foundation of this technology was based on my inventions and patents. LaserPath achieved over 200 design wins in the first 9 months of sales—setting a record. LaserPath's technology included Gate Arrays programmed with a laser in a

ceramic package, tested and delivered to customer in as little as two hours and more typically within 5 business days. This rapid Gate Array turnaround time and large number of design wins drastically shifted the ASIC business from a 12-week delivery to a new standard of 3- week delivery.

11. From 1980-1981, I researched controlled impedance, instant turn-around circuit boards for the Cray 2 computer system. My research was funded by Cray Computer Corporation—Boulder, Colorado Team. This research included the development of laser-programmed printed circuit boards, multi-chip module structures and emitter-coupled logic on-chip wiring. This research was the genesis for my later-developed technology that evolved into LaserPath.

12. In addition to my semiconductor industry experience, I am an inventor on 36 U.S. patents related to interconnects, high-speed connectors and semiconductors. Also, I have a faculty appointment as Adjunct Professor in the Electrical Engineering School at Portland State University in Portland, Oregon. I have also been a guest lecturer at the Jet Propulsion Laboratory (JPL) in Pasadena, California.

13. My professional background and technical qualifications are stated above and are also reflected in my *Curriculum Vitae*, which is attached as IVM

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