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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTELLECTUAL VENTURES MANAGEMENT, LLC Petitioner

v.

Patent of XILINX, INC. Patent Owner

Case IPR2012-00018 Patent 7,566,960 Title: INTERPOSING STRUCTURE

Proposed Claim Amendments

In accordance with 37 C.F.R. 42.121(b), the following claim listing shows the proposed changes, with markings indicating changes in each proposed substitute claim relative to its corresponding original claim. Congruent with the Patent Trial and Appeal Board's guidance, the amendments are presented following the example format provided in the Official Trial Practice Guide, Section II.G.

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Claim Listing

Claims 1-13 (replaced by proposed substitutes).

14. (Proposed substitute for original claim 1) An assembly, comprising: an integrated circuit die having an array of micro-bumps disposed on a surface of the integrated circuit die in a first pattern;

an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern and an array of solder balls disposed on an outside surface of the integrated circuit package,

wherein the first pattern and the second pattern are substantially identical patterns; and

[[an]] <u>a plurality of tiled</u> interposing structure <u>structures</u> disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, <u>at least one of</u> the <u>interposer interposing</u> <u>structures</u> electrically coupling a <u>respective</u> first micro-bump in a first position in the array of micro-bumps to a <u>respective</u> first landing pad located opposite to the first position and to a second landing pad in the array of landing pads.

Claim 15 (Proposed substitute for original claim 2): The assembly of claim [[1]] <u>14</u>, wherein <u>the interposing structures are held together using an elastomer a line</u> <u>extending through the first micro-bump in a direction orthogonal to the surface of</u> the integrated circuit does not extend through the second landing pad of the integrated circuit package.

Claim 16 (Proposed substitute for original claim 3): The assembly of claim [[2]] <u>14</u>, wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has structures have a <u>collective</u> major surface, and wherein the major surface of the integrated circuit die and the <u>collective</u> major surface of the interposing structure structures have have roughly identical surface areas.

Claim 17 (Proposed substitute for original claim 4): The assembly of claim [[3]] <u>14</u>, wherein <u>at least one of</u> the interposing structure <u>structures</u> <u>includes</u> <u>comprises a</u> <u>first conductive layer corresponding to a first capacitor for a first power supply and</u> <u>a second conductive layer corresponding to a second capacitor for a second power</u> <u>supply different from the first power supply</u> no transistor and no PN junction.

Claim 18 (Proposed substitute for original claim 5): The assembly of claim [[4]] <u>14</u>, wherein <u>at least one of</u> the interposing structure includes <u>structures comprises a</u> <u>first conductive layer for a first ground and a second conductive layer for a second</u> <u>ground different from the first ground</u> an array of micro-bumps, wherein the array of micro-bumps of the interposing structure has a pattern that is substantially

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identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.

Claim 19 (Proposed substitute for original claim 6): The assembly of claim [[5]] <u>14</u>, wherein <u>at least one of</u> the interposing structure <u>structures comprises an AC</u> <u>load structure to match a characteristic impedance</u> includes a layer comprising <u>epoxy and fiberglass</u>.

Claim 20 (Proposed substitute for original claim 7): The assembly of claim [[5]] <u>14</u>, wherein <u>at least one of</u> the interposing structure <u>structures comprises a DC load</u> <u>structure to match a characteristic impedance</u> <u>includes a bypass capacitor</u>.

Claim 21 (Proposed substitute for original claim 8): The assembly of claim [[5]] <u>14</u>, wherein the first micro-bump is coupled to the first second landing pad at least in part by a conductor disposed in <u>a corresponding interposing structure selected</u> from the interposing structure structures, wherein the conductor disposed in the <u>corresponding</u> interposing structure extends in a direction parallel to the surface of the integrated circuit.

Claim 22 (Proposed substitute for original claim 9): An assembly, comprising: an integrated circuit die having an array of micro-bumps disposed on a surface of the integrated circuit die in a first pattern;

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an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern and an array of solder balls disposed on an outside surface of the integrated circuit package, wherein the first pattern and the second pattern are substantially identical patterns; and

a plurality of tiled means for electrically coupling the array of landing pads and the array of solder balls, the plurality of means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package;

wherein at least one of the plurality of means for electrically coupling couples a respective first micro-bump in a first position in the array of microbumps to a respective first landing pad disposed opposite the first position and to a second landing pad located in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

Claim 23 (Proposed substitute for original claim 10): The assembly of claim [[9]] <u>22</u>, wherein the <u>plurality of means are held together using an elastomer</u> means is also for providing a bypass current to the integrated circuit die.

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