EXHIBIT 10

Third Edition

ELECTRIC CIRCUIT ANALYSIS

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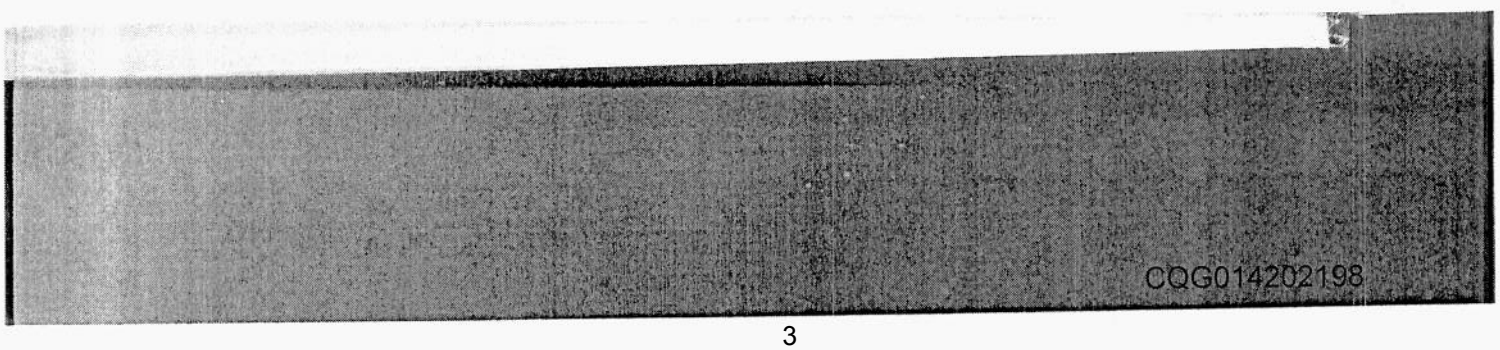
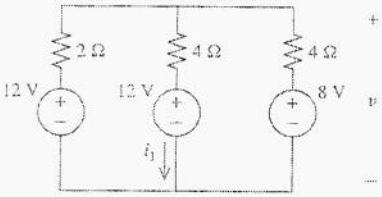


We also need the power through the 3-Ω resistor. Since we know its voltage v,

$$p = \frac{v^2}{R} = \frac{15^2}{3} = 75 \text{ W}$$

Note that we found v by superposition and then used the total voltage v *after* superposition of voltage components to compute the power. Had we computed the power through the resistor in the component problems separately and tried to superpose them, this would have given us a different and erroneous result, since the sum of component powers, $(v^{a2} + v^{b2})/R$, is not the same as the power due to the sum of components, $v^2/R = (v^a + v^b)^2/R$. Even in linear circuits, power does not superpose; only voltage and current do.

EXERCISES



EXERCISE 4.2.2

4.2.1. Solve Exercise 4.1.1 using superposition.

4.2.2. Find v and i_1 by superposition. Check by Thevenin–Norton transformations.

Answer 11 V; $-\frac{1}{4}$ A

4.2.3. Replace the 8 V by $4i_1$ in Exercise 4.2.2, converting an independent source to a dependent source. Find v and i_1 by superposition.

Answer 8 V; −1 A

4.3 NODAL ANALYSIS

In this section we develop a general method of circuit analysis in which voltages are the unknowns to be found. A convenient choice of voltages for many networks is the set of *node voltages*. Since a voltage is defined as existing between two nodes, it is convenient to select one node in the network to be a *reference node* and then associate a voltage at each of the other nodes. *The voltage of each of the nonreference nodes with respect to the reference node is defined to be a node voltage.* It is common practice to select reference directions for these voltages so that the plus ends are all at the nonreference nodes and the minus ends all at the reference node. For a circuit containing N nodes, there will be $N - 1$ nonreference nodes and thus $N - 1$ node voltages. Nodal analysis is a method in which we will break the circuit, that is, solve for a key set of circuit variables, by finding the node voltages themselves. Any other current or voltage will follow easily once the circuit is broken.

The reference node is often chosen to be the node to which the largest number of branches are connected. Many practical circuits are built on a metallic base or chassis, and usually a number of elements are connected to the chassis, which becomes a logical choice for the reference node. In many cases, such as in electric power systems, the chassis is shorted to the earth itself, becoming part of a single chassis–earth node. For

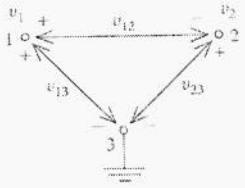


FIGURE 4.8 Reference and nonreference nodes.

this reason, the reference node is frequently referred to as *ground* or the *ground node*. The reference node is thus at ground potential or zero potential, and each other node may be considered to be at some potential above or below zero specified by the value of its node voltage.

The equations of nodal analysis are obtained by applying KCL at the nodes. Recall that each term in a KCL equation is an element current. For a resistor, this current is proportional to its voltage. This voltage, like any element voltage, is equal to a node voltage (if one end of the element is tied to the reference node) or the difference of two node voltages (if both ends are tied to nonreference nodes). For example, in Fig. 4.8 the reference node is node 3 with zero or ground potential. The symbol shown attached to node 3 is the standard symbol for ground, as noted in Chapter 3. The nonreference nodes 1 and 2 have node voltages v_1 and v_2. Thus the element voltage v_{12} with the polarity shown is

$$v_{12} = v_1 - v_2$$

The other element voltages shown are

$$v_{13} = v_1 - 0 = v_1$$

$$v_{23} = v_2 - 0 = v_2$$

These equations may be established by applying KVL around the loops (real or imagined). Evidently, if we know all the node voltages, we may find all the element voltages and thence all the element currents.

The application of KCL at a node, expressing each unknown current in terms of the node voltages, results in a *node equation*. Clearly, simplification in writing the resulting equations is possible when the reference node is chosen to be a node with a large number of elements connected to it. As we shall see, however, this is not the only criterion for selecting the reference node, although it is frequently the overriding one. Since we are going to apply KCL systematically at circuit nodes, the most straightforward case to consider is that of circuits whose only sources are independent current sources. We begin with examples of this type.

In the network shown in Fig. 4.9(a), there are three nodes, dashed and numbered as shown. [This may be easier to see in the redrawn version of Fig. 4.9(b).] Since there are four elements connected to node 3, we select it as the reference node, identifying it by the ground symbol shown.

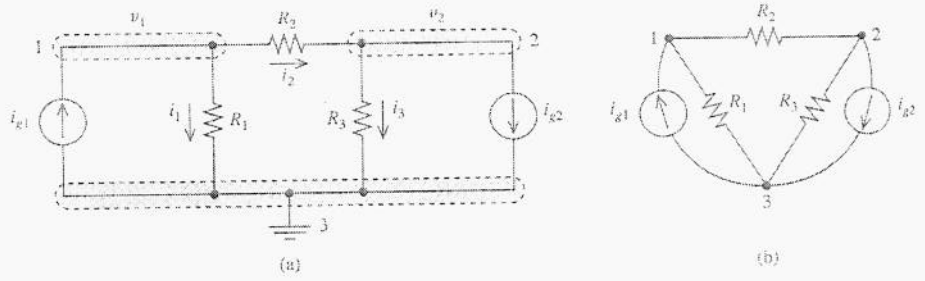


FIGURE 4.9 Circuit containing independent current sources.

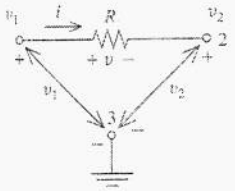


FIGURE 4.10 Single element.

Before writing the node equations, consider the element shown in Fig. 4.10, where v_1 and v_2 are node voltages. The element voltage v is given by

$$v = v_1 - v_2$$

and thus by Ohm's law we have

$$i = \frac{v}{R} = \frac{v_1 - v_2}{R}$$

or

$$i = G(v_1 - v_2)$$

where $G = 1/R$ is the conductance. That is, *the current from node 1 to node 2 through a resistor is the difference of the node voltage at node 1 and the node voltage at node 2 divided by the resistance R, or multiplied by the conductance G.* This relation will allow us to write the node equations rapidly by inspection directly in terms of the node voltages.

Now returning to the circuit of Fig. 4.9, the sum of the currents leaving node 1 must be zero, or

$$i_1 + i_2 - i_{g1} = 0$$

In terms of the node voltages, this equation becomes

$$G_1 v_1 + G_2(v_1 - v_2) - i_{g1} = 0$$

We could have obtained this equation directly using the procedure of the preceding paragraph. Applying KCL at node 2 in a similar manner, we obtain

$$-i_2 + i_3 + i_{g2} = 0$$

or

$$G_2(v_2 - v_1) + G_3 v_2 + i_{g2} = 0$$

Instead of summing currents leaving the node to zero, we could have used the form of KCL that equates the sum of currents leaving the node to the sum of currents entering the node. Had we done so, the terms i_{g1} and i_{g2} would have appeared on the right-hand side:

$$G_1 v_1 + G_2(v_1 - v_2) = i_{g1}$$

$$G_2(v_2 - v_1) + G_3 v_2 = -i_{g2}$$

Rearranging these two equations results in

$$(G_1 + G_2)v_1 - G_2 v_2 = i_{g1} \tag{4.8a}$$

$$-G_2 v_1 + (G_2 + G_3)v_2 = -i_{g2} \tag{4.8b}$$

These equations exhibit a symmetry that may be used to write the equations in the rearranged form (4.8) directly by inspection of the circuit diagram. In (4.8a) the coefficient of v_1 is the sum of conductances of the elements connected to node 1, while the coefficient of v_2 is the negative of the conductance of the element connecting node 1 to node 2. The same statement holds for (4.8b) if the numbers 1 and 2 are interchanged. Thus node 2 plays the role in (4.8b) of node 1 in (4.8a). That is, it is the node at which KCL is applied. In each equation the right-hand side is the current from the current sources that enters the corresponding node.

In general, in networks containing only conductances and current sources, KCL applied at the kth node, with node voltage v_k, may be written as follows. *On the left*

*side of the node k equation, the coefficient of the k*th*-node voltage is the sum of the conductances connected to node k, and the coefficients of the other node voltages are the negatives of the conductances between those nodes and node k. The right side of this equation consists of the net current flowing into node k due to current sources.*

This predictable pattern makes it easy to write down the node equations. Note that the signs, positive on the left-hand side for v_k terms and negative for other node voltage terms, and positive on the right-hand side for current sources flowing into node k, are a consequence of the form of KCL chosen. While other forms could be used quite as correctly, we advocate sticking to the form recommended, with the payoff that the terms will always fall in this pattern. It helps to make the pattern of signs fixed and predictable, so we can focus our attention on the larger issues when analyzing a circuit.

Nodal analysis consists in writing KCL node equations described above at all nonreference nodes in the circuit. This yields $N - 1$ linear equations in a similar number of unknowns (the node voltages). As discussed in Appendix C, these equations are linearly independent and thus are guaranteed to possess a unique solution. The node voltages may be found by a variety of means, including Gauss elimination, Cramer's rule, and matrix inversion.

Example 4.6

Consider the circuit of Fig. 4.11. The bottom node has been selected as the reference node since so many elements connect to it. The resistors are labeled according to their conductances.

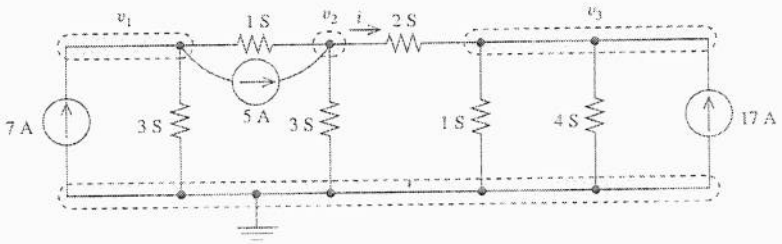


FIGURE 4.11 Circuit for Example 4.6.

Since there are three nonreference nodes, there will be three equations in three unknown node voltages. At node v_1, we note that the sum of conductances is $3 + 1 = 4$, the negative of the conductance connecting node v_2 to node v_1 is -1, and the net source current entering node 1 is $7 - 5 = 2$. Thus the first node equation is

$$4v_1 - v_2 = 2 \tag{4.9}$$

Similarly, at nodes v_2 and v_3, we have

$$-v_1 + 6v_2 - 2v_3 = 5 \tag{4.10a}$$

$$-2v_2 + 7v_3 = 17 \tag{4.10b}$$

We may solve (4.9) and (4.10) for the node voltages using any one of a variety of methods for solving simultaneous equations. Three such methods are matrix inversion, Cramer's rule, and

Gaussian elimination. For the reader who is not familiar with these methods, a discussion is given in Appendix A. Selecting Cramer's rule, first find the determinant of the coefficient matrix, given by

$$\Delta = \begin{vmatrix} 4 & -1 & 0 \\ -1 & 6 & -2 \\ 0 & -2 & 7 \end{vmatrix} = 145 \tag{4.11}$$

To determine v_1, we replace the first column of the coefficient matrix by the vector of constants on the right-hand side of (4.9)–(4.10), compute its determinant, and divide by the determinant of the coefficient matrix already found.

$$v_1 = \frac{\begin{vmatrix} 2 & -1 & 0 \\ 5 & 6 & -2 \\ 17 & -2 & 7 \end{vmatrix}}{\Delta} = 1 \text{ V}$$

v_2 is found by replacing the second and v_3 the third column of the coefficient matrix and calculating as above, yielding $v_2 = 2$ V and $v_3 = 3$ V.

Now that we have broken the circuit by finding the node voltages, we may easily find any other voltage or current. For example, if we want the current i in the 2-S element, it is given by

$$i = 2(v_2 - v_3) = 2(2 - 3) = -2 \text{ A}$$

Note that the coefficient matrix shown in (4.11) is symmetric [the (i, j) and (j, i) elements are equal]. This follows from the fact that the conductance between nodes i and j is that between nodes j and i. Symmetry further simplifies writing the node equations. While symmetry will hold as a general rule for all circuits not containing dependent sources, symmetry of the coefficient matrix cannot be counted on in that case, as we shall see in the next example.

Example 4.7

Consider the circuit of Fig. 4.12, which contains dependent current sources. We will begin by writing the node equations exactly as if the sources were independent. At node 1,

$$(1)(v_1) + (1)(v_1) + (2)(v_1 - v_2) = 5 - 5i$$

and at node 2,

$$\tfrac{1}{2}(v_2) + (2)(v_2 - v_1) = 5i + 2v$$

We next express the controlling variables for the dependent sources, i and v in these equations, in terms of the node voltages. By Ohm's law,

$$i = v_1$$

and by inspection

$$v = v_1 - v_2$$

Substituting the last two equations into the preceding two,

$$(1)(v_1) + (1)(v_1) + (2)(v_1 - v_2) = 5 - 5v_1$$

$$\tfrac{1}{2}(v_2) + (2)(v_2 - v_1) = 5v_1 + 2(v_1 - v_2)$$

These two equations in two unknowns can be solved by Cramer's rule, matrix inversion, or Gauss elimination, as desired. Selecting matrix inversion, we first rewrite as

$$\begin{bmatrix} 9 & -2 \\ -9 & \frac{9}{2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 5 \\ 0 \end{bmatrix} \tag{4.12}$$

The determinant of the coefficient matrix is $(9)\left(\frac{9}{2}\right) - (-9)(-2) = 45/2$ and the inverse is

$$\frac{2}{45}\begin{bmatrix} \frac{9}{2} & 2 \\ 9 & 9 \end{bmatrix} = \begin{bmatrix} \frac{1}{5} & \frac{4}{45} \\ \frac{2}{5} & \frac{2}{5} \end{bmatrix}$$

Then

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{5} & \frac{4}{45} \\ \frac{2}{5} & \frac{2}{5} \end{bmatrix} \begin{bmatrix} 5 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 \\ 2 \end{bmatrix}$$

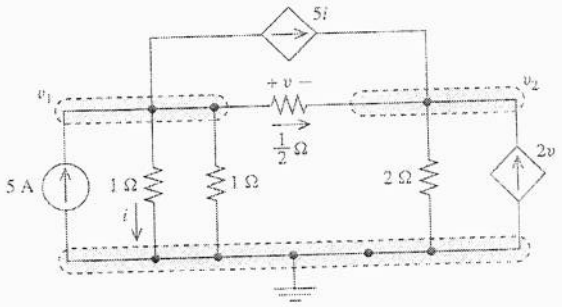
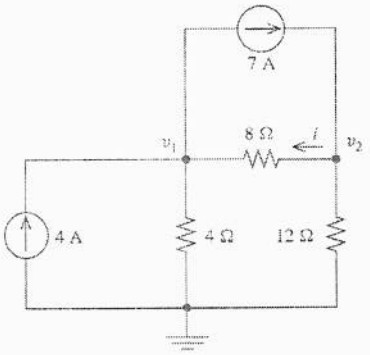


FIGURE 4.12 Circuit containing dependent sources.

From Example 4.7 we see that the presence of dependent sources destroys the symmetry in the coefficient matrix [see (4.12)] and that in such circuits the elements of this matrix may no longer simply be interpreted as sums of conductances, since the dependent sources also contribute. On the other hand, the presence of dependent sources has not significantly complicated nodal analysis, requiring only an additional substitution step, replacing controlling variables by node voltages.

EXERCISES

4.3.1. Take all resistors in Fig. 4.9 to be 1 Ω and both current source functions to be 1 A. Using nodal analysis, find the node voltages and the three labeled currents.



EXERCISE 4.3.2

Answer $v_1 = 1$ V; $v_2 = -1$ V; $i_1 = 1$ A; $i_2 = 2$ A; $i_3 = -1$ A

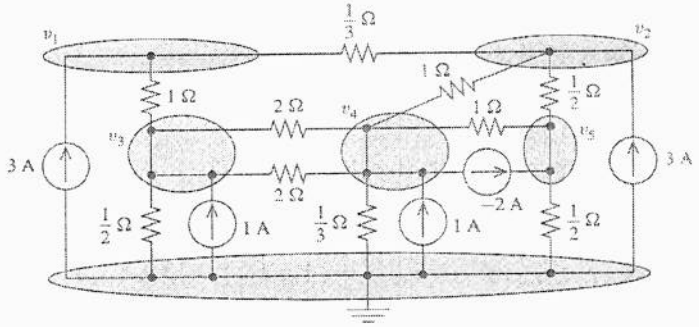
4.3.2. Using nodal analysis, find v_1, v_2, and i.

Answer 4 V; 36 V; 4 A

4.3.3. Write the nodal equations directly in vector-matrix form. Do not solve.

Answer

$$\begin{bmatrix} 4 & -3 & -1 & 0 & 0 \\ -3 & 6 & 0 & -1 & -2 \\ -1 & 0 & 4 & -1 & 0 \\ 0 & -1 & -1 & 6 & -1 \\ 0 & -2 & 0 & -1 & 5 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix} = \begin{bmatrix} 3 \\ 3 \\ 1 \\ 3 \\ -2 \end{bmatrix}$$



EXERCISE 4.3.3

4.4 CIRCUITS CONTAINING VOLTAGE SOURCES

At first glance it may seem that the presence of voltage sources in a circuit complicates nodal analysis. We can no longer write the KCL node equations, since there is no way to express the currents through these circuit elements in terms of their node voltages. As discussed in Chapter 2, the element law for a voltage source does not relate its current to its voltage, so we cannot use it to replace a current unknown by a voltage unknown in the node equation.

However, as we shall see, nodal analysis in the presence of voltage sources proves no more complicated, requiring only a small modification to the basic method for writing the equations of nodal analysis presented in Section 4.3. In fact, we will come to welcome voltage sources, since they reduce the number of simultaneous node equations that must be solved, yielding one less equation per voltage source.

Example 4.8

To illustrate the procedure, let us consider the circuit of Fig. 4.13. For convenience we have labeled the resistors by their conductances. Note that we have enclosed voltage sources in separate regions indicated by dashed lines. Recalling that the generalized form of KCL states that all currents entering a closed region must sum to zero

EXHIBIT 11

FOURTH EDITION

MICROELECTRONIC CIRCUITS

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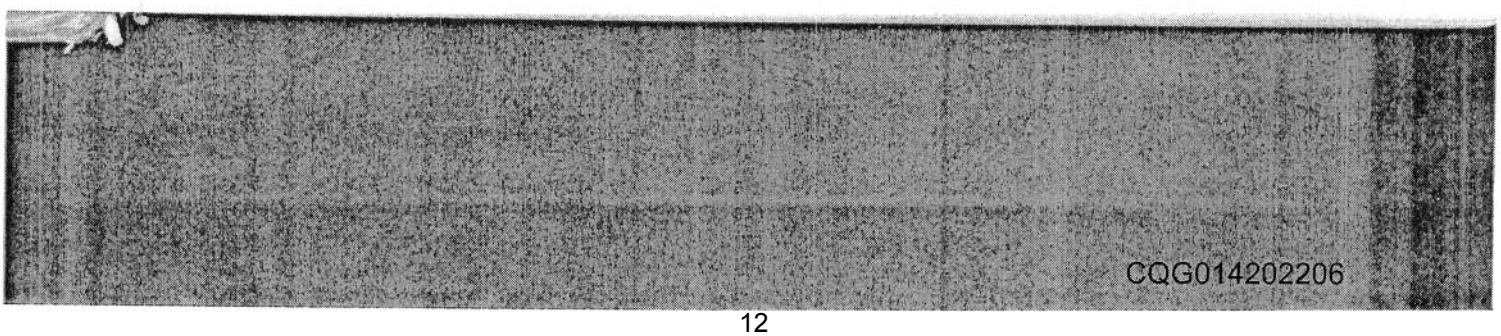

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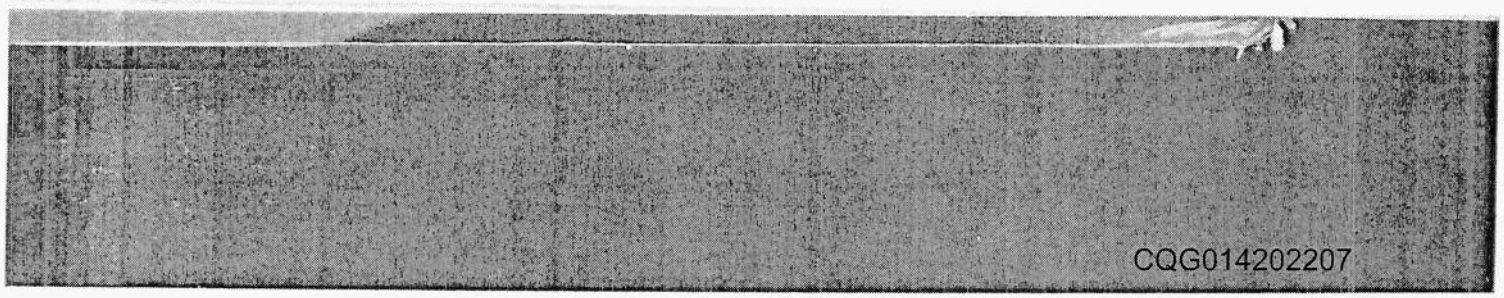
Cover Illustration: The chip shown is the ADXL-50 surface-micromachined accelerometer. For the first time, sensor and signal conditioning are combined on a single monolithic chip. In its earliest application, it was a key factor in the improved reliability and reduced cost of modern automotive airbag systems. Photo reprinted with permission of Analog Devices, Inc.



The basic building blocks of digital systems are logic circuits and memory circuits. We shall study both in this book, beginning in Section 1.7 with the most fundamental digital circuit, the digital logic inverter.

One final remark: Although the digital processing of signals is at present all-pervasive, there remain many signal processing functions that are best performed by analog circuits. Indeed, many electronic systems include both analog and digital parts. It follows that a good electronics engineer must be proficient in the design of both analog and digital circuits. Such is the aim of this book.

Exercise

1.4 Consider a 4-bit digital word $D = b_3b_2b_1b_0$ (see Eq. 1.3) used to represent an analog signal v_A that varies between 0 V and +15 V.

(a) Give D corresponding to $v_A = 0$ V, 1 V, 2 V, and 15 V.

(b) What change in v_A causes a change from 0 to 1 in: (i) b_0, (ii) b_1, (iii) b_2, and (iv) b_3?

(c) If $v_A = 5.2$ V, what do you expect D to be? What is the resulting error in representation?

Ans. (a) 0000, 0001, 0010, 1111; (b) +1 V, +2 V, +4 V, +8 V; (c) 0101, −4%

1.4 AMPLIFIERS

In this section, we shall introduce a fundamental signal-processing function that is employed in some form in almost every electronic system, namely, signal amplification.

Signal Amplification

From a conceptual point of view the simplest signal-processing task is that of **signal amplification.** The need for amplification arises because transducers provide signals that are said to be "weak," that is, in the microvolt (μV) or millivolt (mV) range and possessing little energy. Such signals are too small for reliable processing, and processing is much easier if the signal magnitude is made larger. The functional block that accomplishes this task is the **signal amplifier.**

It is appropriate at this point to discuss the need for **linearity** in amplifiers. When amplifying a signal, care must be exercised so that the information contained in the signal is not changed and no new information is introduced. Thus when feeding the signal shown in Fig. 1.2 to an amplifier, we want the output signal of the amplifier to be an exact replica of that at the input, except of course for having larger magnitude. In other words, the "wiggles" in the output waveform must be identical to those in the input waveform. Any change in waveform is considered to be **distortion** and is obviously undesirable.

An amplifier that preserves the details of the signal waveform is characterized by the relationship

$$v_o(t) = Av_i(t) \tag{1.4}$$

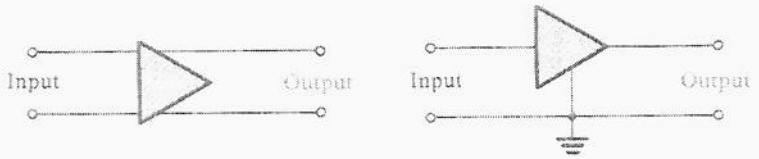
where v_i and v_o are the input and output signals, respectively, and A is a constant representing the magnitude of amplification, known as **amplifier gain.** Equation (1.4) is a linear relationship; hence the amplifier it describes is a **linear amplifier.** It should be easy to see that if the relationship between v_o and v_i contains higher powers of v_i, then the waveform of v_o will no longer be identical to that of v_i. The amplifier is then said to exhibit **nonlinear distortion.**

The amplifiers discussed so far are primarily intended to operate on very small input signals. Their purpose is to make the signal magnitude larger and therefore are thought of as **voltage amplifiers.** The **preamplifier** in the home stereo system is an example of a voltage amplifier. However, it usually does more than just amplify the signal; specifically, it performs some shaping of the frequency spectrum of the input signal. This topic, however, is beyond our need at this moment.

At this time we wish to mention another type of amplifier, namely, the power amplifier. Such an amplifier may provide only a modest amount of voltage gain but substantial current gain. Thus while absorbing little power from the input signal source to which it is connected, often a preamplifier, it delivers large amounts of power to its load. An example is found in the power amplifier of the home stereo system, whose purpose is to provide sufficient power to drive the loudspeaker. Here we should note that the loudspeaker is the output transducer of the stereo system: it converts the electric output signal of the system into an acoustic signal. A further appreciation of the need for linearity can be acquired by reflecting on the power amplifier. A linear power amplifier causes both soft and loud music passages to be reproduced without distortion.

Amplifier Circuit Symbol

The signal amplifier is obviously a two-port network. Its function is conveniently represented by the circuit symbol of Fig. 1.10(a). This symbol clearly distinguishes the input and output ports and indicates the direction of signal flow. Thus, in subsequent diagrams it will not be necessary to label the two ports "input" and "output." For generality we have shown the amplifier to have two input terminals that are distinct from the two output terminals. A more common situation is illustrated in Fig. 1.10(b), where a common terminal exists between the input and output ports of the amplifier. This common terminal is used as a reference point and is called the **circuit ground.**



(a) (b)

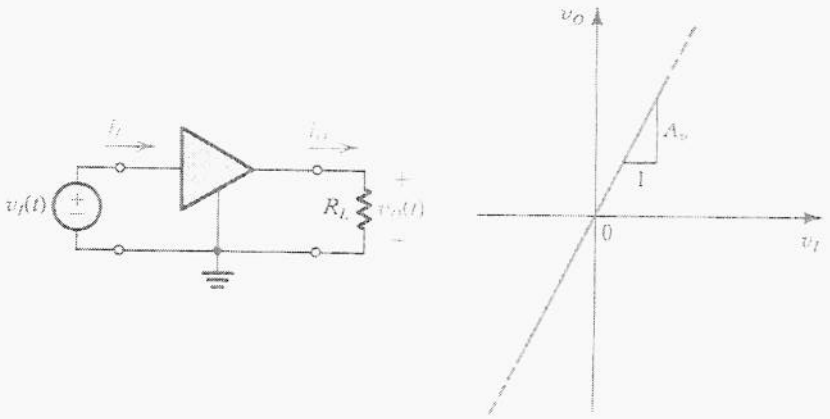
Fig. 1.10 (a) Circuit symbol for amplifier. (b) An amplifier with a common terminal (ground) between the input and output ports.

Voltage Gain

A linear amplifier accepts an input signal $v_I(t)$ and provides at the output, across a load resistance R_L (see Fig. 1.11(a)), an output signal $v_O(t)$ that is a magnified replica of $v_I(t)$. The **voltage gain** of the amplifier is defined by

$$\text{Voltage gain } (A_v) \equiv \frac{v_O}{v_I} \tag{1.5}$$

Fig. 1.11(b) shows the **transfer characteristic** of a linear amplifier. If we apply to the input of this amplifier a sinusoidal voltage of amplitude $\hat{V}$, we obtain at the output a sinusoid of amplitude $A_v\hat{V}$.



(a) (b)

Fig. 1.11 **(a)** A voltage amplifier fed with a signal $v_I(t)$ and connected to a load resistance R_L. **(b)** Transfer characteristic of a linear voltage amplifier with voltage gain A_v.

Power Gain and Current Gain

An amplifier increases the signal power, an important feature that distinguishes an amplifier from a transformer. In the case of a transformer, although the voltage delivered to the load could be greater than the voltage feeding the input side (the primary), the power delivered to the load (from the transformer secondary) is less than or at most equal to the power supplied by the signal source. On the other hand, an amplifier provides the load with power greater than that obtained from the signal source. That is, amplifiers have power gain. The **power gain** of the amplifier in Fig. 1.11(a) is defined as

$$\text{Power gain } (A_p) \equiv \frac{\text{load power } (P_L)}{\text{input power } (P_I)} \tag{1.6}$$

$$\equiv \frac{v_O i_O}{v_I i_I} \tag{1.7}$$

where i_O is the current that the amplifier delivers to the load (R_L), $i_O = v_O/R_L$, and i_I is the current the amplifier draws from the signal source. The **current gain** of the amplifier is defined as

$$\text{Current gain } (A_i) = \frac{i_O}{i_I} \tag{1.8}$$

From Eqs. (1.5) to (1.8) we note that

$$A_p = A_v A_i \tag{1.9}$$

Expressing Gain in Decibels

The amplifier gains defined above are ratios of similarly dimensioned quantities. Thus they will be expressed either as dimensionless numbers or, for emphasis, as V/V for the voltage gain, A/A for the current gain, and W/W for the power gain. Alternatively, for a number of reasons, some of them historic, electronics engineers express amplifier gain with a logarithmic measure. Specifically the voltage gain A_v can be expressed as

$$\text{Voltage gain in decibels} = 20 \log|A_v| \quad \text{dB}$$

and the current gain A_i can be expressed as

$$\text{Current gain in decibels} = 20 \log|A_i| \quad \text{dB}$$

Since power is related to voltage (or current) squared, the power gain A_p can be expressed in decibels as follows:

$$\text{Power gain in decibels} = 10 \log A_p \quad \text{dB}$$

The absolute values of the voltage and current gains are used because in some cases A_v or A_i may be negative numbers. A negative gain A_v simply means that there is a 180° phase difference between input and output signals; it does not imply that the amplifier is **attenuating** the signal. On the other hand, an amplifier whose voltage gain is, say, −20 dB is in fact attenuating the input signal by a factor of 10 (that is, $A_v = 0.1$ V/V).

The Amplifier Power Supplies

Since the power delivered to the load is greater than the power drawn from the signal source, the question arises as to the source of this additional power. The answer is found by observing that amplifiers need dc power supplies for their operation. These dc sources supply the extra power delivered to the load as well as any power that might be dissipated in the internal circuit of the amplifier (such power is converted to heat). In Fig. 1.11(a) we have not explicitly shown these dc sources.

Figure 1.12(a) shows an amplifier that requires two dc sources: one positive of value V_1 and one negative of value V_2. The amplifier has two terminals, labeled V^+ and V^-, for connection to the dc supplies. For the amplifier to operate, the terminal labeled V^+ has to be connected to the positive side of a dc source whose voltage is V_1 and whose negative side is connected to the circuit ground. Also, the terminal labeled V^- has to be connected to the negative side of a dc source whose voltage is V_2 and whose positive side is connected

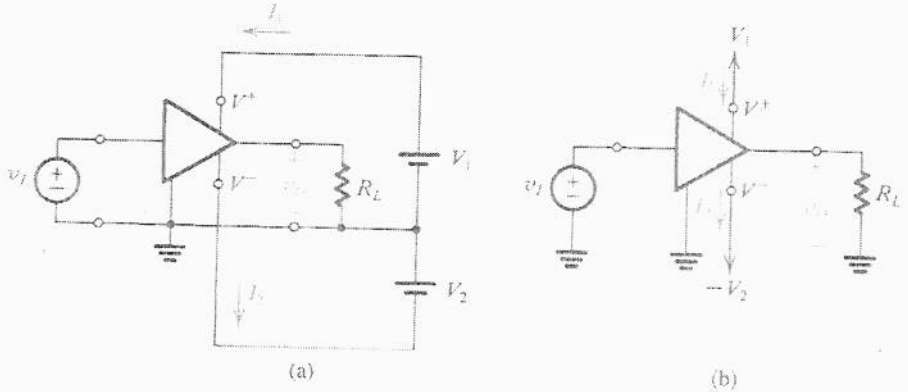


Fig. 1.12 An amplifier that requires two dc supplies (shown as batteries) for operation.

to the circuit ground. Now, if the current drawn from the positive supply is denoted I_1 and that from the negative supply is I_2 (see Fig. 1.12(a)), then the dc power delivered to the amplifier is

$$P_{dc} = V_1 I_1 + V_2 I_2$$

If the power dissipated in the amplifier circuit is denoted $P_{\text{dissipated}}$, the power-balance equation for the amplifier can be written as

$$P_{dc} + P_I = P_L + P_{\text{dissipated}}$$

where P_I is the power drawn from the signal source, and P_L is the power delivered to the load. Since the power drawn from the signal source is usually small, the amplifier **efficiency** is defined as

$$\eta = \frac{P_L}{P_{dc}} \times 100 \tag{1.10}$$

The power efficiency is an important performance parameter for amplifiers that handle large amounts of power. Such amplifiers, called power amplifiers, are used, for example, as output amplifiers of stereo systems.

In order to simplify circuit diagrams, we shall adopt the convention illustrated in Fig. 1.12(b). Here the V^+ terminal is shown connected to an arrowhead pointing upward and the V^- terminal to an arrowhead pointing downward. The corresponding voltage is indicated next to each arrowhead. Note that in many cases we will not explicitly show the connections of the amplifier to the dc power sources. Finally, we note that some amplifiers require only one power supply.

EXAMPLE 1.1

Consider an amplifier operating from ±10-V power supplies. It is fed with a sinusoidal voltage having 1 V peak and delivers a sinusoidal voltage output of 9 V peak to a 1-kΩ load. The amplifier draws a current of 9.5 mA from each of its two power supplies. The

input current of the amplifier is found to be sinusoidal with 0.1 mA peak. Find the voltage gain, the current gain, the power gain, the power drawn from the dc supplies, the power dissipated in the amplifier, and the amplifier efficiency.

SOLUTION

$$A_v = \frac{9}{1} = 9 \text{ V/V}$$

or

$$A_v = 20 \log 9 = 19.1 \text{ dB}$$

$$\hat{I}_o = \frac{9 \text{ V}}{1 \text{ k}\Omega} = 9 \text{ mA}$$

$$A_i = \frac{\hat{I}_o}{\hat{I}_i} = \frac{9}{0.1} = 90 \text{ A/A}$$

or

$$A_i = 20 \log 90 = 39.1 \text{ dB}$$

$$P_L = V_{o\text{rms}} I_{o\text{rms}} = \frac{9}{\sqrt{2}} \frac{9}{\sqrt{2}} = 40.5 \text{ mW}$$

$$P_I = V_{i\text{rms}} I_{i\text{rms}} = \frac{1}{\sqrt{2}} \frac{0.1}{\sqrt{2}} = 0.05 \text{ mW}$$

$$A_p = \frac{P_L}{P_I} = \frac{40.5}{0.05} = 810 \text{ W/W}$$

or

$$A_p = 10 \log 810 = 29.1 \text{ dB}$$

$$P_{\text{dc}} = 10 \times 9.5 + 10 \times 9.5 = 190 \text{ mW}$$

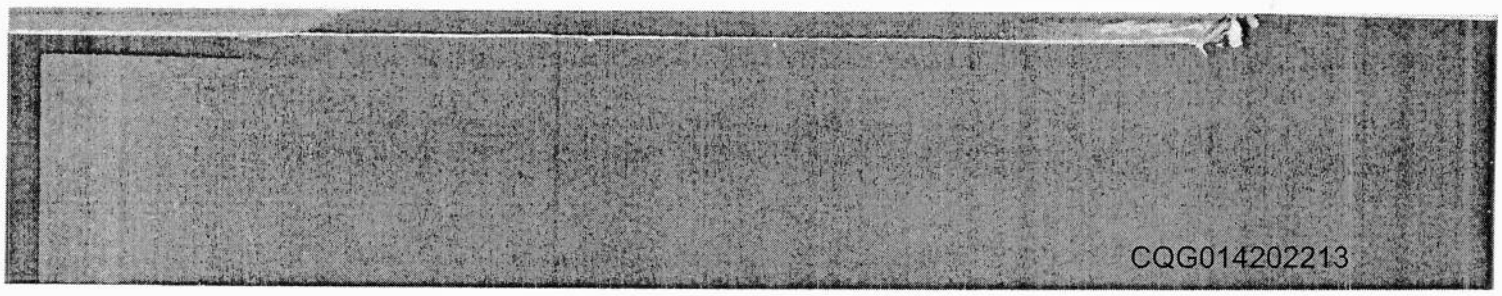
$$P_{\text{dissipated}} = P_{\text{dc}} + P_I - P_L$$
$$= 190 + 0.05 - 40.5 = 149.6 \text{ mW}$$

$$\eta = \frac{P_L}{P_{\text{dc}}} \times 100 = 21.3\%$$

From the above example we observe that the amplifier converts some of the dc power it draws from the power supplies to signal power that it delivers to the load.

Amplifier Saturation

Practically speaking, the amplifier transfer characteristic remains linear over only a limited range of input and output voltages. For an amplifier operated from two power supplies the output voltage cannot exceed a specified positive limit and cannot decrease below a specified



negative limit. The resulting transfer characteristic is shown in Fig. 1.13, with the positive and negative saturation levels denoted L_+ and L_-, respectively. Each of the two saturation levels is usually within 1 or 2 volts of the voltage of the corresponding power supply.

Obviously, in order to avoid distorting the output signal waveform, the input signal swing must be kept within the linear range of operation.

$$\frac{L_-}{A_v} \leq v_I \leq \frac{L_+}{A_v}$$

Figure 1.13 shows two input waveforms and the corresponding output waveforms. We note that the peaks of the larger waveform have been clipped off because of amplifier saturation.

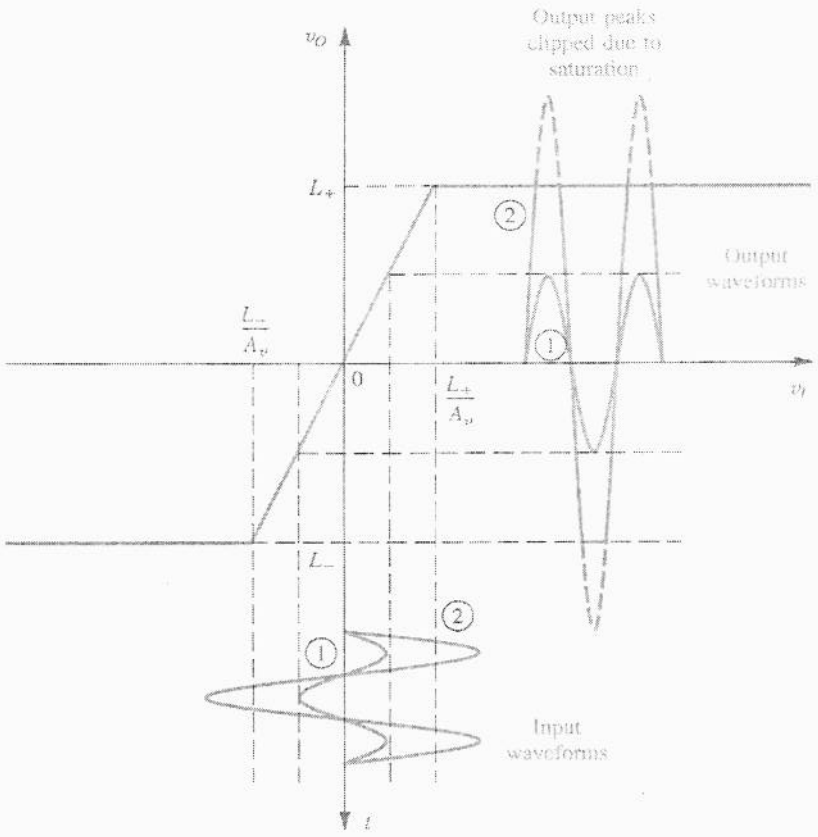
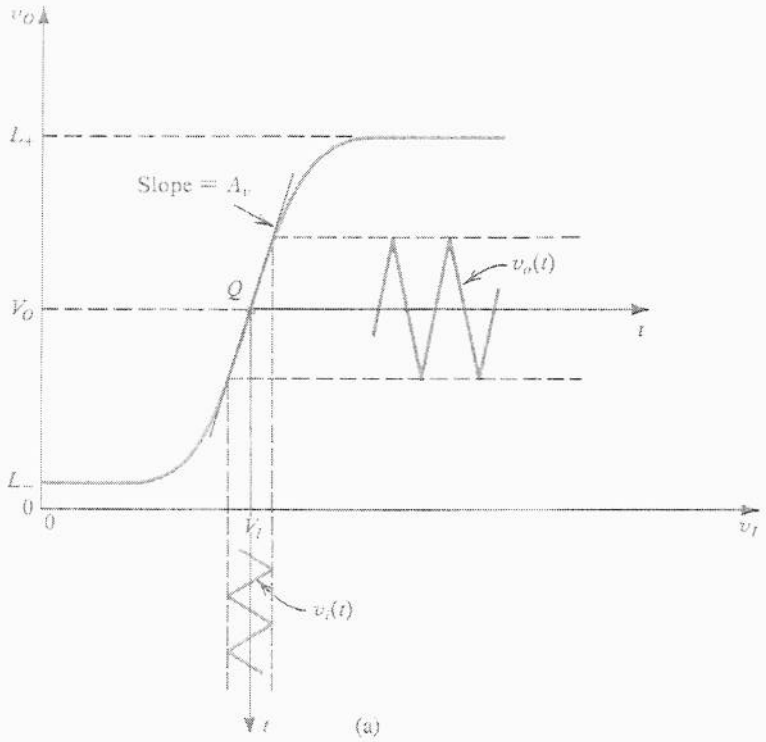


Fig. 1.13 An amplifier transfer characteristic that is linear except for output saturation.

Nonlinear Transfer Characteristics and Biasing

Except for the output saturation effect discussed above, the amplifier transfer characteristics have been assumed to be perfectly linear. In practical amplifiers the transfer characteristic

may exhibit nonlinearities of various magnitudes, depending on how elaborate the amplifier circuit is, and on how much effort has been expended in the design to ensure linear operation. Consider as an example the transfer characteristic depicted in Fig. 1.14. Such a characteristic is typical of simple amplifiers that are operated from a single (positive) power supply. The transfer characteristic is obviously nonlinear and, because of the single-supply operation, is



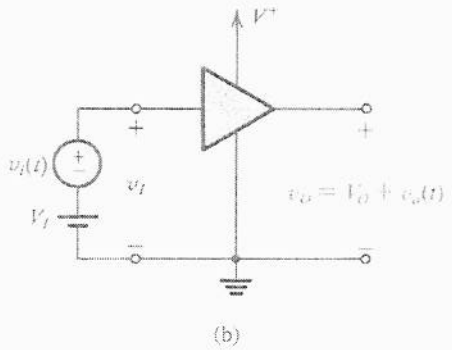


Fig. 1.14 (a) An amplifier transfer characteristic that shows considerable nonlinearity. (b) To obtain linear operation the amplifier is biased as shown, and the signal amplitude is kept small.

not centered around the origin. Fortunately, a simple technique exists for obtaining linear amplification from an amplifier with such a nonlinear transfer characteristic.

The technique consists of first **biasing** the circuit to operate at a point near the middle of the transfer characteristic. This is achieved by applying a dc voltage V_I, as indicated in Fig. 1.14, where the operating point is labeled Q and the corresponding dc voltage at the output is V_O. The point Q is known as the **quiescent point**, the **dc bias point**, or simply the **operating point**. The time-varying signal to be amplified, $v_i(t)$, is then superimposed on the dc bias voltage V_I as indicated in Fig. 1.14. Now, as the total instantaneous input $v_I(t)$,

$$v_I(t) = V_I + v_i(t)$$

varies around V_I, the instantaneous operating point moves up and down the transfer curve around the operating point Q. In this way, one can determine the waveform of the total instantaneous output voltage $v_O(t)$. It can be seen that by keeping the amplitude of $v_i(t)$ sufficiently small, the instantaneous operating point can be confined to an almost linear segment of the transfer curve centered about Q. This in turn results in the time-varying portion of the output being proportional to $v_i(t)$; that is,

$$v_O(t) = V_O + v_o(t)$$

with

$$v_o(t) = A_v v_i(t)$$

where A_v is the slope of the almost linear segment of the transfer curve; that is,

$$A_v = \left.\frac{dv_O}{dv_I}\right|_{\text{at } Q}$$

In this manner, linear amplification is achieved. Of course, there is a limitation: The input signal must be kept sufficiently small. Increasing the amplitude of the input signal can cause the operation to be no longer restricted to an almost linear segment of the transfer curve. This in turn results in a distorted output signal waveform. Such nonlinear distortion is undesirable: The output signal contains additional spurious information that is not part of the input. We shall use this biasing technique and the associated small-signal approximation frequently in the design of transistor amplifiers.

EXAMPLE 1.2

A transistor amplifier has the transfer characteristic

$$v_O = 10 - 10^{-11} e^{40 v_I} \tag{1.11}$$

which applies for $v_I \geq 0$ V and $v_O \geq 0.3$ V. Find the limits L_- and L_+ and the corresponding values of v_I. Also, find the value of the dc bias voltage V_I that results in $V_O = 5$ V and the voltage gain at the corresponding operating point.

SOLUTION

The limit L_- is obviously 0.3 V. The corresponding value of v_I is obtained by substituting $v_O = 0.3$ V in Eq. (1.10); that is,

$$v_I = 0.690 \text{ V}$$

The limit L_+ is determined by $v_I = 0$ and is thus given by

$$L_+ = 10 - 10^{-11} \simeq 10 \text{ V}$$

To bias the device so that $V_O = 5$ V we require a dc input V_I whose value is obtained by substituting $v_O = 5$ V in Eq. (1.10) to find:

$$V_I = 0.673 \text{ V}$$

The gain at the operating point is obtained by evaluating the derivative dv_O/dv_I at $v_I = 0.673$ V. The result is

$$A_v = -200 \text{ V/V}$$

which indicates that this amplifier in an inverting one, that is, the output is 180° out of phase with the input. A sketch of the amplifier transfer characteristic (not to scale) is shown in Fig. 1.15, from which we observe the inverting nature of the amplifier.

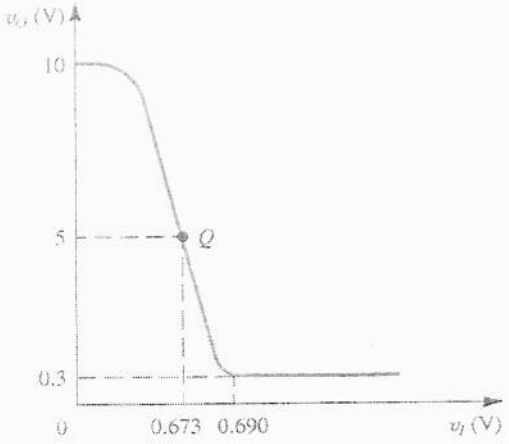


Fig. 1.15 A sketch of the transfer characteristic of the amplifier of Example 1.2. Note that this amplifier is inverting (that is, with a gain that is negative).

Once an amplifier is properly biased and the input signal is kept sufficiently small, the operation is assumed to be linear. We can then employ the techniques of linear circuit analysis to analyze the signal operation of the amplifier circuit. The following two sections provide a review and application of these analysis techniques.

Symbol Convention

At this point, we draw the reader's attention to the terminology used above and which we shall employ throughout the book. Total instantaneous quantities are denoted by a lowercase symbol with an uppercase subscript, for example, $i_A(t)$, $v_C(t)$. Direct-current (dc) quantities will be denoted by an uppercase symbol with an uppercase subscript, for example, I_A, V_C. Finally, incremental signal quantities will be denoted by a lowercase symbol with a lowercase subscript, for example $i_a(t)$, $v_c(t)$. This notation is illustrated in Fig. 1.16.

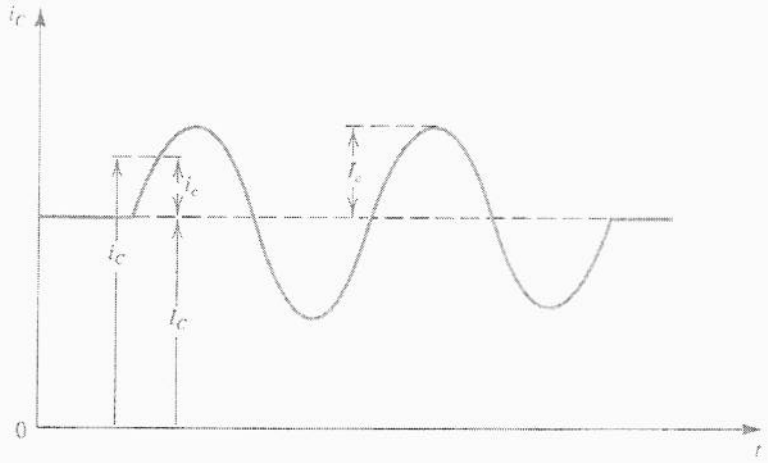


Fig. 1.16 Symbol convention employed throughout the book.

Exercises

1.5 An amplifier has a voltage gain of 100 V/V and a current gain of 1000 A/A. Express the voltage and current gains in decibels and find the power gain.

Ans. 40 dB; 60 dB; 50 dB

1.6 An amplifier operating from a single 15-V supply provides a 12-V peak-to-peak sine-wave signal to a 1-kΩ load, and draws negligible input current from the signal source. The dc current drawn from the 15-V supply is 8 mA. What is the power dissipated in the amplifier and what is the amplifier efficiency?

Ans. 102 mW; 15%

1.7 The objective of this exercise is to investigate the limitation of the small-signal approximation. Consider the amplifier of Example 1.2 with a positive input signal of 1 mV superimposed on the dc bias voltage V_I. Find the corresponding signal at the output for two situations: (a) Assume the amplifier is linear around the operating point; that is, use the value of gain evaluated in Example 1.2. (b) Use the transfer characteristic of the amplifier. Repeat for input signals of 5 mV and 10 mV.

Ans. −0.2 V, −0.204 V; −1 V, −1.107 V; −2 V, −2.459 V

1.5 CIRCUIT MODELS FOR AMPLIFIERS

A good part of this book is concerned with the design of amplifier circuits using transistors of various types. Such circuits will vary in complexity from those using a single transistor to those with 20 or more devices. In order to be able to apply the resulting amplifier circuit as a building block in a system, one must be able to characterize, or **model,** its terminal

amp has characteristics that closely approach the assumed ideal. This implies that it is quite easy to design circuits using the IC op amp. Also, op amp circuits work at levels that are quite close to their predicted theoretical performance. It is for this reason that we are studying op amps at this early stage. It is expected that by the end of this chapter the reader should be able to design nontrivial circuits successfully using op amps.

As already implied, an IC op amp is made up of a large number of transistors, resistors, and (usually) one capacitor connected in a rather complex circuit. Since we have not yet studied transistor circuits, the circuit inside the op amp will not be discussed in this chapter. Rather, we will treat the op amp as a circuit building block and study its terminal characteristics and its applications. This approach is quite satisfactory in many op-amp applications. Nevertheless, for the more difficult and demanding applications it is quite useful to know what is inside the op-amp package. This topic will be studied in Chapter 10. Finally, it should be mentioned that more advanced applications of op amps will appear in later chapters.

2.1 THE OP-AMP TERMINALS

From a signal point of view the op amp has three terminals: two input terminals and one output terminal. Figure 2.1 shows the symbol we shall use to represent the op amp. Terminals 1 and 2 are input terminals, and terminal 3 is the output terminal. As explained in Section 1.4, amplifiers require dc power to operate. Most IC op amps require two dc power supplies, as shown in Fig. 2.2. Two terminals, 4 and 5, are brought out of the op-amp package and connected to a positive voltage V^+ and a negative voltage V^-, respectively. In Fig. 2.2(b) we explicitly show the two dc power supplies as batteries with a common ground. It is interesting to note that the reference grounding point in op-amp circuits is just the common terminal of the two power supplies; that is, no terminal of the op amp package

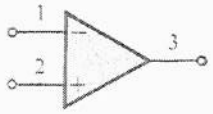


Fig. 2.1 Circuit symbol for the op amp.

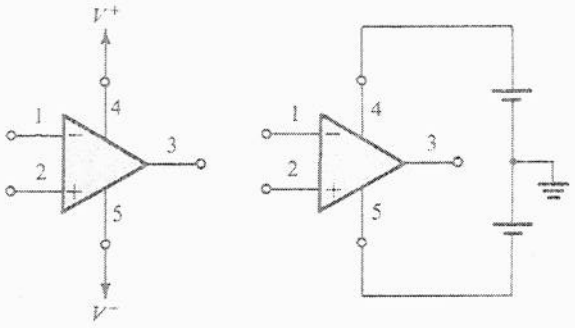


Fig. 2.2 The op amp shown connected to dc power supplies.

is physically connected to ground. In what follows we will not explicitly show the op-amp power supplies.

In addition to the three signal terminals and the two power-supply terminals, an op amp may have other terminals for specific purposes. These other terminals can include terminals for frequency compensation and terminals for offset nulling: both functions will be explained in later sections.

Exercise

2.1 What is the minimum number of terminals required by a single op amp? What is the minimum number of terminals required on an integrated-circuit package containing four op amps (called a quad op amp)?

Ans. 5; 14

2.2 THE IDEAL OP AMP

We now consider the circuit function of the op amp. The op amp is designed to sense the difference between the voltage signals applied at its two input terminals (that is, the quantity $v_2 - v_1$), multiply this by a number A, and cause the resulting voltage $A(v_2 - v_1)$ to appear at output terminal 3. Here it should be emphasized that when we talk about the voltage at a terminal we mean the voltage between that terminal and ground; thus v_1 means the voltage applied between terminal 1 and ground.

The ideal op amp is not supposed to draw any input current; that is, the signal current into terminal 1 and the signal current into terminal 2 are both zero. In other words, the input impedance of an ideal op amp is supposed to be infinite.

How about the output terminal 3? This terminal is supposed to act as the output terminal of an ideal voltage source. That is, the voltage between terminal 3 and ground will always be equal to $A(v_2 - v_1)$ and will be independent of the current that may be drawn from terminal 3 into a load impedance. In other words, the output impedance of an ideal op amp is supposed to be zero.

Putting together all of the above, we arrive at the equivalent circuit model shown in Fig. 2.3. Note that the output is in phase with (has the same sign as) v_2 and out of phase with (has the opposite sign of) v_1. For this reason, input terminal 1 is called the **inverting input terminal** and is distinguished by a "−" sign, while input terminal 2 is called the **noninverting input terminal** and is distinguished by a "+" sign.

As can be seen from the above description, the op amp responds only to the *difference* signal $v_2 - v_1$ and hence ignores any signal *common* to both inputs. That is, if $v_1 = v_2 = 1$ V, then the output will—ideally—be zero. We call this property **common-mode rejection,** and we conclude that an ideal op amp has infinite common-mode rejection. We will have more to say about this point later. For the time being note that the op amp is a **differential-input, single-ended-output** amplifier, with the latter term referring to the fact that the output appears between terminal 3 and ground. Furthermore, gain A is called the **differential gain,** for obvious reasons. Perhaps not so obvious is another name that we will

Exerci

2.2 Con
circuit an
cases, us
and v_3
−3.6 V a

Ans. (a)

11.16 Consider a low-pass notch with $\omega_0 = 1$ rad/s, $Q = 10$, $\omega_n = 1.2$ rad/s, and a dc gain of unity. Find the frequency and magnitude of the transmission peak. Also find the high-frequency transmission.

Ans. 0.986 rad/s; 3.17; 0.69

11.5 THE SECOND-ORDER LCR RESONATOR

In this section we shall study the second-order LCR resonator shown in Fig. 11.17(a). The use of this resonator to derive circuit realizations for the various second-order filter functions will be demonstrated. Also, it will be shown in the next section that replacing the inductor L by a simulated inductance obtained using an op amp–RC circuit results in an op amp–RC resonator. The latter forms the basis of an important class of active-RC filters to be studied in the next section.

The Resonator Natural Modes

The natural modes of the parallel resonance circuit of Fig. 11.17(a) can be determined by applying *an excitation that does not change the natural structure of the circuit*. Two possible ways of exciting the circuit are shown in Figs. 11.17(b) and (c). In Fig. 11.17(b) the resonator is excited with a current source I connected in parallel. Since as far as the natural

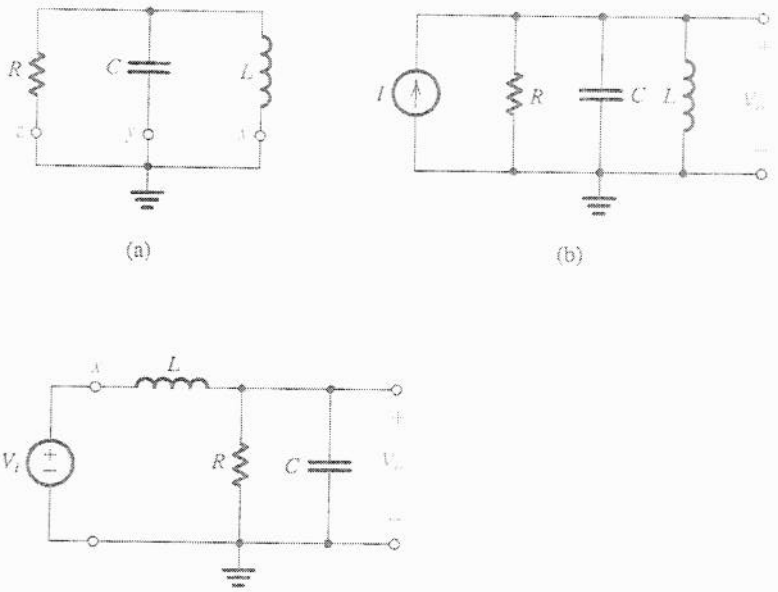


Fig. 11.17 (a) The second-order parallel LCR resonator. (b) and (c) Two ways for exciting the resonator of (a) without changing its *natural structure*. The resonator poles are the poles of V_o/I and V_o/V_i.

response of a circuit is concerned, an independent ideal current source is equivalent to an open circuit, the excitation of Fig. 11.17(b) does not alter the natural structure of the resonator. Thus the circuit in Fig. 11.17(b) can be used to determine the natural modes of the resonator by simply finding the poles of any response function. We can for instance take the voltage V_o across the resonator as the response and thus obtain the response function $V_o/I = Z$, where Z is the impedance of the parallel resonance circuit. It is obviously more convenient, however, to work in terms of the admittance Y; thus

$$\frac{V_o}{I} = \frac{1}{Y} = \frac{1}{(1/sL) + sC + (1/R)} = \frac{s/C}{s^2 + s(1/CR) + (1/LC)} \tag{11.31}$$

Equating the denominator to the standard form $s^2 + s(\omega_0/Q) + \omega_0^2$ leads to

$$\omega_0^2 = 1/LC \tag{11.32}$$

and

$$\omega_0/Q = 1/CR \tag{11.33}$$

Thus,

$$\omega_0 = 1/\sqrt{LC} \tag{11.34}$$

$$Q = \omega_0 CR \tag{11.35}$$

These expressions should be familiar to the reader from earlier studies of parallel resonance circuits in introductory courses on circuit theory.

An alternative way of exciting the parallel LCR resonator for the purpose of determining its natural modes is shown in Fig. 11.17(c). Here, node x of inductor L has been disconnected from ground and connected to an ideal voltage source V_i. Now, since as far as the natural response of a circuit is concerned, an ideal independent voltage source is equivalent to a short circuit, the excitation of Fig. 11.17(c) does not alter the natural structure of the resonator. Thus we can use the circuit in Fig. 11.17(c) to determine the natural modes of the resonator. These are the poles of any response function. For instance, we can select V_o as the response variable and find the transfer function V_o/V_i. The reader can easily verify that this will lead to the natural modes determined above.

In a design problem, we will be given ω_0 and Q and will be asked to determine L, C, and R. Equations (11.34) and (11.35) are two equations in the three unknowns. The one available degree of freedom can be utilized to set the impedance level of the circuit to a value that results in practical component values.

Realization of Transmission Zeros

Having selected the component values of the LCR resonator so as to realize a given pair of complex-conjugate natural modes, we now consider the use of the resonator to realize a desired filter type (e.g., LP, HP, etc.). Specifically, we wish to find out where to inject the input voltage signal V_i so that the transfer function V_o/V_i is the desired one. Toward that end, note that in the resonator circuit in Fig. 11.17(a) any of the nodes labeled x, y, or z can be disconnected from ground and connected to V_i without altering the circuit's natural

modes. When this is done the circuit takes the form of a voltage divider, as shown in Fig. 11.18(a). Thus the transfer function realized is

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{11.36}$$

We observe that *the transmission zeros are the values of s at which $Z_2(s)$ is zero, provided that $Z_1(s)$ is not simultaneously zero, and the values of s at which $Z_1(s)$ is infinite, provided that $Z_2(s)$ is not simultaneously infinite*. This statement makes physical sense: The output will be zero either when $Z_2(s)$ behaves as a short circuit or when $Z_1(s)$ behaves as an open circuit. If there is a value of s at which both Z_1 and Z_2 are zero, then V_o/V_i will be finite and no transmission zero is obtained. Similarly, if there is a value of s at which both Z_1 and Z_2 are infinite, then V_o/V_i will be finite and no transmission zero is realized.

Realization of the Low-Pass Function

Using the scheme outlined above we see that to realize a low-pass function, node x is disconnected from ground and connected to V_i, as shown in Fig. 11.18(b). The transmission zeros of this circuit will be at the value of s for which the series impedance becomes infinite (sL becomes infinite at $s = \infty$) and the value of s at which the shunt impedance becomes zero ($1/[sC + (1/R)]$ becomes zero at $s = \infty$). Thus this circuit has two transmission zeros at $s = \infty$, as an LP is supposed to. The transfer function can be written either by inspection or by using the voltage-divider rule. Following the latter approach, we obtain

$$T(s) = \frac{V_o}{V_i} = \frac{Z_2}{Z_1 + Z_2} = \frac{Y_1}{Y_1 + Y_2} = \frac{1/sL}{(1/sL) + sC + (1/R)} = \frac{1/LC}{s^2 + s(1/CR) + (1/LC)} \tag{11.37}$$

Realization of the High-Pass Function

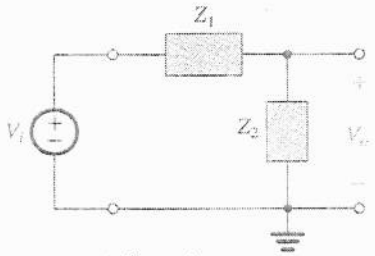
To realize the second-order high-pass function, node y is disconnected from ground and connected to V_i, as shown in Fig. 11.18(c). Here the series capacitor introduces a transmission zero at $s = 0$ (dc), and the shunt inductor introduces another transmission zero at $s = 0$ (dc). Thus, by inspection, the transfer function may be written as

$$T(s) = \frac{V_o}{V_i} = \frac{a_2 s^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \tag{11.38}$$

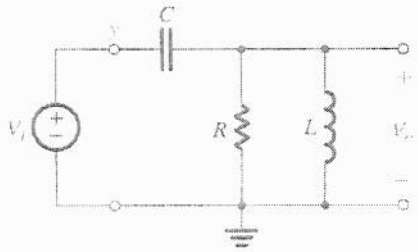
where ω_0 and Q are the natural mode parameters given by Eqs. (11.34) and (11.35) and a_2 is the high-frequency transmission. The value of a_2 can be determined from the circuit by observing that as s approaches ∞, the capacitor approaches a short circuit and V_o approaches V_i, resulting in $a_2 = 1$.

Realization of the Bandpass Function

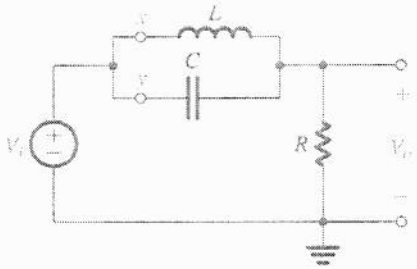
The bandpass function is realized by disconnecting node z from ground and connecting it to V_i, as shown in Fig. 11.18(d). Here the series impedance is resistive, and thus does not



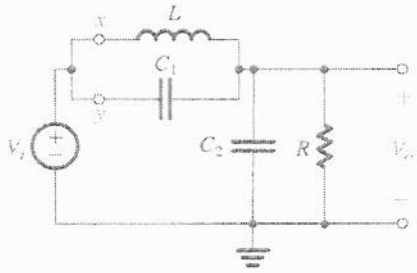
(a) General structure



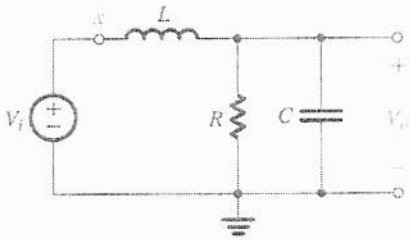
(c) HP



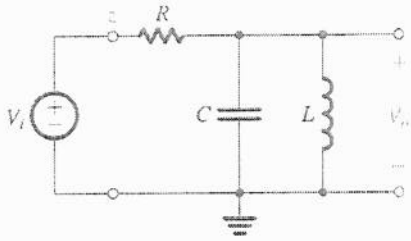
(e) Notch at ω_0



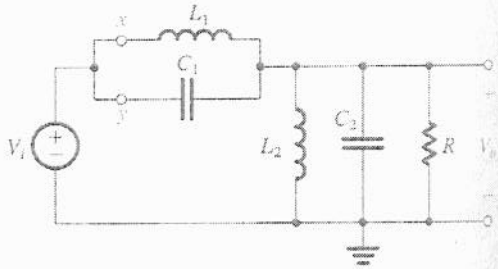
(g) LPN ($\omega_n > \omega_0$)



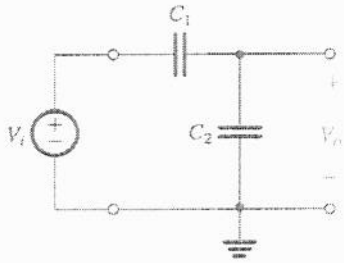
(b) LP



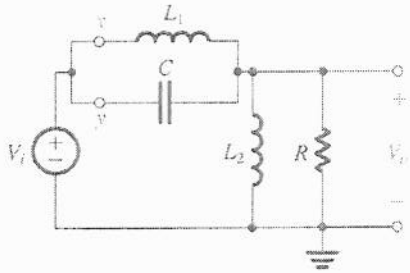
(d) BP



(f) General notch



(h) LPN as $s \to \infty$



(i) HPN ($\omega_n < \omega_0$)

Fig. 11.18 Realization of various second-order filter functions using the LCR resonator of Fig. 11.17(b): (a) general structure, (b) LP, (c) HP, (d) BP, (e) notch at ω_0, (f) general notch, (g) LPN ($\omega_n \geq \omega_0$), (h) LPN as $s \to \infty$, (i) HPN ($\omega_n < \omega_0$).

introduce any transmission zeros. These are obtained as follows: One zero at $s = 0$ is realized by the shunt inductor, and one zero at $s = \infty$ is realized by the shunt capacitor. At the center-frequency ω_0, the parallel LC tuned circuit exhibits an infinite impedance, and thus no current flows in the circuit. It follows that at $\omega = \omega_0$, $V_o = V_i$. In other words, the center-frequency gain of the bandpass filter is unity. Its transfer function can be obtained as follows:

$$T(s) = \frac{Y_R}{Y_R + Y_L + Y_C} = \frac{1/R}{(1/R) + (1/sL) + sC}$$
$$= \frac{s\,(1/CR)}{s^2 + s\,(1/CR) + (1/LC)} \tag{11.39}$$

Realization of the Notch Functions

To obtain a pair of transmission zeros on the $j\omega$-axis we use a parallel resonance circuit in the series arm, as shown in Fig. 11.18(e). Observe that this circuit is obtained by disconnecting both nodes x and y from ground and connecting them together to V_i. The impedance of the LC circuit becomes infinite at $\omega = \omega_0 = 1/\sqrt{LC}$, thus causing zero transmission at this frequency. The shunt impedance is resistive and thus does not introduce transmission zeros. It follows that the circuit in Fig. 11.18(e) will realize the notch transfer function

$$T(s) = a_2 \frac{s^2 + \omega_0^2}{s^2 + s\,(\omega_0/Q) + \omega_0^2} \tag{11.40}$$

The value of the high-frequency gain a_2 can be found from the circuit to be unity.

To obtain a notch filter realization in which the notch frequency ω_n is arbitrarily placed relative to ω_0, we adopt a variation on the above scheme. We still use a parallel LC circuit in the series branch, as shown in Fig. 11.18(f) where L_1 and C_1 are selected so that

$$L_1 C_1 = 1/\omega_n^2 \tag{11.41}$$

Thus the L_1C_1 tank circuit will introduce a pair of transmission zeros at $\pm j\omega_n$, provided that the L_2C_2 tank is not resonant at ω_n. Apart from this restriction, the values of L_2 and C_2 must be selected so as to ensure that the natural modes have not been altered; thus

$$C_1 + C_2 = C \tag{11.42}$$

$$L_1 /\!/ L_2 = L \tag{11.43}$$

In other words, when V_i is replaced by a short circuit, the circuit should reduce to the original LCR resonator. Another way of thinking about the circuit of Fig. 11.18(f) is that it is obtained from the original LCR resonator by lifting part of L and part of C off ground and connecting them to V_i.

It should be noted that in the circuit of Fig. 11.18(f), L_2 does *not* introduce a zero at $s = 0$ because at $s = 0$, the L_1C_1 circuit also has a zero. In fact, at $s = 0$ the circuit reduces to an inductive voltage divider with the dc transmission being $L_2/(L_1 + L_2)$. Similar comments can be made about C_2 and the fact that it does *not* introduce a zero at $s = \infty$.

The LPN and HPN filter realizations are special cases of the general notch circuit of Fig. 11.18(f). Specifically, for the LPN,

$$\omega_n > \omega_0.$$

thus

$$L_1C_1 < (L_1//L_2)(C_1 + C_2)$$

This condition can be satisfied with L_2 eliminated (i.e., $L_2 = \infty$ and $L_1 = L$), resulting in the LPN circuit in Fig. 11.18(g). The transfer function can be written by inspection as

$$T(s) = \frac{V_o}{V_i} = a_2 \frac{s^2 + \omega_n^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \tag{11.44}$$

where $\omega_n^2 = 1/LC_1$, $\omega_0^2 = 1/L(C_1 + C_2)$, $\omega_0/Q = 1/CR$, and a_2 is the high-frequency gain. From the circuit we see that as $s \to \infty$, the circuit reduces to that in Fig. 11.18(h), for which

$$\frac{V_o}{V_i} = \frac{C_1}{C_1 + C_2}$$

Thus

$$a_2 = \frac{C_1}{C_1 + C_2} \tag{11.45}$$

To obtain an HPN realization we start with the circuit of Fig. 11.18(f) and use the fact that $\omega_n < \omega_0$ to obtain

$$L_1C_1 > (L_1//L_2)(C_1 + C_2)$$

which can be satisfied while selecting $C_2 = 0$ (i.e., $C_1 = C$). Thus we obtain the reduced circuit shown in Fig. 11.18(i). Observe that as $s \to \infty$, V_o approaches V_i and thus the high-frequency gain is unity. Thus, the transfer function can be expressed as

$$T(s) = \frac{V_o}{V_i} = \frac{s^2 + (1/L_1C)}{s^2 + s(1/CR) + [1/(L_1//L_2)\,C]} \tag{11.46}$$

Realization of the All-Pass Function

The all-pass transfer function

$$T(s) = \frac{s^2 - s(\omega_0/Q) + \omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \tag{11.47}$$

can be written as

$$T(s) = 1 - \frac{s\,2(\omega_0/Q)}{s^2 + s(\omega_0/Q) + \omega_0^2} \tag{11.48}$$

The second term on the right-hand side is a bandpass function with a center-frequency gain of 2. We already have a bandpass circuit (Fig. 11.18d) but with a center-frequency gain of unity. We shall therefore attempt an all-pass realization with a flat gain of 0.5, that is,

$$T(s) = 0.5 - \frac{s(\omega_0/Q)}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

This function can be realized using a voltage divider with a transmission ratio of 0.5 together with the bandpass circuit of Fig. 11.18(d). To effect the subtraction, the output of the all-

Exercis

11.17 U
with a 3-c

Ans. Sel

11.18 U
at a 60-H
3 dB over
10 kΩ.

Ans. C =
practical i

11.6 SEC

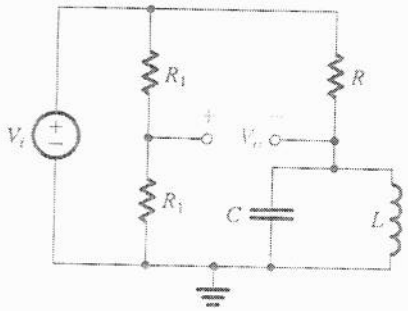


Fig. 11.19 Realization of the second-order all-pass transfer function using a voltage divider and an LCR resonator.

pass circuit is taken between the output terminal of the voltage divider and that of the bandpass filter, as shown in Fig. 11.19. Unfortunately this circuit has the disadvantage of lacking a common ground terminal between the input and the output. An op amp–RC realization of the all-pass function will be presented in the next section.

Exercises

11.17 Use the circuit of Fig. 11.18(b) to realize a second-order low-pass function of the maximally flat type with a 3-dB frequency of 100 kHz.

Ans. Selecting $R = 1\ \text{k}\Omega$, we obtain $C = 1125$ pF and $L = 2.25$ mH.

11.18 Use the circuit of Fig. 11.18(e) to design a notch filter to eliminate a bothersome power-supply hum at a 60-Hz frequency. The filter is to have a 3-dB bandwidth of 10 Hz (i.e., the attenuation is greater than 3 dB over a 10-Hz band around the 60-Hz center frequency; see Exercise 11.15 and Fig. 11.16d). Use $R = 10\ \text{k}\Omega$.

Ans. $C = 1.6\ \mu$F and $L = 4.42$ H (Note the large inductor required. This is the reason passive filters are not practical in low-frequency applications.)

11.6 SECOND-ORDER ACTIVE FILTERS BASED ON INDUCTOR REPLACEMENT

In this section, we study a family of op amp–RC circuits that realize the various second-order filter functions. The circuits are based on an op amp–RC resonator obtained by replacing the inductor L in the LCR resonator with an op amp–RC circuit that has an inductive input impedance.

The Antoniou Inductance-Simulation Circuit

Over the years, many op amp–RC circuits have been proposed for simulating the operation of an inductor. Of these, one circuit invented by A. Antoniou (see Antoniou, 1969) has proved to be the "best." By "best" we mean that the operation of the circuit is very tolerant to the nonideal properties of the op amps, in particular their finite gain and bandwidth. Figure 11.20(a) shows the Antoniou inductance simulation circuit. If the circuit is fed at its