

Find authenticated court documents without watermarks at docketalarm.com.

IMPORTANT NOTICES

Texas Instruments reserves the right to make changes at any time to improve design and to supply the best possible product for the spectrum of users.

The TMS7000 Family Microarchitecture User's Guide (MP #061) is printed in the United States of America and is copyrighted by Texas Instruments Incorporated. All rights reserved. No part of these publications may be reproduced in any manner including storage in a retrieval system or transmittal via electronic means, or other reproduction in any form or any method (electronic, mechanical, photocopying, recording, or otherwise) without prior written permission of Texas Instruments Incorporated.

Information contained in these publications is believed to be accurate and reliable. However, responsibility is neither assumed for its use nor for any infringement of patents or rights of others that may result from its use. No license is granted by implication or otherwise under any patent or patent right of Texas Instruments or others.

DOCKET

Δ

LARM

Find authenticated court documents without watermarks at docketalarm.com.

TMS7000 FAMILY MICROARCHITECTURE USER'S GUIDE

TABLE OF CONTENTS

		PA	GE
1.	INTRO		1
	1.1	General Information	1
	1.2	Initial Family Members	1
	1.3	TMS7000 Eamily Address Snace	2
	1.0	Basic TMS7000 Architecture	3
			-
2.	MICRO		5
	2 1	Microinstruction Format	5
	2.1	Microinstruction Cycle Timing	6
	2.2	Memory Cycle Timing	7
	231	Short Memory References	7
	2.0.1		9
	2.3.2	Long memory networks	10
	2.5.5	Memory Control Signals	11
	2.4		• •
3	TMS7		13
5.	2 1		13
	2.1		13
	3.2		15
	3.3		15
	3.4	AL DUS	16
	3.5		16
	3.0		17
	3./		18
	3.0	ALD Operation	20
	3.9	Solution Solution	20
	3.10	IK negister.	21
	3.11	Status negister.	23
	3.11.1	STC – Status Carry Bit	24
	3.11.2	SISB — Status Sign Bit	24
	3.11.3	STEZ – Status equal to Zero Bit.	24
	3.11.4	STINT – Status interrupt Enable Bit	24
	3.12	BCD Constant Register	24
	3.13	Other Registers	27
4	MICDO		20
4.	WICH		20
	4.1	Overview	20
	4.2	Dispatch Conditions	29
	4.2.1	Unconditional Branching — JUNC	29
	4.2.2	Function Dispatch – IRL	29
	4.2.3	lest Sign Bit – JI/	30
	4.2.4	lest it Zero – JUZ	31
	4.2.5	lest if Interrupt – INI.	31
	4.2.6	Group Dispatch – IRH	32
	4.2.7	lest it Carry – JC	33
	4.2.8	Test Status Register — MJMP	34
	4.3	Reset Operation	35

iii

DOCKET A L A R M Find authenticated court documents without watermarks at <u>docketalarm.com</u>.

LIST OF FIGURES

FIGURE	PAG	ĴΕ
1-1	TMS7000 Family Address Space	2
1-2	TMS7000 Overall Block Diagram	3
2-1	Sample of a MICASM Statement	6
2-2	Microinstruction Cycle Phases	7
2-3	On-Chip RAM Memory Cycle Timing	8
2-4	Long Memory Cycle Timing	9
2-5	Interrupt Vector Reads	10
2-6	Interrupt Vector References	11
3-1	Central Processing Unit Data Paths	14
3-2	P BUS Sources	15
3-3	N BUS Sources	15
3-4	AL BUS Source	16
3-5	AH BUS Sources	16
3-6	LOWWRITE (1-0) Description	16
3-7	O BUS Destinations .	17
3-8	MD BUS Destinations	18
3-9	ALU Block Diagram	18
3-10	ALU Functions	19
3-11	ALU Carry in Values	19
3-12	A Microcode Example	20
3-13	Shift/ALU Carry-in Controls	21
3-14	Shifter Operation	22
3-15	IB Register Formats	22
3-16	Status Register	23
3-17	ST Register Sources	23
3-18	BCD Correction Constant Generation	25
3-19	BCD Arithmetic Operation Timing	26
3-20	MICASM Statement	27
4-1	Microinstruction Dispatch Example	28
4-2	Next Micro Address Generation	29
4-3	RI Disnatch	20
4-4	17 Dispatch	30
4-5	IIZ Dispatch	30
4-6	INT Dispatch	21 21
4.7	TMS2000 Group Numbers	27
4-8	IRH Dispatch	33 27
4-9	IC Dispatch	20
4-10	Marco Jump Conditions)4)/
- 1 -10 /1-11	M IMD Dispata)4)/
-+-11	יוטוטויו האים אינטויו אינטא א	24

LIST OF TABLES

TABLE	F	PAC	GE
2-1	Microinstruction Word Format		5
2-2	Memory Control		12

SECTION 1

INTRODUCTION

1.1 GENERAL INFORMATION

The Texas Instruments TMS7000 Family of single-chip microcomputers is based around a microprogrammable Central Processing Unit (CPU), which can be interfaced to combinations of on-chip RAM, ROM, and I/O circuitry to provide a powerful family of single-chip microcomputers. The TMS7000 CPU implements a 64K byte logical address space and interfaces with I/O registers, timer circuit controls, and other useful on-chip functions by referencing certain addresses within the address space.

This document contains a description of the internal architecture of the TMS7000. It describes primarily the operation of CPU; the memory and on-chip I/O circuitry may vary among the TMS7000 family members, and will be described in the documentation for those individual devices. This document is intended to present information regarding the internal architecture of the TMS7000 family necessary for microcoding these devices. A symbolic microinstruction assembler called MICASM is provided for assembling microcode instruction mnemonics. This assembler is described in the TMS7000 Microassembler User's Guide.

Other information relating to the TMS7000 Family of microcomputers is contained in the following documents:

- TMS7000 8-Bit Microcomputer Data Manual (MP #008A)
- TMS7000 Assembly Language Programmer's Guide (MP #916)
- TMS7000 Microassembler User's Guide (MP #457)
- TMS7000 Microcode Development Guide (MP #458)
- TMS7000 Microprogrammer's Reference Card (MP #459)

The standard instruction set executed by the TMS7000 Family is described in the TMS7000 Assembly Language Programmer's Guide. Internally, the TMS7000 is a microprogrammed processor, whose operation is controlled by a sequence of microinstructions. The internal microprogram is stored in the CPU in the Control ROM, or CROM. Each microinstruction in the microprogram has the same format, consisting of bit fields which control the following operations:

- The gating of microregisters onto internal buses
- The operation of the internal Arithmetic Logic Unit (ALU)
- The appropriate shifting of the ALU results
- The gating of ALU results back into microregisters
- The memory controls to on-chip and off-chip memory
- The next microinstruction to be executed.

This format is called a horizontal microinstruction format, because every component of the microarchitecture is controlled by a single microinstruction word. Such an organization permits a high degree of parallelism in the operation of the microarchitecture.

1.2 INITIAL FAMILY MEMBERS

DOCKET

The TMS7000, TMS7020, and TMS7040 are the initial members of the TMS7000 8-bit Microcomputer Family. The TMS7020 provides 128 bytes of RAM, 2K bytes of ROM, and four 8-bit I/O ports. The TMS7040 provides the same 128 bytes of RAM but contains 4K bytes of ROM. The TMS7000 is identical to the TMS7020/7040, but it has no on-chip ROM. Throughout this document, TMS7000 will in general refer to any member of the TMS7000 family, unless explicitly stated otherwise.

DOCKET



Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time** alerts and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

