Trials@uspto.gov
571-272-7822

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

JP MORGAN CHASE & CO., and
JP MORGAN CHASE BANK, N.A.,
Petitioner,

v.

MAXIM INTEGRATED PRODUCTS, INC.,
Patent Owner.

Case CBM2014-00179
Patent 5,940,510

Before TREVOR M. JEFFERSON, MITCHELL G. WEATHERLY, and KERRY BEGLEY, *Administrative Patent Judges*.

BEGLEY, *Administrative Patent Judge*.

DECISION
Institution of Covered Business Method Patent Review
37 C.F.R. § 42.208

JP Morgan Chase & Co. and JP Morgan Chase Bank, N.A. (collectively, "Petitioner") filed a Petition requesting covered business method patent review ("CBM review") of claims 1–3, 5, and 6 of U.S. Patent No. 5,904,510 (Ex. 1001, "the '510 patent"). Paper 1 ("Pet."). Maxim Integrated Products, Inc. ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp.").

Pursuant to 35 U.S.C. § 324(a), CBM review may not be instituted unless "the information presented in the petition . . . , if such information is not rebutted, would demonstrate that it is more likely than not that at least 1 of the claims challenged in the petition is unpatentable." For the reasons that follow, we determine that the Petition, taking into account the Preliminary Response, demonstrates that it is more likely than not that the challenged claims of the '510 patent are unpatentable. We institute review of the challenged claims on certain asserted grounds of unpatentability.

I. BACKGROUND

A. RELATED PROCEEDINGS

Patent Owner has asserted the '510 patent against Petitioner in the U.S. District Court for the Western District of Pennsylvania, *Maxim Integrated Products, Inc. v. JP Morgan Chase & Co.*, No. 2:12-cv-01641-JFC ("the District Court Case"). Pet. 4–6; Paper 6, 2. This case was consolidated, with many other cases involving the '510 patent filed in various district courts, into a multidistrict litigation proceeding in the Western District of Pennsylvania, *In re: Maxim Integrated Products, Inc.*, MDL No. 2354, Misc. No. 12-244-JFC (W.D. Pa.) ("the MDL Proceeding"). Pet. 4–6; Paper 6, 2–4.

In addition, the '510 patent is the subject of a pending *ex parte* reexamination proceeding, Control No. 90/013,063 ("the Reexamination Proceeding"). Pet. 6–7; Paper 6, 1. The '510 patent also was previously the subject of a petition for CBM review filed by Petitioner and PNC Bank, N.A. ("PNC") in CBM2014-00038, in which review was not instituted, as further detailed in Section II.A.1 below.

B. THE '510 PATENT

The '510 patent is directed to a "system, apparatus, and method for communicating valuable data," more specifically, a "cash equivalent," to and from a "portable module." Ex. 1001, [57], 1:59–61. A consumer can carry the portable module, fill it with a cash equivalent at an "add-money station," and spend the stored cash equivalent "when buying products and services in the market place." *Id.* at [57], 1:61–2:2. For example, a consumer can "take cash out of an ATM" and "put the cash value into the portable module," and can use monetary value on the portable module to "pay for a train fare." *Id.* at 7:13–35, 8:30–37.

In a preferred embodiment, portable module 102 communicates to microprocessor based device 104, which is connected to secure microprocessor based module 108. *Id.* at 1:64–66, 2:32–34, 2:59–61. Portable module 102 is a "rugged read/write data carrier," comprising memory 202, memory controller 204, counter 206 "for keeping track of the number of transactions the module has performed," timer 208 "to time stamp transactions performed by the module," unique identification number 210, and input/output control circuit 212. *Id.* at 3:39–4:24. Microprocessor based device 104, in turn, "can be any of an unlimited number of devices,"

for example, "a personal computer, an add-a-fare machine at a train or bus station (similar to those in today's District of Columbia metro stations), a turn style, a toll booth, a bank's terminal, . . . a washing machine at a Laundromat, . . . or any device that controls access, or meters a monetary equivalent." *Id.* at 2:36–45. Finally, secure microprocessor based module 108 comprises "microprocessor 12, a real time clock 14, control circuitry 16, a math coprocessor 18, memory circuitry 20, input/output circuitry 26, and an energy circuit 34." *Id.* at 4:24–32. In particular, math coprocessor 18 "handle[s] the complex mathematics of [Rivest-Shamir-Adleman ("RSA")] encryption and decryption or other types of math intensive encryption or decryption techniques." *Id.* at 4:60–65.

C. ILLUSTRATIVE CLAIM

Claim 1, the sole independent claim of the '510 patent, is illustrative of the claimed subject matter:

> 1. A system for communicating data securely, comprising:
> a first portable module comprising:
> a nonvolatile memory for storing a first data;
> a first real time clock circuit for time stamping data transactions;
> a counter for counting a transaction count;
> an input/output circuit;
> a substantially unique electronically readable identification number readable by said input/output circuit; and
> a memory control circuit in electrical communication with said nonvolatile memory, said real time clock, said counter, and said input/output circuit;
> a portable module reader that can be placed in communication with said first portable module, said portable module reader can be connected to a plurality of other devices;

a secure microcontroller based module in electronic communication with said portable module reader, said secure microcontroller comprising:
a microcontroller core;
a math coprocessor, in communication with said microcontroller core, for processing encryption calculations;
an energy circuit for storing energy;
a memory circuit connected to said microcontroller core;
a memory circuit in communication with said microcontroller core; and
a second real time clock circuit in communication with said microcontroller,
said combination of said portable module reader and said secure microcontroller performing secure data transfers with said first portable module.

Ex. 1001, 24:1–36 (line breaks added).

D. ASSERTED GROUNDS

Petitioner challenges the '510 patent claims on the following grounds.

Challenged Claims	Basis	Reference[s]
1–3	§ 103	Cremin and Hawkes
5, 6	§ 103	Cremin, Hawkes, and Rivest
1–3, 5, 6	§ 101	

These asserted grounds rely upon the following § 102(b) prior art references (Pet. 23–25):

International Patent Application Publication No. WO 83/03018 (published Sept. 1, 1983) (Ex. 1003, "Cremin").

INTEGRATED CIRCUIT CARDS, TAGS AND TOKENS ix–xv, 1–38, 81–91, 136–164 (P.L. Hawkes et al., eds. 1990) (Ex. 1004, "Hawkes").

R. L. Rivest et al., *A Method for Obtaining Digital Signatures and Public-Key Cryptosystems*, 21 COMM. OF THE ACM 2, 120 (1978) (Ex. 1005, "Rivest").

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