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United States Patent [19]

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Lee

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[54] **ONE-WIRE BUS ARCHITECTURE**

[75] Inventor: **Robert D. Lee, Denton, Tex.**

[73] Assignee: **Dallas Semiconductor Corporation, Dallas, Tex.**

[21] Appl. No.: **352,581**

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[51] Int. Cl.⁵ **G06F 13/18; G06K 19/06**

[52] U.S. Cl. **395/425; 395/400; 364/DIG. 1; 235/492; 365/189.03; 365/189.06**

[58] Field of Search **365/189.03, 189.06, 365/194; 357/74; 335/488, 489, 492; 368/87, 88; 70/228; 395/425, 400; 340/825.08**

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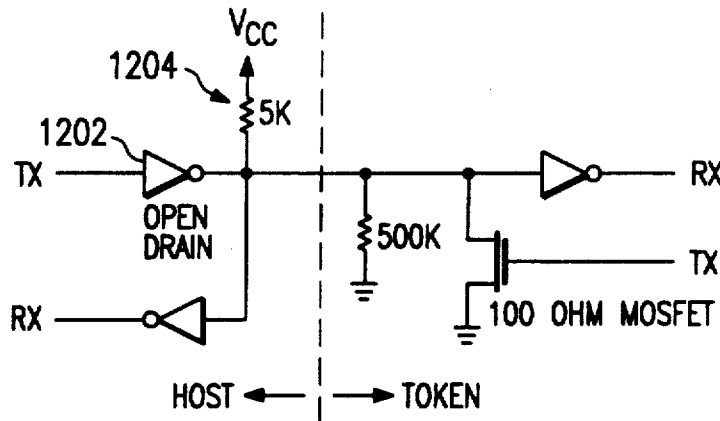
Primary Examiner—Joseph L. Dixon

Assistant Examiner—Jack A. Lane
Attorney, Agent, or Firm—Worsham, Forsythe, Sampels & Wooldridge

[57] **ABSTRACT**

A system architecture which provides efficient data communication, over a one-wire bus, with a portable data module which does not necessarily include any accurate time delay circuit whatsoever. The time delay circuit in the module can be extremely crude. An open-collector architecture is used, with electrical relations defined to absolutely minimize the drain on the portable module's battery. A protocol has been specified so that the module never sources current to a data line of the one-wire bus, but only sinks current. The protocol includes signals for read; write-zero; write-one; and reset. Each one-bit transaction is initiated by a falling edge of a voltage signal from the host. The time delay circuit in the module defines a delay, after which (in write mode) the module tests the data state of the data line. In read mode, after a falling edge of a voltage signal from the host the module does or does not turn on a pull-down transistor, depending on the value of the bit read. Thus, the host system, after the falling edge, attempts to pull the data line high again, and then tests the potential of the data line to ascertain the value of the bit read.

6 Claims, 17 Drawing Sheets



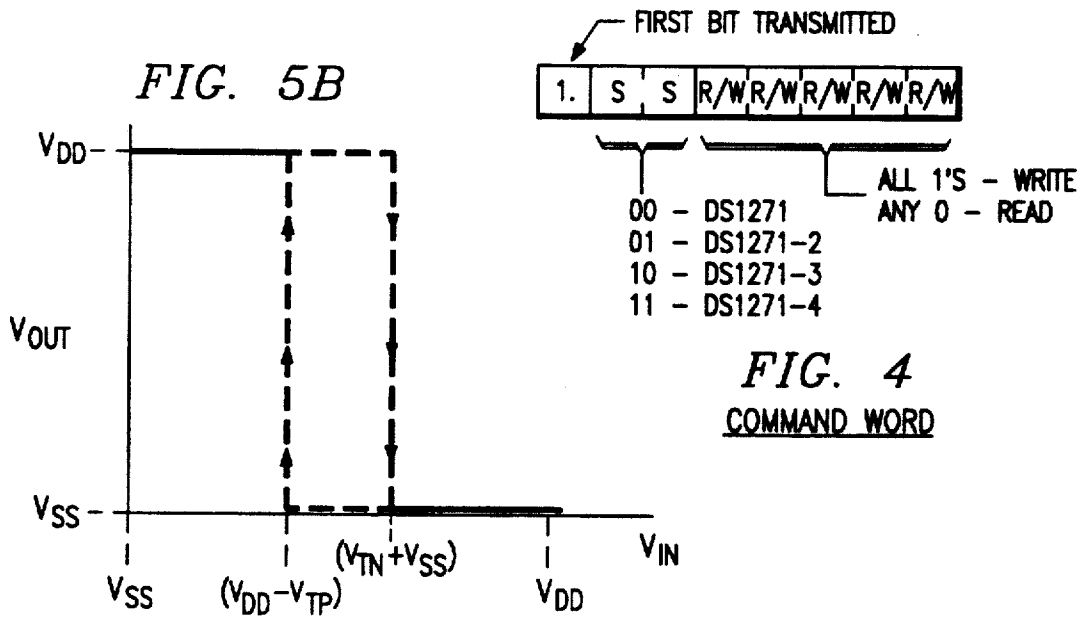
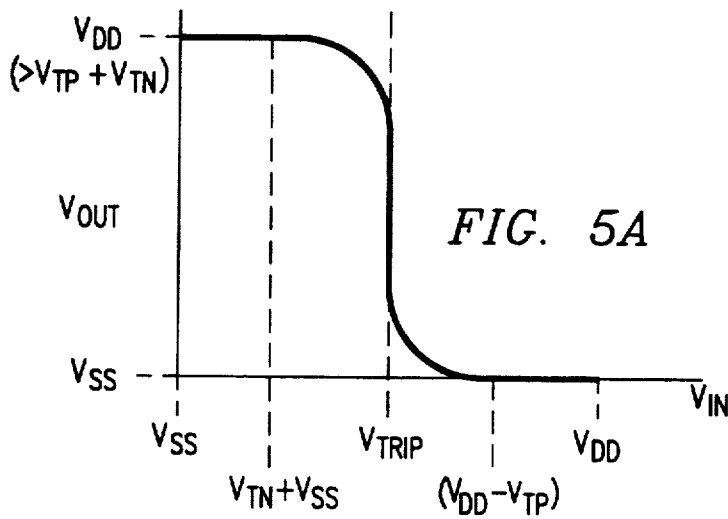
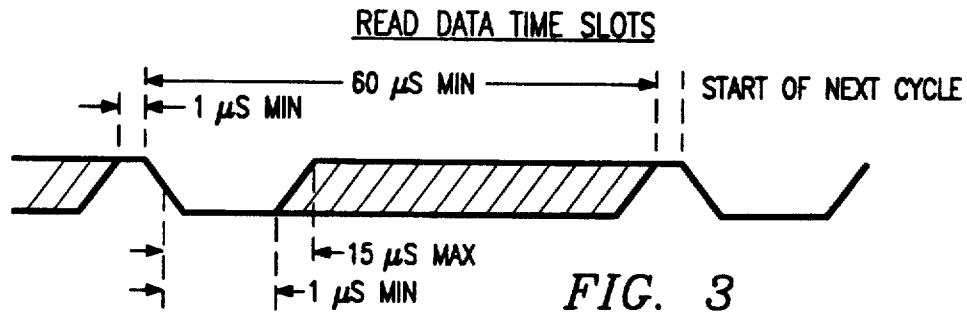


FIG. 6

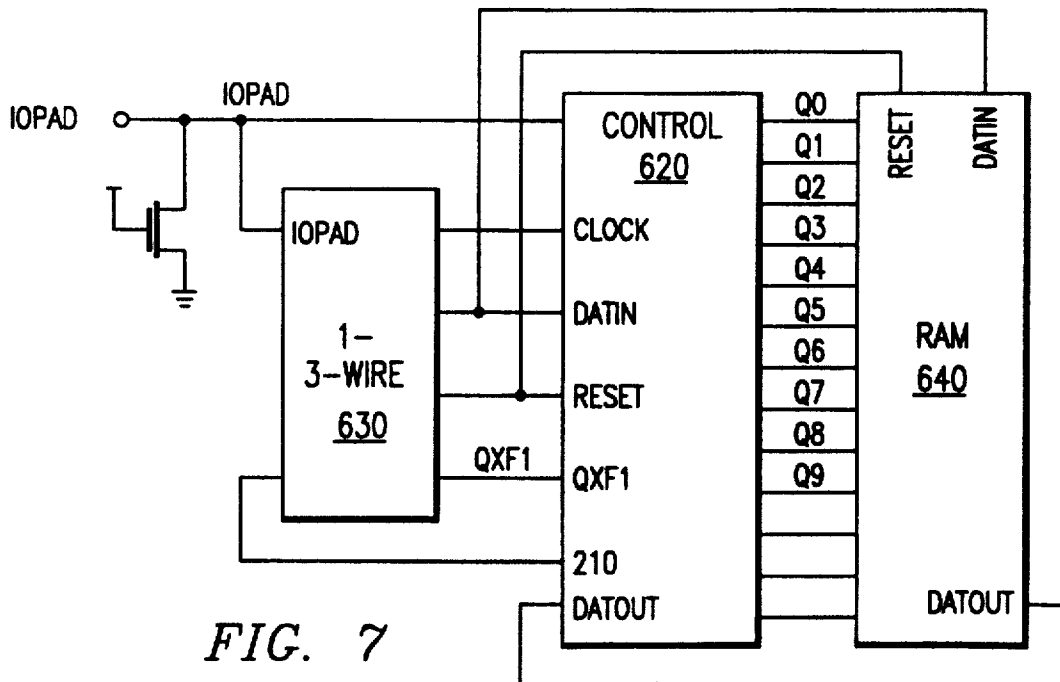
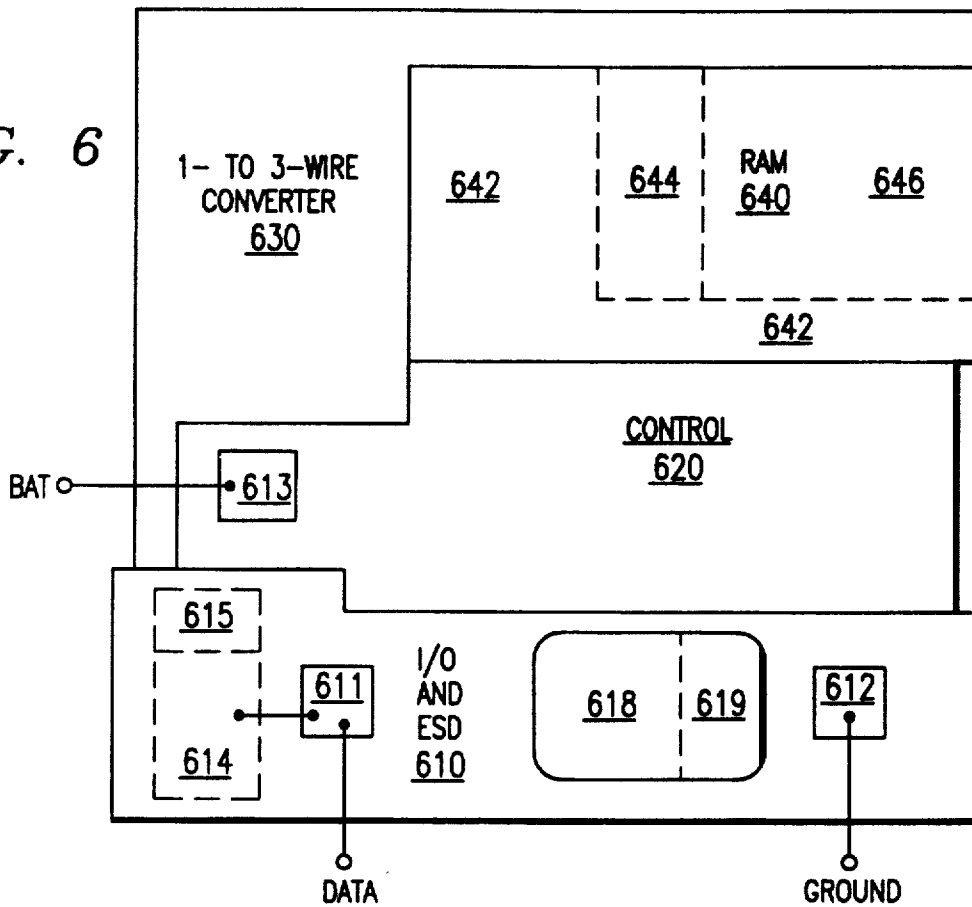


FIG. 7

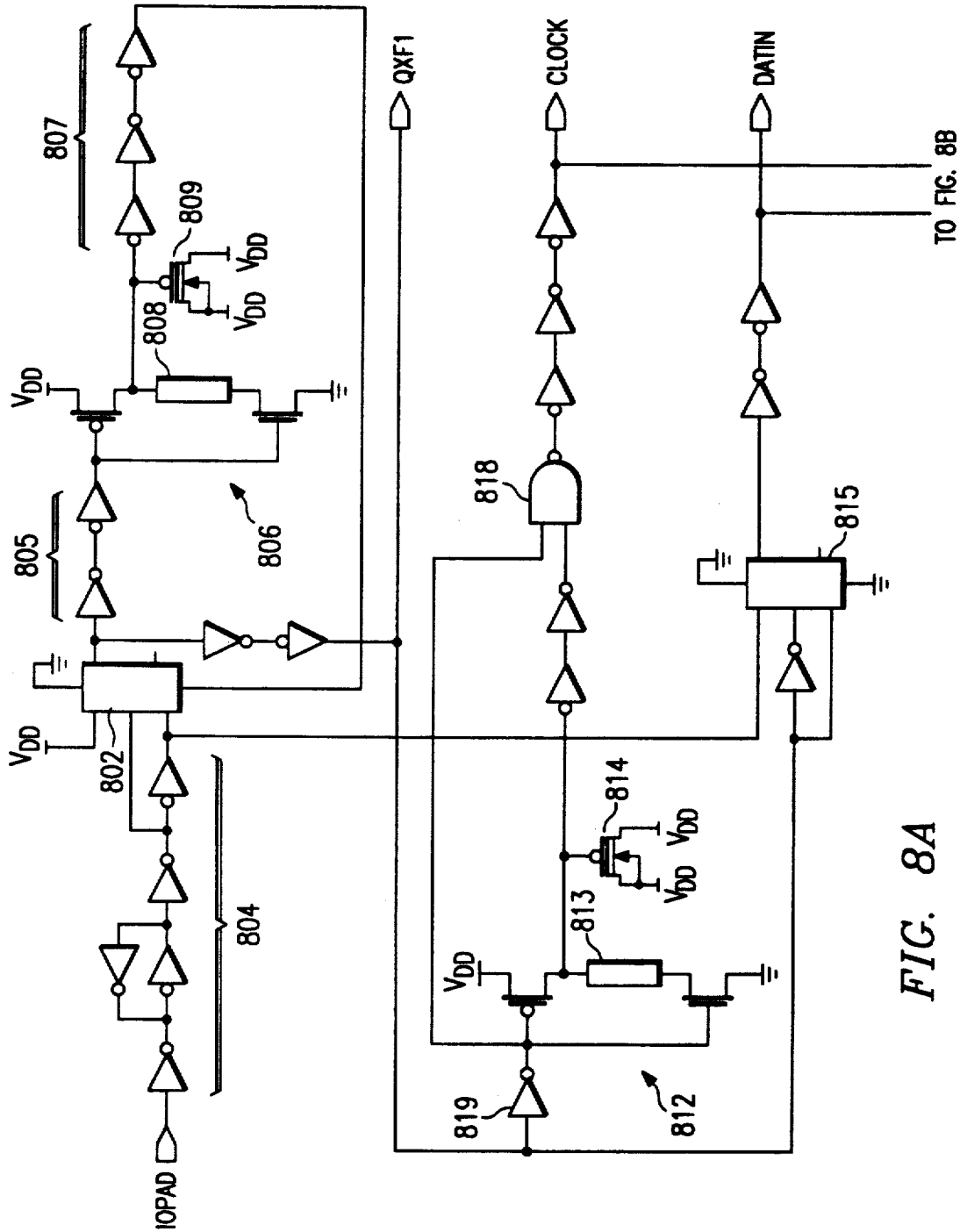


FIG. 8A

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