EXHIBIT 2033

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United States Court of Appeals for the Federal Circuit

KILOPASS TECHNOLOGY, INC.,
Plaintiff-Appellee,

v.

SIDENSE CORPORATION,
Defendant-Appellant.

2013-1193

Appeal from the United States District Court for the Northern District of California in No. 10-CV-2066, Judge Susan Y. Illston.

Decided: December 26, 2013

DARALYN J. DURIE, Durie Tangri, LLP, of San Francisco, California, argued for plaintiff-appellee. With her on the brief was EUGENE NOVIKOV.

ROGER L. COOK, Kilpatrick Townsend & Stockton, LLP, of San Francisco, California, argued for defendant-appellant. With him on the brief were ROBERT D. TADLOCK and SARA B. GIARDINA. Of counsel on the brief was JOSHUA H. LEE, of Atlanta, Georgia.

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Before RADER, *Chief Judge,* LOURIE and O'MALLEY, *Circuit Judges.*

Opinion for the court filed by *Circuit Judge* O'MALLEY.

Concurring opinion filed by *Chief Judge* RADER.

O'MALLEY, *Circuit Judge.*

This appeal arises from the United States District Court for the Northern District of California. The district court granted summary judgment in favor of Sidense Corporation ("Sidense"), holding that it did not infringe Kilopass Technology, Inc.'s ("Kilopass's") U.S. Patents 6,940,751 ("the '751 patent"), 6,777,757, and 6,856,540. *Kilopass Tech., Inc. v. Sidense Corp.*, No. 10-2066, 2012 WL 3545286 (N.D. Cal. Aug. 16, 2012). We summarily affirmed that decision under Federal Circuit Rule 36. *Kilopass Tech., Inc. v. Sidense Corp.*, 501 F. App'x 980 (Fed. Cir. 2013). While that appeal was pending, Sidense filed a motion in the district court seeking an award of attorneys' fees under 35 U.S.C. § 285, which the district court denied. *Kilopass Tech., Inc. v. Sidense Corp.*, No. 10-02066, 2012 WL 6599428 (N.D. Cal. Dec. 18, 2012). Sidense now appeals from the district court's denial of that motion. We vacate and remand for reconsideration consistent with this opinion.

I

Kilopass and Sidense are competitors in the embedded non-volatile memory ("NVM") market. Memory cells use transistors to store information. NVM memory consists of memory devices that retain their information (or state) when power is removed. Kilopass markets technology used to create its 1.5T NVM memory technology. Sidense has a competing 1T-Fuse product, the design and technology of which it licenses to its customers, who in turn use those designs to build embedded memory cells.

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Kilopass's patents cover a memory cell comprised of transistors located at the cross-points of a column bitline and a row wordline. Each transistor has a "gate" connected to a column bitline and a "source" connected to a row wordline. '751 patent col. 5 ll. 32–40. Opposite the source is a "drain" that is not connected to any bitlines or wordlines. *Id.* Beneath the gate is a substrate separated from the gate by a dielectric oxide. *Id.* col. 7 l. 17. The dielectric oxide is engineered to "break down" when a sufficient voltage is applied to the gate. *Id.* col. 7 ll. 14–16. If the gate oxide breaks down, a conductive link forms between the source and drain, allowing current to flow through the transistor. *Id.* col. 7 ll. 16–20. The flow of current indicates that the transistor is in a programmed state, while the absence of current flow indicates that it is in a non-programmed state. *Id.*

Kilopass's '751 patent, which is representative of the patents in suit, is directed to a programmable memory cell utilizing a transistor at the intersection of a column bitline and a row wordline. '751 patent Abstract. Representative claim 1 reads as follows:

> 1. A programmable memory cell useful in a memory array having column bitlines and row wordlines, the memory cell comprising:
>
> a transistor having a gate,
>
> a gate dielectric between the gate and over a substrate,
>
> and *first and second doped semiconductor regions* formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region there between and under said gate;
>
> and wherein *the second doped semiconductor region of the transistor is connected to one of said row wordlines*,

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> and wherein said gate dielectric is formed such that the gate dielectric is more susceptible to breakdown near the first doped semiconductor region than said second doped semiconductor region.

Id. col. 14 ll. 30–44 (emphases added).

Claim 1 of the '751 patent requires a first and second doped semiconductor region of the memory cell where the second doped region is connected to one of the wordlines. *Id.* Sidense's 1T-Fuse cells, however, utilize a shallow trench isolation ("STI") region for the transistor drain instead of a first doped region. *Kilopass*, 2012 WL 3545286, at *10; J.A. 10604. The claim also requires the second doped region to be connected to a row wordline, but Sidense's 1T-Fuse product connects the second doped region to the column bitline. *Kilopass*, 2012 WL 3545286, at *7; J.A. 10604–05. These differences formed the basis of the district court's noninfringement determination, which we affirmed. *Kilopass*, 2012 WL 3545286, at *7–11, *aff'd*, 501 F. App'x 980 (Fed. Cir. 2013).

II

In 2005, Kilopass's founder and an inventor on all three of Kilopass's patents, Jack Peng, reviewed an international patent application submitted by Sidense that was directed to protecting Sidense's competing 1T-Fuse memory cell. Peng believed that the 1T-Fuse was similar to Kilopass's patented cells, except that Sidense used a split gate implementation. *Kilopass*, 2012 WL 3545286, at *9. Peng contacted a patent attorney at the law firm Perkins Coie to discuss potential infringement. In an e-mail to the Perkins attorney, Peng explained that "[Kilopass] did not file [a] dedicated patent for this split gate implementation" and that "we should [have] . . . a long time ago even though we were very busy." J.A. 10576, 10580. According to Peng, it was not a priority to Kilopass at that time because Sidense's "split gate

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