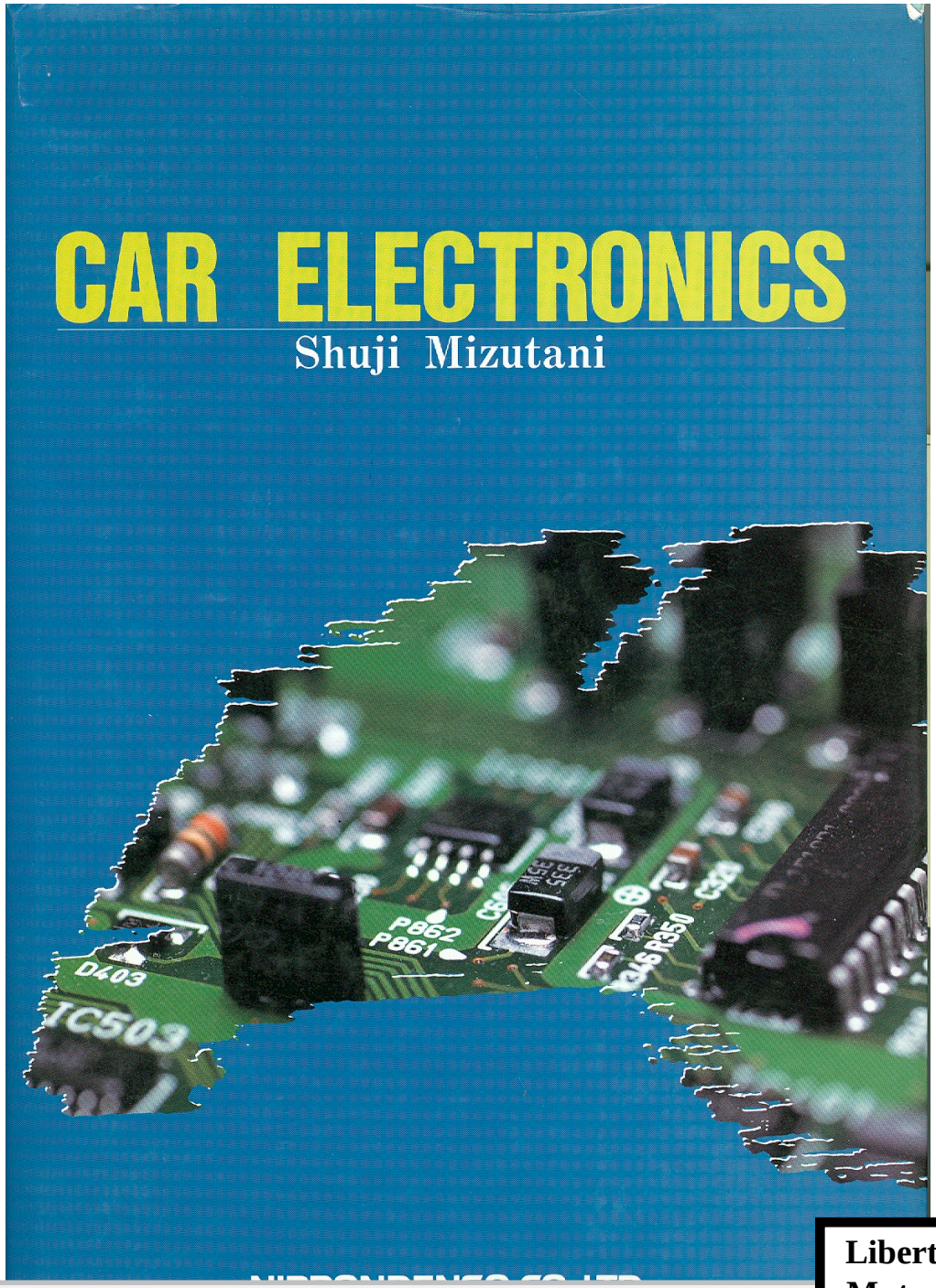
Exhibit 1017



CAR ELECTRONICS

Shuji Mizutani

NIPPONDENSO CO.,LTD.

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Table 7.1 Protocol Comparisons

Standard / Techno-logy Item	SAE J 1850		
	10.4 KbPS	41.6 KbPS	125 KbPS
DATA HANDLING	×		
ID FILTERRING	△ (Hardware, software)		
CPU INTERFACE	×		
ACCESS	○ CSMA/CD		
PRIORITY CONTROL	○ Non-destructive contention-based arbitration		
ADDRESSING	△ (Physical address, functional adress, physical adress + functional address)		
ACKNOWLEDGE (RESPONSE)	△ None 1 byte from 1 reception node (ID or address) Plural bytes (each byte transmitted from 1 reception node)		
ERROR DETECTION	△ 8 bitCRC ($X^8+X^4+X^3+X^2+1$) Use is optional • Message length check • Range over check • Ineffective bit check • Frame error check	○ 8 bit CRC ($X^8+X^4+X^3+X^2+1$) • Message length check • Range over check • Ineffective bit check • Frame error check	○←
MESSAGE LENGTH	○ Less than or equal 101 bits		
SYNC. METHOD	○ Bit synchronization = Self-synchronization type		
CODE	○ VPW	○ PWM	○ ×
TRANSMISSION RATE	○ 10.4 kbps	○ 41.6 kbps	○ 125 kbps
NUMBER OF NODES	○ MAX 32	○ MAX 32	×
BUS INTERFACE	Voltage driven	△ Differential voltage driven Parallel voltage driven	×
MEDIA	○ Single wire	○ Parallel double wire Twisted pair wire	×
TOPOLOGY	○ Path		
Source	Draft SAE J 1850 DEC 89 Revision 12/4/89		

Note : × : Not reviewed/not specified ○ : One proposition is reviewed
△ : Alternatives are available or freedom of selection is given within a given range.
A portion is reviewed