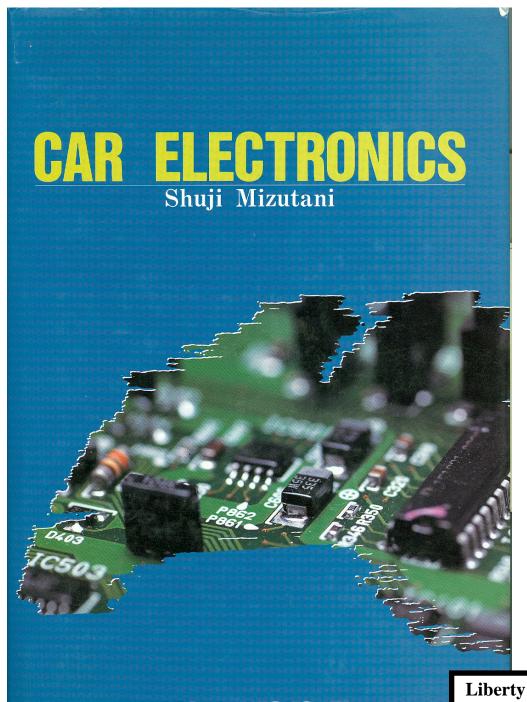
Exhibit 1017



DOCKET A L A R M Mutual Exhibit 1017

CAR ELECTRONICS

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Table 7.1 Protocol Comparisons

Standard	1 SAE		
	J 1850		
Techno-logy Item	10.4 KbPS	41.6 KbPS	125 KbPS
DATA HANDLING	×		
ID FILTERRING	△(Hardware, software)		
CPU INTERFACE	×		
ACCESS	○ CSMA/CD		
PRIORITY CONTROL	○ Non-destructive contention-based arbitration		
ADDRESSING	\triangle (Physical address, functional adress, physical address + functional address)		
ACKNOWLEDGE (RESPONSE)	△ None 1 byte from 1 reception node(ID or address) Plural bytes(each byte transmitted from 1 reception node)		
ERROR DETECTION	 △ 8 bitCRC (X*+X⁴+X*+X²+1) Use is optional Message length check Range over check Ineffective bit check Frame error check 	 8 bit CRC (X*+X⁴+X*+X²+1) Message length check Range over check Ineffective bit check Frame error check 	O←
MESSAGE LENGTH	○ Less than or equal 101 bits		
SYNC. METHOD	○ Bit synchronization = Self-synchronization type		
CODE	○ VPW	○ PWM	O×
TRANSMISSION RATE	○ 10.4 kbps	○ 41.6 kbps	○ 125 kbps
NUMBER OF NODES	○ MAX 32	O MAX 32	×
BUS INTERFACE	Voltage driven	△ Differential voltage driven Parallel voltage driven	×
MEDIA	○ Single wire	O Parallel double wire Twisted pair wire	×
TOPOLOGY	○ Path		
Source	Draft SAE J 1850 DEC 89 Revision 12/4/89		

Note: ×: Not reviewed/not specified ○: One proposition is reviewed

△: Alternatives are available or freedom of selection is given within a given range.

A portion is reviewed

