- **Powerful 16-Bit TMS320C5x CPU**
- **20-, 25-, 35-, and 50-ns Single-Cycle Instruction Execution Time for 5-V Operation**
- **25-, 40-, and 50-ns Single-Cycle Instruction Execution Time for 3-V Operation**
- **Single-Cycle 16 × 16-Bit Multiply/Add**
- **224K × 16-Bit Maximum Addressable External Memory Space (64K Program, 64K Data, 64K I/O, and 32K Global)**
- **2K, 4K, 8K, 16K, 32K × 16-Bit Single-Access On-Chip Program ROM**
- **1K, 3K, 6K, 9K × 16-Bit Single-Access On-Chip Program/Data RAM (SARAM)**
- **1K Dual-Access On-Chip Program/Data RAM (DARAM)**
- **Full-Duplex Synchronous Serial Port for Coder/Decoder Interface**
- **Time-Division-Multiplexed (TDM) Serial Port**
- **Hardware or Software Wait-State Generation Capability**
- **On-Chip Timer for Control Operations**
- **Repeat Instructions for Efficient Use of Program Space**
- **Buffered Serial Port**
- **Host Port Interface**
- **Multiple Phase-Locked Loop (PLL) Clocking Options (×1, ×2, ×3, ×4, ×5, ×9 Depending on Device)**
- **Block Moves for Data/Program Management**
- **On-Chip Scan-Based Emulation Logic**
- **Boundary Scan**
- **Five Packaging Options**
  - **100-Pin Quad Flat Package (PJ Suffix)**
  - **100-Pin Thin Quad Flat Package (PZ Suffix)**
  - **128-Pin Thin Quad Flat Package (PBK Suffix)**
  - **132-Pin Quad Flat Package (PQ Suffix)**
  - **144-Pin Thin Quad Flat Package (PGE Suffix)**
- **Low Power Dissipation and Power-Down Modes:**
  - **47 mA (2.35 mA/MIP) at 5 V, 40-MHz Clock (Average)**
  - **23 mA (1.15 mA/MIP) at 3 V, 40-MHz Clock (Average)**
  - **10 mA at 5 V, 40-MHz Clock (IDLE1 Mode)**
  - **3 mA at 5 V, 40-MHz Clock (IDLE2 Mode)**
  - **5 μA at 5 V, Clocks Off (IDLE2 Mode)**
- **High-Performance Static CMOS Technology**
- **IEEE Standard 1149.1† Test-Access Port (JTAG)**

description

The TMS320C5x generation of the Texas Instruments (TI™) TMS320 digital signal processors (DSPs) is fabricated with static CMOS integrated circuit technology; the architectural design is based upon that of an earlier TI DSP, the TMS320C25. The combination of advanced Harvard architecture, on-chip peripherals, on-chip memory, and a highly specialized instruction set is the basis of the operational flexibility and speed of the ’C5x‡ devices. They execute up to 50 million instructions per second (MIPS).

The ’C5x devices offer these advantages:

- Enhanced TMS320 architectural design for increased performance and versatility
- Modular architectural design for fast development of spin-off devices
- Advanced integrated-circuit processing technology for increased performance
- Upward-compatible source code (source code for ’C1x and ’C2x DSPs is upward compatible with ’C5x DSPs.)
- Enhanced TMS320 instruction set for faster algorithms and for optimized high-level language operation
- New static-design techniques for minimizing power consumption and maximizing radiation tolerance

TI is a trademark of Texas Instruments Incorporated.
† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture
‡ References to ’C5x in this document include both TMS320C5x and TMS320LC5x devices unless specified otherwise.

description (continued)

Table 1 provides a comparison of the devices in the ’C5x generation. It shows the capacity of on-chip RAM and ROM memories, number of serial and parallel I/O ports, execution time of one machine cycle, and type of package with total pin count.

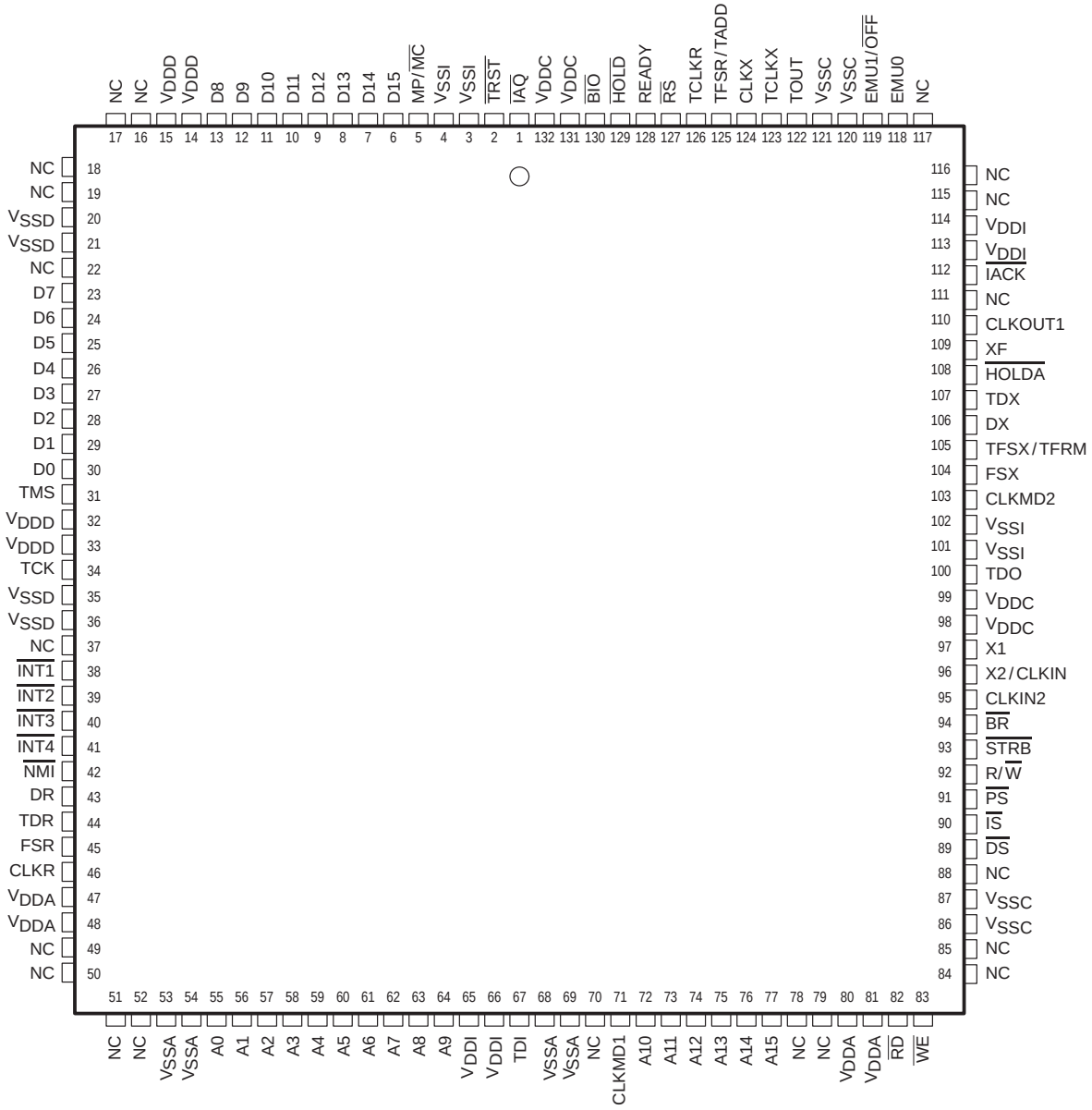
Table 1. Characteristics of the ’C5x Processors

TMS320 DEVICES	ON-CHIP MEMORY (16-BIT WORDS)				I/O PORTS		POWER SUPPLY (V)	CYCLE TIME (ns)	PACKAGE TYPE QFP‡
	DARAM		SARAM	ROM					
	DATA	DATA + PROG	DATA + PROG	PROG	SERIAL	PARALLEL†			
TMS320C50	544	512	9K	2K§	2	64K	5	50/35/25	132 pin
TMS320LC50	544	512	9K	2K§	2	64K	3.3	50/40/25	132 pin
TMS320C51	544	512	1K	8K§	2	64K	5	50/35/25/20	100/132 pin
TMS320LC51	544	512	1K	8K§	2	64K	3.3	50/40/25	100/132 pin
TMS320C52	544	512	–	4K§	1¶	64K	5	50/35/25/20	100 pin
TMS320LC52	544	512	–	4K§	1¶	64K	3.3	50/40/25	100 pin
TMS320C53	544	512	3K	16K§	2	64K	5	50/35/25	132 pin
TMS320LC53	544	512	3K	16K§	2	64K	3.3	50/40/25	132 pin
TMS320C53S	544	512	3K	16K§	2¶	64K	5	50/35/25	100 pin
TMS320LC53S	544	512	3K	16K§	2¶	64K	3.3	50/40/25	100 pin
TMS320LC56	544	512	6K	32K	2#	64K	3.3	35/25	100 pin
TMS320LC57	544	512	6K	32K	2#	64K + HPI‖	3.3	35/25	128 pin
TMS320C57S	544	512	6K	2K§	2#	64K + HPI‖	5	50/35/25	144 pin
TMS320LC57S	544	512	6K	2K§	2#	64K + HPI‖	3.3	50/35	144 pin

† Sixteen of the 64K parallel I/O ports are memory mapped.
‡ QFP = Quad flatpack
§ ROM boot loader available
¶ TDM serial port not available
# Includes auto-buffered serial port (BSP) but TDM serial port not available
‖ HPI = Host port interface

Pinouts for each package are device-specific.

TMS320C50, TMS320LC50, TMS320C51, TMS320LC51, TMS320C53, TMS320LC53
PQ PACKAGE
(TOP VIEW)



NOTE: NC = No connect (These pins are reserved.)

Pin Functions for Devices in the PQ Package

SIGNAL	TYPE	DESCRIPTION
PARALLEL INTERFACE BUS		
A0–A15	I/O/Z	16-bit external address bus (MSB: A15, LSB: A0)
D0–D15	I/O/Z	16-bit external data bus (MSB: D15, LSB: D0)
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data, and I/O space select outputs, respectively
$\overline{STRB}$	I/O/Z	Timing strobe for external cycles and external DMA
R/$\overline{W}$	I/O/Z	Read/write select for external cycles and external DMA
$\overline{RD}$, $\overline{WE}$	O/Z	Read and write strobes, respectively, for external cycles
READY	I	External bus ready/wait-state control input
$\overline{BR}$	I/O/Z	Bus request. Arbitrates global memory and external DMA
SYSTEM INTERFACE/CONTROL SIGNALS		
$\overline{RS}$	I	Reset. Initializes device and sets PC to zero
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select. Enables internal ROM
$\overline{HOLD}$	I	Puts parallel I/F bus in high-impedance state after current cycle
$\overline{HOLDA}$	O/Z	Hold acknowledge. Indicates external bus in hold state
XF	O/Z	External flag output. Set/cleared through software
$\overline{BIO}$	I	I/O branch input. Implements conditional branches
TOUT	O/Z	Timer output signal. Indicates output of internal timer
$\overline{IAQ}$	O/Z	Instruction acquisition signal
$\overline{IACK}$	O/Z	Interrupt acknowledge signal
$\overline{INT1}$–$\overline{INT4}$	I	External interrupt inputs
$\overline{NMI}$	I	Nonmaskable external interrupt
SERIAL PORT INTERFACE (SPI)		
DR	I	Serial receive-data input
DX	O/Z	Serial transmit-data output. In high-impedance state when not transmitting
CLKR	I	Serial receive-data clock input
CLKX	I/O/Z	Serial transmit-data clock. Internal or external source
FSR	I	Serial receive-frame-synchronization input
FSX	I/O/Z	Serial transmit-frame-synchronization signal. Internal or external source
TDM SERIAL-PORT INTERFACE		
TDR	I	TDM serial receive-data input
TDX	O/Z	TDM serial transmit-data output. In high-impedance state when not transmitting
TCLKR	I	TDM serial receive-data clock input
TCLKX	I/O/Z	TDM serial transmit-data clock. Internal or external source
TFSR / TADD	I/O/Z	TDM serial receive-frame-synchronization input. In the TDM mode, TFSR/TADD is used to output/input the address of the port.
TFSX/TFRM	I	TDM serial transmit-frame-synchronization signal. Internal or external source. In the TDM mode, TFSX/TFRM becomes TFRM, the TDM frame synchronization.

LEGEND:
I = Input
O = Output
Z = High impedance

Pin Functions for Devices in the PQ Package (Continued)

EMULATION/IEEE STANDARD 1149.1 TEST ACCESS PORT (TAP)		
TDI	I	TAP scan data input
TDO	O/Z	TAP scan data output
TMS	I	TAP mode select input
TCK	I	TAP clock input
$\overline{\text{TRST}}$	I	TAP reset (with pulldown resistor). Disables TAP when low
EMU0	I/O/Z	Emulation control 0. Reserved for emulation use
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulation control 1. Puts outputs in high-impedance state when low
CLOCK GENERATION AND CONTROL		
X1	O	Oscillator output
X2/CLKIN	I	Clock/oscillator input
CLKIN2	I	Clock input
CLKMD1, CLKMD2	I	Clock-mode select inputs
CLKOUT1	O/Z	Device system-clock output
POWER SUPPLY CONNECTIONS		
V_{DDA}	S	Supply connection, address-bus output
V_{DDD}	S	Supply connection, data-bus output
V_{DDC}	S	Supply connection, control output
V_{DDI}	S	Supply connection, internal logic
V_{SSA}	S	Supply connection, address-bus output
V_{SSD}	S	Supply connection, data-bus output
V_{SSC}	S	Supply connection, control output
V_{SSI}	S	Supply connection, internal logic

LEGEND:
I = Input
O = Output
S = Supply
Z = High impedance

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