EXHIBIT K

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Miller et al.

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(54) **MULTI CHIP MODULE**

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(65) **Prior Publication Data**

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Related U.S. Application Data

(62) Division of application No. 10/265,751, filed on Oct. 7, 2002, now Pat. No. 6,680,532.

(51) **Int. Cl.**[7] **H01L 23/10**

(52) **U.S. Cl.** **257/706**; 257/707; 257/712; 257/713; 257/762

(58) **Field of Search** 257/706, 707, 257/712, 713, 762; 361/702, 709, 712; 261/713

(56) **References Cited**

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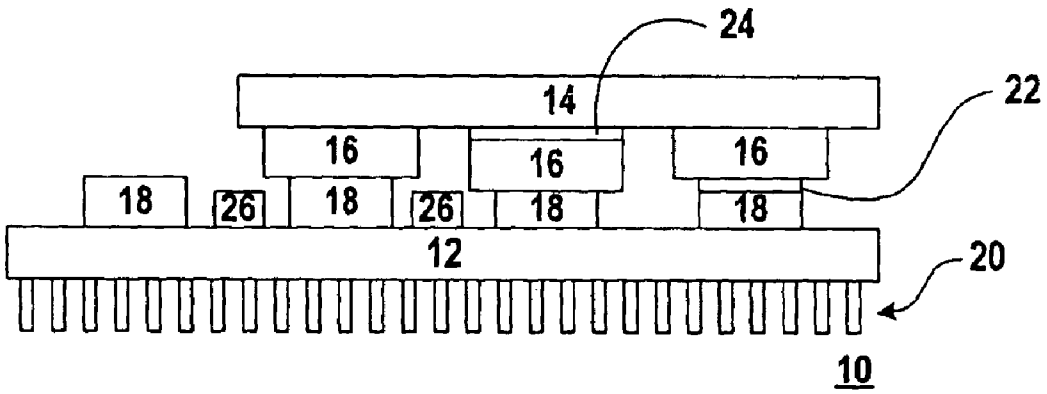
(57) **ABSTRACT**

A multi chip package, which includes a package substrate having a first side and an opposing second side. The first side is for receiving package electrical connections. Integrated circuits are electrically connected and structurally connected by their first sides to the second side of the package substrate. Heat spreaders are disposed adjacent the second side of the integrated circuits, where one each of the heat spreaders is associated with one each of the integrated circuits. A single stiffener having a first side and an opposing second side covers all of the integrated circuits and heat spreaders, where the first side of the stiffener is disposed adjacent the second side of the heat spreaders.

18 Claims, 2 Drawing Sheets



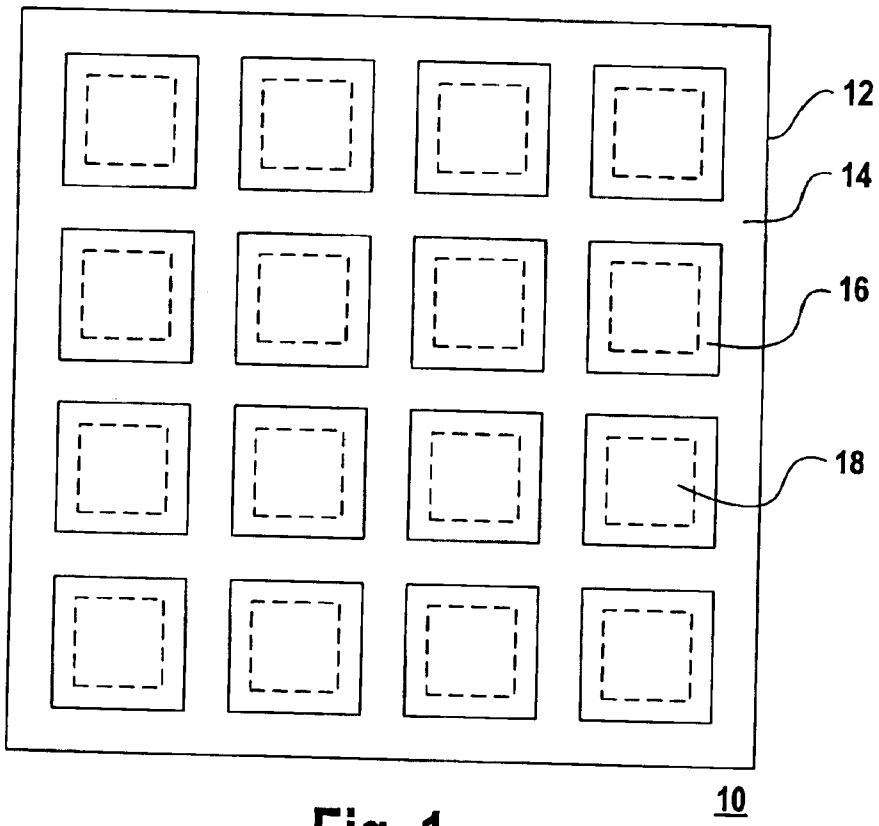


Fig. 1

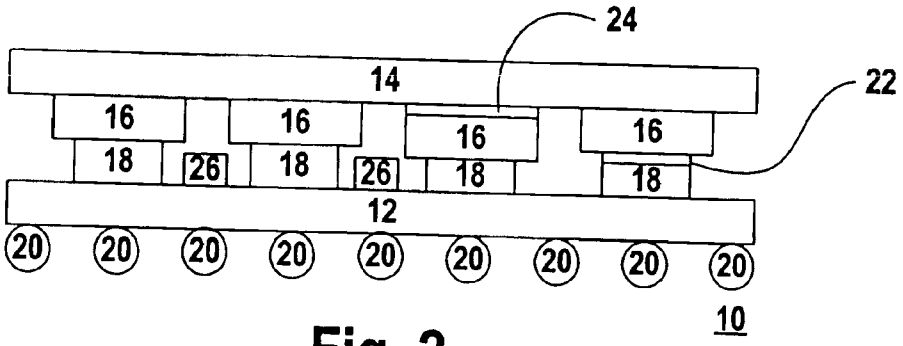


Fig. 2

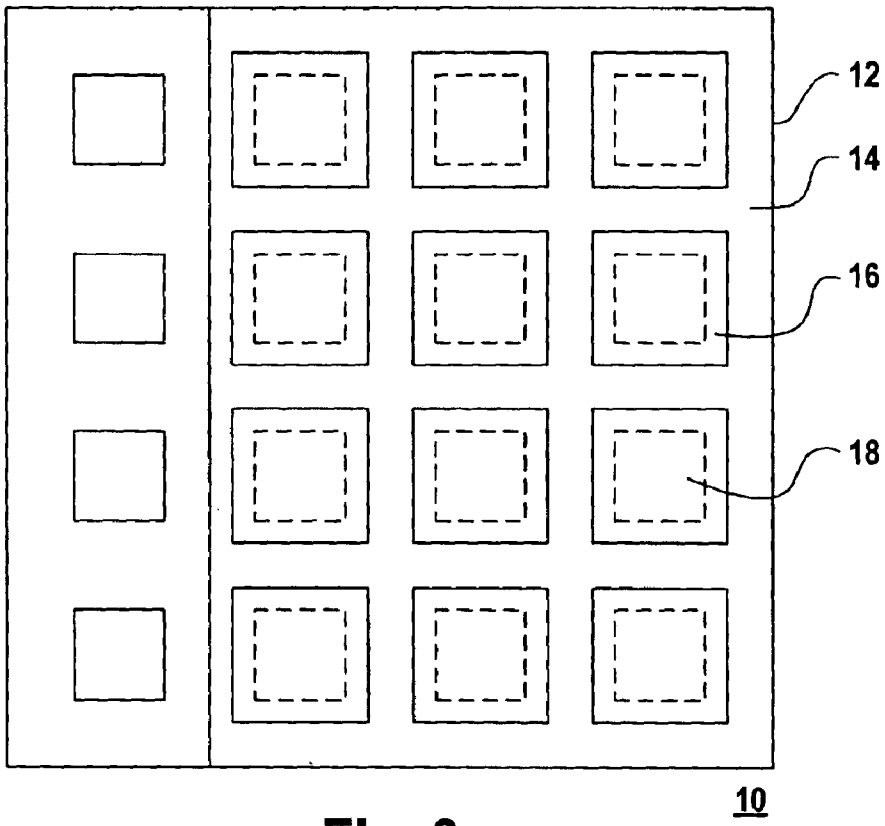


Fig. 3

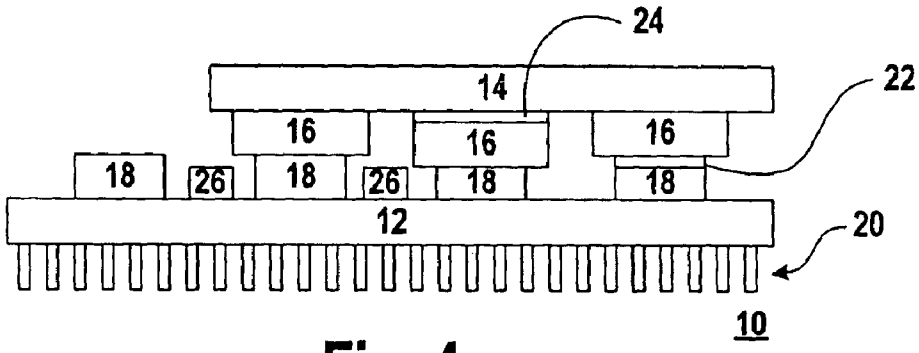


Fig. 4

MULTI CHIP MODULE

This is a divisional of application Ser. No. 10/265,751 filed Oct. 7, 2002 now U.S. Pat. No. 6,680,532.

FIELD

This invention relates to the field of integrated circuit fabrication. More particularly, this invention relates to packaging of integrated circuits.

BACKGROUND

It is often desirable to have two or more integrated circuits packaged together. For example, it is often convenient to have one or more logic integrated circuits, such as application specific integrated circuits, packaged with one or more memory integrated circuits, such as random access memory and read only memory. In such an arrangement, the memory integrated circuits can conveniently contain information such as operational instructions for the logic integrated circuit and, additionally, other memory integrated circuits can also receive information that is sent from or is to be sent to other circuits. By placing such desired integrated circuits within a single package, a designer can generally increase the speed and reduce the complexity and cost of the overall circuit design. Circuit reliability and tolerance may also increase.

Because of the device density of most integrated circuits, they tend to produce an appreciable amount of thermal energy, which is released as heat. Also, as there is a desire to continually reduce the size of completed integrated circuits, including the packaging, many packaging materials are somewhat flexible. These two factors of heat production and package flexibility tend to place certain constraints on integrated circuit package design. For example, because of the heat that is produced by an integrated circuit, a heat spreader is typically added to the package. The heat spreader is intended to conduct heat away from the integrated circuit. Typically, the heat spreader is placed on the top of the package as a lid.

Next, because the packages tend to be somewhat flexible, stiffener rings are typically included in a package design, to increase the rigidity and overall structural integrity of the package design. The stiffener ring is typically an annular structure that is placed around an integrated circuit, which resides within a center void of the stiffener ring, and which is coplanar with the stiffener ring.

However, when there are more than one integrated circuit within a single package, the use of stiffener rings becomes more complex. If a stiffener ring is added around each integrated circuit in the package, then a relatively large amount of space is used for stiffener rings, which increases the size of the package. However, if a stiffener ring is omitted from one or more of the integrated circuits, then the structural integrity of the package is somewhat compromised.

What is needed, therefore, is a package design that provides adequate heat dissipation and structural support for a multi chip module.

SUMMARY

The above and other needs are met by a multi chip package according to the present invention, which includes a package substrate having a first side and an opposing second side. The first side is for receiving package electrical connections. Integrated circuits are electrically connected and structurally connected by their first sides to the second side of the package substrate. Heat spreaders are disposed adjacent the second side of the integrated circuits, where one each of the heat spreaders is associated with one each of the integrated circuits. A single stiffener having a first side and an opposing second side covers all of the integrated circuits and heat spreaders, where the first side of the stiffener is disposed adjacent the second side of the heat spreaders.

In this manner, a single stiffener is used for the integrated circuit package, where the stiffener is disposed on a layer that is not coplanar with the integrated circuits. Thus, the integrated circuits may be placed closer together, and the overall surface area size of the integrated circuit package can be reduced without compromising the structural integrity of the integrated circuit package, as would tend to occur by merely removing one or more stiffeners. In addition, a separate heat spreader is dedicated to each monolithic integrated circuit, thereby improving heat dissipation from the integrated circuits individually, and thereby from the package generally.

In various preferred embodiments of the invention, a thermal epoxy is disposed between the second side of each of the integrated circuits and the first side of each of the heat spreaders, where the thermal epoxy conducts thermal energy to the heat spreaders and away from the integrated circuits. Additionally, a thermal epoxy is preferably disposed between the second side of each of the heat spreaders and the first side of the stiffener, where the thermal epoxy conducts thermal energy to the stiffener and away from the heat spreaders. Preferably, discrete components are also electrically connected to the second side of the package substrate, coplanar with the integrated circuits. In a most preferred embodiment, ball grid array package electrical connections are disposed on the first side of the package substrate. The heat spreaders and the stiffener are preferably formed of copper.

According to another aspect of the invention there is provided a multi chip package, which includes a package substrate having a first side and an opposing second side. The first side is for receiving package electrical connections. Integrated circuits are electrically connected and structurally connected by their first sides to the second side of the package substrate. Heat spreaders are disposed adjacent the second side of the integrated circuits, where a single one of the heat spreaders is associated with a single one of the integrated circuits, but not all of the integrated circuits have an associated heat spreader. A single stiffener having a first side and an opposing second side covers all of the integrated circuits and heat spreaders, where the first side of the stiffener is disposed adjacent the second side of the heat spreaders.

According to yet another aspect of the invention there is provided a multi chip package, which includes a package substrate having a first side and an opposing second side. The first side is for receiving package electrical connections. Integrated circuits are electrically connected and structurally connected by their first sides to the second side of the package substrate. Heat spreaders are disposed adjacent the second side of the integrated circuits, where one each of the heat spreaders is associated with one each of the integrated circuits. A single stiffener having a first side and an opposing second side covers some but not all of the integrated circuits and heat spreaders, where the first side of the stiffener is disposed adjacent the second side of the heat spreaders.

BRIEF DESCRIPTION OF THE DRAWINGS

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