IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PACT XPP SCHWEIZ AG Plaintiff, v. INTEL CORPORATION Defendant.	Case No. _____ **JURY TRIAL DEMANDED**

COMPLAINT

Plaintiff PACT XPP Schweiz AG, for its Complaint against Intel Corporation ("Intel" or "Defendant"), hereby alleges as follows:

PARTIES

1. Plaintiff PACT XPP Schweiz AG is a Swiss corporation, with its principal place of business in Switzerland. PACT XPP Schweiz AG is the assignee of all patents identified in this Complaint including all rights to sue for past and future damages for infringement of said patents.

2. Upon information and belief, Intel is a Delaware corporation with its corporate headquarters in Santa Clara, California and manufacturing facilities in Oregon, Arizona, New Mexico, Massachusetts, and numerous other countries.

3. Intel, founded in 1968, has over an 80% market share in computer processor technology, and over $70 Billion in revenues producing $29.4 Billion of cash from operations and returned nearly $16.3 Billion to shareholders in 2018 based on a gross profit margin of 61.7% of revenues. Intel's two major operating segments are the PC Client Group, which produced over $37 Billion in revenue for 2018 and focuses on the processors found in consumer-

grade netbooks and desktops, and the Data Center Group, which produced over $32 Billion in revenue and focuses on processors found in enterprise-level servers.

NATURE OF THE ACTION

4. This is a civil action for patent infringement of the following patents by Defendant Intel: U.S. Patent Nos. 7,928,763 ("the '763 Patent"), 8,301,872 ("the '872 Patent"), 8,312,301 ("the '301 Patent"), 8,471,593 ("the '593 Patent"), 8,686,549 ("the '549 Patent"), 8,819,505 ("the '505 Patent"), 9,037,807 ("the '807 Patent"), 9,075,605 ("the '605 Patent"), 9,170,812 ("the '812 Patent"), 9,250,908 ("the '908 Patent"), 9,436,631 ("the '631 Patent"), and 9,552,047 ("the '047 Patent") (collectively, the "Asserted Patents"). This action is based upon the Patent Laws of the United States, 35 U.S.C. § 1 *et seq.*

JURISDICTION AND VENUE

5. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. This Court has personal jurisdiction over Intel because Intel is incorporated in Delaware. Intel also manufactures products that are and have been used, offered for sale, sold, and purchased in the District of Delaware.

7. Under 28 U.S.C. §§ 1391(b)-(d) and 1400(b), venue is proper in this judicial district because Intel is incorporated in this district, has committed acts of infringement within this judicial district giving rise to this action, has previously filed suit in Delaware, and does business in this district. Venue is also proper based on parties' stipulation to refile the previously dismissed Complaint originally filed in this District on February 7, 2019.

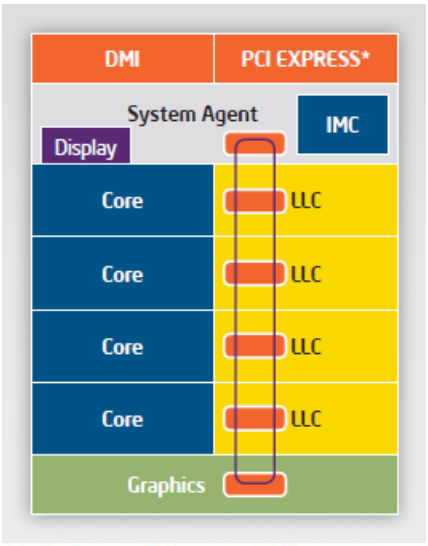
FACTUAL BACKGROUND

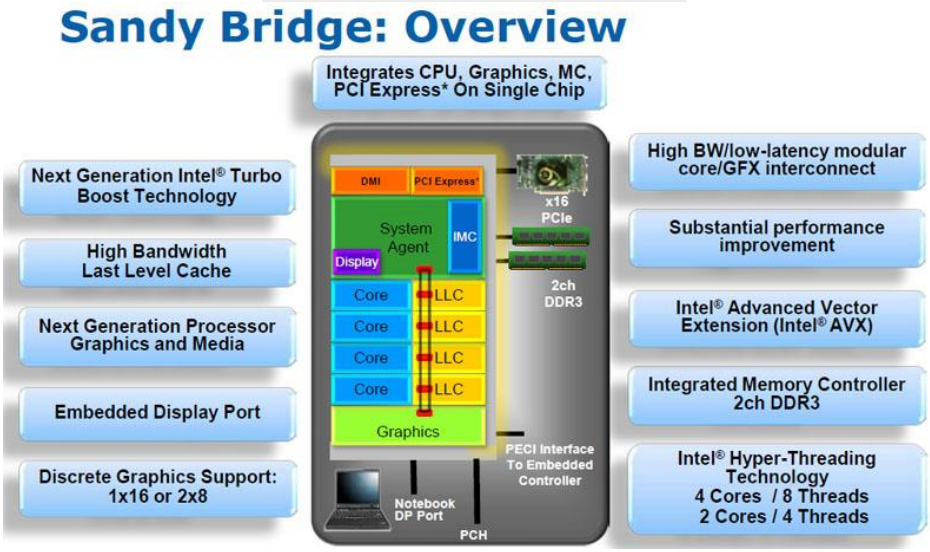
8. PACT XPP Schweiz's predecessor and assignor PACT XPP TECHNOLOGIES AG (Lichtenstein) (hereinafter collectively referred to as "PACT") was founded in 1996 in

Germany by Martin Vorbach. Mr. Vorbach (the lead inventor on all of PACT's patents) has been experimenting with parallel computing since the mid-1980s. Mr. Vorbach embarked on the design of a completely different type of a multi-core computer architecture—that was the forerunner of Intel's multi-core processors. Mr. Vorbach focused his designs on multi-core processing systems including how to handle more complex algorithms with large amounts of data involving multiple processors on a single chip. Because of this, he encountered unique challenges that the general CPU market would not face for years to come and was granted over 70 U.S. patents. On information and belief, Intel's multi-core processors at issue were not released until 2011, years after the priority dates of the Asserted Patents.

9. For example, one challenge Mr. Vorbach had to solve was how to move and access data in a multi-core system from one core to the next for large pipelined operations. This led to his development of bus architectures for multicore processors with multiple paths, including those using ring bus systems, for both configuring cores and accessing data in the cores and in local memory including the patents identified herein.

10. It was not until 2011 that Intel released its "Sandy Bridge" chip architecture accused of infringement in this Complaint. Sandy Bridge included a ring-based interconnect for communication between multiple processor cores, processor graphics and cache system. The ring bus architecture takes up less space on the die while also scaling well for larger core counts—in contrast to Intel's earlier dual core designs. Intel coupled this with a last level cache (LLC) that could be alternately shared among the cores. In 2017, Intel introduced a mesh bus architecture, which is a modified version of the ring bus that also implements Mr. Vorbach's invention.





11. This architecture has been incorporated into most of Intel's Core Series processor family—the i3, i5, i7, and i9 processors—found in computers and on information and belief other processors manufactured and sold by Intel. Starting with the second generation (code-named Sandy Bridge, released 2011), these processors have contained a variant of the above-described ring bus (or equivalents) and LLC feature set including the Sandy Bridge, Ivy Bridge, Haswell, Broadwell, Skylake, Kaby Lake, Coffee Lake architectures and, on information and belief, other processors including ring bus architecture (or equivalents). According to Intel's

most recent reported financial results for 2018,[1] its revenue was over $32 Billion for its Data Center Group and $37.0 Billion for its PC center group.

12. Another contribution Mr. Vorbach made to the multi-core system is to change the clock frequencies of part of the multi-core system in a particular way to take advantage of the processing power of certain cores and in the meantime achieve power efficiency. This invention was adopted by Intel in its Turbo Boost technology many years later. For example, Turbo Boost 2.0 was introduced in 2011 with the Sandy Bridge microarchitecture, and Turbo Boost Max 3.0 was introduced in 2016 with the Broadwell microarchitecture. On information and belief, Turbo-Boost-enabled processors have been manufactured since 2008.

13. Another contribution Mr. Vorbach made to the multi-core system is a stacking technique, according to which the multi-core processors and the bus system are stacked on a plurality of dies in an efficient way. Intel just adopted this stacking technique in recent announcements.

14. In December 2018, Intel hosted an Architecture Day conference in California for analysts and media that allowed Intel's top executives, architects and fellows to reveal their next-generation technologies to a captive audience. During the conference, Intel announced that it had created a new 3D packaging technology, called "Foveros." Foveros is expected to extend die stacking beyond passive interposers and stacked memory to high-performance logic, such as CPU. In January 2019, during the CES conference, Intel made further announcement of a new product, Lakefield, that implements the Foveros technology. The Foveros technology, however,

[1] https://www.intc.com/investor-relations/investor-education-and-news/investor-news/press-release-details/2019/Intel-Reports-Fourth-Quarter-2018-Financial-Results/default.aspx

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