EXHIBIT A

EXHIBIT A – JOINT CLAIM CONSTRUCTION CHART

US Patent (Claims)	Claim Term	IPB's Construction	OmniVision's C
6,538,324 (1, 5)	multi-layered structure of first and second films	This term has its plain and ordinary meaning and need not be construed.	multi-layered structure o films covering the entire of the copper wiring laye
6,709,950 (12, 17)	trench isolation on the semiconductor substrate	insulating material filling a trench, which is etched into the semiconductor substrate	This term has its plain an and need not be construe
6,709,950 (12, 17)	forming . . . on	formed directly or indirectly on	This term has its plain an and need not be construe
6,709,950 (12)	first sidewalls on both side surfaces of the gate electrode	This term has its plain and ordinary meaning and need not be construed.	first sidewalls substantial surfaces of the gate elect
6,709,950 (12)	second sidewalls on a side surface of a step portion	This term has its plain and ordinary meaning and need not be construed.	second sidewalls substan surface of a step portion
6,709,950 (12)	a sixth step of forming a laminated film made of a silicon oxide film and a silicon nitride film on the entire top surface of the substrate	a sixth step of forming a laminated film made of a silicon oxide film and a silicon nitride film directly or indirectly on the entire top surface of the substrate	a sixth step of forming a of a layer of silicon oxide layer of silicon nitride fil surface of the substrate

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US Patent (Claims)	Claim Term	IPB's Construction	OmniVision's C
6,794,677 (1, 4)	sum perimeter . . . per unit area	This term has its plain and ordinary meaning and need not be construed.	Indefinite
6,794,677 (1)	a sum perimeter of the first linear pattern, the second linear pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first linear pattern per unit area.	This term has its plain and ordinary meaning and need not be construed. In the alternative only, this term may be construed as: a perimeter per unit area of the first pattern, second pattern, and the dummy pattern is equal to or less than the perimeter per unit area of the first linear pattern.	Indefinite
6,794,677 (4)	a sum perimeter of the first gate electrode pattern, the second gate electrode pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first gate electrode pattern per unit area.	This term has its plain and ordinary meaning and need not be construed. In the alternative only, this term may be construed as: a perimeter per unit area of the first gate electrode pattern, the second gate electrode pattern, and the dummy pattern is equal to or less than the perimeter per unit area of the first gate electrode pattern.	Indefinite
6,794,677 (1)	a dummy pattern being inserted in the region in which	This term has its plain and ordinary meaning and need not be construed.	Indefinite

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US Patent (Claims)	Claim Term	IPB's Construction	OmniVision's C
	the second circuit pattern is placed	In the alternative only, this term may be construed as: a dummy pattern being inserted in the logic region in which the second circuit pattern is placed.	
6,794,677 (4)	a dummy pattern being inserted in the logic region in which the second circuit pattern is placed	This term has its plain and ordinary meaning and need not be construed.	Indefinite
8,378,401 (1, 29) 8,084,796 (1, 3) 8,106,431 (1, 5, 9)	a plurality of read-out lines each being selectively connected to at least two of the [plurality of] transfer transistors	This term has its plain and ordinary meaning and need not be construed.	Indefinite
8,378,401 (1, 4, 29) 8,084,796 (1, 3) 8,106,431 (1, 4, 5, 9, 12)	photodiode	This term has its plain and ordinary meaning and need not be construed.	a photoelectric conversio incident light is converte and where photoelectric stored.
8,378,401 (1, 29)	'401, '796 (claim 1): a plurality of	This term has its plain and ordinary meaning and need not be construed.	Indefinite

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US Patent (Claims)	Claim Term	IPB's Construction	OmniVision's C
8,084,796 (1, 3) 8,106,431 (1, 4, 5, 9)	floating diffusion sections each being connected to ones of the plurality of photodiodes via each of a plurality of transfer transistors '431 (claims 1, 5, 9),'796 (claim 3): a plurality of floating diffusion sections each being connected to ones of the photodiodes via each of a plurality of transfer transistors '431 (claim 4): wherein each of said plurality of floating diffusion sections is shared by said ones of the plurality of photodiodes which are adjacent to each other in the column direction		

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