
EXHIBIT I

1. A semiconductor integrated circuit device comprising:

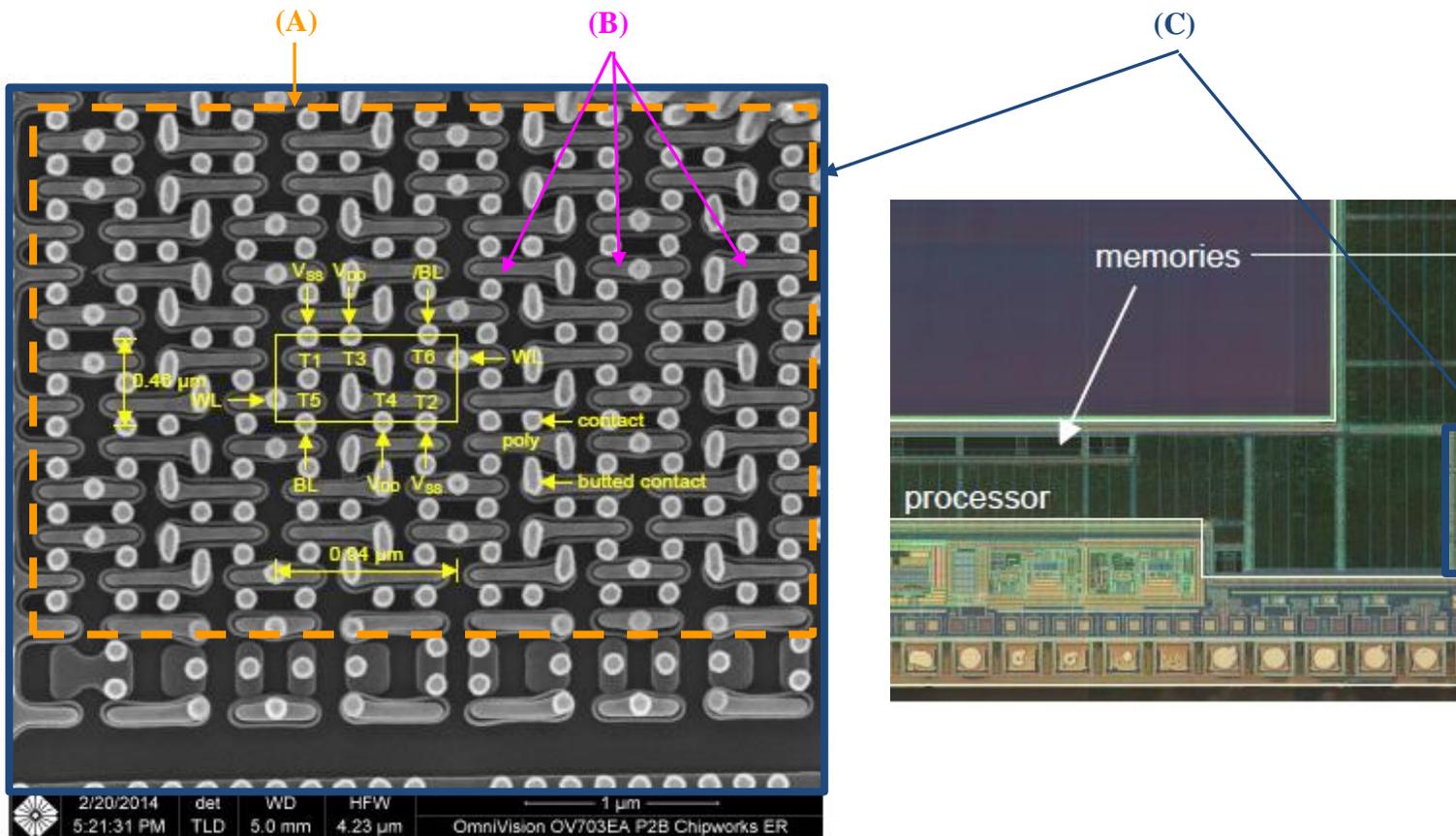
(A) a first circuit pattern having (B) a first linear pattern and placed in (C) a region in which a group of elements in a repetitive pattern are formed; and

(D) a second circuit pattern having (E) a second linear pattern and placed in (F) a region in which components of another group of elements are formed,

(G) a dummy pattern being inserted in (F) the region in which (D) the second circuit pattern is placed such that a sum of (B) the first linear pattern, (E) the second linear pattern, and (G) the dummy pattern per unit area is equal to or greater than the perimeter of (B) the first linear pattern per unit area.

Claim 1

A semiconductor integrated circuit device comprising: (A) a first circuit pattern having (B) a first linear pattern and a region in which a group of elements having a repetitive pattern are formed; and



Claim 1

(D) a second circuit pattern having (E) a second linear pattern and placed in (F) a region in which components of a group of elements are formed, (G) a dummy pattern being inserted in (F) the region in which (D) the second circuit pattern is placed

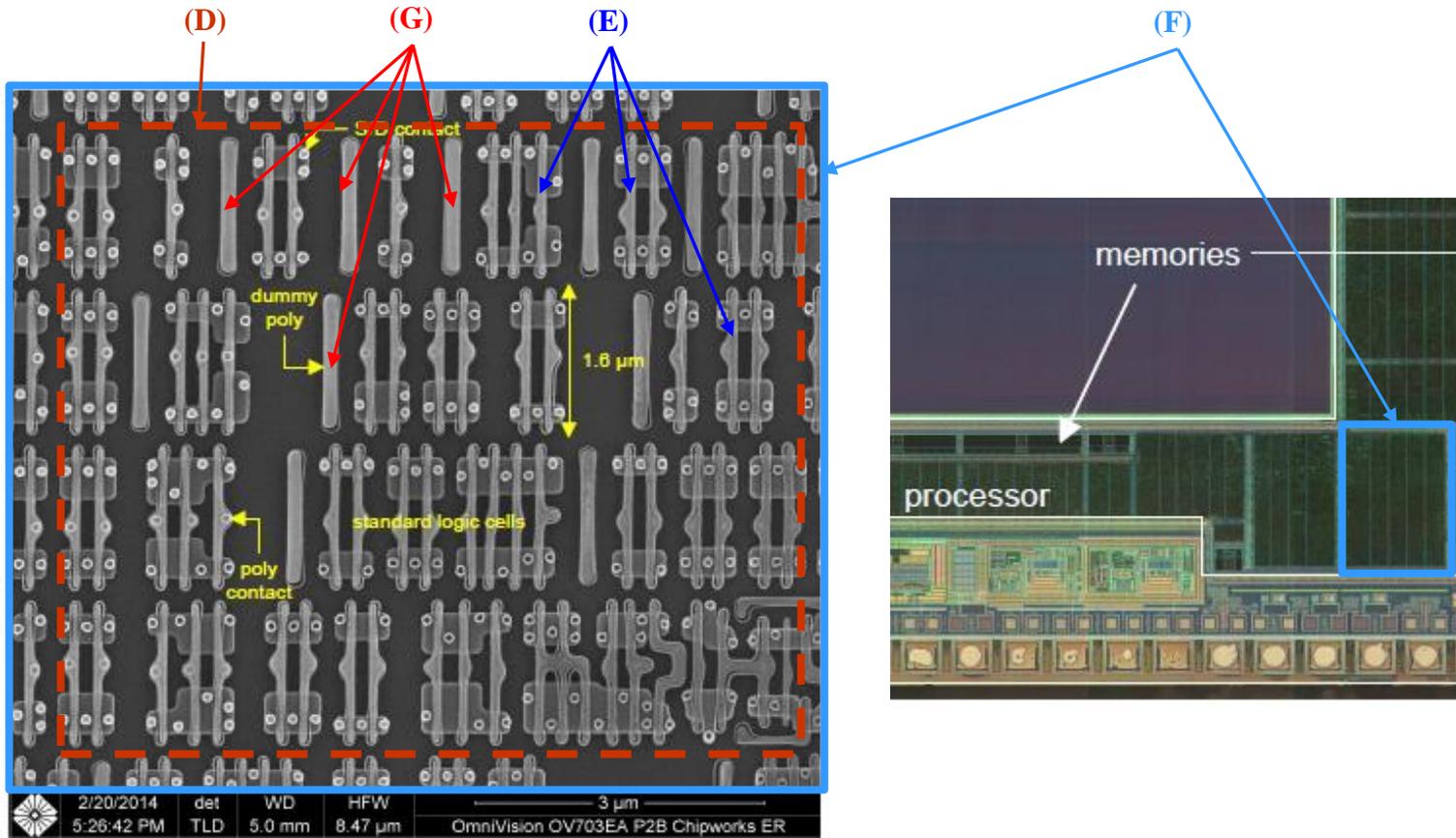


Figure 2.4.1 Overview of Standard Logic

Claim 1

such that a sum perimeter of (B) the first linear pattern, (E) the second linear pattern, and (G) the dummy pattern equal to or less than a perimeter of (B) the first linear pattern per unit area.

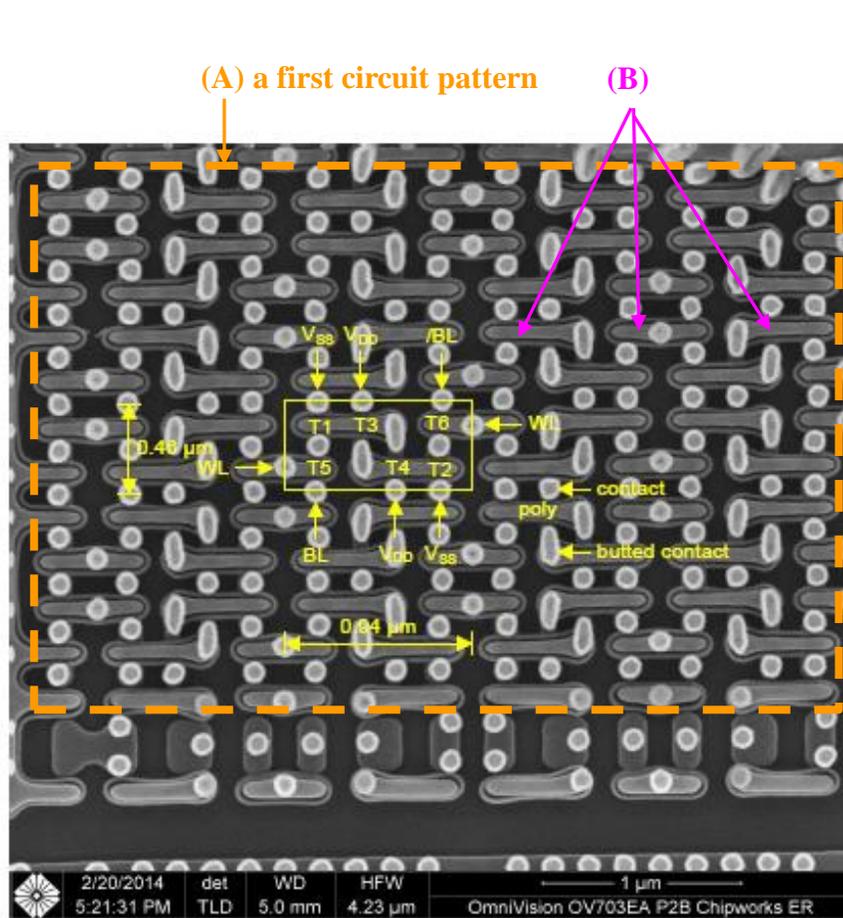


Figure 5.2.4 6T SRAM at Poly

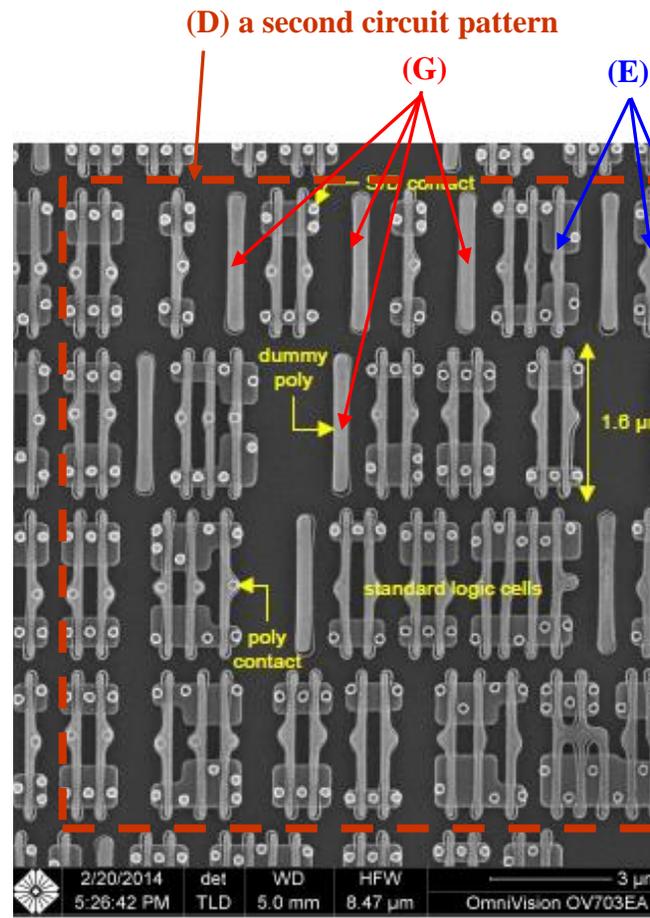


Figure 2.4.1 Overview of Standard

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