EXHIBIT M

1. A solid state imaging apparatus comprising:

(A) a plurality of photodiodes arranged in an array;

(B) a plurality of floating diffusion sections each being connected to ones of the plurality of photodiodes via each of **(C) a plurality of transfer transistors**;

(D) a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors;

(E) a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

(F) a plurality of pixel amplifier transistors each detecting and outputting the potential of one of the plurality of floating diffusion sections;

(G) a plurality of signal lines each transferring an output from one of the plurality of pixel amplifier transistors,

wherein **(A) the plurality of photodiodes** include **(a1) a first photodiode**, **(a2) a second photodiode**, **(a3) a third photodiode**, **(a4) a fourth photodiode**,

(C) the plurality of transfer transistors include **(c1) a first transfer transistor, (c2) a second transfer transistor, (c3) a third transfer transistor** and **(c4) a fourth transfer transistor**,

(D) the plurality of read-out lines include **(d1) a first read-out line, (d2) a second read-out line, (d3) a third read-out line, (d4) a fourth read-out line**,

(DA) (d1) the first read-out line is adjacent to **(d2) the second read-out line**,

(DB) (d2) the second read-out line is disposed between **(d1) the first read-out line** and **(d3) the third read-out line**,

(DC) (d3) the third read-out line is disposed between **(d2) the second read-out line** and **(d4) the fourth read-out line**,

(DD) (d1) the first read-out line is connected to **(a1) the first photodiode** in row m via **(c1) the first transfer transistor**, m being a positive integer,

(DE) (d2) the second read-out line is connected to **(a2) the second photodiode** in the row m via **(c2) the second transfer transistor**,

(DF) (d3) the third read-out line is connected to **(a3) the third photodiode** in row m+1 via **(c3) the third transfer transistor**,

(DG) (d4) the fourth read-out line is connected to **(a4) the fourth photodiode** in the row m+1 via **(c4) the fourth transfer transistors**,

(AA) (a1) the first photodiode and **(a3) the third photodiode** are disposed in one of column n and column n+1, where n is a positive integer,

(AB) (a2) the second photodiode and **(a4) the fourth photodiode** are disposed in the other of the column n and the column n+1, and **(H)** one of the column n and the column n+1 is disposed between one of **(G) the plurality of signal lines** and the other of the column n and the column n+1.
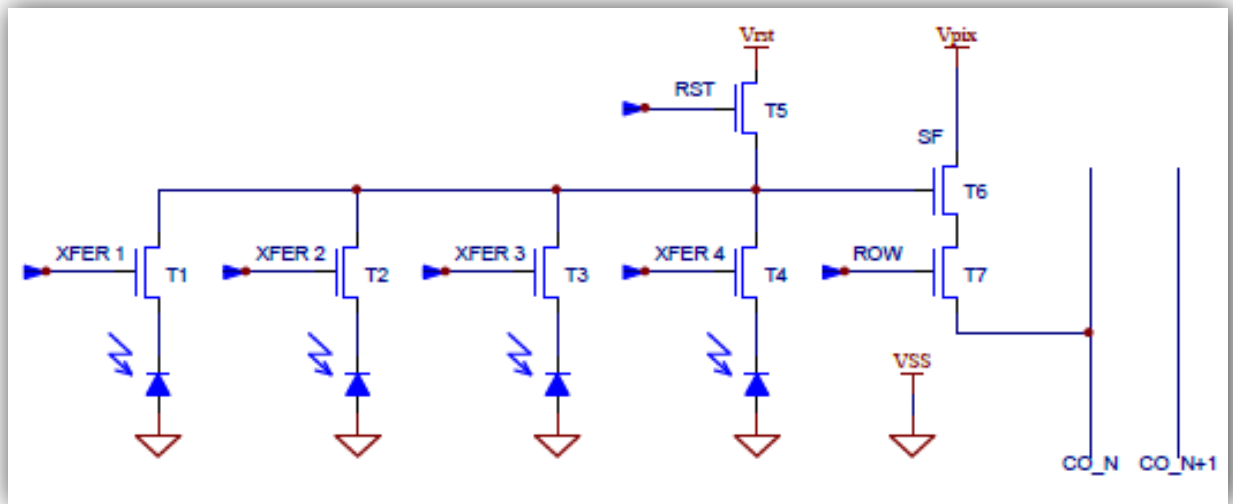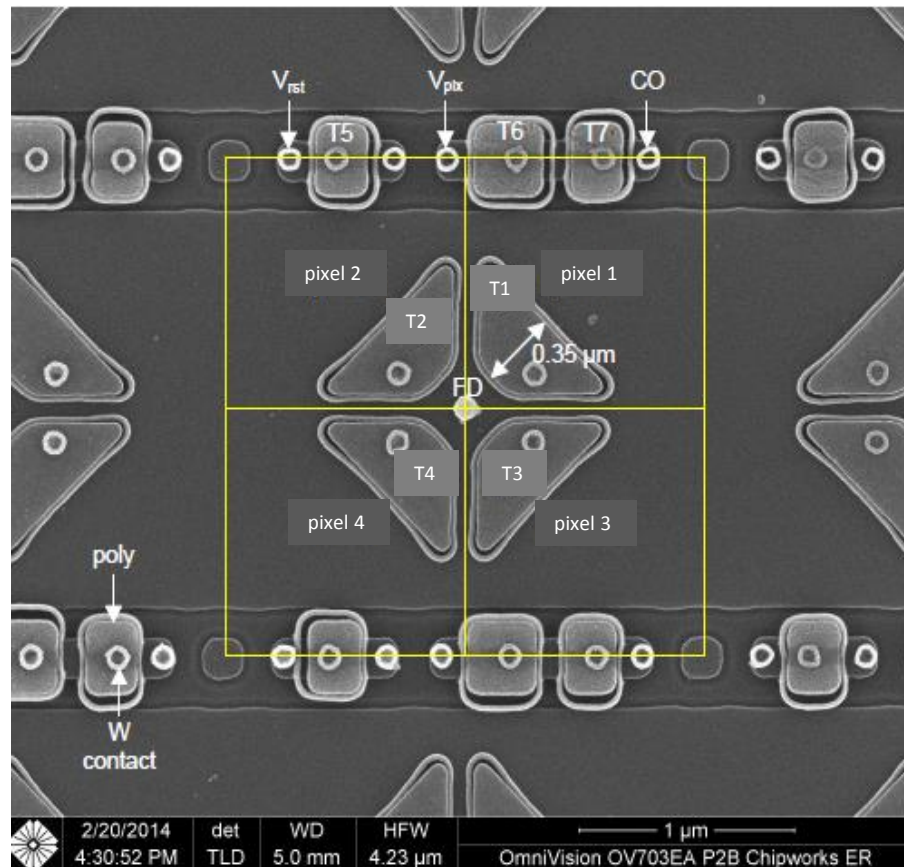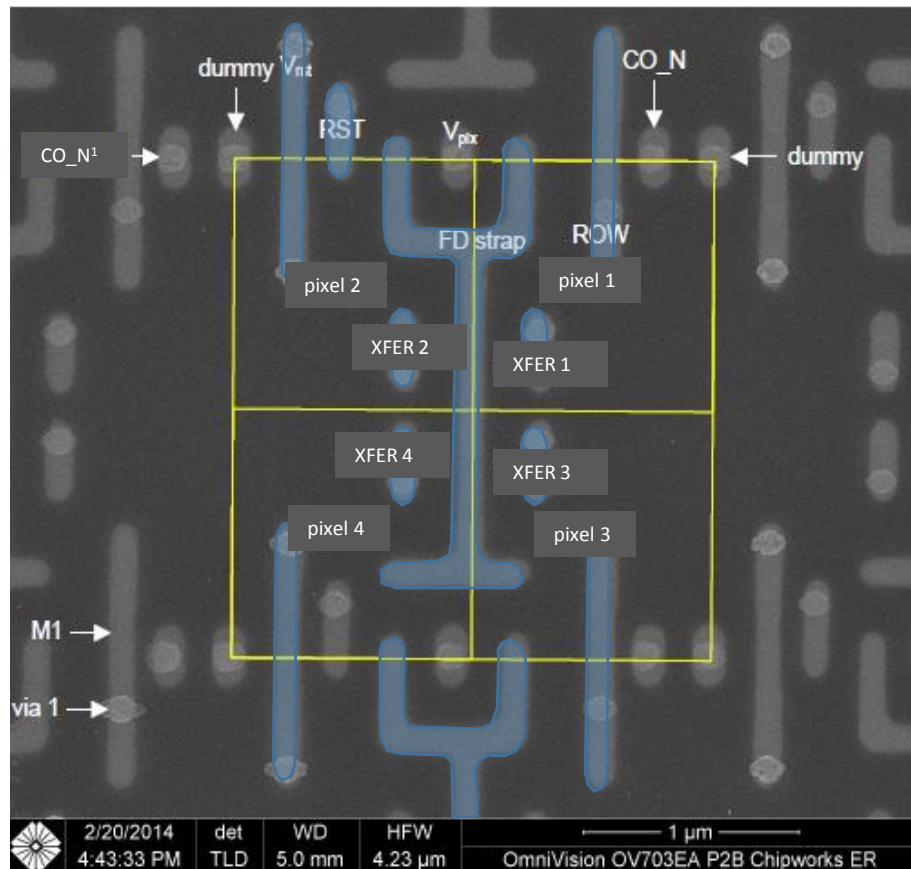
Pixel Circuit Diagram

Figure 4.1.1 Shared Pixel Schematic

The shared pixel schematic for the four-shared pixel architecture is shown in Figure 4.1.1. T
four photodiodes output through the transfer transistors (T1 – T4) to a common floating diffu
(FD).

Shared Pixels at Contact/Poly - SEM

EXHIBIT M - USP 8,978,401 - OmniVision Technologies, Inc. OV8888 (Pinegel)

Shared Pixels at Via 1/Metal 1 - SEM

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