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# EXHIBIT K

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1. A solid state imaging apparatus comprising:

**(A) a plurality of photodiodes** arranged in an array;

**(B) a plurality of floating diffusion sections** each being connected to ones of the plurality of photodiodes via each of **(C) the plurality of transfer transistors**;

**(D) a plurality of read-out lines** each being selectively connected to at least two of **(C) the plurality of transfer transistors**;

**(E) a plurality of pixel amplifier transistors** each detecting and outputting the potential of each of the plurality of floating diffusion sections;

and **(F) a plurality of power supply lines** applying voltage to drain sections of the pixel amplifier transistors, wherein

**(A) the plurality of photodiodes** includes **(a1) a first photodiode** and **(a2) a second photodiode**,

**(D) the plurality of read-out lines** includes **(d1) a first read-out line** and **(d2) a second read-out line**,

**(C) the plurality of transfer transistors** includes **(c1) a first transfer transistor** and **(c2) a second transfer transistor**;

**(a1) the first photodiode** is in **row n**, where **n** is a positive integer, **(a2) the second photodiode** is in **row n+1**, **(a1) the first photodiode** and **(a2) the second photodiode** are **in the same column**,

one of **(B) the plurality of floating diffusion sections** is connected to **(a1) the first photodiode** via **(c1) the first transfer transistor**

and is connected to **(a2) the second photodiode** via **(c2) the second transfer transistor**,

**(D) the plurality of read-out lines** are disposed between **(a1) the first** and **(a2) the second photodiodes**,

**(d1) the first read-out line** is connected to **(c1g) a gate of the first transfer transistor**,

**(d2) the second read-out line** is connected to **(c2g) a gate of the second transfer transistor**, and

**(D) the plurality of read-out lines** and one of **(F) the plurality of power supply lines** intersect with each other.

### Pixel Circuit Diagram

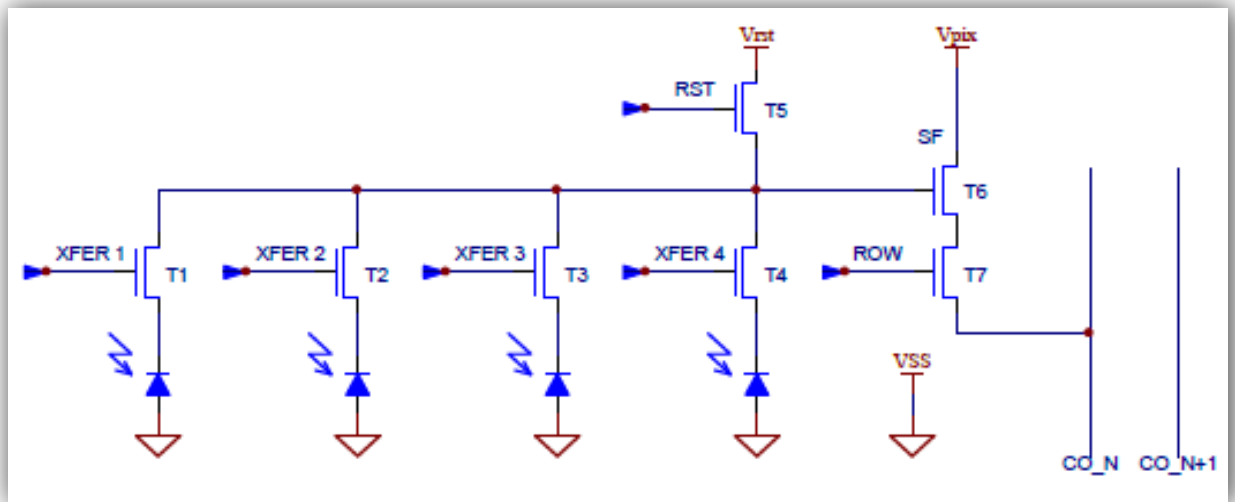
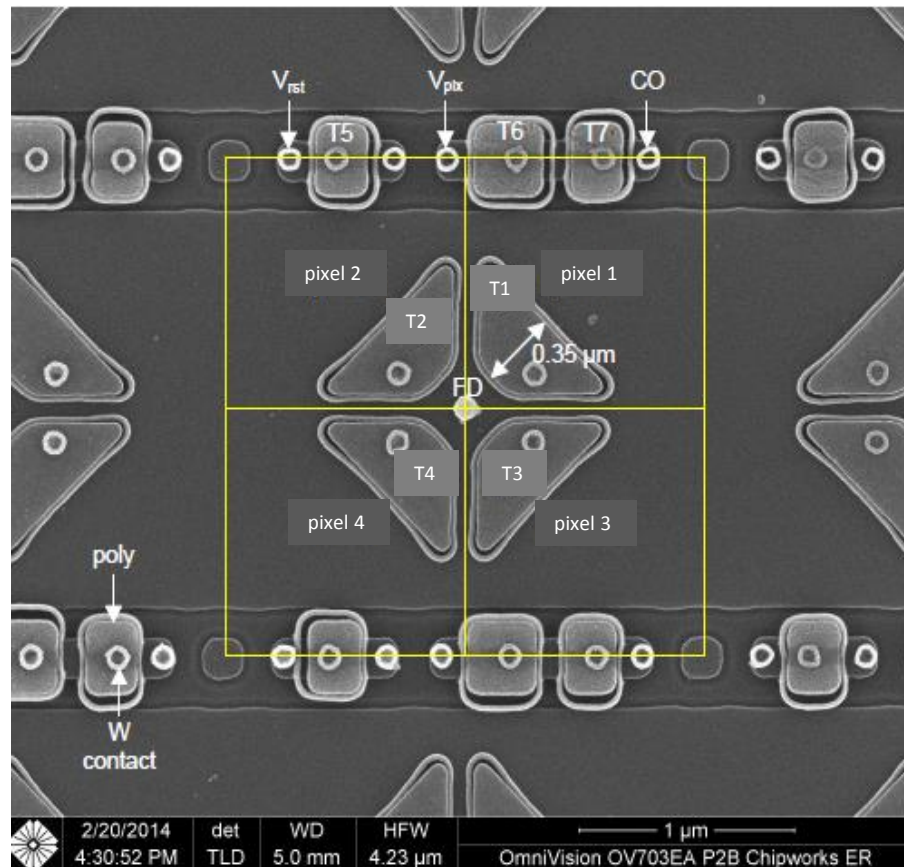


Figure 4.1.1 Shared Pixel Schematic

The shared pixel schematic for the four-shared pixel architecture is shown in Figure 4.1.1. The four photodiodes output through the transfer transistors (T1 – T4) to a common floating diffusion (FD).



Shared Pixels at Contact/Poly - SEM



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