FIG. 34

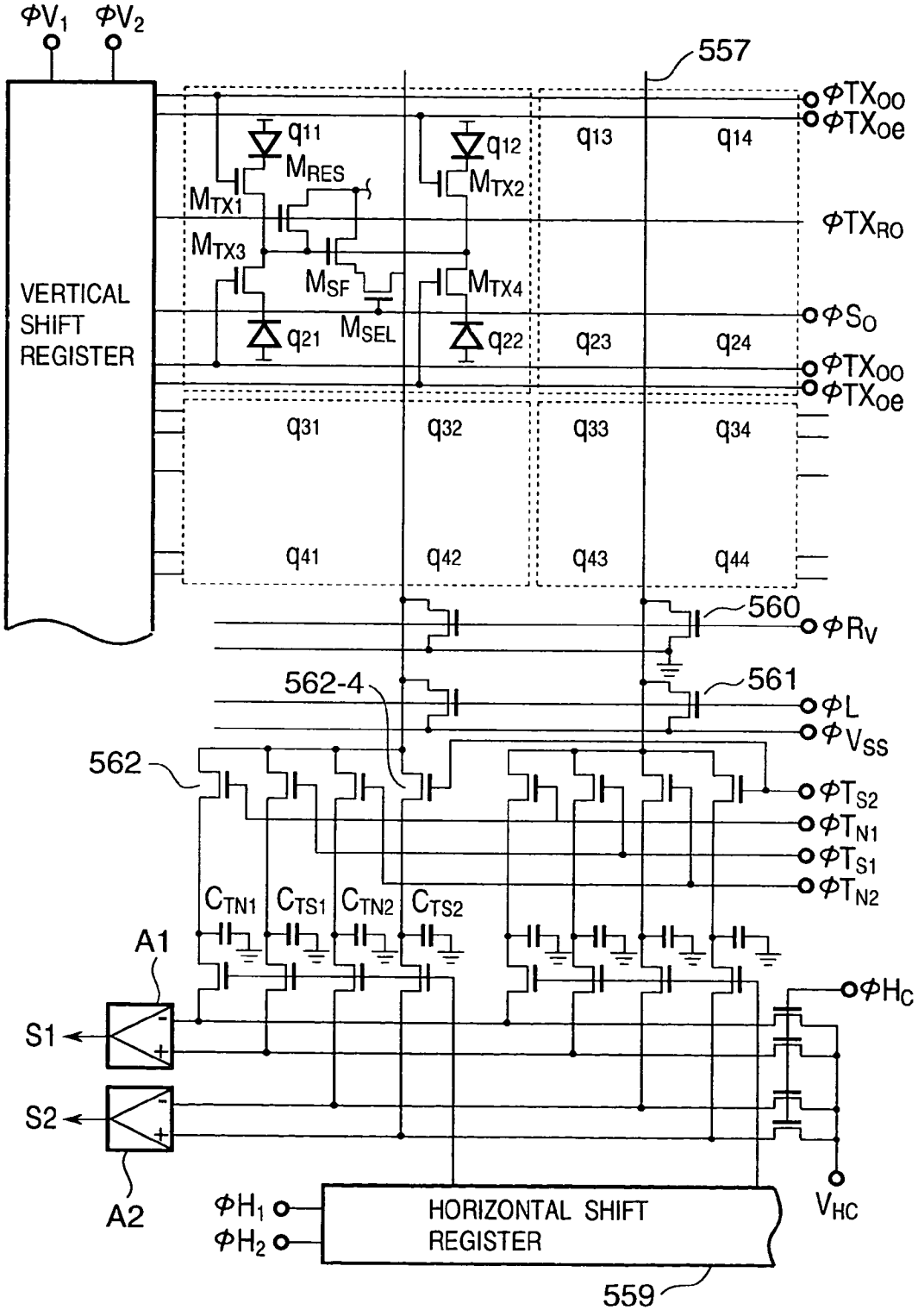

φV1
φV2
557
φTXoo
φTXoe
φTXRO
φSo
φTXoo
φTXoe
VERTICAL SHIFT REGISTER
q11
MRES
MTX1
MTX3
MSF
MSEL
q12
MTX2
MTX4
q13
q14
q21
q22
q23
q24
q31
q32
q33
q34
q41
q42
q43
q44
560
φRV
562-4
561
φL
φVSS
562
φTS2
φTN1
φTS1
φTN2
CTN1
CTS1
CTN2
CTS2
A1
φHC
S1
S2
A2
φH1
φH2
HORIZONTAL SHIFT REGISTER
VHC
559

FIG. 35

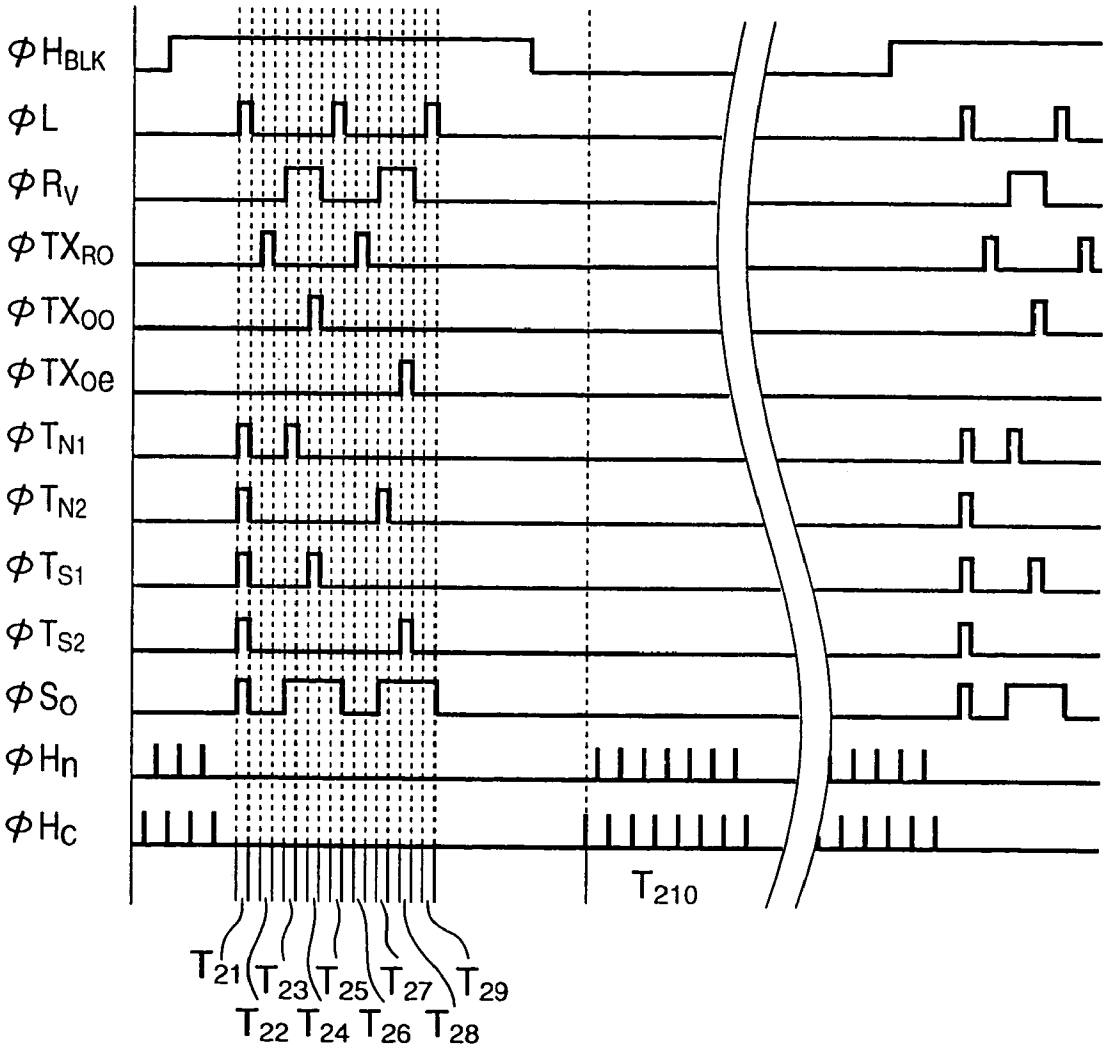

φ H_BLK
φ L
φ R_V
φ TX_RO
φ TX_OO
φ TX_Oe
φ T_N1
φ T_N2
φ T_S1
φ T_S2
φ S_O
φ H_n
φ H_C
T210
T21 T23 T25 T27 T29
T22 T24 T26 T28

FIG. 36

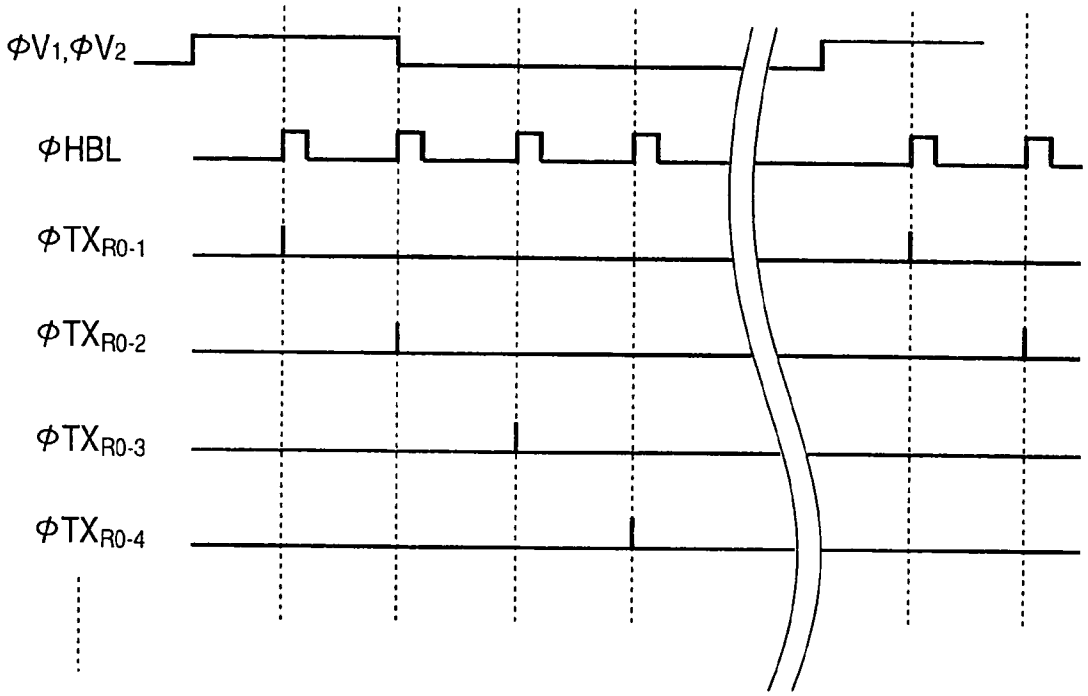


FIG. 37

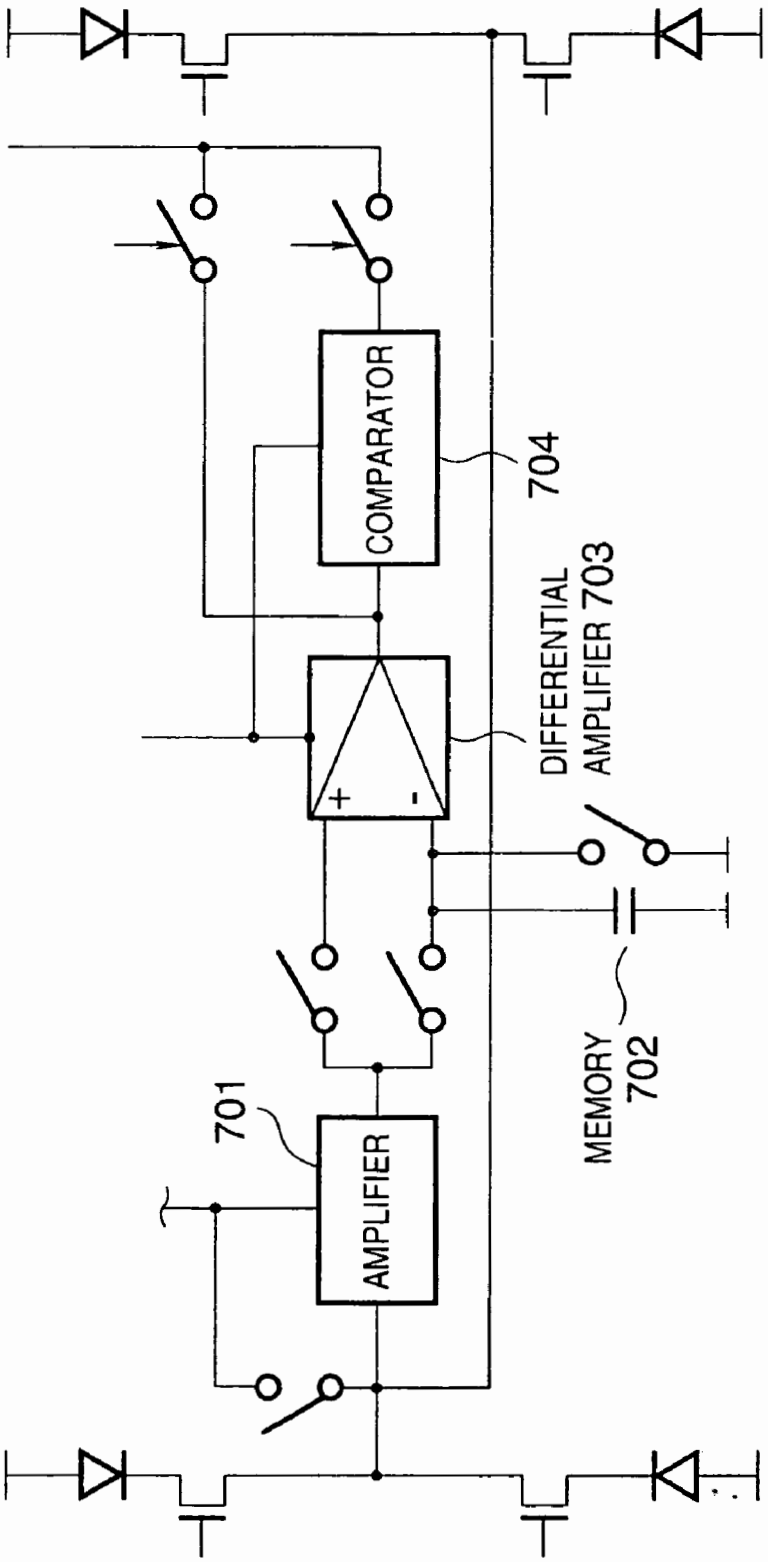

COMPARATOR
704
DIFFERENTIAL AMPLIFIER 703
+
-
MEMORY 702
701
AMPLIFIER

FIG. 38

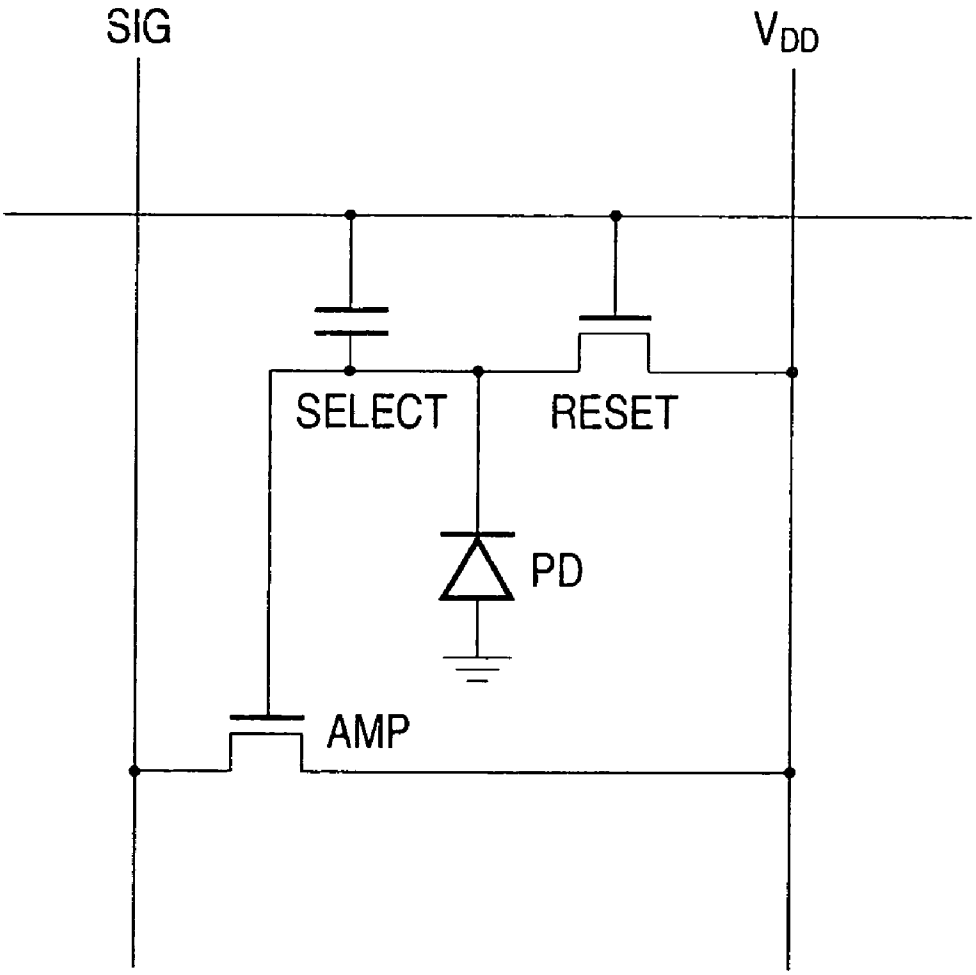


FIG. 39

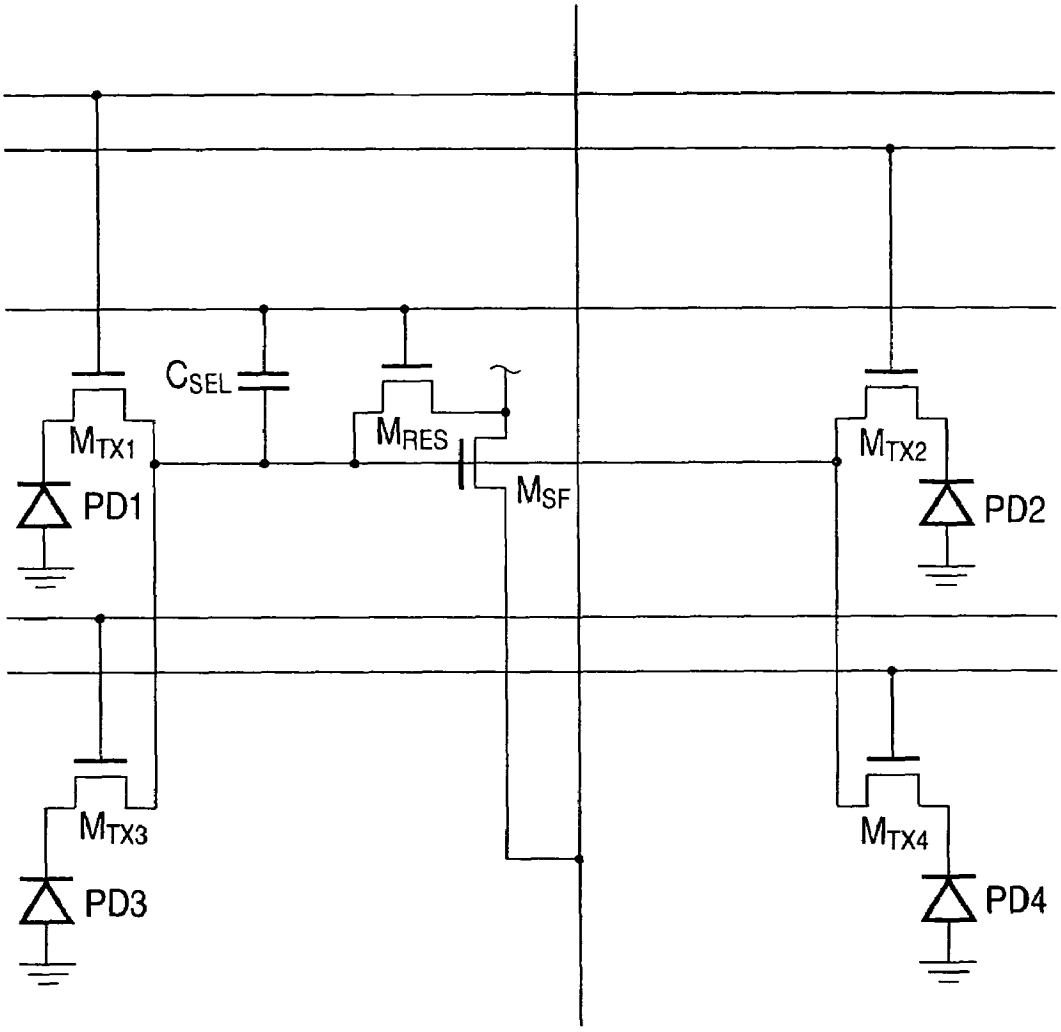


FIG. 40

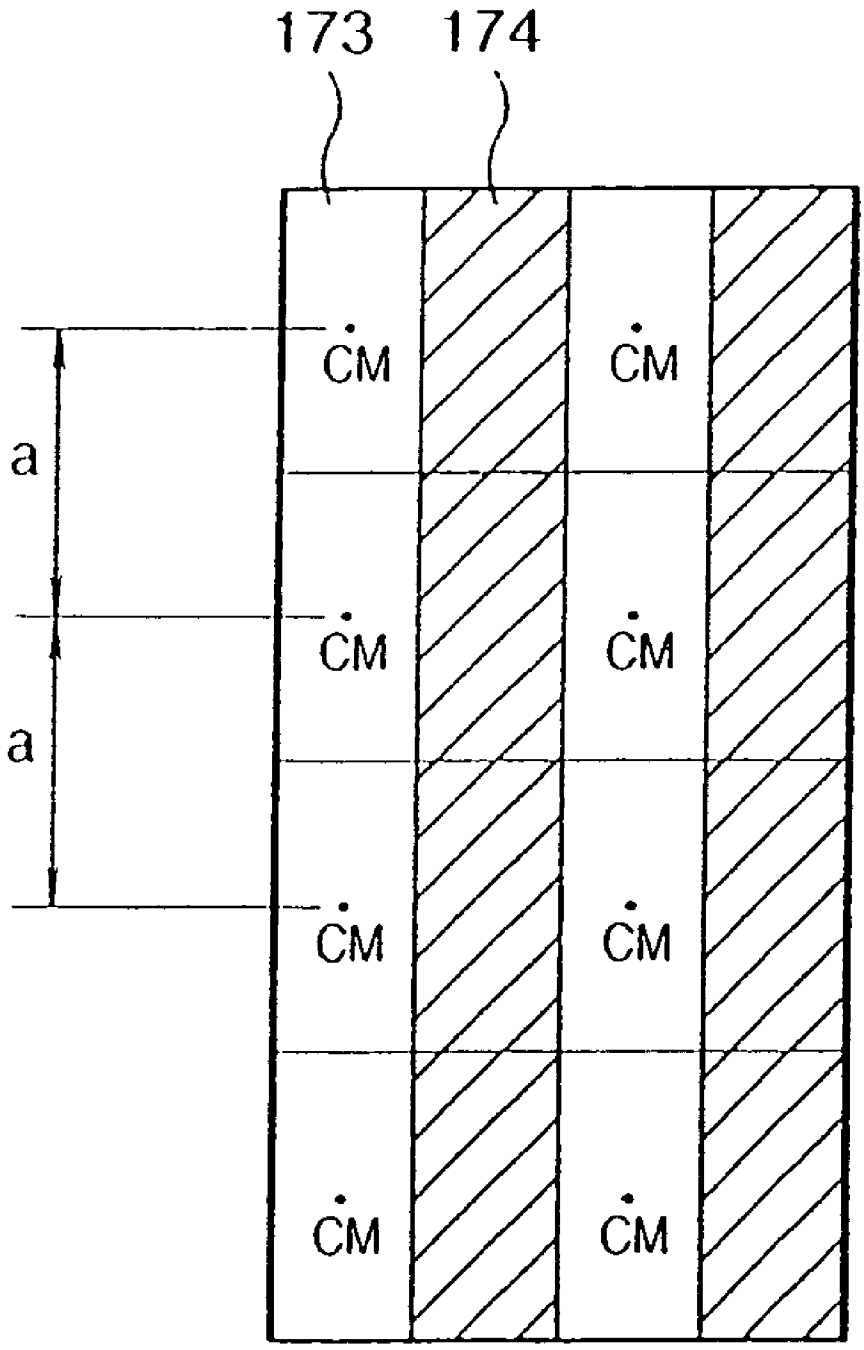


FIG. 41

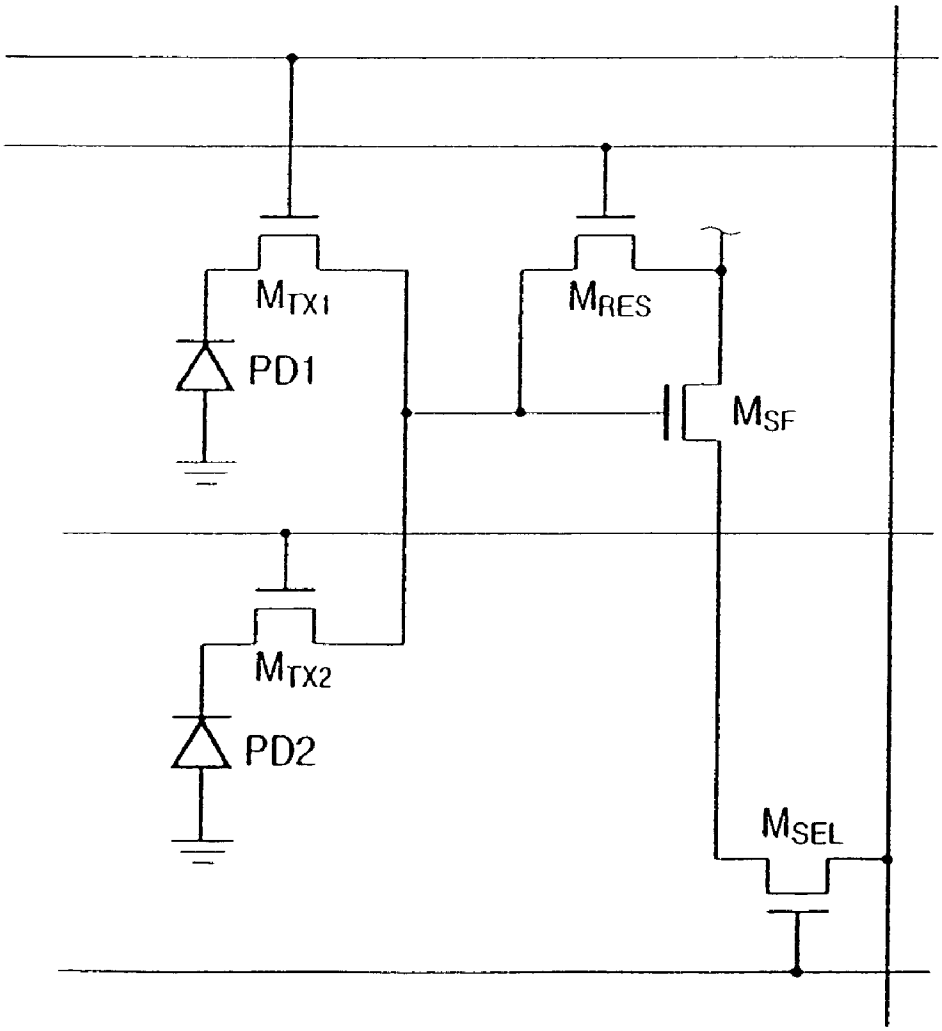


FIG. 42

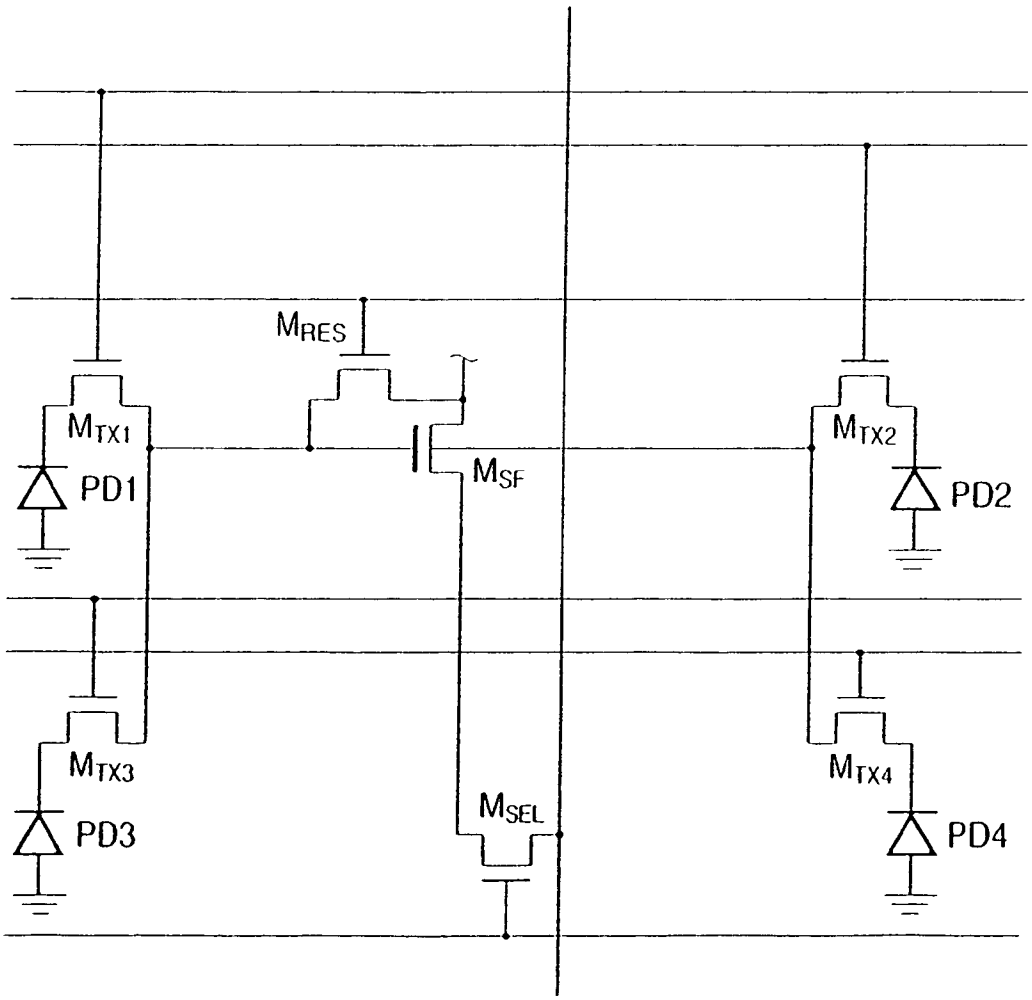


FIG. 43

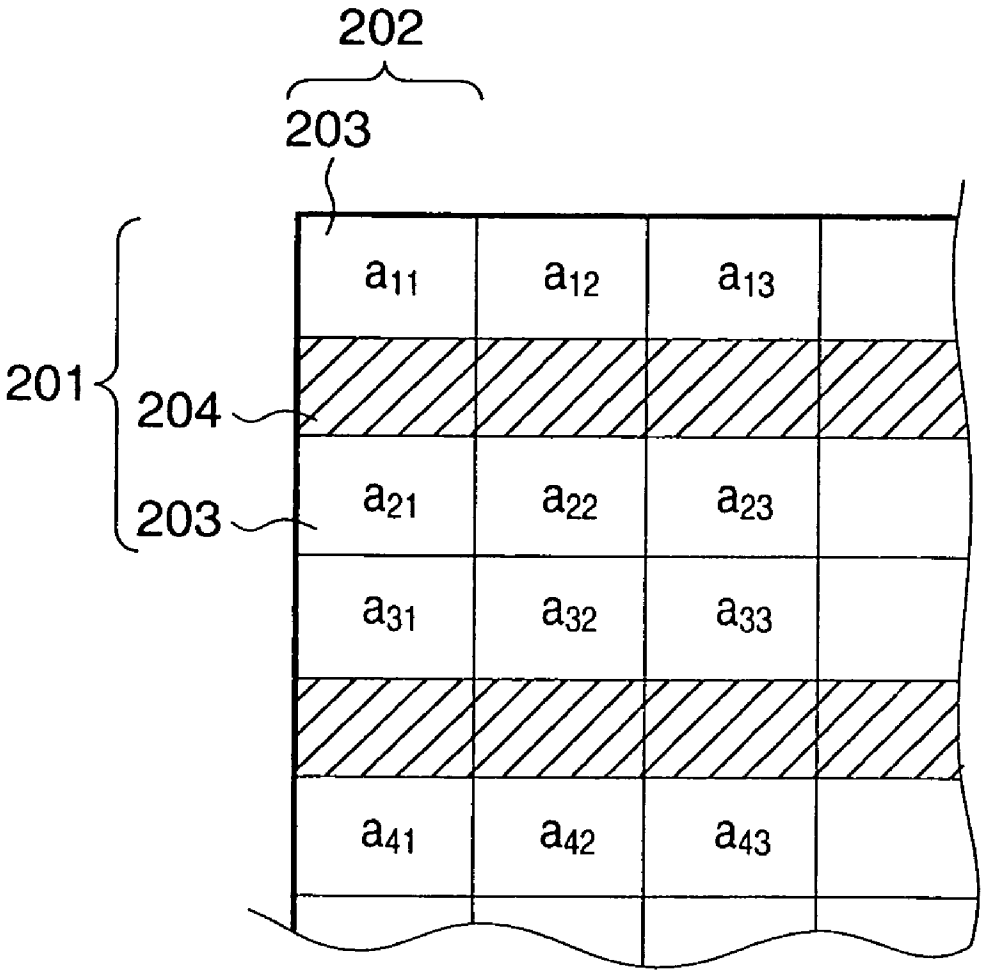

202
203
201
204
203
a11
a12
a13
a21
a22
a23
a31
a32
a33
a41
a42
a43

FIG. 44

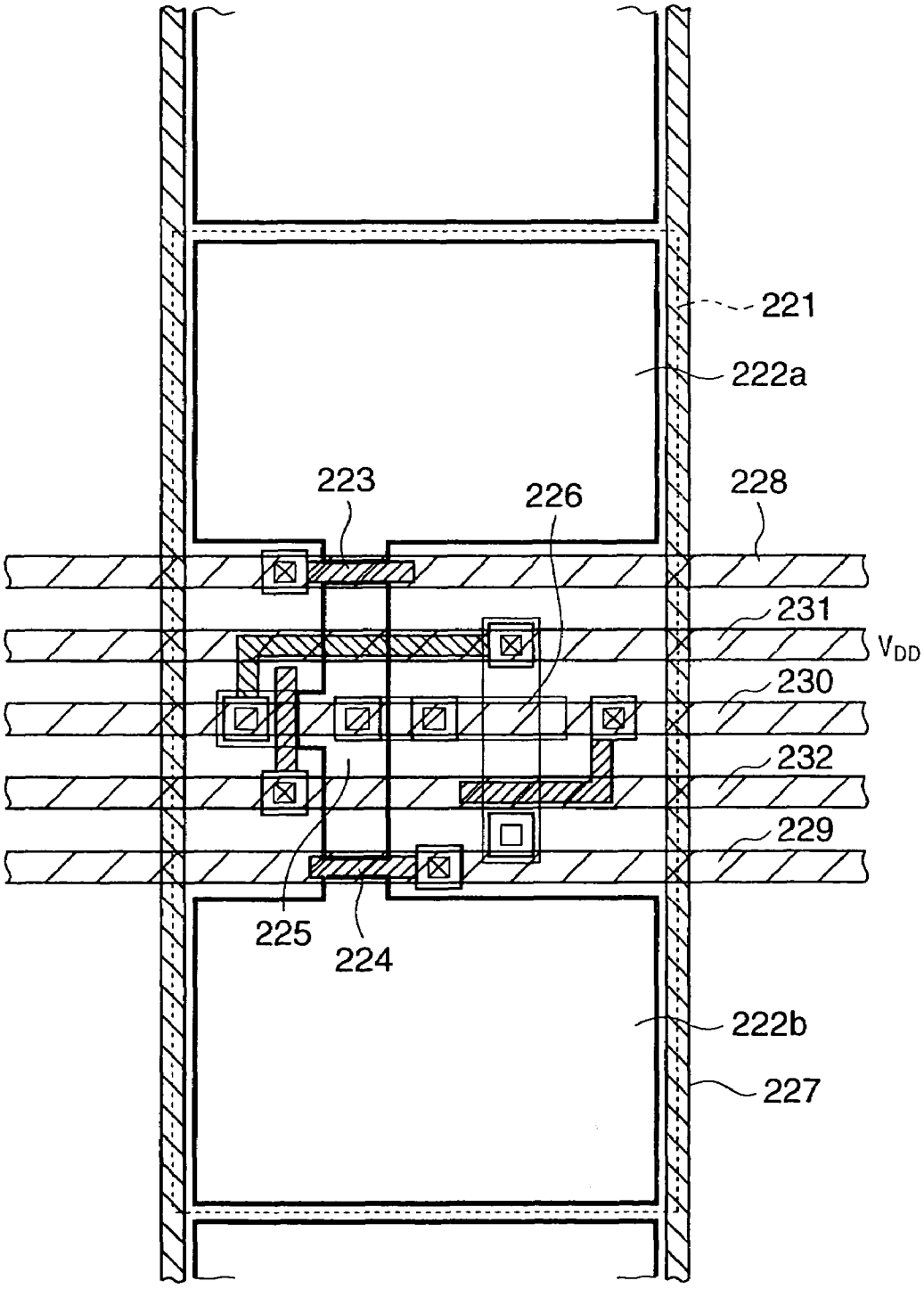


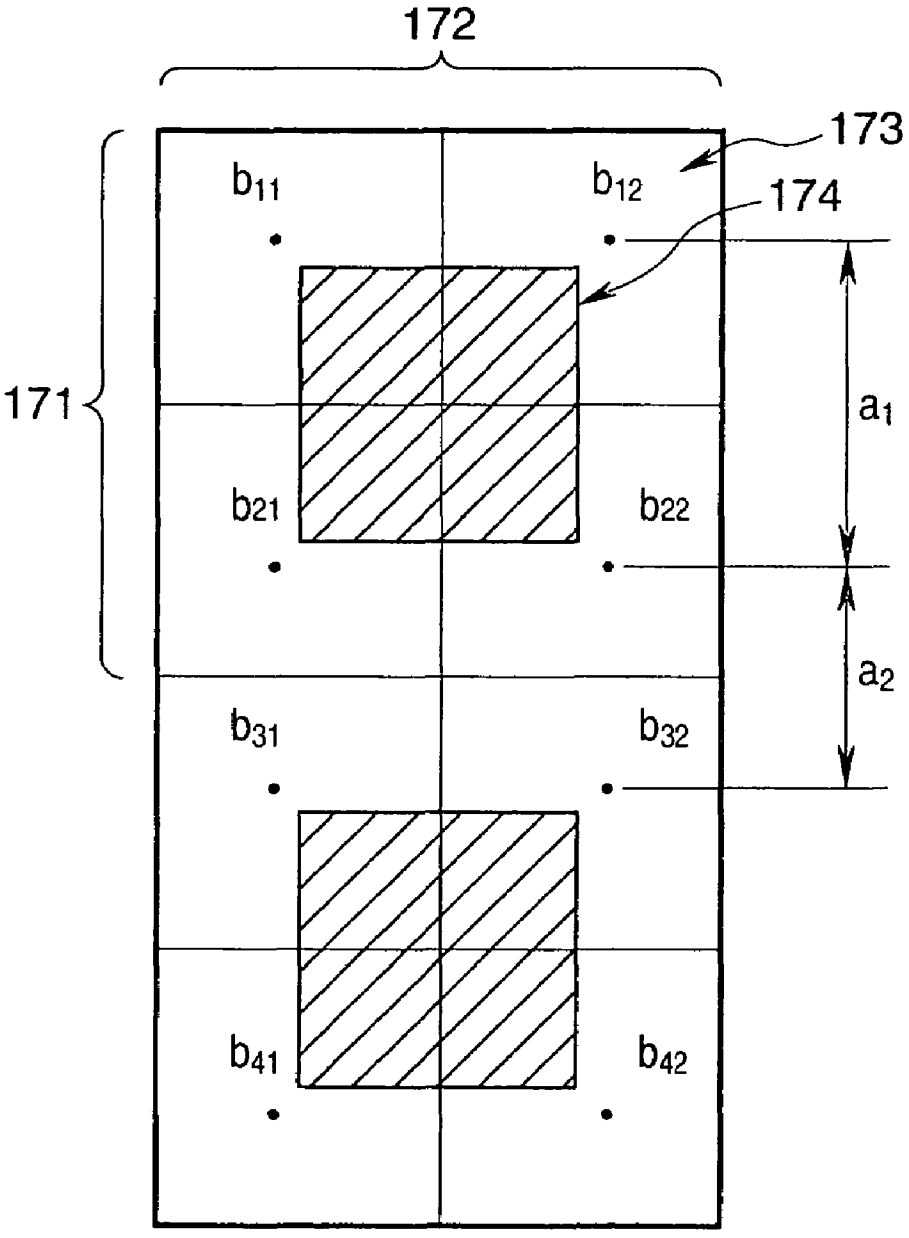
FIG. 45A

R	G	R	G
G	B	G	B
R	G	R	G

FIG. 45B

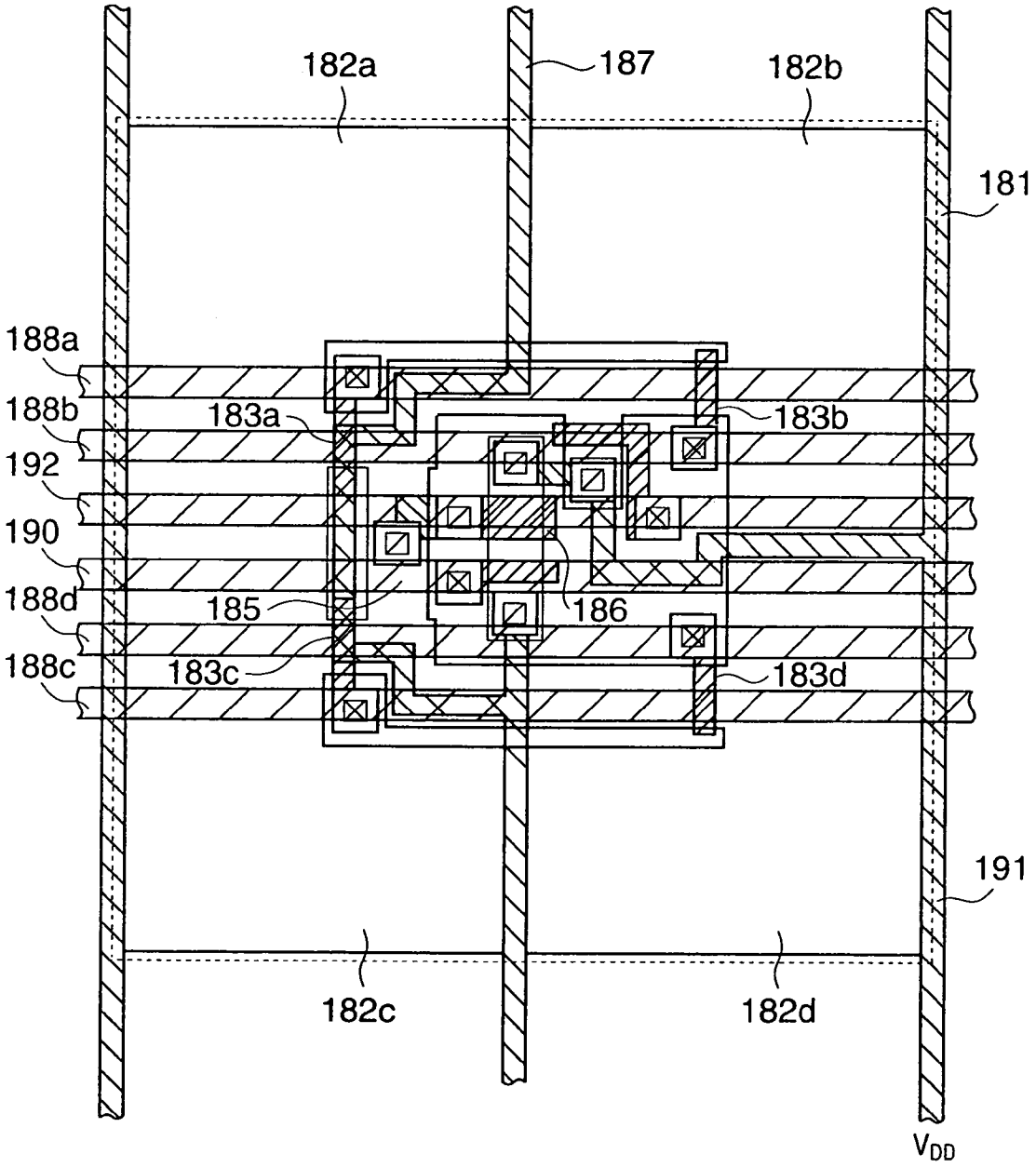
Cy	Ye
Mg	G
Cy	Ye
G	Mg

FIG. 46



$a_1 > a > a_2$

FIG. 47


182a
187
182b
181
188a
188b
183a
183b
192
190
188d
185
186
188c
183c
183d
191
182c
182d
V_{DD}

ARRANGEMENT OF CIRCUITS IN PIXELS, EACH CIRCUIT SHARED BY A PLURALITY OF PIXELS, IN IMAGE SENSING APPARATUS

BACKGROUND OF THE INVENTION

The present invention relates to an image sensing apparatus in which a plurality of pixels share a common circuit and an image sensing system using the apparatus.

Conventionally, as an image sensing apparatus using a gain cell, or an active pixel sensor (APS), there are image sensing apparatuses utilizing MOS FET, JFET, bipolar transistor.

These image sensing apparatuses amplify photo-charges generated by photodiodes, that are photoelectric conversion elements, by various methods, then output the amplified photo-charge signals as image information. Since an amplifier for amplifying photo-charge exists in each pixel, the pixel is called a gain cell or an APS.

An APS includes an amplifier and its controller in each pixel, therefore, the percentage of an area reserved for the photoelectric conversion element in a pixel (area ratio) or area where light incidents in a pixel (aperture) tends to be small. This may cause deterioration of the dynamic range, sensitivity, and the S/N ratio of an image sensing apparatus.

As described above, when an amplifier is provided in each pixel, as shown in FIG. **40**, the aperture decreases. To prevent the decrease in the area or the aperture caused by the amplifier, methods of sharing an amplifier by a plurality of pixels, as disclosed in the Japanese Patent Application Laid-Open Nos. 63-100879 and 9-46596, have been proposed.

FIGS. **41** and **42** illustrate configurations shown in the above documents. Referring to FIGS. **41** and **42**, reference PD**1** to PD**4** denote photodiodes as photoelectric conversion elements; M_{TX1} to M_{TX4} are MOS transistors for transferring photo-charges generated by the photodiodes PD**1** to PD**4**; M_{RES} is a MOS transistor for resetting the MOS transistors M_{TX1} to M_{TX4}; and M_{SF} and M_{SEL} are MOS transistors configuring an amplifier (source follower). M_{SEL} also functions as a selection switch for selecting a pixel.

However, in the Japanese Patent Application Laid-Open Nos. 63-100879 and 9-46596, no practical layout of the foregoing elements on a chip when a plurality of pixels share a single amplifier is discussed.

Further, there is no description about a layout in a case where an amplifier, shared by a plurality of pixels, is replaced by another unit.

SUMMARY OF THE INVENTION

The present invention has been made in consideration of the above situation, and has as its first object to provide an image sensing apparatus, in which a common circuit, such as an amplifier, is shared by a plurality of pixels, achieving good performance without deterioration in resolution.

Further, it is the second object of the present invention to provide an image sensing apparatus having a noise reduction system, preferably used in the image sensing apparatus, in which a common circuit is shared by a plurality of pixels.

It is the third object of the present invention to provide an image sensing system using the foregoing image sensing apparatuses as a sensor unit.

According to the present invention, the foregoing first object is attained by providing an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in either one or two dimensions, wherein the plurality of photoelectric conversion elements are arranged at a predetermined interval.

The first object is also attained by providing an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in two dimensions, wherein photoelectric conversion elements, out of the plurality of photoelectric conversion elements, which are covered by a color filter that contributes mostly to forming a luminance signal are arranged in a same interval both in the horizontal and vertical directions by arranging adjoining rows or columns of photoelectric conversion elements shifted from each other.

Further, the first object is also attained by providing an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in either one or two dimensions, characterized by comprising adjustment means for adjusting centers of mass of light-receiving areas of the plurality of photoelectric conversion elements provided in a central portion of the image sensing apparatus, so as to be apart at a same spatial interval.

Furthermore, the first object is also attained by providing an image sensing apparatus having a plurality of unit cells, each including a plurality of photoelectric conversion elements and a common circuit shared by the plurality of photoelectric conversion elements, arranged in either one or two dimensions, characterized by comprising adjustment means for adjusting centers of mass of light-receiving areas of photoelectric conversion elements selected from the plurality of photoelectric conversion elements, provided in a central portion of the image sensing apparatus, on the basis of a predetermined condition, so as to be apart at a same spatial interval.

Further, to achieve the second object of the present invention, noise reading means for reading a noise of the common circuit; first signal reading means for reading a first signal through the common circuit; second signal reading means for reading a second signal through the common circuit; and noise reduction means for reducing the noise from the first and second signals are further provided.

Alternatively, noise reading means for reading a noise of the common circuit; signal reading means for reading a plurality of signals through the common circuit; and noise reduction means for reducing the noise from the plurality of signals are further provided.

Further, the third object of the present invention is achieved by providing an image sensing system having the image sensing apparatus as described above, a lens system for forming an image on the image sensing apparatus, and a signal processing circuit for processing an output signal from the image sensing apparatus.

Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the FIG. **5**res thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodi-

ments of the invention and, together with the description, serve to explain the principles of the invention.

FIG. **1** is a block diagram illustrating a configuration of the image sensing system according to an embodiment of the present invention;

FIG. **2**A shows a layout of amplifiers in pixels according to a first embodiment of the present invention;

FIG. **2**B shows another layout of amplifiers in pixels according to the first embodiment of the present invention;

FIG. **3** shows a practical pattern layout of two photodiodes and an amplifier according to the first embodiment of the present invention;

FIG. **4** is a brief view of FIG. **3** from which a part of lines are omitted;

FIG. **5** shows another practical pattern layout of two photodiodes and an amplifier according to the first embodiment of the present invention;

FIG. **6** is a brief view of FIG. **5** from which a part of lines are omitted;

FIG. **7** is an enlarged view showing vicinity of a floating diffusion portion according to the first embodiment of the present invention;

FIG. **8** is an enlarged view showing vicinity of the floating diffusion portion according to the first embodiment of the present invention;

FIG. **9** is a circuit diagram of a unit cell of a CMOS sensor in which two photodiodes share one amplifier according to the first embodiment of the present invention;

FIG. **10** is a circuit diagram of the image sensing apparatus including a signal processing circuit according to the first embodiment of the present invention;

FIG. **11** is a timing chart for operating an image sensing apparatus according to the first and second embodiments of the present invention;

FIG. **12** is a timing chart for operating the apparatus according to the first and second embodiments of the present invention;

FIG. **13** shows a layout of common circuits in pixels according to the second embodiment of the present invention;

FIG. **14** shows another layout of common circuits in pixels according to the second embodiment of the present invention;

FIG. **15** is a practical pattern layout of the common circuits each shared by two photodiodes according to the second embodiment of the present invention;

FIG. **16** is a circuit diagram of the image sensing apparatus including a signal processing circuit according to the second embodiment of the present invention;

FIG. **17** is a circuit diagram of a unit cell configured with a common circuit and photodiodes according to the second embodiment of the present invention;

FIG. **18** is an explanatory view for explaining a signal processing circuit;

FIG. **19** is a layout of amplifiers in pixels according to a third embodiment of the present invention;

FIG. **20** is another layout of amplifiers in pixels according to the third embodiment of the present invention;

FIG. **21** is another layout of amplifiers in pixels according to the third embodiment of the present invention;

FIG. **22** is another layout of amplifiers in pixels according to the third embodiment of the present invention;

FIG. **23** is a practical pattern layout of four photodiodes and an amplifier according to the third embodiment of the present invention;

FIG. **24** is another practical pattern layout of four photodiodes and an amplifier according to the third embodiment of the present invention;

FIG. **25** is an explanatory view for explaining a variation of a layout;

FIG. **26** shows a practical pattern layout according to the third embodiment of the present invention;

FIG. **27** shows another layout of light-receiving areas according to the third embodiment of the present invention;

FIG. **28** shows another practical pattern layout of four photodiodes and an amplifier according to the third embodiment of the present invention;

FIG. **29** is an example when on-chip lens according to the third embodiment of the present invention;

FIG. **30** is a circuit diagram of a unit cell of a CMOS sensor having the aforesaid configurations according to the third embodiment of the present invention;

FIG. **31** is a circuit diagram of the image sensing apparatus including a signal processing unit according to the third embodiment of the present invention;

FIG. **32** is a timing chart for operating an image sensing apparatus according to the third embodiment of the present invention;

FIG. **33** is a circuit diagram of an image sensing apparatus including the signal processing unit according to a first modification of the third embodiment of the present invention;

FIG. **34** is a circuit diagram of an image sensing apparatus including a signal processing unit according to a second modification of the third embodiment of the present invention;

FIG. **35** is a timing chart for operating the image sensing apparatus shown in FIG. **34** according to the second modification of the third embodiment of the present invention;

FIG. **36** is a timing chart during a vertical blanking period according to the second configuration of the third embodiment of the present invention;

FIG. **37** shows a configuration of a common circuit according to a fourth embodiment of the present invention;

FIG. **38** is a circuit diagram of a unit cell of another image sensor to which the present invention is applied;

FIG. **39** is a circuit diagram of a configuration of an amplifier shared by four photodiodes according to an embodiment of the present invention;

FIG. **40** shows a conventional layout of amplifiers in pixels;

FIG. **41** is a circuit diagram of a conventional configuration;

FIG. **42** is a circuit diagram of another conventional configuration;

FIG. **43** shows a layout of common circuits in pixels when each common circuit is shared by two pixels;

FIG. **44** shows a practical pattern layout of two photodiodes and an amplifier shown in FIG. **43**;

FIGS. **45**A and **45**B shows color filter arrangements;

FIG. **46** is a layout of common circuits in pixels when each common circuit is shared by four pixels; and

FIG. **47** shows a practical pattern layout of four photodiodes and an amplifier.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described in detail below in accordance with the accompanying drawings.

<Possible Arrangements of Pixels and Common Circuit>

First, possible arrangements of a plurality of pixels and a common circuit, shared by the pixels, based on the disclosure of the Japanese Patent Application Laid-Open Nos. 63-100879 and 9-46596, are described below. In the following explanation, an amplifier is used as an example of the common circuit in an image sensing apparatus.

FIG. **43** shows an example of a layout of common circuits in pixels, when each common circuit is shared by two pixels. In FIG. **43**, a case where each amplifier, as the common circuit, is shared by two pixels in two rows is shown, and, more specifically, each amplifier **204** is arranged between two photodiodes **203** above and below the row of the amplifiers **204** (such as, pairs of photodiodes a_{11} and a_{21}, a_{42} and a_{22}, a_{31} and a_{41}, a_{32} and a_{42}, and so on). Note, a photodiode **203**, which is a photoelectric conversion element, and one half of the amplifier **204** configure a pixel. Reference numeral **201** indicates a unit cell repeated in the column direction, and reference numeral **202** indicates the unit cell repeated in the row direction.

FIG. **44** shows a practical pattern layout of two photodiodes and an amplifier (a signal unit cell). The image sensing apparatus is a CMOS sensor, in this case.

Referring to FIG. **44**, reference numeral **221** denotes the unit cell (area surrounded by a dash line), which are referred to by reference numerals **201** and **202** in FIG. **43**, having a size of two pixels, and repeatedly arranged in both the row and column directions. Light incidents on photodiodes **222***a* and **222***b* (areas surrounded by bold lines, correspond to the photodiode pairs a_{11} and a_{21}, a_{12} and a_{22}, a_{31} and a_{41}, a_{32} and a_{42}, and so on, shown in FIG. **43**) is converted into electrical charges (photo-charges), and accumulated within the photodiodes **222***a* and **222***b*. The accumulated photo-charges are respectively transferred to a floating diffusion portion **225** (also surrounded by a bold line) via a transfer gate **223** for an odd row and a transfer gate **224** for an even row, further transferred to the gate (floating gate) **226** of a MOS-type amplifier, which is the amplifier **204**. Current flowing through the MOS-type amplifier is modulated, and the output current is taken out from the pixel array via a vertical signal line **227**.

X-Y addressing of the two dimensional pixel array, as shown in FIG. **43**, in the image sensing apparatus is realized by the vertical signal line **227**, an odd-row scanning line **228**, an even-row scanning line **229**, and a row selection line **230**. In addition, a power line **231** for supplying electric power V_{DD} and a reset line **232** for resetting the floating diffusion portion **225** and the gate **226** to a predetermined voltage are also arranged in the horizontal direction.

The lines **228** to **232** are arranged above the wiring of the unit cells, and the lines are basically wide. The area under these five opaque lines **228** to **232** does not receive light, therefore, the amplifier **204** is arranged under the lines **228** to **232**. For the above reason, the two photodiodes sharing the amplifier are considered to be arranged on the upper and lower sides of the amplifier.

With this layout, however, since the centers of mass (CM) of the photodiodes are not equal, as seen in FIG. **43**, the following problems arise.

First, if the pixel array outputs signals of a single color, since spatial frequency and resolution are different in one part from the other, the resolution deteriorates, and moreover, moiré appears.

It is possible to cover the pixel array with a color filter whose color arrangement is as shown in FIG. **45**A or **45**B. In designing the color filter, colors may be arranged so that difference between intervals between pixels corresponding to each color is minimized. In this case, however, the color arrangement is strictly limited.

Further, if the Bayer filter as shown in FIG. **45**A is used, intervals between pixels corresponding to green (G) filter, which contributes most to luminance (Y) signals that the human eye is most sensitive to, are not equal. More specifically, considering the positions of the photodiodes, e.g., a_{12}, a_{23}, and a_{32} corresponding to the green filter, the distance between the photodiodes a_{12} and a_{23} in the column direction is different from the distance between the photodiodes a_{23} and a_{32} in the column direction. Thus, the filter arrangement causes different intervals between pixels corresponding to green filter, resulting in a moiré problem; therefore, the quality of an obtained image is not good.

Next, referring to FIG. **46**, an example of a layout of common circuits in pixels when each common circuit is shared by four pixels, is explained.

In this case, an amplifier, i.e., the common circuit, is shared by adjoining four pixels in two rows and two columns (2×2), and each amplifier **174** is surrounded by four photodiodes **173** (such as 2×2 photodiodes b_{11}, b_{12}, b_{21}, and b_{22}, and b_{31} b_{32}, b_{41}, and b_{42}). In FIG. **46**, reference numeral **171** indicates a unit cell repeated in the column direction, and reference numeral **172** indicates the unit cell repeated in the row direction.

FIG. **47** shows a practical pattern layout of four photodiodes and an amplifier. The image sensing apparatus is a CMOS sensor in this case, too.

Referring to FIG. **47**, reference numeral **181** denotes the unit cell (area surrounded by a dash line), which is referred to by reference numerals **171** and **172** in FIG. **46**, having a size of four pixels, and repeatedly arranged in both the row and column directions. Light incidents on photodiodes **182***a* to **182***d* (correspond to either one of groups of the photodiodes, b_{11}, b_{12}, b_{21}, and b_{22}, and b_{31}, b_{32}, b_{41}, and b_{42} shown in FIG. **46**) is converted into electrical charges (photo-charges), and accumulated within the photodiodes **182***a* to **182***d*. The accumulated charges are respectively transferred to a floating diffusion portion **185** via transfer gates **183***a* to **183***d*, respectively, further transferred to the gate **186** of a MOS-type amplifier, which is the amplifier **174**. Current flowing through the MOS-type amplifier is modulated, and the output current is taken out from the pixel array via a vertical signal line **187**.

X-Y addressing of the two dimensional pixel array, as shown in FIG. **46**, in the image sensing apparatus is realized by the vertical signal line **187**, scanning lines **188***a* to **188***d*, and a row selection line **190**. In addition, a power line **191** for supplying electric power V_{DD} is arranged in the column direction, and a reset line **192** for resetting the floating diffusion portion **185** and the gate **186** to a predetermined voltage are arranged in the horizontal direction.

The lines **188** to **192** are arranged above the wiring of the unit cells, and the lines are basically wide. The area under these six opaque lines **188** to **192** does not receive light, therefore, the amplifier **174** is arranged under the lines **188** to **182**. For the above reason, the four photodiodes sharing the amplifier are considered to be arranged around the amplifier.

With this layout, however, since the intervals between the centers of mass (CM) of photodiodes are not equal, as seen in FIG. **46**, the following problem arises.

If the pixel array outputs signals of a single color, since spatial frequency and resolution are different in one part from another, the resolution deteriorates, and moreover, moiré appears. The moiré is a serious problem, and an image sensing apparatus with a moiré problem does not sell on the

market. This can be said for any image sensing apparatus having a configuration in which any number of pixels share a single common circuit.

Accordingly, the inventors of the present application have developed image sensing apparatuses having improved arrangements of pixels and circuits shared by a plurality of pixels.

The image sensing apparatuses will be described below in detail.

<Basic Configuration of Image Sensing Apparatus>

FIG. **1** is a block diagram illustrating a configuration of the image sensing apparatus according to an embodiment of the present invention.

As shown in FIG. **1**, light incoming through an optical system **21** forms an optical image on a CMOS sensor **22**, and converted into electric charges by a pixel array arranged on the CMOS sensor. The photo-charges are further converted, processed and outputted by a signal processing circuit **23** in a predetermined method. The processed signals are recorded on an information storage medium or outputted by a recording/transmission system **24**. The recorded or transmitted information is retrieved by a retrieving system **27**. The CMOS sensor **22** and the signal processing circuit **23** are controlled by a timing controller **25**, and the optical system **21**, the timing controller **25**, the recording/transmission system **24**, and the retrieving system **27** are controlled by a system controller **26**.

Next, the CMOS sensor **22** according to the present invention will be described in detail.

First Embodiment

FIG. **2**A shows a layout of amplifiers **12** in pixels when each amplifier **12** is shared by two pixels adjoining in the column direction, and FIG. **2**B shows a layout of amplifiers **12** in pixels when each amplifier **12** is shared by two pixels adjoining in the row direction.

In FIG. **2**A, two photoelectric conversion elements **11** (such as, pairs of the elements P_{11}, and P_{21}, P_{31} and P_{41}, P_{12} and P_{22}, P_{32} and P_{42}, and so on) sharing one amplifier **12** are arranged next to each other in the column direction, and the amplifier **12** is arranged along the adjoining pixels. In this manner, intervals between the centers of mass of the photoelectric conversion elements **11** (e.g., P_{11}, P_{21}, P_{31}, P_{41}, P_{12}, P_{22}, P_{32}, P_{42}) in both the row and column directions become equal. Reference numeral **13** indicates a unit cell repeated in the column direction, and reference numeral **14** indicates the unit cell repeated in the row direction.

Further, in FIG. **2**B, two photoelectric conversion elements **11** (such as, pairs of the elements P_{11} and P_{12}, P_{13} and P_{14}, P_{21} and P_{22}, P_{23} and P_{24}, P_{31} and P_{32}, P_{33} and P_{34}, and so on) sharing one amplifier **12** are arranged next to each other in the row direction, and the amplifier **12** is arranged along the adjoining pixels. In this manner, intervals between the centers of mass of the photoelectric conversion elements **11** (P_{11}, P_{12}, P_{13}, P_{14}, P_{21}, P_{22}, P_{23}, P_{24}, P_{31}, P_{32}, P_{33}, P_{34}) in both the row and column directions also become equal. Reference numeral **15** indicates a unit cell repeated in the column direction, and reference numeral **16** indicates the unit cell repeated in the row direction.

In the first embodiment, the number, N, of photoelectric conversion elements **11** sharing each amplifier **12** is two (N=2), however, the number N may be an arbitrary number greater than 2.

[Layout **1**]

FIG. **3** shows a practical pattern layout of two photodiodes and an amplifier in the CMOS sensor **22**, and FIG. **4** is a brief view of FIG. **3** from which a part of lines are omitted.

The CMOS sensor, as shown in FIG. **3**, is formed on a singlecrystalline silicon substrate based on a layout rule 0.4 μm. Each pixel is a square, 8 μm each side, and a source follower amplifier, as the amplifier **12**, is shared by two adjoining pixels arranged in the column direction. Therefore, the size of a unit cell **31**, shown by a dash line and is referred to by reference numerals **13** and **14** in FIG. **2**A, is 8 μm×16 μm. A plurality of unit cells **31** are arranged in two dimensions.

The photodiodes **32***a* and **32***b*, i.e., the photoelectric conversion elements, are formed on the right portion of respective pixels, and the shapes of the photodiodes **32***a* and **32***b* are almost mirror images. Further, the photodiodes **32***a* and **32***b* are designed so that the center of masses (CM) of light-receiving areas of the photodiodes **32***a* and **32***b* are located at a substantially identical position of each pixel. In FIG. **3**, the areas of the photodiodes **32***a* and **32***b*, and the area of a floating diffusion (FD) portion **35** are shown by bold lines. Further, in FIG. **3**, reference numeral **38** denotes an odd-row scanning line for controlling each transfer gate **33** in an odd-number row; **39**, an even-row scanning line for controlling each transfer gate **34** in an even-number row; **40**, a row selection line; and **42**, a reset line for controlling the gate **43** of a MOS transistor. In FIG. **4**, the lines **38** to **42** are not shown.

Photo-charges accumulated in the photodiodes **32***a* and **32***b* are transferred to the FD portion **35** via the transfer gate **33** for the odd-number row and the transfer gate **34** for the even-number row. The size of the both transfer gates **33** and **34** is L=0.4 μm, W=1.0 μm (L is a channel length and W is a channel width). The FD portion **35** is connected to the gate **36** of a source follower via an aluminum (Al) wire having a width of 0.4 μm, and the photo-charge transferred to the FD portion **35** modulates the gate voltage of the gate **36**. The size of the MOS transistor of the gate **36** is L=0.8 μm, W=1.0 μm, and the total capacitance of the FD portion **35** and the gate **36** is about 5 fF. Since Q=CV; the gate voltage of the gate **36** changes by 3.2 volts in response to the transference of 10^5 electrons.

Current flowing in from a V_{DD} terminal **41** is modulated by the MOS transistor of the gate **36**, and transferred to a vertical signal line **37**. Current flowing through the vertical signal line **37** is processed by a signal processing circuit (not shown) and formed into image information.

Thereafter, in order to set the potentials of the photodiodes **32***a* and **32***b*, the FD portion **35**, and the gate **36** to the predetermined potential V_{DD}, the gate **43** of the MOS transistor connected to the reset line **42** is opened (at this time, the transfer gate **33** for the add-number row and the transfer gate **34** for the even-number row are also opened), thereby the photodiodes **32***a* and **32***b*, the FD portion **35**, and the gate **36** are electrically connected to the V_{DD} terminal **41**.

Thereafter, the transfer gates **35** and **36** are closed, thereby the accumulation of photo-charges in the photodiodes **32***a* and **32***b* start again.

The total number of the lines arranged in each unit cell in the horizontal direction is four, specifically, the odd-row scanning line **38**, the even-row scanning line **39**, the row selection line **40**, and the reset line **42**. The four lines are arranged in such a manner that two lines each are arranged on the upper and lower ends of each pixel, as shown in FIG. **3**.

Since these lines are thick wires and provided over pixels, as described above, an increase in the number of lines results in an increase in area which can not receive light, which reduces aperture. Further, if the number of lines provided over a row is different from the number of lines arranged over another row, such that two lines in one row and three lines in the other row, the apertures and the centers of mass of photodiodes adjoining in the column direction become different in one row from the other.

In layout **1**, the power supply voltage V_{DD} is provided to every pixel by connecting a power supply (not shown) with each pixel via a metal light-shield layer (not shown), arranged on the top layer of the CMOS sensor, and the V_{DD} terminal **41**, formed as a through hole, in order to avoid the problem described in the previous paragraph.

With the layout **1** as described above, it is possible to provide a CMOS sensor having a plurality of pixels, arranged in the same interval from each other, which have relatively high area ratio or high aperture.

It should be noted that the area ratio or aperture may be further increased by using known on-chip convex lenses, for instance.

Further, the metal layer used for supplying the power supply voltage V_{DD} is not limited to a light-shield film, and may be an electrode material used for forming capacitor, for instance, placed over the entire pixel.

[Layout **2**]

FIG. **5** shows another practical pattern layout of two photodiodes and an amplifier in the CMOS sensor **22**, and FIG. **6** is a brief view of FIG. **5** from which several lines are omitted. Further, FIGS. **7** and **8** are enlarged views showing vicinity of an FD portion. Specifically, FIG. **7** is a view when a wire over a gate **54** is omitted, and FIG. **8** is a view when a wire is provided-over the gate **54**.

Referring to FIGS. **6** to **8**, the areas of photodiodes **52***a* and **52***b*, and an FD portion **55** are shown by bold lines. The layout **2** also shows a case where two adjoining pixels share a single amplifier, similarly to the layout **1**, but the two adjoining pixels are arranged in the row direction. The centers of mass of the two adjoining photodiodes are located at a substantially same position of the each photodiode.

Referring to FIGS. **5** and **6**, reference numerals **52***a* and **52***b* are the photodiodes; **53**, a transfer gate for an odd-number column; **54**, a transfer gate for an even-number column; **55**, the FD portion; **56**, the gate of a source follower; **57**, a vertical signal line; **58**, an odd-column scanning line for controlling the transfer gate **53** in an odd-number column; **59**, an even-column scanning line for controlling the transfer gate **54** in an even-number column; **60**, a row selection line; and **62**, a reset line for controlling the gate **63** of a MOS transistor. Note, a wire connecting the gate **56** of the source follower and the FD portion **55** crosses over the gate **54** as shown in FIG. **8**.

In layout **2**, the area ratio or the aperture is improved comparing to the layout **1** in which sharing an amplifier with two pixels adjoining in the column direction. Accordingly, a CMOS sensor of wide dynamic range, high sensitivity, and high S/N ratio is realized.

In layout **2**, necessary four lines are arranged, and a power supply line **61** for providing a voltage V_{DD} is arranged in the column direction on the side of photodiodes opposite to the side of the vertical signal line **57**.

[Noise Reduction]

The inventors of the present application also have developed a signal read circuit, for reducing noise, suitably used in an image sensing apparatus having a configuration, as described above, in which a plurality of pixels share an amplifier.

The noise reduction operation is explained with reference to FIGS. **9** and **10**.

FIG. **9** shows a circuit configuration of a unit cell of a CMOS sensor in which two photoelectric conversion elements share one amplifier. Referring to FIG. **9**, PD**1** and PD**2** denote photodiodes as photoelectric conversion elements; M_{TX1} and M_{TX2}, MOS transistors for transferring photo-charges accumulated in the photodiodes PD**1** and PD**2** to an FD portion; M_{RES}, a MOS transistor for resetting the FD portion; and M_{SF} and M_{SEL}, MOS transistors configuring a source follower. The MOS transistor M_{SEL} also functions as a selection switch for selecting a photodiode.

First, reset operation is performed by turning on the MOS transistor M_{RES}, then, noise signal is read out from the MOS transistors M_{SF} and M_{SEL} configuring the source follower. Next, photo-charge accumulated in the photodiode PD**1** is transferred to the gate of the MOS transistor M_{SF} via the MOS transistor M_{TX1}, then read out as a first signal via the MOS transistors M_{SF} and M_{SEL}. Thereafter, reset operation is performed again, and photo-charge accumulated in the photodiode PD**2** is transferred to the gate of the MOS transistor M_{SF} via the MOS transistor M_{TX2}, then read out as a second signal via the MOS transistors M_{SF} and M_{SEL}. Accordingly, the noise signal, the first signal, and the second signal are obtained, and, by subtracting the noise signal from the first and second signals, a signal corresponding to the photodiode PD**1** without the noise component as well as a signal corresponding the photodiode PD**2** without the noise component are obtained.

Further, it is possible to add the photo-charge signal corresponding to the photodiode PD**1** and the photo-charge signal corresponding to the photodiode PD**2** by transferring photo-charge accumulated in the photodiode PD**2** to the gate of the MOS transistor M_{SF} while photo-charge accumulated in the photodiode PD**1** is kept at the gate of the MOS transistor M_{SF} by changing operation timing.

Next, the image sensing apparatus including a signal processing circuit according to the first embodiment will be explained below. FIG. **10** shows an equivalent circuit of the image sensing apparatus including the signal processing circuit according to the first embodiment, and FIGS. **11** and **12** are timing charts for operating the apparatus.

Referring to FIGS. **10** and **11**, vertical scanning operation is initiated in response to the pulse, which indicates a vertical blanking period, of a signal ϕV_1 or ϕV_2. First, a signal ϕTX_{RO-1} which is applied to the reset line **62** of the first row is activated during a horizontal blanking period (i.e., when a signal ϕHBL is high), and signals ϕTX_{RO-i} (i is a row number. Below, the last part of the subscript, –i, is omitted.) for subsequent lines are activated in the same manner. Accordingly, all the pixels in every row are reset to the reset potential V_{DD}.

In each horizontal blanking period, during a period T_1, a signal ϕL becomes high and a transistor **81**, connected to the vertical signal line **57**, is turned on and the vertical signal line **57** is reset. Simultaneously, signals ϕT_N, ϕT_{S1} and ϕT_{S2} also become high, and transistors **82-1**, **82-2**, and **82-3** are turned on. Accordingly the upstream part of transistors for reading signals, **84-1**, **84-2**, and **84-3**, and capacitors **83-1**, **83-2**, and **83-3** (C_{TN}, C_{TS1}, C_{TS2}) are electrically connected to the vertical signal line **57**, and reset. Accordingly, residual charges in the capacitors **83-1**, **83-2**, and **83-3**, for instance, are removed.

Thereafter, in a period T_2, the signal ϕTX_{R0} to be applied to the reset line **62** is changed to high, and the floating gate, which is the gate of the source follower amplifier configured with the MOS transistors M_{SF} and M_{SEL} in each unit cell, is reset to the voltage V_{DD}.

Then, in a period T_3, a signal ϕRV becomes high and a transistor **80** for grounding, connected to the vertical signal line **57**, is turned on, and the vertical signal line **57** is grounded. Simultaneously, the signal ϕT_N is changed to high in order to connect the capacitor **83-1** (C_{TN}) for storing a noise component to the vertical signal line **57**, and the transistor **82-1** is turned on. At this time, a signal ϕS_O to be applied to the row selection line **60** is high, and current corresponding to the potential (about V_{DD}) at the floating gate of the MOS transistor M_{SF} flows from the V_{DD} terminal **41** to the capacitor **83-1** (C_{TN}), thereby the capacitor **83-1** (C_{TN}) stores charge corresponding to the noise component.

Next, in a period T_4, a signal ϕTX_{OO} applied to the odd-column scanning line **58** is changed to high, in turn, the transfer gate (MOS transistor M_{TX1}, in this case) in an odd-number column is turned on, and photo-charge accumulated in the photodiode PD**1** is transferred to the floating gate of the MOS transistor M_{SF}. The capacitor **83-1** (C_{TN}) for storing the noise component is disconnected from the vertical signal line **57** when the signal ϕT_N becomes low, and the capacitor **83-2** (C_{TS1} for storing a photo-charge signal is connected, in turn, when the signal ϕT_{S1} is changed to high. Thus, charge accumulated in the photodiode PD**1**, for instance, in an odd-number column is stored in the capacitor **83-2** (C_{TS1}) via the vertical signal line **57**.

Next, in a period T_5, the signal ϕL becomes high, and only the vertical signal line **57** is reset. Since the signals ϕS_O, ϕT_N, ϕT_{S1} and ϕT_{S2}, are low, other portions are not reset, and their states are preserved.

Next, the signal ϕTX_{RO} applied to the reset line **62** is changed to high between periods T_5 and T_6, and the gate of the source follower amplifier (i.e., the gate of MOS transistor M_{SF}) is reset to the potential V_{DD}.

In the period T_6, a signal ϕTX_{Oe} applied to the even-column scanning line **59** is changed to high, and photo-charge accumulated in the photodiode PD**2** in an even-number column is transferred to the floating gate of the MOS transistor M_{SF}. At this time, the signal ϕT_{S2} is changed to high, thus the capacitor **83-3** (C_{TS2}) for storing another photo-charge signal is electrically connected to the vertical signal line **57**, and photo-charge accumulated in the photodiode PD**2**, for instance, in an even-number column is stored in the capacitor **83-3** (C_{TS2}) via the vertical signal line **57**.

In the aforesaid manner, charges corresponding to the noise component, a first signal, and a second signal are respectively stored in the capacitors **83-1**, **83-2**, and **83-3** (C_{TN}, C_{TS1}, C_{TS2}) by each column for a row.

Next, in a period T_7, in order to sequentially transfer the charges stored in the capacitors **83-1**, **83-2**, and **83-3** (C_{TN}, C_{TS1}, C_{TS2}) to amplifiers **86-1** to **86-3**, respectively, a horizontal scanning signal ϕHn is changed to high for each columns controlled by a horizontal shift register **71**, and transistors **84-1** to **84-3**, provided for each column, are turned on; thereby the capacitors **83-1** to **83-3** (C_{TN}, C_{TS1}, C_{TS2}) are connected to the respective amplifiers **86-1** to **86-3**. From the capacitors **83-1** to **83-3** (C_{TN}, C_{TS1}, C_{TS2}), the noise component, the first signal, and the second signal are outputted, and from a differential amplifier **87-1**, a signal S**1** obtained by subtracting the noise component from the first signal is outputted, and a signal S**2** obtained by subtracting the noise component from the second signal is outputted from a differential amplifier **87-2**. Note that accumulation of photo-charges in the photodiodes is also performed during the period T_7.

In a case where the signal ϕTX_{RO} to be applied to the reset line **62** between the period T_5 and the period T_6 is not changed to high and reset operation is not performed, photo-charge generated by the photodiode PD**2** in an even-number column is transferred to the floating gate of the MOS transistor M_{SF} where photo-charge generated by the photodiode PD**1** remains; accordingly, a signal of the photodiode PD**1** in the odd-number column and a signal of the photodiode PD**2** in the even-number row are stored in the capacitor **83-3** (C_{TS2}) via the vertical signal line **57**. Therefore, a noise component, a signal corresponding to one photodiode (single signal component), and a signal corresponding to two photodiodes (double signal component) are stored in the capacitors **83-1** to **83-3** (C_{TN}, C_{TS1}, C_{TS2}). Then, the noise component, the single signal component, and the double signal component are outputted to the amplifiers **86-1** to **86-3** during the period T_7. Thereafter, the noise component is subtracted from the single signal component by the differential amplifier **87-1** and a signal S**1** is outputted. Similarly, the noise component is subtracted from the double signal component by the differential amplifier **87-2** and a signal S**2** is outputted.

Further, the first embodiment of the present invention is not limited to two-dimensional array, and capable of applying to an one-dimensional line sensor.

According to the first embodiment as described above, it is possible to realize a high precision image sensor without causing deterioration of performance, such as deterioration of resolution and generation of moiré, for instance. In addition, yield of image sensing apparatus becomes high.

Second Embodiment

Next, the second embodiment of the present invention will be explained.

FIGS. **13** and **14** show other layouts of amplifiers **12**, as common circuits, and photodiodes **11** when each amplifier **12** is shared by two photodiodes **11**.

As shown in FIG. **13**, the photodiodes **11** are arranged so that adjoining rows are shifted from each other by one half pitch. In odd-number rows, pixels covered by green (G) filter (referred to as "G pixel" hereinafter), which contribute mainly to a luminance (Y) signal, are respectively set across the amplifiers from pixels covered by red (R) filter (referred to as "R pixel" hereinafter), which contribute to a color-difference signal, and in even-number rows, G pixels are respectively set across the amplifiers from pixels covered by blue (B) filter (referred to as "B pixel" hereinafter), which also contributes to a color-difference signal. By arranging the G pixels in adjoining rows, shifted by one and half pitches in the row direction, intervals between G pixels in the row direction becomes the same, further, intervals between the G pixels in the column direction also become the same. Accordingly problem of moiré is solved, and a sensed image does not look deteriorated.

Further, FIG. **14** shows an example when photodiodes **11** are arranged so that adjoining columns are shifted from each other by one half pitch.

Next, FIG. **15** shows a practical pattern layout of two photodiodes and an amplifier, as the common circuit, shared by the two photodiodes **11** arranged on right and left sides of the amplifier **12**, as shown in FIG. **13**.

The CMOS sensor, as shown in FIG. **15**, is formed on a singlecrystalline silicon substrate. Each pixel is a square, 8

μm each side, shown by a dash line **341**. As described above, plural pairs of photodiodes are arranged in a two-dimensional array. Between each pair of two photodiodes, the common circuit is arranged. A photodiode covered by G filter (G photodiode) is set on the left side of the common circuit, and a photodiode covered by R or B filter (R/B photodiode) is set on the right side of the common circuit. In FIG. **15**, an amplifier, using MOS transistors, is used as the common circuit, as an example. The layout rule is 0.4 μm, and an area, area ratio, an aperture area, and aperture ratio of a photodiode **342** as a photoelectric conversion element is 57.96 μM^2, 60.4%, 28.88 μm^2 and 30.1%, respectively. These figures are very high comparing to conventional figures.

Reference numeral **343** denotes a transfer gate for transferring photo-charge from a G photodiode **342** to a floating diffusion (FD) portion **345** and reference numeral **344** denotes a transfer gate for transferring photo-charge from an R/B photodiodes **342'** also to the FD portion **345**. The transfer gates **343** and **344** are MOS transistors, and the channel length and the channel width of each MOS transistor is 0.4 μm and 1.0 μm, respectively. Reference numeral **347** denotes a reset gate for resetting the FD portion **345** to a potential of a power supply voltage V_{DD} through a terminal **350**, and reference numeral **346** denotes a gate of a MOS-type source follower amplifier. The potential of the gate **346** changes depending upon the transferred charge, and the amplifier modulates current flowing in from the V_{DD} terminal **350**.

The total capacitance of the FD portion **345** and the gate **346** is about 10 fF, and as the area of the photodiodes increases, the capacitance also increases. The modulated current is eventually outputted to a vertical signal line **349** via a selection gate **348** for selectively outputting the current.

Further, reference numerals **351** to **354** denote scanning lines for applying a predetermined potential to the selection gate **348**, the transfer gates **343** and **344**, and the reset gate **347**, respectively.

[Noise Reduction]

Next, signal processing for reducing noise preferably used in the above-described image sensor is explained.

FIG. **16** is an equivalent circuit diagram according to the second embodiment. In FIG. **16**, the same units and elements as those shown in FIGS. **10** and **15** are referred to by the same reference numerals. Further, FIG. **17** is an equivalent circuit diagram of a unit cell **374**, surrounded by a dash line in FIG. **16** and whose pattern layout is shown in FIG. **15**, configured with a common circuit **372** and photodiodes arranged on the both sides of the common circuit **372**.

In FIG. **17**, reference numeral **350** is the V_{DD} terminal; **345**, the FD portion; **363**, a reset unit, such as a MOS transistor (reset MOS), for resetting the FD portion **345**; **364** and **364'**, transfer units, such as MOS transistors (transfer MOS), for transferring photo-charges from the photodiodes **342** and **342'** to the FD portion **345**; **365**, an amplifier, such as a MOS transistor, for amplifying the change in the potential at the FD portion **345**; and **366**, a MOS transistor for selection (selection MOS) for selectively outputting a signal from the amplifier **365** to the vertical signal line **349**. Further, the scanning lines **354**, **351**, **352** and **353** are for applying potentials for turning on or off the reset MOS **363**, the selection MOS **366**, the transfer MOS **364**, and the transfer MOS **364'**, respectively. In the unit cell **374**, the MOS transistors **363**, **364**, **364'**, **365**, and **366** configure the common circuit. Further, in the pattern layout shown in FIG. **15**, the transfer gate **343** corresponds to the gate of the transfer MOS **364** of FIG. **17**, the transfer gate **344** corresponds to the gate of the transfer MOS **364'**, the reset gate **347** corresponds to the gate of the reset MOS **363**, and the selection gate **348** corresponds to the gate of the selection MOS **366**.

Next, referring to the circuit diagrams shown in FIGS. **16** and **17**, and timing charts shown in FIGS. **11** and **12**, the noise reduction operation is explained.

Referring to FIG. **11**, vertical scanning operation is initiated in response to the pulse, which indicates a vertical blanking period, of a signal ϕV_1 or ϕV_2. First, a signal $\phi TX_{RO\text{-}1}$ which is applied to the reset line **354** of the first row is activated during a horizontal blanking period (i.e., when a signal φHBL is high), and signals $\phi TX_{RO\text{-}i}$ (i is a row number. Below, the last part of the subscript, –i, is omitted.) for subsequent lines are applied in the same manner. Accordingly, all the pixels in every row are reset to the reset potential V_{DD}.

In each horizontal blanking period, during a period T_1, a signal φL becomes high, as shown in FIG. **12**, and a transistor **81**, connected to the vertical signal line **349**, is turned on and the vertical signal line **349** is reset. Simultaneously, signals ϕT_N, ϕT_{S1} and ϕT_{S2} also become high, and transistors **82-1**, **82-2**, and **82-3** are turned on. Accordingly wires in the upstream of transistors for reading signals, **84-1**, **84-2**, and **84-3**, and capacitors **83-1**, **83-2**, and **83-3** (C_{TN}, C_{TS1}, C_{TS2}) are electrically connected to the vertical signal line **349**, and reset. Accordingly, residual charge in the capacitors **83-1**, **83-2**, and **83-3**, for instance, are removed.

Thereafter, in a period T_2, the signal ϕTX_{R0} to be applied to the reset line **354** is changed to high, and the floating gate, which is the gate of the source follower amplifier configured with the MOS transistors **365** and **366** in each unit cell is reset to the voltage V_{DD}.

Then, in a period T_3, a signal φRV becomes high and a transistor **80** for grounding, connected to the vertical signal line **349**, is turned on, and the vertical signal line **349** is grounded. Simultaneously, the signal ϕT_N is changed to high in order to connect the capacitor **83-1** (C_{TN}) for storing a noise component to the vertical signal line **349**, and the transistor **82-1** is turned on. At this time, a signal ϕS_O to be applied to the row selection line **351** is high, and current corresponding to the potential (about V_{DD}) at the floating gate of the MOS transistor **365** flows from the V_{DD} terminal **350** to the capacitor **83-1** (C_{TN}), thereby the capacitor **83-1** (C_{TN}) stores charge corresponding to the noise component.

Next, in a period T_4, a signal ϕTX_{OO} applied to the G pixel scanning line **353** is changed to high, in turn, transfer gate (MOS transistor **364**) for the G pixel is turned on, and photo-charge accumulated in the photodiode **342** is transferred to the floating gate of the MOS transistor **365**. The capacitor **83-1** (C_{TN}) for storing the noise component is disconnected from the vertical signal line **349** when the signal ϕT_N becomes low, and the capacitor **83-2** (C_{TS1}) for storing a photo-charge signal is connected, in turn, when the signal ϕT_{S1} is changed to high. Thus, charge accumulated in the G photodiode **342**, for instance, is stored in the capacitor **83-2** (C_{TS1}) via the vertical signal line **349**.

Next, in a period T_5 the signal φL becomes high, and only the vertical signal line **349** is reset. Since the signals ϕS_O, ϕT_N, ϕT_{S1}, and ϕT_{S2} are low, other portions are not reset, and their states are preserved.

Next, the signal ϕTX_{RO} applied to the reset line **354** is changed to high between periods T_5 and T_6, and the FD portion **345** is reset to the potential V_{DD}.

In the period T_6, a signal ϕTX_{Oe} applied to the R/B pixel scanning line **352** is changed to high, and photo-charge

accumulated in the R/B photodiode **342'** is transferred to the floating gate of the MOS transistor **365**. At this time, the signal ϕT_{S2} is changed to high, thus the capacitor **83-3** (C_{TS2}) for storing another photo-charge signal is electrically connected to the vertical signal line **349**, and charge accumulated in the R/B photodiodes **342'**, for instance, is stored in the capacitor **83-3** (C_{TS2}) via the vertical signal line **349**.

In the aforesaid manner, charges corresponding to the noise component, a first signal, and a second signal are respectively stored in the capacitors **83-1**, **83-2**, and **83-3** (C_{TN}, C_{TS1}, C_{TS2}) by each column for a row.

Next, in a period T_7, in order to sequentially transfer the charges stored in the capacitors **83-1**, **83-2**, and **83-3** (C_{TN}, C_{TS1}, C_{TS2}) to amplifiers **86-1** to **86-3**, respectively, a horizontal scanning signal ϕHn is changed to high for each columns controlled by a horizontal shift register **71**, and transistors **84-1** to **84-3**, provided for each column, are turned on; thereby the capacitors **83-1** to **83-3** (C_{TN}, C_{TS1}, C_{TS2}) are connected to the amplifiers **86-1** to **86-3**. From the capacitors **83-1** to **83-3** (C_{TN}, C_{TS1}, C_{TS2}), the noise component, the first signal, and the second signal are outputted, and from a differential amplifier **87-1**, a G component signal obtained by subtracting the noise component from the first signal is outputted, and an R/B component signal obtained by subtracting the noise component from the second signal is outputted from a differential amplifier **87-2**. Note that accumulation of photo-charges in the photodiodes is also performed during the period T_7.

In a case where the signal ϕTX_{RO} to be applied to the reset line **354** between the period T_5 and the period T_6 is not changed high and reset operation is not performed, photo-charge generated by the R/B photodiodes **342'** is transferred to the floating gate of the MOS transistor **365** where photo-charge generated by the G photodiode **342** remains; accordingly, a signal of the G photodiode **342** and a signal of the R/B photodiode **342'** are stored in the capacitor **83-3** (C_{TS2}) via the vertical signal line **349**. Therefore, a noise component, a signal corresponding to one photodiode (single signal component), and a signal corresponding to two photodiodes (double signal component) are stored in the capacitors **83-1** to **83-3** (C_{TN}, C_{TS1}, C_{TS2}). Then, the noise component, the single signal component, and the double signal component are outputted to the amplifiers **86-1** to **86-3** during the period T_7. Thereafter, the noise component is subtracted from the single signal component by the differential amplifier **87-1** and a G component signal is outputted. Similarly, the noise component is subtracted from the double signal component by the differential amplifier **87-2** and a G+R/B component signal is outputted.

The signal processing circuit **23**, shown in FIG. **1**, according to the second embodiment is explained with reference to FIG. **18**.

The G and R/B component signals output from the CMOS sensor **22** are converted into luminance (Y) signals and color difference (C_R, C_B) signals. Note that low frequency component of the luminance signals are generated using R, G, and B signals of at least two adjoining rows.

Further, high frequency component of the luminance signals are generated using high frequency component of G signals in at least two adjoining rows. Accordingly, an image of high resolution and good color reproduction is obtained.

According to the second embodiment as described above, it is possible to obtain an image sensing apparatus of good sensitivity, high resolution, and wide dynamic range.

Third Embodiment

Next, the third embodiment of the present invention will be explained with reference to accompanying drawings.

FIG. **19** shows a layout of amplifiers **12** in pixels when each amplifier **12** is shared by four (2 rows×2 columns) pixels, according to the third embodiment.

In FIG. **19**, each amplifier **12** is arranged in the center of four pixels, and four photoelectric conversion elements **11** (e.g., q_{11}, q_{12}, q_{21}, q_{22}) are arranged as they surround the amplifier **12**.

Further, a light-shield unit **17** is provided for each pixel in an area which is symmetry to a portion of the amplifier **12** occupying the pixel with respect to the center of the pixel. Therefore, the center of mass of each photoelectric conversion element **11** is in the center of each pixel. Accordingly, the centers of mass of the photoelectric conversion elements **11** (q_{11}, q_{12}, q_{21}, q_{22}, q_{31}, q_{32}, q_{41}, q_{42}) are arranged at a same interval, D, both in the row and column directions.

FIG. **20** shows another layout of amplifiers **12** in pixels when each amplifier **12** is arranged at the boundary of four pixels arranged in a 2×2 array in the row direction, and the four photoelectric conversion elements **11** (e.g., q_{11}, q_{12}, q_{21}, q_{22}) are arranged so as to sandwich each amplifier **12**.

In addition, light-shield unit **17** is arranged in three peripheral areas, other than the peripheral area where the amplifier **12** occupies, of the pixel, as shown in FIG. **20**. Therefore, the centers of mass of the photoelectric conversion elements **11** (q_{11}, q_{12}, q_{21}, q_{22}, q_{31}, q_{32}, q_{41}, q_{42}) are located at the same interval, D, both in the row and column directions.

The arrangement as shown in FIG. **20** is rotated by 90 degrees, namely, an arrangement in which row direction and column direction are exchanged, is also possible.

Further, in an arrangement as shown in FIG. **21**, G filter, which contributes most to resolution, is arranged in the upper left pixel and the lower right pixel among four pixels configuring a unit cell **30**. In the pixel covered by green filter (G pixel), a light-shield unit **17** is provided in an area which is symmetry to a portion of the amplifier **12**, arranged at a central portion of the unit cell **30**, occupying the pixel with respect to the center of the pixel. Therefore, the center of mass of the photoelectric conversion element **11** of the G pixel is at the center of the G pixel. With this configuration, intervals, D, of the photoelectric conversion elements q_{11} and q_{12} of G pixels become the same both in the row and column directions.

Further, a pixel covered by red filter (R pixel) is arranged in the upper right pixel in the unit cell **30**, and a pixel covered by blue filter (B pixel) is arranged in the lower left pixel in the unit cell **30**. These pixels do not have light-shield units, differing from the G pixels; however, since a single R pixel and a single B pixel are arranged in each unit cell **30**, the intervals between adjacent R and B pixels become identical, namely **2**D.

FIG. **22** is another layout of amplifiers **12** in pixels. In this layout, areas occupied by the amplifier **12** and the light-shield units **17** are reduced in the G pixels.

[Layout **1**]

FIG. **23** shows a practical pattern layout of four photodiodes and an amplifier in the CMOS sensor **22** in FIG. **1**.

The CMOS sensor, as shown in FIG. **23**, is formed on a singlecrystalline silicon substrate based on a layout rule 0.4 μm. Each pixel is a square, 8 μm each side, and a source follower amplifier, as the amplifier **12**, is shared by four pixels arranged in a 2×2 array. Therefore, the size of a unit

cell **481**, shown by a dash line, is 16 μm×16 μm. A plurality of unit cells **481** are arranged in two dimensions.

Photodiodes **482***a*, **482***b*, **482***c*, and **482***d* are formed diagonally in each pixel, and the shapes of the photodiodes **482***a* to **482***d* are nearly symmetry with respect to the center of the unit cell **481** as well as symmetry with respect to vertical and horizontal lines passing over the center of the unit cell **481**. Further, the center of mass (CM) of each photodiode is designed to be at the same position in each pixel. Further, reference numeral **495** denotes a light-shield unit.

Reference numeral **488***a* is a scanning line for controlling a transfer gate **483***a*; **490**, a row selection line; and **492**, a reset line for controlling a gate **493** of a MOS transistor.

Photo-charges accumulated in the photodiodes **482***a* to **482***d* are transferred to a floating diffusion (FD) portion **485** via transfer gates **483***a* to **483***d*, respectively. The size of the transfer gates **483***a* to **483***d* is L=0.4 μm, W=1.0 μm (L is a channel length and W is a channel width).

The FD portion **485** is connected to the gate **486** of a source follower via an aluminum (Al) wire having a width of 0.4 μm, and the photo-charge transferred to the FD portion **485** modulates the gate voltage of the gate **486**. The size of the MOS transistor of the gate **486** is L= 0.8 μm, W=1.0 μm, and the total capacitance of the FD portion **485** and the gate **486** is about 5 fF. Since Q=CV, the gate voltage of the gate **486** changes by 3.2 volts in response to the transference of 10^5 electrons.

Current flowing in from a V_{DD} terminal **491** is modulated by the MOS transistor of the gate **486**, and transferred to a vertical signal line **487**. Current flowing through the vertical signal line **487** is processed by a signal processing circuit (not shown) and formed into image information.

Thereafter, in order to set the potentials of the photodiodes **482***a* to **482***d*, the FD portion **485**, and the gate **486** to the predetermined potential V_{DD}, the gate **486** of the MOS transistor connected to the reset line **482** is opened (at this time, the transfer gates **483***a* to **483***d* are also opened), thereby the photodiodes **482***a* to **482***d*, the FD portion **485**, and the gate **486** are electrically connected to the V_{DD} terminal **491**.

Thereafter, the transfer gates **483***a* to **483***d* are closed, thereby the accumulation of photo-charges in the photodiodes **482***a* to **482***d* start again.

In layout **1**, the lines **488***a* to **488***d*, **490** and **492**, passing over the unit cell **481** in the horizontal direction, are all formed with indium tin oxide, transparent conductor, of 1500 Å thickness. Therefore, areas of the photodiodes **482***a* to **482***d* under the aforesaid lines can also receive light, and the center of mass of each photodiode matches the center of mass of light-receiving area of the photodiode.

According to the Layout **1** in the third embodiment, it is possible to provide a CMOS sensor with relatively high area ratio and high aperture ratio, in which photodiodes are arranged at an equal pitch.

[Layout **2**]

FIG. **24** shows another practical pattern layout of four photodiodes and an amplifier in the CMOS sensor **22**.

Referring to FIG. **24**, reference numerals **502***a* to **502***b* denote the photodiodes; **503***a* to **503***d*, transfer gates; **505**, an FD portion; **506**, the gate of a source follower; **507**, a vertical signal line; **508***a* to **508***d*, scanning lines; **510**, a row selection line; and **512**, a reset line for controlling the gate **513** of a MOS transistor.

In layout **2** of the third embodiment, since three lines out of lines **508***a* to **508***d*, **510**, and **512** pass through the central portion of each pixel. Therefore, if these lines are metal wires which shield light incoming toward the photodiodes **502***a* to **502***d*, the center of mass of the light-receiving area of each photodiode does not shift, and remains at the center of each pixel.

In layout **2** of the third embodiment, opaque metal wires with small resistance are generally used, time constant of the lines in the horizontal direction is improved, and a high-speed image sensing apparatus is obtained.

In the aforesaid layout **1** and layout **2** of the third embodiment, the portion under the shield unit is not effectively used. It is possible to extend the area of a photodiode, as a photoelectric conversion element, under the light-shield unit, and make the extended area function as a charge accumulation unit.

[Layout **3**]

In layout **2** of the third embodiment, since the lines pass through the center of each pixel where light-receiving efficiency is high, sensitivity of the image sensing apparatus may not be good. Accordingly, an improved layout is shown in FIG. **26** as the layout **3** of the third embodiment. FIG. **26** is a practical pattern layout of the layout shown in FIG. **20**.

In layout **3** of the third embodiment, transfer gates **523***a* to **523***d*, the gate **526** of a source follower, and the gate **533** of a MOS transistor for resetting are formed under scanning lines **528***a* to **528***d*, a row selection line **530**, and a reset line **532**; therefore, it is possible to maximize the size and aperture of each of photodiodes **522***a* to **522***d*. In addition, the aperture of each photodiode is at the center of each pixel. Further, light-shield units are formed in an area where horizontal and vertical wires are formed.

Further, in layout **3** of the third embodiment, the source follower, as the amplifier **12** shown in FIG. **20**, and the MOS transistor for resetting are separately arranged in periphery of each photodiode in the row direction, thus, compactly arranged under wires running in the row direction.

Further, since there is a large area which is not yet used under wires in the upper right pixel, it is possible to add a new configuration, such as a smart sensor.

According to the layout **3** of the third embodiment, the area and aperture of a photodiode are increased comparing to the layout **2**, it is possible to provide a high-sensitive image sensing apparatus with wide dynamic range. In addition, if the size of each pixel is further reduced and the size of the aperture of the photodiode becomes small, e.g., wavelength of light, each side, the problem such that light will not enter the photodiode will not arise. Thus, the layout **3** would remain as an efficient layout for the future.

In layout **3** of the third embodiment, the amplifier **12** is arranged at the central portion of each unit cell, and the center of mass of a light-receiving area is designed to match the center of mass of a pixel. However, the present invention is not limited to this, and the shape of apertures of pixels may be arbitrarily designed as long as the shape is identical and arranged in a fixed position in every pixel, as shown in FIG. **27**, for instance.

In other words, by designing the apertures to have the same shape and arranged in a predetermined position in each pixel, intervals between the centers of mass of light receiving areas become the same.

[Layout **4**]

FIG. **28** shows a practical pattern layout, corresponding to FIG. **21**, of four photodiodes and an amplifier in the CMOS sensor **22** in FIG. **1**.

In layout **4** of the third embodiment, colors of a color filter and positions of the colors are predetermined. Specifically, in the four pixels arranged in a 2×2 array, the upper left and lower right pixels are covered with green filter (G pixels)

which contributes most to luminance signals, the upper right pixel is covered with red filter (R pixel), and the lower left pixel is covered with blue filter (B pixel).

In layout **4**, the amplifier **12** and other peripheral circuits are arranged so that photodiodes **542***a* and **542***d* of the G pixels have the maximum area and aperture ratio.

Further, the center of mass of light-receiving area of a G pixel matches the center of mass of the G pixel, thus, the intervals between the centers of mass of G pixels are equal.

According to the layout **4** of the third embodiment, it is possible to provide a high sensitive image sensing apparatus.

[On-chip Lens and Other Variations]

FIG. **29** shows an example when on-chip lens is used in the CMOS sensor **22** in FIG. **1**.

Referring to FIG. **29**, an on-chip lens **602** is formed on each pixel in a unit cell **601**. Light incoming from outside of the CMOS sensor **22** is collected by the on-chip lens **602** and incidents on the aperture **603**. Reference numeral **604** denotes an imaging area where light is gathered by the on-chip lens **602**.

By controlling the design and the position of the on-chip lens, the position of the imaging area can be set relatively freely.

Thus, when a plurality of pixels share a single amplifier, if photodiodes, as photoelectric conversion elements, could not be arranged at a same interval, image signals as if they are obtained by photodiodes which are arranged at a same interval can be obtained by controlling the designs and positions of on-chip lenses.

Further, if an image sensing lens used in the image sensing apparatus is not telecentric, an incoming angle of light which incidents on a sensor chip in the central portion is different from an outer portion. Thus, by setting apertures of photodiodes in the outer portion of the CMOS sensor at different intervals, image signals as if they are obtained by photodiodes which are arranged at a same interval can be obtained.

According to the layout **1** to layout **4** of the third embodiment, light-shield units which are optical members are adjusted to make intervals between light-receiving areas identical. With the on-chip lens, the intervals of light receiving areas are made identical virtually by adjusting the designs and positions of the on-chip lenses, i.e., other optical members.

It should be noted that a configuration using an optical member, such as an on-chip lens, is also applicable to the first and second embodiments.

[Noise Reduction]

The inventors of the present application also have developed a signal read circuit for reducing noise suitably used in an image sensing apparatus having a configuration, as described above, in which a plurality of pixels share an amplifier.

FIG. **30** is a circuit diagram of a unit cell of the CMOS sensor having any of the aforesaid configurations.

Referring to FIG. **30**, references q_{11}, q_{12}, q_{21}, and q_{22} are photodiodes as photoelectric conversion elements; M_{TX1} to M_{TX4}, MOS transistors for transferring photo-charges accumulated in the photodiodes q_{11}, q_{12}, q_{21}, and q_{22} to a floating diffusion (FD) portion; M_{RES}; a MOS transistor for resetting the FD portion; and M_{SF} and M_{SEL}, MOS transistors configuring a source follower. The MOS transistor M_{SEL} also functions as a selection switch for selecting a photodiode.

Next, an operation of the image sensing apparatus including a signal processing circuit according to the third embodiment is explained. FIG. **31** is an equivalent circuit of the image sensing apparatus including the signal processing unit.

FIG. **32** is a timing chart for operating the image sensing apparatus shown in FIG. **31**.

Referring to FIGS. **31** and **32**, vertical scanning operation is initiated in response to the pulse, which indicates a vertical blanking period, of a signal ϕV_1 or ϕV_2. First, a signal ϕTX_{RO} which is applied to a reset line **573** of the first row is activated during a horizontal blanking period (i.e., when a signal ϕHBL is high), and signals for subsequent lines are applied in the same manner. Accordingly, all the pixels in every row are reset to the reset potential V_{DD}.

In each horizontal blanking period, as shown in FIG. **32**, during a period T_{11}, a signal ϕL becomes high and a transistor **561**, connected for a vertical signal line **557**, is turned on and the vertical signal line **557** is reset. Simultaneously, signals ϕT_N, ϕT_{S1} and ϕT_{S2} also become high, and transistors **562-1** to **562-3** are turned on. Accordingly wires in the upstream of transistors for reading signal, **564-1** to **564-3**, and capacitors **563-1** to **563-3** (C_{Tn}, C_{TS1}, C_{TS2}) are electrically connected to the vertical signal line **557**, and reset. Accordingly, residual charges in the capacitors **563-1** to **563-3**, for instance, are removed.

Thereafter, in a period T_{12}, a signal ϕTX_{RO} to be applied to the reset line **573** is changed to high, and the floating gate, which is the gate of the source follower amplifier configured with the MOS transistors M_{SF} and M_{SEL} in each unit cell, is reset to the voltage V_{DD}.

Then, in a period T_{13}, a signal ϕRV becomes high and a transistor **560** for grounding, connected to the vertical signal line **557**, is turned on, and the vertical signal line **557** is grounded. Simultaneously, the signal ϕT_N is changed to high in order to connect the capacitor **563-1** (C_{TN}) for storing a noise component to the vertical signal line **557**, and the transistor **562-1** is turned on. At this time, a signal ϕS_O to be applied to a row selection line **574** is high, and current corresponding to the potential (about V_{DD}) at the floating gate of the MOS transistor M_{SF} flows from a V_{DD} terminal to the capacitor **563-1** (C_{SF}) thereby the capacitor **563-1** (C_{TN}) stores charge corresponding to the noise component.

Next, in a period T_{14}, a signal ϕTX_{OOO} applied to the odd-column scanning line **571** is changed to high, in turn, a transfer gate (MOS transistor M_{TX1}, in this case) for an odd-number column in an odd-number row is turned on, and photo-charge accumulated in the photodiode q_{11} is transferred to the floating gate of the MOS transistor M_{SF}. The capacitor **563-1** (C_{TN}) for storing the noise component is disconnected from the vertical signal line **557** when the signal ϕT_N becomes low, and the capacitor **563-2** (C_{TS1}) for storing a photo-charge signal is connected, in turn, when the signal ϕT_{S1} is changed to high. Thus, charge accumulated in the photodiode q_{11}, for instance, in an odd-number column in an odd-number row is stored in the capacitor **563-2** (C_{TS1}) via the vertical signal line **557**.

Next, in a period T_{151} the signal ϕL becomes high, and only the vertical signal line **557** is reset. Since the signals ϕS_O, ϕT_N, ϕT_{S1}, and ϕT_{S2}, are low, other portions are not reset, and their states are preserved.

Next, the signal ϕTX_{RO} applied to the reset line **573** is changed to high between periods T_{15} and T_{16}, and the gate of the source follower amplifier (i.e., the gate of MOS transistor M_{SF}) is reset to the potential V_{DD}.

In the period T_{16}, a signal ϕTX_{OeO} applied to a scanning line **572** is changed to high, and photo-charge accumulated in the photodiode q_{12} in an even-number column in an odd-number row is transferred to the floating gate of the

MOS transistor M_{SF}. At this time, the signal ϕT_{S2} is changed to high, and photo-charge accumulated in the photodiode P_{12} is stored in the capacitor **563-3** (C_{TS2}) via the vertical signal line **557**, in the similar manner.

In the aforesaid manner, charges corresponding to the noise component, a first signal, and a second signal are respectively stored in the capacitors **563-1**, **563-2**, and **563-3** (C_{TN}, C_{TS1}, C_{TS2}) by each column for a row.

Next, in a period T_{17}, in order to sequentially transfer the charges stored in the capacitors **563-1** to **563-3** (C_{TN}, C_{TS1}, C_{TS2}) to amplifiers **566-1** to **566-3**, respectively, a horizontal scanning signal ϕHn is changed to high for each columns controlled by a horizontal shift register **559**, and transistors **564-1** to **564-3**, provided for each column, are turned on; thereby the capacitors **563-1** to **563-3** (C_{TN}, C_{TS1}, C_{TS2}) are connected to the respective amplifiers **566-1** to **566-3**. From the capacitors **563-1** to **563-3** (C_{TN}, C_{TS1}, C_{TS2}), the noise component, the first signal, and the second signal are outputted, and from a differential amplifier **567-1**, a signal **S1** obtained by subtracting the noise component from the first signal is outputted, and a signal **S2** obtained by subtracting the noise component from the second signal is outputted from a differential amplifier **567-2**. Note that accumulation of photo-charges by the photodiodes are also performed during the period T_{17}.

Further, by changing signals ϕTX_{OOe} and ϕTX_{Oee} to high instead of the signals ϕTX_{OOO} and ϕTX_{OeO} in the aforesaid operation, signals corresponding to photo-charges accumulated in the photodiodes q_{21} and q_{22} in an even-number row are read out and a noise component is subtracted from those photo-charge signals to obtain the signals **S1** and **S2**.

First Modification of the Third Embodiment

Next, another configuration of an image sensing apparatus including a signal processing circuit is explained.

FIG. **33** is an equivalent circuit of the image sensing apparatus including the signal processing unit.

In the modification **1**, four capacitors **563-2** to **563-5** (C_{TS1} to C_{TS4}) are provided for storing photo-charge signals, and different information can be stored in the respective capacitors **563-2** to **563-5**. More specifically, a signal corresponding to photo-charge accumulated in the photodiode q_{11} is stored in the capacitor **563-2** (C_{TS1}), and a signal corresponding to photo-charge accumulated in the photodiode q_{22} is stored in the capacitor **563-5** (C_{TS4}), for instance. Therefore, processes performed in the downstream of amplifiers **566** may be operated at a half clock speed to achieve the same throughput of the image sensing apparatus having the configuration shown in FIG. **31**. Accordingly, the amplifiers **566**, the differential amplifiers **567**, and other signal processing circuits may be also operated at a half clock speed comparing to the configuration shown in FIG. **31**. Thus, required speed of the operating elements is decreased, and it is possible to use inexpensive lower performance elements to configure the circuit. As a result, the cost of the system is reduced.

Note, the charges to be stored in the capacitors are not limited to those respectively corresponding to photo-charges accumulated in the respective photodiodes, and added charges may be stored by controlling operation of the transfer gates and the reset MOS. When the CMOS sensor **22** has the configuration as shown in FIG. **21**, for instance, it is possible to store a photo-charge signal of the G photodiode q_{11} in the capacitor **563-2** (C_{TS1}), a photo-charge signal of the G photodiode q_{22} in the capacitor **563-3** (C_{TS2}) and a photo-charge signal of the R photodiode q_{12} and the B photodiode q_{21} in the capacitor **563-4** (C_{TS3}). It is effective to apply this configuration to a smart sensor using each pixel more intelligently.

According to the configuration as explained in the third embodiment and the first modification of the third embodiment, it is possible to reduce noise caused by variation in characteristics of amplifiers each provided for each unit cell.

Second Modification of the Third Embodiment

Next, a case of operating the image sensing apparatus of the second modification of the third embodiment will be explained with reference to FIGS. **34** and **35**. FIG. **34** is an equivalent circuit of an image sensing apparatus including a signal processing circuit, and FIG. **35** is a timing chart for operating the image sensing apparatus shown in FIG. **34**.

First, during a horizontal blanking period, photo-charges accumulated in pixels are transferred and photodiodes are reset to an initial state.

During a period T_{211} the vertical signal lines **557** are reset by changing a signal ϕR_v to high to remove residual charges on the vertical signal lines **557**. At the same time, residual charges in the capacitors C_{TN1}, C_{TN2}, C_{TS1}, C_{TS2} are removed by changing signals ϕT_{N1}, ϕT_{N2}, ϕT_{S1} and ϕT_{S2} to high.

During a period T_{22}, in advance of transferring photo-charges of photodiodes in odd-number columns in a first row (q_{11}, q_{13}, . . . , $q_{1(n-1)}$), the gates of amplifiers (the gates of the MOS amplifiers M_{SF}) are reset by changing a signal ϕTX_{RO} to high and residual charges in the gates are removed. After resetting the gates, reset noise remains.

During a period T_{23}, the reset noise from the period T_{22} and offset voltages of the amplifiers are transferred to capacitors C_{TN1}. The output terminals of the amplifiers are electrically connected to the vertical signal lines **557** by changing a signal ϕS_O to high, and a signal ϕL is also changed to high to turn on MOS transistors **561** for activating the amplifiers. Further, a signal T_{N1} is changed to high to electrically connect the capacitors C_{TN1} with the respective vertical signal lines **557**. Accordingly, noise is stored in the capacitors C_{TN1}.

During a period T_{241} photo-charges of photodiodes in odd-number columns in a first row (q_{11}, q_{13}, . . . , $q_{1(n-1)}$ are transferred to the capacitors C_{TS1}. By changing the signals ϕL, ϕT_{S1}, and ϕS_O to high, the amplifiers and the capacitors C_{TS1} are electrically connected.

When a signal ϕTX_{OO} becomes high, photo-charge is transferred from each photodiode in the odd-number column in the first row to the amplifier. With this operation, the photo-charge is added to the reset noise from the period T_{22} at the gate of the amplifier. This gate voltage is further superposed on the offset voltage, and a signal **(S1+N1)** is stored in each capacitor C_{TS1}.

During the periods T_{25} to T_{28}, photo-charges of photodiodes in even-number columns in the first row (q_{12}, q_{14}, . . . , q_{1n}) are transferred to the capacitors C_{TS2}. The basic operation is the same as that performed during the periods T_{21} to T_{24}, except a signal ϕTX_{Oe} is changed to high instead of the signal ϕTX_{OO} a signal ϕT_{N2} is changed to high instead of the signal ϕT_{N1}, and a signal ϕT_{S2} is changed to high instead of the signal ϕT_{S1}.

During a period T_{29}, residual charges in the vertical signal lines **557**, the amplifiers, and the transfer MOS are removed, thereby transference of reset noise and photo-charge signals are completed.

After the aforesaid processes, noise signals **N1** and **N2**, and signals **(S1+N1)** and **(S2+N2)** are stored in the capaci-

tors C_{TN1}, C_{TN2}, C_{TS1}, and C_{TS2}, respectively. These signals are outputted via horizontal signal lines in response to signals φH1 and φH2 controlled by a horizontal shift register **559** during a period T_{210}. Then, in a differential amplifier A1, the noise signal N1 is subtracted from the signal (S1+N1), thereby a signal S1 is outputted, and in a differential amplifier A2, the noise signal N2 is subtracted from the photo-charge signal (S2+N2), thereby a signal S2 is outputted.

Accordingly, photo-charge signals faithfully corresponding to the photo-charges accumulated in the photodiodes q_{11} to q_{1n} in the first row are obtained. Charging operation starts when photo-charges are transferred to the gate in the period T_{24} and T_{28}.

In the next horizontal blanking period, the same operation performed for the first row as described above is repeated for the second row. After reading out the photo-charges of photodiodes in the second row, the amplifier, shared by four pixels, are put into a disconnected state until the next vertical blanking period when next operation is performed.

In order to read out photo-charges by two rows, another set of capacitors C_{TN1}, C_{TS1} and C_{TS2}, and differential amplifiers A1 and A2 are to be added to the configuration shown in FIG. **34**. More specifically, in the aforesaid operation, photo-charges are read out by a single row in a non-interlace operation, whereas photo-charges of two rows are read out in one horizontal period.

FIG. **36** is a timing chart during a vertical blanking period.

While a single vertical blanking period, the aforesaid operation performed during the horizontal blanking period is repeated number-of-row times. The vertical shift register outputs operation pulses ϕTX_{OO}, ϕTX_{Oe}, ϕTX_{RO}, and ϕS_O for each horizontal blanking period for each row.

As described above, in the second modification of the third embodiment, in addition to removing noise due to variation in characteristics of amplifiers as described in the third embodiment and in the first modification of the third embodiment, reset noise is also removed.

Fourth Embodiment

Next, the fourth embodiment of the present invention will be explained.

In the fourth embodiment, a case where an additional function is added to an amplifier, a common circuit in the aforesaid embodiments, shared in a unit cell is explained.

FIG. **37** shows a configuration of the common circuit with the additional function.

In the downstream of an amplifier **701**, memory **702**, a differential amplifier **703**, and a comparator **704** are added. The noise, as described in the foregoing embodiments, is temporarily stored in the memory **702**, a signal (S-N) is transferred to the positive terminal of the differential amplifier **703**, and the differential amplifier **703** takes the difference between the noise and the signal (S-N), thereby, a signal S, including no noise component, is obtained. The signal is transferred to a vertical signal line. Or, depending upon utilization purpose of the signal, the obtained signal can be digitized by the comparator **704**.

Further, by replacing the comparator **704** with an analog-digital (A/D) converter, a digital signal can be obtained. The digital signal output from the A/D converter may be either a serial signal or a parallel signal. The circuit may be arbitrary changed depending upon utilization purpose.

Other Embodiments

The present invention is not limited to a general CMOS sensor as shown in FIG. **41** or **42**, and may be applied to an image sensor as disclosed in ISSCC98/SESS:ON 11/IMAGESENSORS/PAPER FA11.8 pp182, shown in FIG. **38**.

In this case, a configuration of an amplifier shared by e.g., four photodiodes, may be the one as shown in FIG. **39**.

Further, the present invention is not limited to a CMOS sensor, and applicable to any APS sensors.

Furthermore, in the first to fourth embodiments, a plurality of photoelectric conversion elements are arranged to share a single amplifier, forming a unit cell altogether, however, the amplifier may be replaced by other unit which processes signals, outputted from a plurality of photoelectric conversion elements. For instance, an A/D conversion circuit (U.S. Pat. No. 5,461,425) and a signal processing circuit, e.g., an image compressor (Journal of Television Society vol. 150, no. 3, pp. 335 to 338, 1995) may be used in place of the amplifier.

The present invention is not limited to the above embodiments and various changes and modifications can be made within the spirit and scope of the present invention. Therefore to apprise the public of the scope of the present invention, the following claims are made.

What is claimed is:

1. An image sensing apparatus having a plurality of unit cells arranged in two dimensions, each unit cell including a plurality of photoelectric conversion elements and a common circuit shared by and arranged between said plurality of photoelectric conversion elements included in the same unit cell that the common circuit belongs to,

wherein said common circuit includes at least a transistor, signals from said plurality of photoelectric conversion elements are coupled to the transistor and processed, and the transistor outputs the processed signals to an output line,

wherein a first distance between a center of mass of photo-receiving areas of adjoining photoelectric conversion elements included in a given unit cell is substantially equal to a second distance between the center of mass of the photo-receiving areas of the adjoining photoelectric conversion elements included in different unit cells, and a third distance between a center of mass of the photo-receiving area of a photoelectric conversion element included in the given unit cell and the center of mass of the photo-receiving area of the adjoining photoelectric conversion element included in an adjoining unit cell,

wherein said common circuit is arranged at the edge of each plurality of photoelectric conversion elements arranged in a horizontal direction, and

wherein said unit cell is configured with a plurality of pixels each including a photoelectric conversion element, and contacts between layers of each pixel are arranged so that a number of conductors passing over each unit cell, as well as one of the contacts which is not connected to a conductor passing over the unit cell is connected to a light-shield film of the pixel.

2. An image sensing apparatus having a plurality of unit cells arranged in two dimensions, each unit cell including a plurality of photoelectric conversion elements and a common circuit shared by and arranged between said plurality of photoelectric conversion elements included in the same unit cell that the common circuit belongs to,

wherein said common circuit includes at least a transistor, signals from said plurality of photoelectric conversion

elements are coupled to the transistor and processed, and the transistor outputs the processed signals to an output line,

wherein a first distance between a center of mass of photo-receiving areas of adjoining photoelectric conversion elements included in a given unit cell is substantially equal to a second distance between the center of mass of the photo-receiving areas of the adjoining photoelectric conversion elements included in different unit cells, and a third distance between a center of mass of the photo-receiving area of a photoelectric conversion element included in the given unit cell and the center of mass of the photo-receiving area of the adjoining photoelectric conversion element included in an adjoining unit cell,

wherein said common circuit is arranged at the edge of each plurality of photoelectric conversion elements arranged in a vertical direction, and

wherein said unit cell is configured with a plurality of pixels each including a photoelectric conversion element, and contacts between layers of each pixel are arranged so that a number of conductors passing over each unit cell, as well as one of the contacts which is not connected to a conductor passing over the unit cell is connected to a light-shield film of the pixel.

3. An image sensing apparatus having a plurality of unit cells arranged in two dimensions, each unit cell including a plurality of photoelectric conversion elements and a common circuit shared by and arranged between said plurality of photoelectric conversion elements included in the same unit cell that the common circuit belongs to,

wherein said common circuit includes at least a transistor, signals from said plurality of photoelectric conversion elements are coupled to the transistor and processed, and the transistor outputs the processed signals to an output line,

wherein a first distance between a center of mass of photo-receiving areas of adjoining photoelectric conversion elements included in a given unit cell is substantially equal to a second distance between the center of mass of the photo-receiving areas of the adjoining photoelectric conversion elements included in different unit cells, and a third distance between a center of mass of the photo-receiving area of a photoelectric conversion element included in the given unit cell and the center of mass of the photo-receiving area of the adjoining photoelectric conversion element included in an adjoining unit cell, and

wherein said common circuit is digital signal conversion means for converting a signal from each of said plurality of photoelectric conversion element into a digital signal.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,977,684 B1
APPLICATION NO. : 09/299874
DATED : December 20, 2005
INVENTOR(S) : Seiji Hashimoto et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2,
Line 62, "Fig. 5res" should read -- Figures --.

Column 4,
Line 13, "when" should read -- of an --; and
Line 55, "shows" should read -- show --.

Column 5,
Line 14, "and a_{21}, a_{42}" should read -- and a_{21}, a_{12} --.

Column 6,
Line 22, "and b_{31}" should read -- and b_{31}, --; and
Line 33, "incidents" should read -- incident --.

Column 8,
Line 7, "singlecrystalline" should read -- single crystalline --; and
Line 42, "Q=CV;" should read -- Q=CV, --.

Column 9,
Line 35, "provided-over" should read -- provided over --; and
Line 42, "of the" should read -- for --.

Column 10,
Line 31, "corresponding the" should read -- corresponding to the --.

Column 11,
Line 26, "(C_{TSI}" should read -- (C_{TSI}) --; and
Line 58, "columns" should read -- column --.

Column 12,
Line 28, "an" should read -- a --;
Line 54, "becomes" should read -- become --; and
Line 67, "singlecrystalline" should read -- single crystalline --.

Column 13,
Line 12, "57.96 μM^2," should read -- 57.96 μm^2, --.

Column 15,
Line 17, "columns" should read -- column --.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,977,684 B1
APPLICATION NO. : 09/299874
DATED : December 20, 2005
INVENTOR(S) : Seiji Hashimoto et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 16,
Lines 13 and 40, "symmetry" should read -- symmetrical --; and
Line 64, "singlecrystalline" should read -- single crystalline --.

Column 17,
Lines 5 and 6, "symmetry" should read -- symmetrical --.

Column 20,
Line 40, "(C_{SF})" should read -- (C_{TN}), --; and
Line 56, "period T_{151}" should read -- period T_{15}, --.

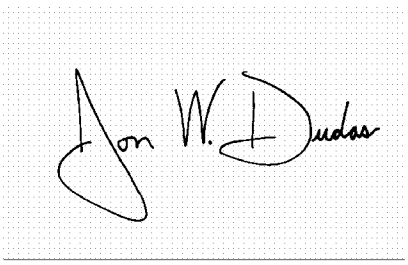
Column 21,
Line 2, "photodiode P_{12}" should read -- photodiode q_{12} --; and
Line 12, "columns" should read -- column --.

Column 22,
Line 19, "period T_{211}" should read -- period T_{21}, --;
Line 41, "period T_{241}" should read -- period $_{24}$, --; and
Line 58,"signal ϕTX_{00}" should read -- signal ϕTX_{00},--.

Column 26,
Line 24, "element" should read -- elements --.

Signed and Sealed this

Twenty-seventh Day of June, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

US 20020018131A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2002/0018131 A1**

Kochi (43) **Pub. Date: Feb. 14, 2002**

(54) **IMAGE PICKUP APPARATUS**

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(21) Appl. No.: **09/854,563**

(22) Filed: **May 15, 2001**

(30) **Foreign Application Priority Data**

May 16, 2000 (JP) 143674/2000

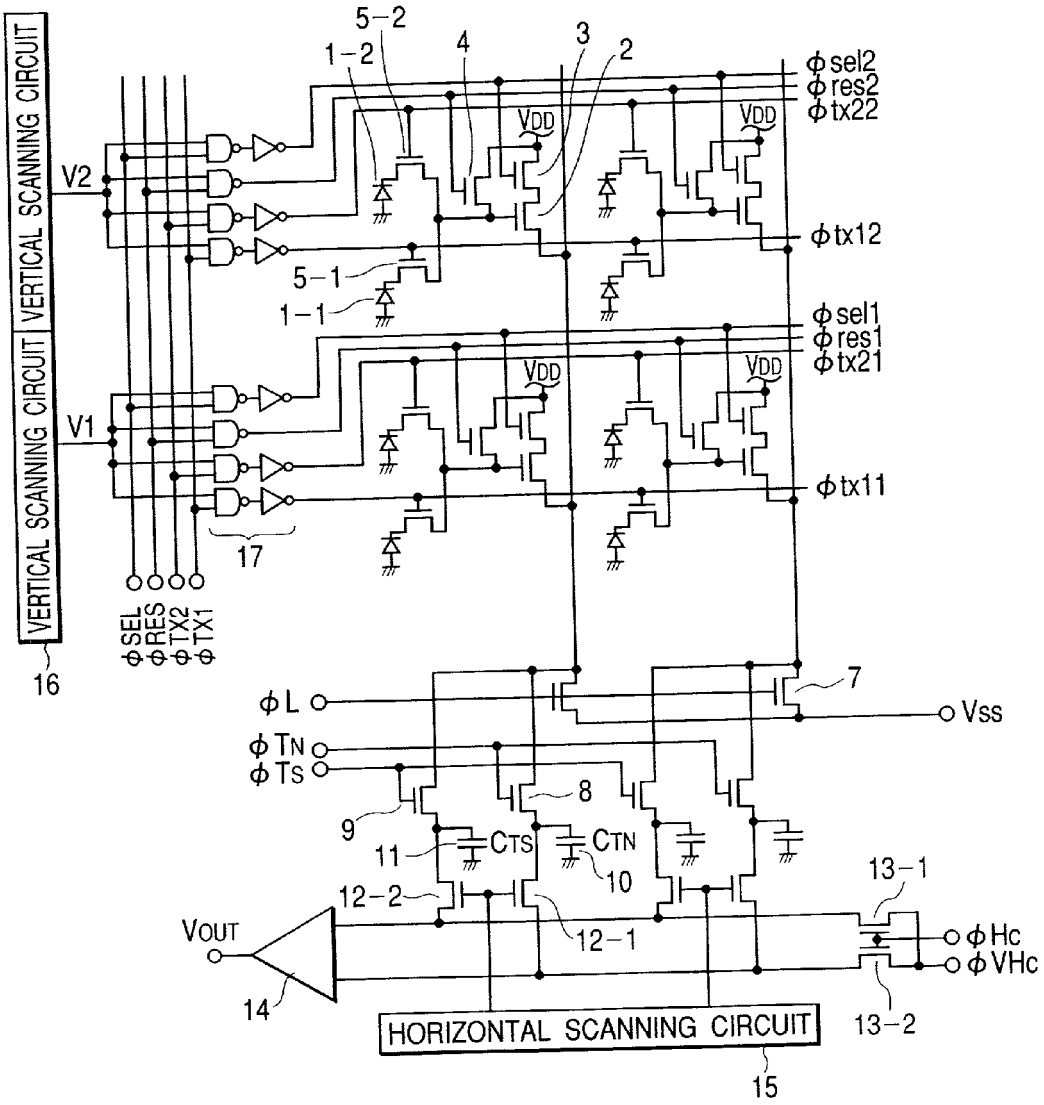
Publication Classification

(51) **Int. Cl.**[7] **H04N 3/14**; H04N 5/335

(52) **U.S. Cl.** **348/304**; 348/308

(57) **ABSTRACT**

To implement a solid-state image pickup element in which the peripheral circuit is downsized, there is provided a solid-state image pickup element including a plurality of pixel blocks each having a plurality of photoelectric conversion elements, a plurality of transfer switches each having one terminal connected to a corresponding photoelectric conversion element, a signal input portion commonly connected to the other terminal of each of the plurality of transfer switches, and an amplifier connected to the signal input portion, and a scanning circuit for outputting a scanning clock for each pixel block.



Patent Application Publication Feb. 14, 2002 Sheet 1 of 10 US 2002/0018131 A1

FIG. 1

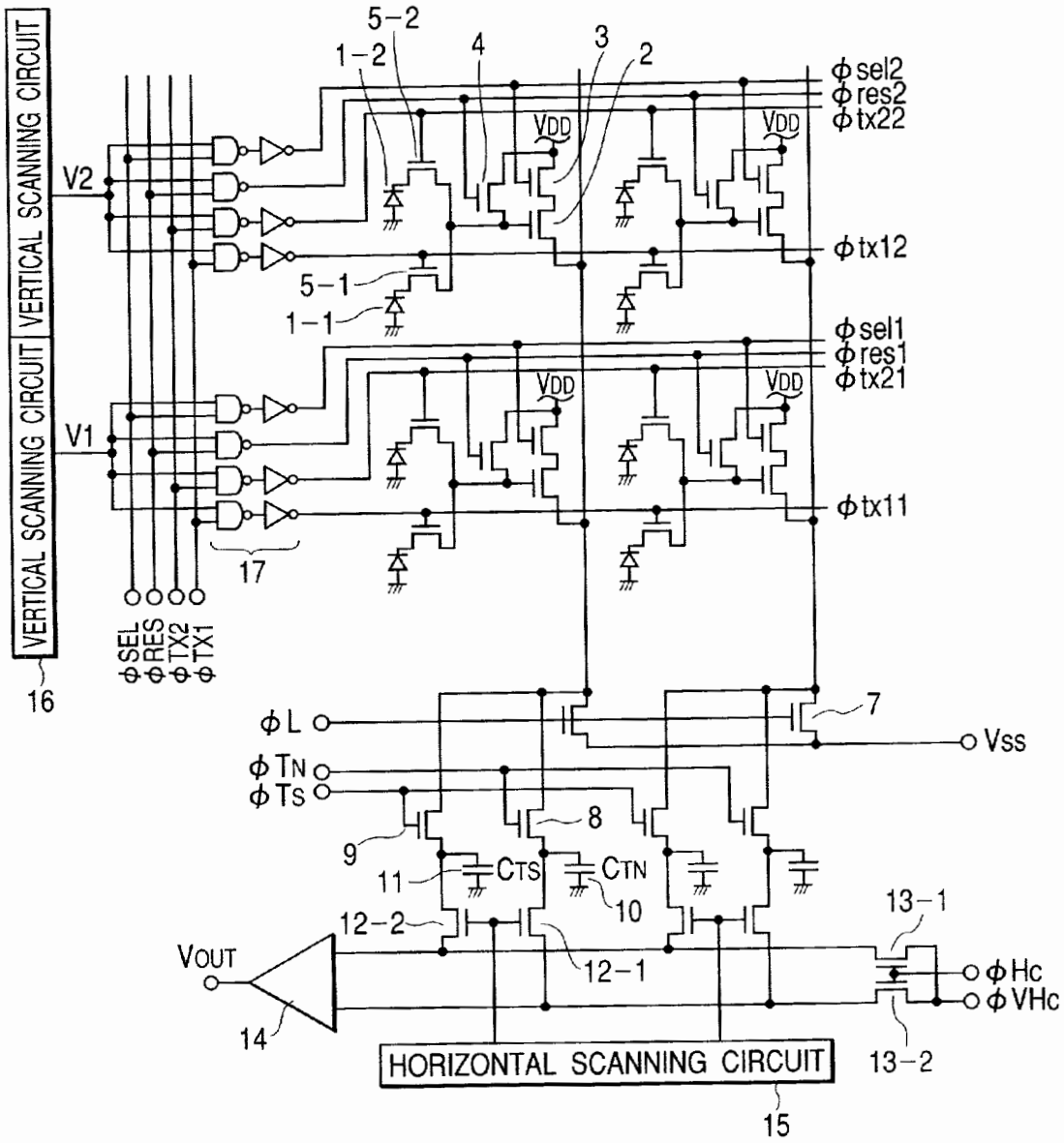


FIG. 2

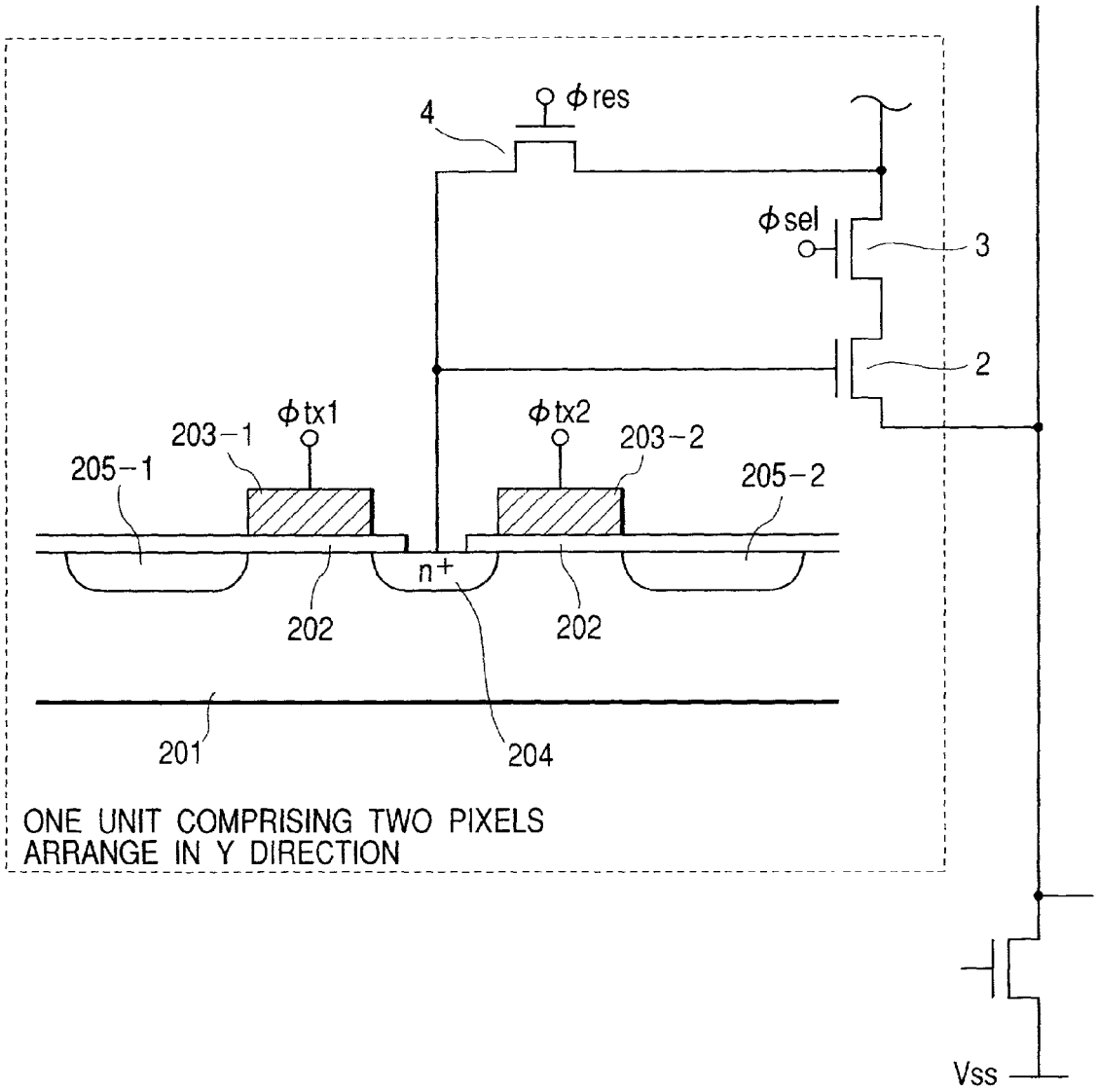

4
φres
φsel
3
2
φtx1
φtx2
203−1
203−2
205−1
205−2
n+
202
202
201
204
ONE UNIT COMPRISING TWO PIXELS ARRANGE IN Y DIRECTION
Vss

FIG. 3

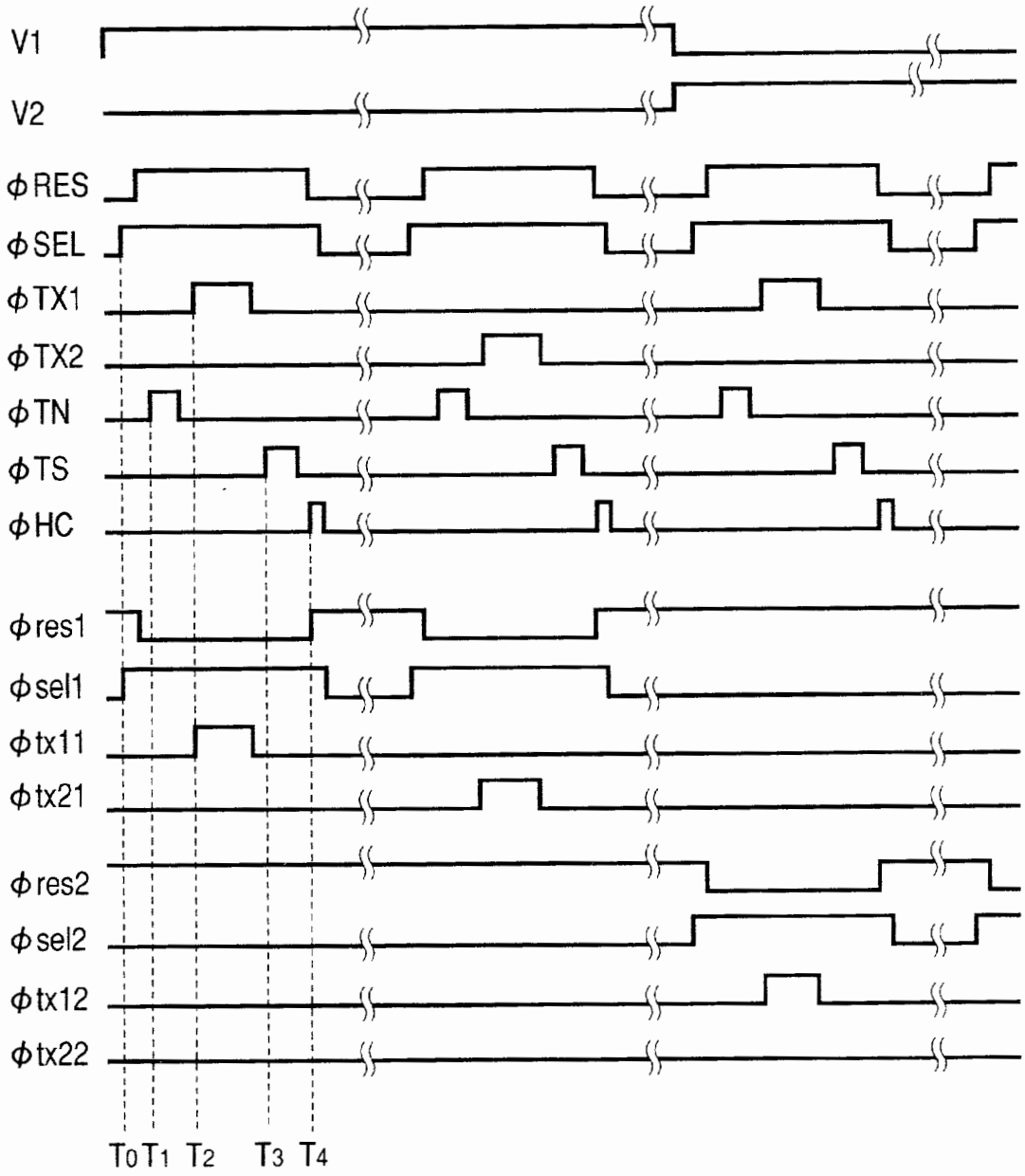

V1
V2
φRES
φSEL
φTX1
φTX2
φTN
φTS
φHC
φres1
φsel1
φtx11
φtx21
φres2
φsel2
φtx12
φtx22
T0 T1 T2 T3 T4

FIG. 4

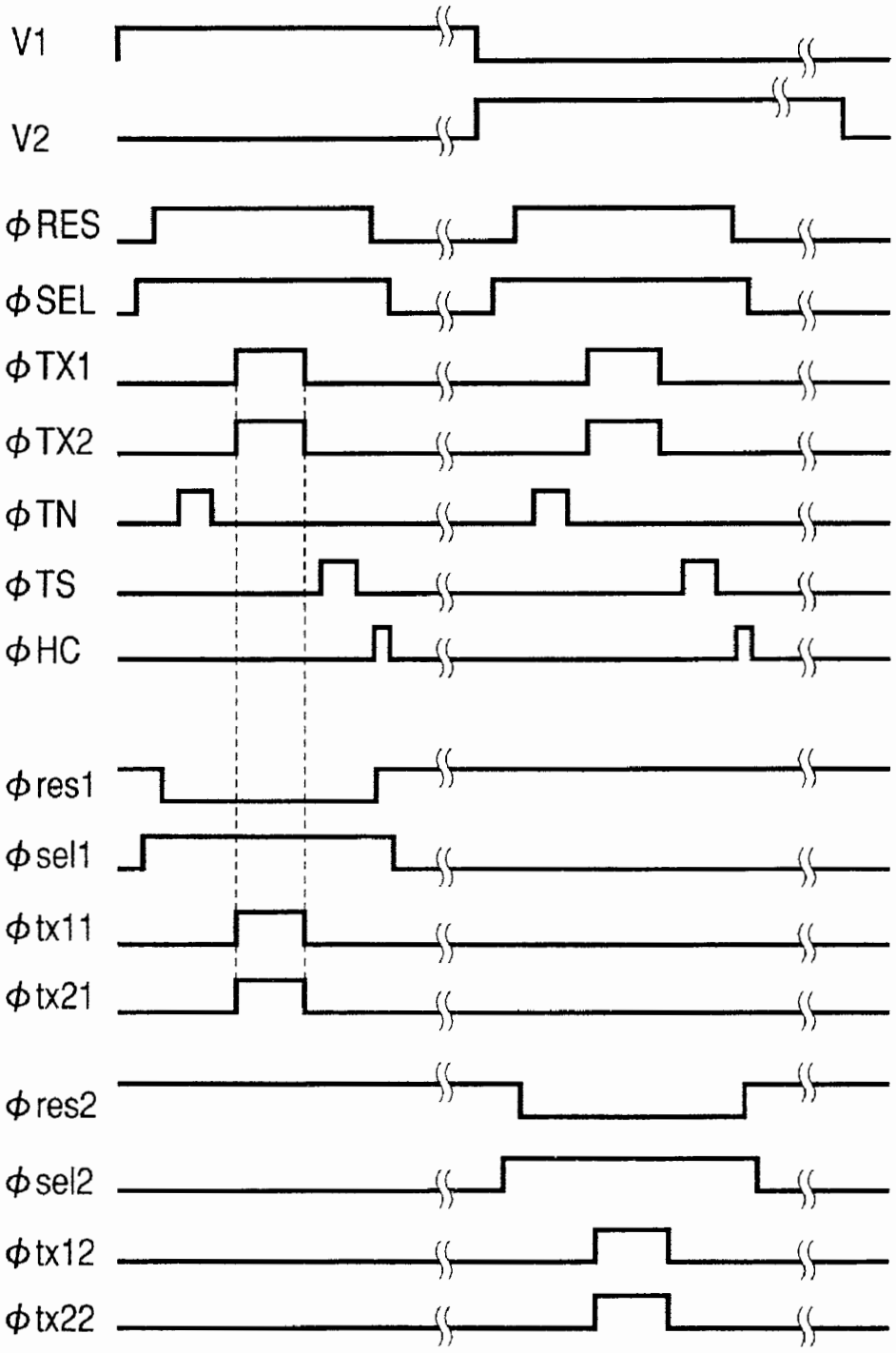

V1
V2
φRES
φSEL
φTX1
φTX2
φTN
φTS
φHC
φres1
φsel1
φtx11
φtx21
φres2
φsel2
φtx12
φtx22

FIG. 5

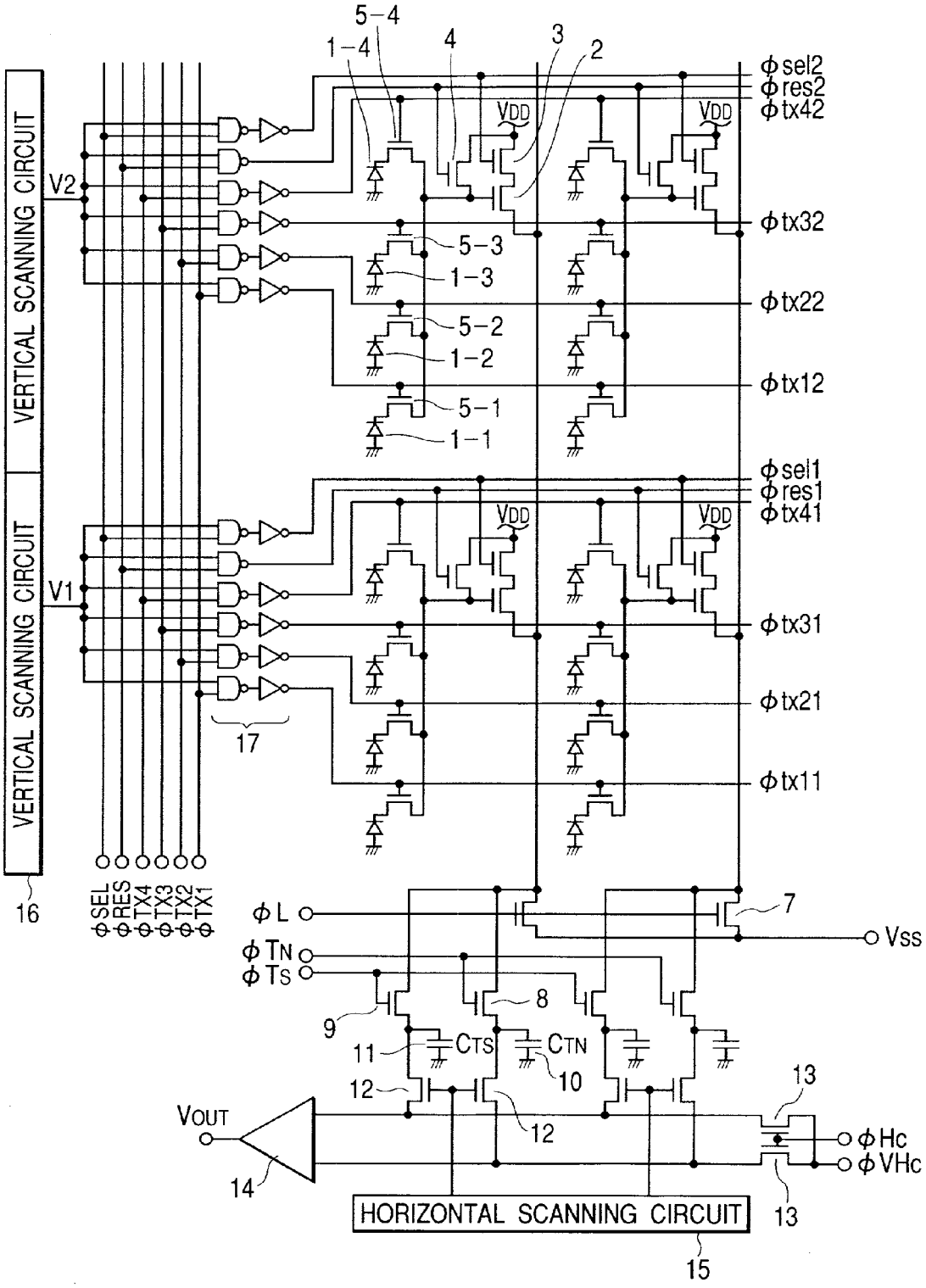

VERTICAL SCANNING CIRCUIT
VERTICAL SCANNING CIRCUIT
V2
V1
16
17
5-4
1-4
4
3
2
φsel2
φres2
φtx42
φtx32
φtx22
φtx12
φsel1
φres1
φtx41
φtx31
φtx21
φtx11
VDD
5-3
1-3
5-2
1-2
5-1
1-1
φSEL
φRES
φTX4
φTX3
φTX2
φTX1
φL
φTN
φTS
7
Vss
8
9
11
CTS
CTN
10
12
13
VOUT
14
φHc
φVHc
HORIZONTAL SCANNING CIRCUIT
15

FIG. 6

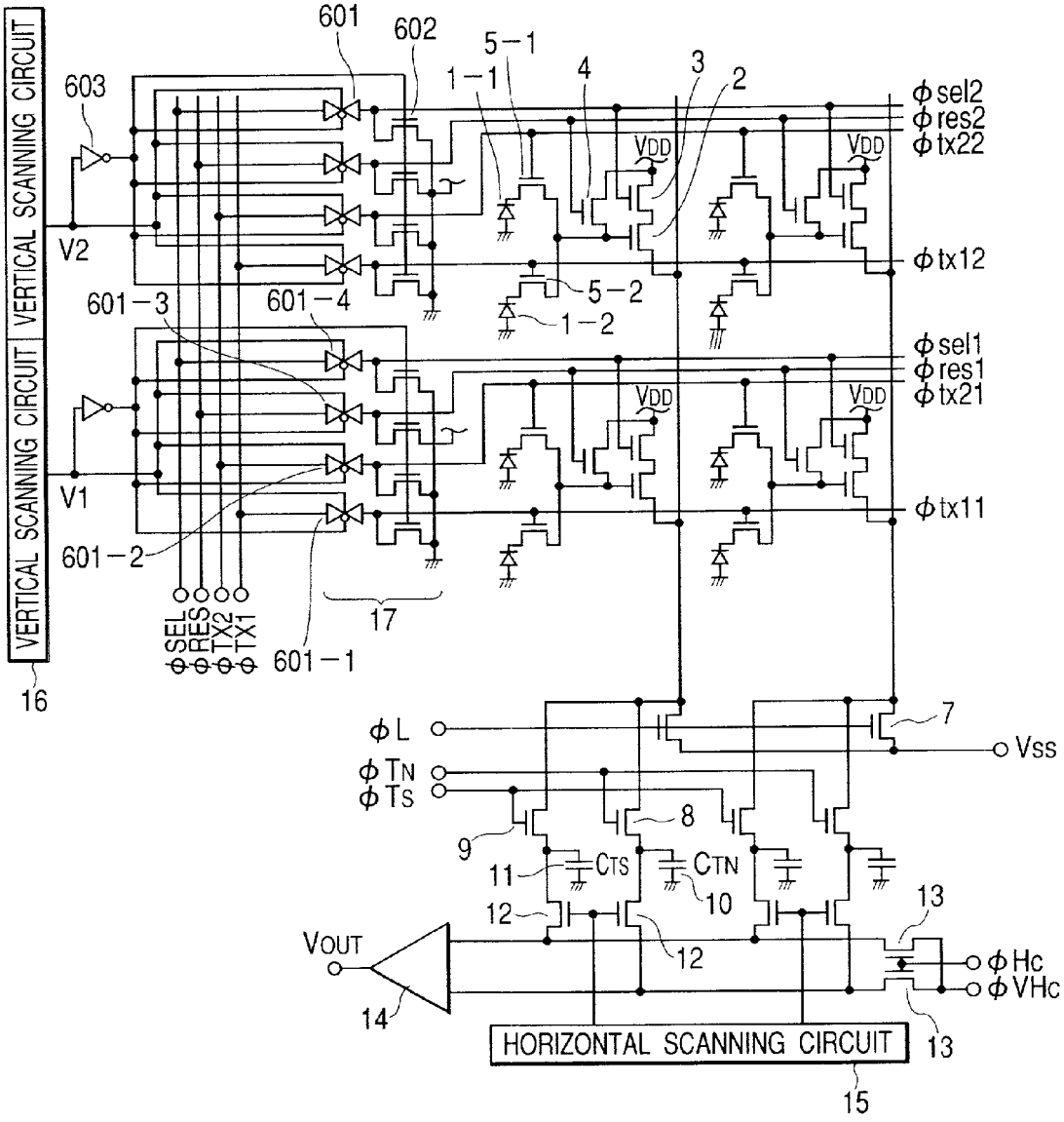

VERTICAL SCANNING CIRCUIT
VERTICAL SCANNING CIRCUIT
16
603
601
602
5-1
1-1
4
3
2
φsel2
φres2
φtx22
VDD
VDD
V2
φtx12
5-2
1-2
601-3
601-4
φsel1
φres1
φtx21
VDD
VDD
V1
φtx11
601-2
SEL
RES
TX2
TX1
17
601-1
φL
Vss
7
φTN
φTS
8
9
11
CTS
CTN
10
12
13
VOUT
12
φHc
φVHc
14
HORIZONTAL SCANNING CIRCUIT
13
15

FIG. 7

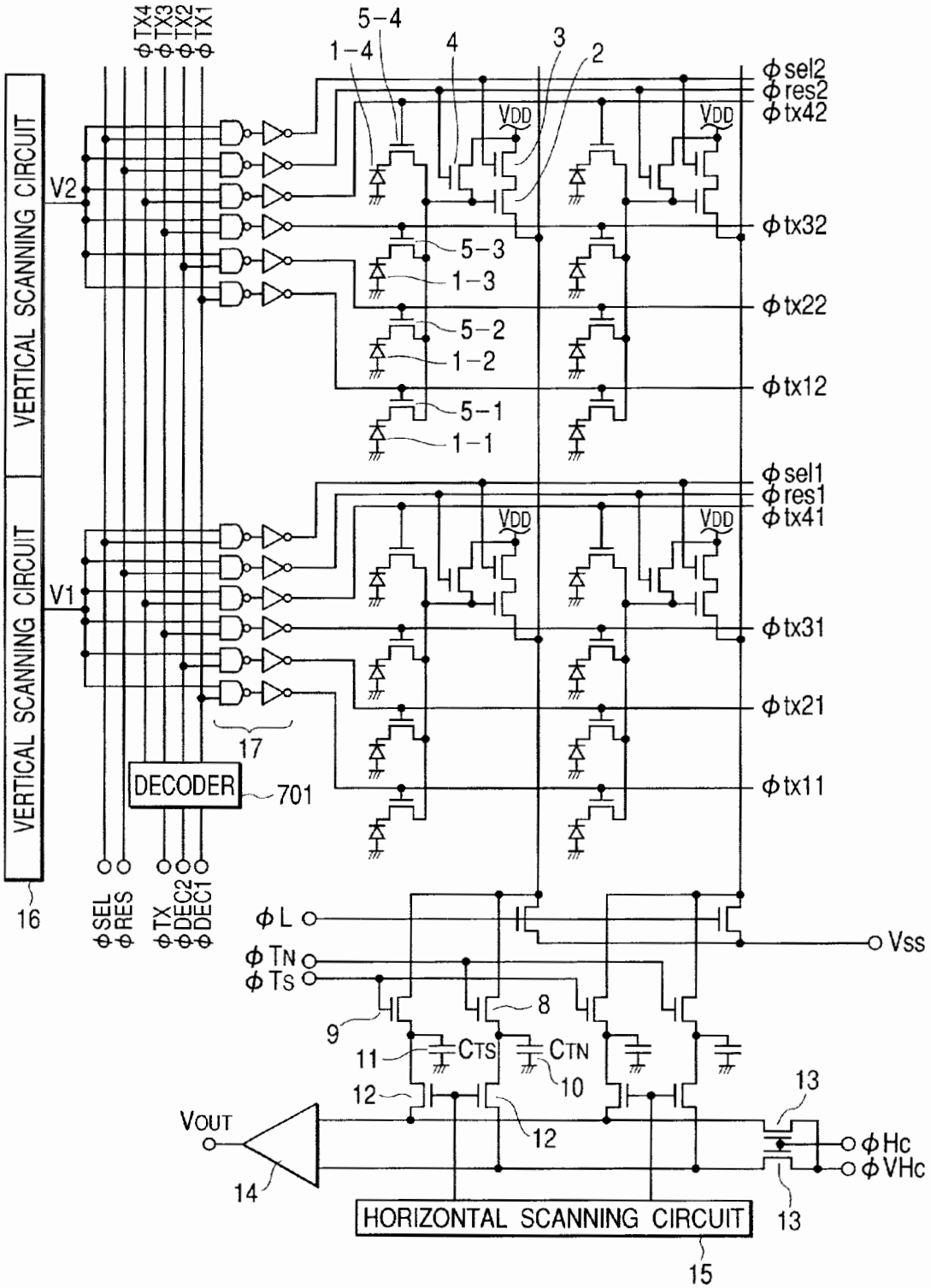

TX4
TX3
TX2
TX1
5-4
1-4
4
3
2
φsel2
φres2
φtx42
VDD
V2
φtx32
5-3
1-3
φtx22
5-2
1-2
φtx12
5-1
1-1
VERTICAL SCANNING CIRCUIT
φsel1
φres1
φtx41
V1
φtx31
φtx21
φtx11
17
DECODER
701
16
φSEL
φRES
φTX
DEC2
DEC1
φL
φTN
φTS
Vss
9
8
11
CTS
CTN
10
12
13
VOUT
φHc
φVHc
14
HORIZONTAL SCANNING CIRCUIT
15

FIG. 8

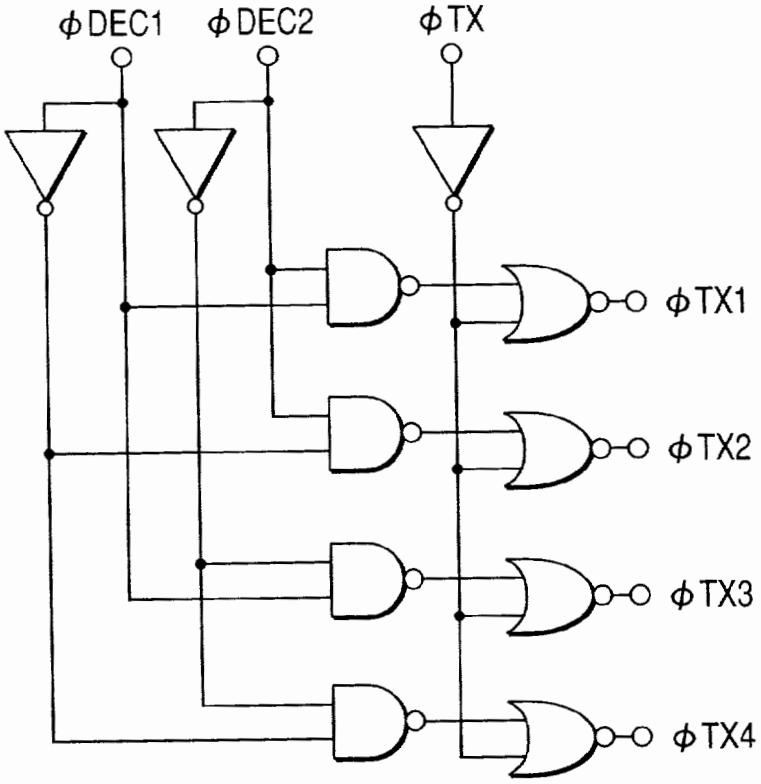

φDEC1
φDEC2
φTX
φTX1
φTX2
φTX3
φTX4

FIG. 9

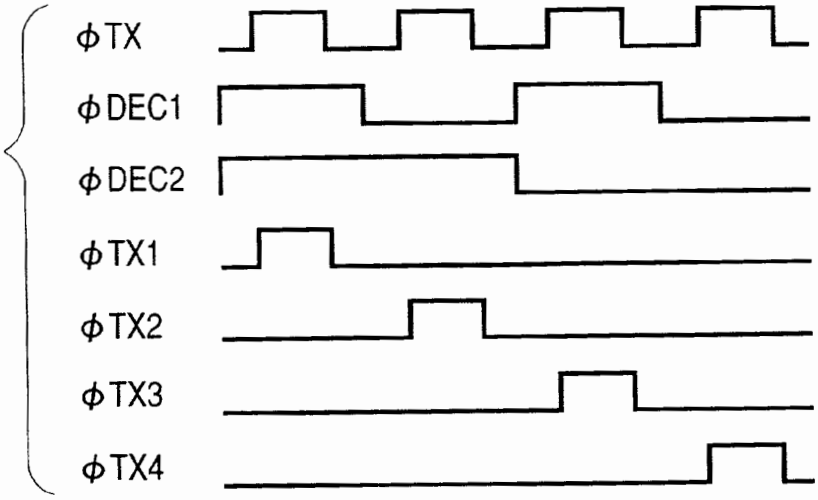

φTX
φDEC1
φDEC2
φTX1
φTX2
φTX3
φTX4

FIG. 10

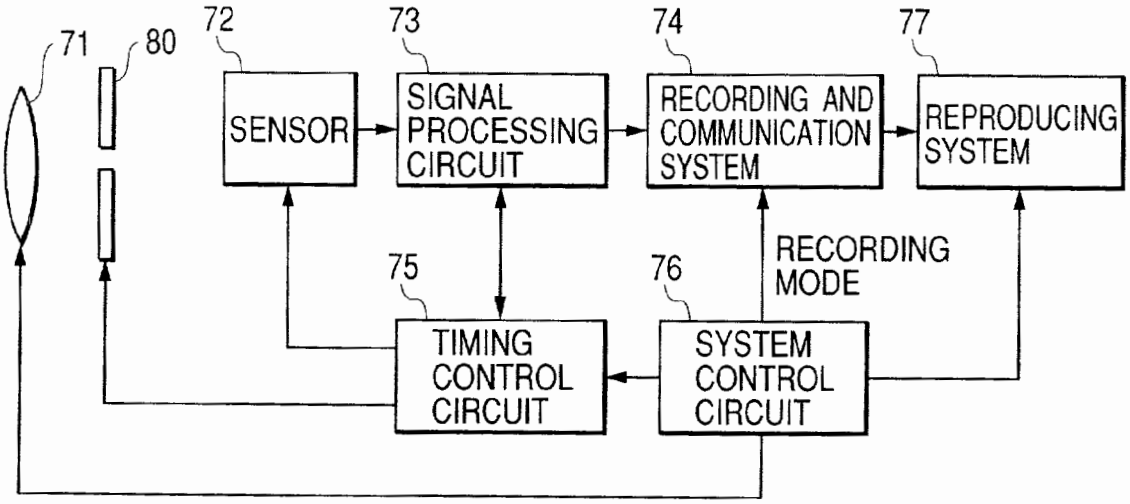

71
80
72
73
74
77
SENSOR
SIGNAL PROCESSING CIRCUIT
RECORDING AND COMMUNICATION SYSTEM
REPRODUCING SYSTEM
RECORDING MODE
75
76
TIMING CONTROL CIRCUIT
SYSTEM CONTROL CIRCUIT

FIG. 11

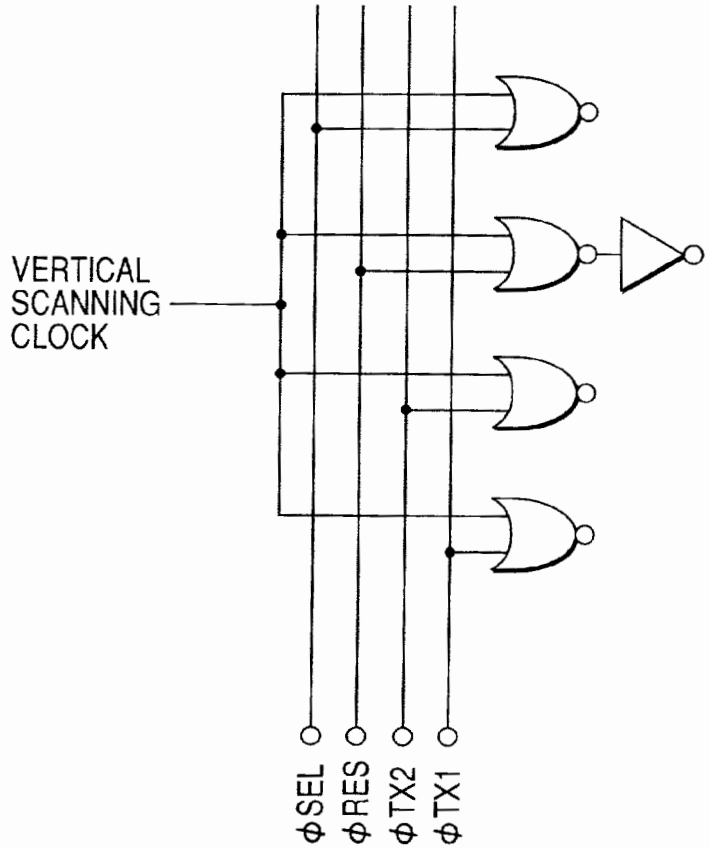

VERTICAL SCANNING CLOCK
φSEL
φRES
φTX2
φTX1

FIG. 12

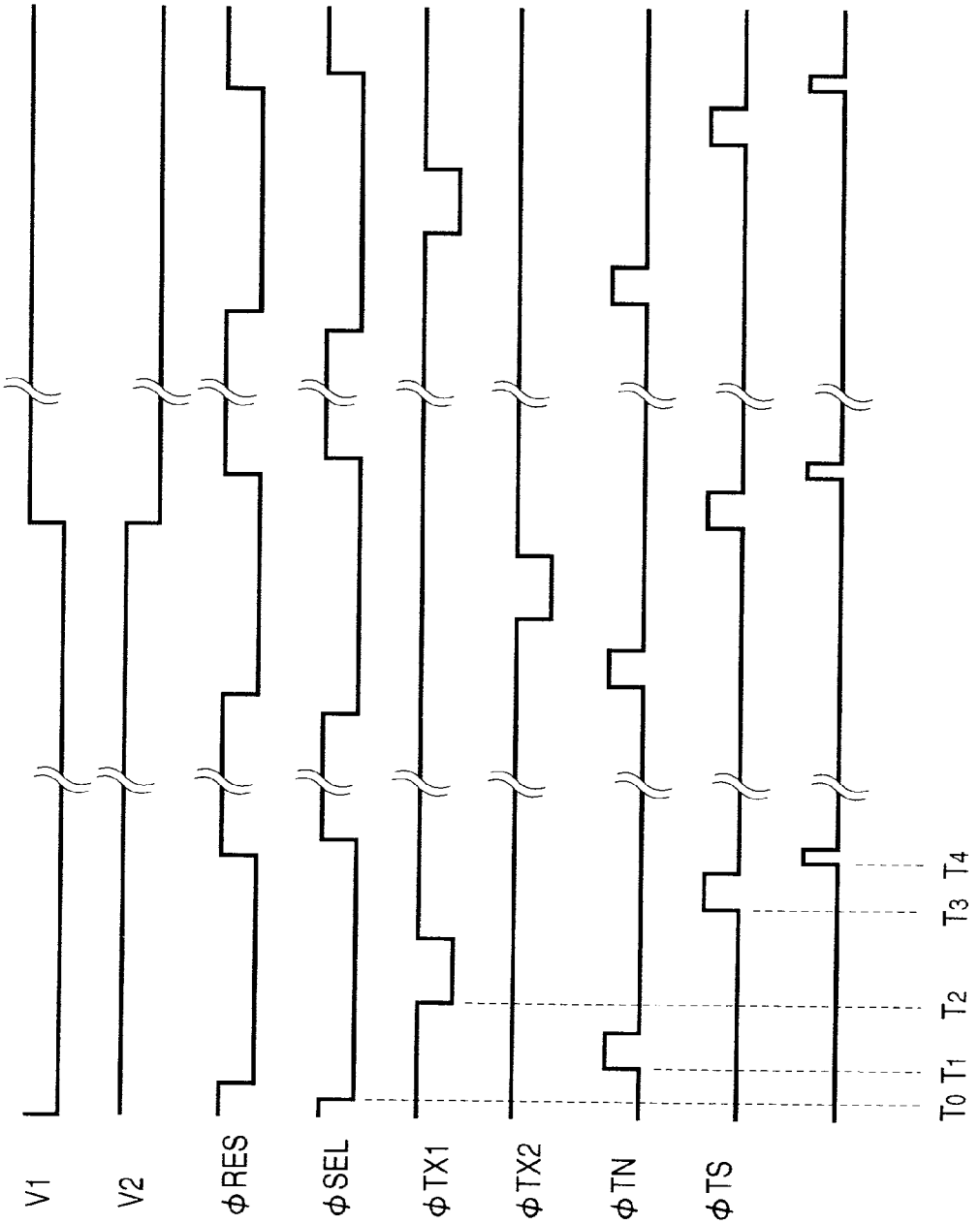


IMAGE PICKUP APPARATUS

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a solid-state image pickup element for obtaining an image signal and an image pickup apparatus using the same and, more particularly, to a CMOS compatible XY address amplifier type solid-state image pickup element and an image pickup apparatus using the same.

[0003] 2. Related Background Art

[0004] Conventional solid-state image pickup elements have a MOS structure made up of a conductor such as a metal capable of performing photoelectric conversion, an insulator such as an oxide, and a semiconductor, and are classified into an FET type and CCD type depending on the photocarrier moving method. Solid-state image pickup elements are used in various fields including a solar battery, image camera, copying machine, and facsimile apparatus, and are technically being increased in conversion efficiency and integration density. One of such solid-state image pickup elements is a CMOS process compatible sensor (to be referred to as a CMOS sensor hereinafter). Sensors of this type are proposed in documents, e.g., IEEE Transactions on Electron Device Vol. 41, pp. 452-453, 1994. Another CMOS sensor is disclosed in Japanese Laid-Open Patent Application No. 9-46596 in which the sensor is suitable for downsizing of pixels and addition/non-addition of a pixel signal can be arbitrarily switched.

[0005] In the prior art, downsizing cannot be effectively achieved unless the pitch of a vertical scanning circuit is also decreased along with pixel reduction.

[0006] Further, a scanning circuit for efficiently performing addition/non-addition switching operation has not satisfactorily been examined.

SUMMARY OF THE INVENTION

[0007] It is an object of the present invention to provide a solid-state image pickup element much smaller than a conventional solid-state image pickup element.

[0008] To achieve the above object, according to an aspect of the present invention, there is provided a solid-state image pickup element comprising a plurality of pixel blocks each having a plurality of photoelectric conversion elements, a plurality of transfer switches for transferring signals from the respective photoelectric conversion elements, and a common amplifier for receiving signals from the plurality of transfer switches, and a scanning circuit for outputting a scanning clock for each pixel block.

[0009] In this arrangement, the circuit scale of the scanning circuit can be reduced, resulting in a small area of the solid-state image pickup element.

[0010] The above and other objects and features of the present invention will be apparent from the following description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] **FIG. 1** is a circuit diagram for explaining the first embodiment of the present invention;

[0012] **FIG. 2** is a sectional view showing a pixel according to the first embodiment of the present invention;

[0013] **FIG. 3** is a first timing chart according to the first embodiment of the present invention;

[0014] **FIG. 4** is a second timing chart according to the first embodiment of the present invention;

[0015] **FIG. 5** is a circuit diagram for explaining the second embodiment of the present invention;

[0016] **FIG. 6** is a circuit diagram for explaining the third embodiment of the present invention;

[0017] **FIG. 7** is a circuit diagram for explaining the fourth embodiment of the present invention;

[0018] **FIG. 8** is a circuit diagram showing a decoder circuit;

[0019] **FIG. 9** is a timing chart showing the operation of the decoder circuit;

[0020] **FIG. 10** is a schematic block diagram showing an image pickup system according to the present invention;

[0021] **FIG. 11** is a circuit diagram showing an arrangement when an arithmetic processing unit is constituted by OR and NOR gates; and

[0022] **FIG. 12** is a timing chart showing the operation of the arrangement in **FIG. 11**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023] Preferred embodiments of the present invention will be described in detail below with reference to the accompanying drawings.

[0024] **FIG. 1** is a circuit diagram showing the equivalent circuit of a solid-state image pickup element according to the first embodiment of the present invention. In **FIG. 1**, reference numerals **1-1** and **1-2** denote photoelectric conversion elements such as photodiodes; **5-1** and **5-2**, transfer switch MOS transistors; **4**, a reset MOS transistor; **2**, an input MOS transistor of a source follower amplifier; **3**, a vertical selection MOS transistor; **7**, a source follower load transistor; **8**, a dark output transfer MOS transistor; **9**, a bright output transfer transistor; **10**, a dark output accumulation capacitor; **11**, a bright output accumulation capacitor; **12-1** and **12-2**, horizontal transfer MOS transistors for transferring dark and bright outputs, respectively; **13-1** and **13-2**, horizontal output line reset MOS transistors; **14**, a differential output amplifier; **15**, a horizontal scanning circuit; **16**, vertical scanning circuits arranged for respective pixel blocks; and **17**, an arithmetic operation processing unit constituted by AND and NAND gates in the first embodiment.

[0025] **FIG. 2** is a sectional view of a pixel. In **FIG. 2**, reference numeral **201** denotes a p-type well; **202**, a gate oxide layer; **203-1** and **203-2**, gate electrodes of transfer MOS transistors formed from poly-Si or the like; **204**, an n^+-type FD (Floating Diffusion) portion serving as a signal input portion; **205-1** and **205-2**, photoelectric conversion portions. The FD portion **204** is connected to the two photoelectric conversion portions **205-1** and **205-2** via the transfer MOS transistors **5-1** and **5-2**. In **FIG. 2**, the drains of the two transfer MOS transistors **5-1** and **5-2** and the FD

portion **204** are shared by each other, thus increasing the sensitivity by micropatterning and reduction in the capacitance of the FD portion **204**. Alternatively, the two transfer MOS transistors **5-1** and **5-2** may have their own drains which are connected by a metal line to form an FD portion.

[**0026**] The operation will be described briefly with reference to the timing chart of **FIG. 3**. In **FIG. 3**, V1 and V2 represent vertical scanning timing clocks sequentially output from the vertical scanning circuit **16**; RES, an external reset clock input to the arithmetic processing unit **17**; ϕSEL, an external vertical selection clock input to the arithmetic processing unit **17**; and ϕTX1 and ϕTX2, first and second external transfer clocks input to the arithmetic processing unit **17**.

[**0027**] The photoelectric conversion element **1** is reset by turning on the transfer switch **5** and reset switch **4**. After the transfer switch **5** is turned off, accumulation operation starts. At the end of the accumulation time, AND operation of ϕSEL and the timing clock V1 from the vertical scanning circuit **16** are performed, so that a vertical selection clock ϕsell goes high at time T0, and then the vertical selection MOS transistor **3** is turned on to operate source follower amplifiers corresponding to the pixels on the first and second lines. Similarly, NAND operation of ϕRES and the timing clock Vi from the vertical scanning circuit **16** are performed, so that a reset clock ϕres1 goes low, and then the reset of the FD portion **204** is stopped, so that the FD portion **204** is floated. At time T1, a clock ϕTN goes high, and the dark voltage of the FD portion **204** is output to the accumulation capacitor C_{TN} **10** by source follower operation.

[**0028**] To output photoelectrical conversion outputs from the pixels on the first line, AND operation of ϕTX1 and the timing clock V1 from the vertical scanning circuit **16** are performed at time T2, so that a transfer cl ock ϕtx11 goes high to turn on the transfer MOS transistor **5**, and then signal charges are transferred to the FD portion **204**. With this receiving of the charges, the potential of the FD portion **204** appears to change depending on light. At time T3, a clock ϕTS goes high, and the voltage of the FD portion **204** is output to the accumulation capacitor C_{TS} **11** by source follower operation. At this time, dark and bright outputs from the pixels on the first line are respectively accumulated in the accumulation capacitors C_{TN} **10** and C_{TS} **11**. At time T4, a horizontal output line reset clock ϕHC temporarily goes high to reset the horizontal output line. The dark and bright outputs from the pixels are output in response to a scanning timing signal from the horizontal scanning circuit **15** during the horizontal transfer period. Then, the differential output amplifier **14** obtains a differential output Vout between the two outputs, thereby outputting a signal having a high S/N ratio from which random noise and fixed pattern noise of pixels are removed.

[**0029**] The operation can be easily switched to signal read-out of the second line by clock operation using the transfer clock ϕX2 instead of the external transfer clock ϕTX1 at the same timing in the above-described read sequence.

[**0030**] The first embodiment realizes sensor read operation by generating a vertical scanning timing signal only once while controlling the pixel arrays of the two, first and second lines. Thus, the circuit arrangement of the vertical scanning circuit can be simplified, the vertical scanning circuit can be reduced along with pixel reduction, and a small-size solid-state image pickup element can be implemented.

[**0031**] In the first embodiment, a pair of circuits for generating the reset clock ϕres and vertical selection clock ϕsel necessary for read of each of the first and second lines are arranged for and shared by the two, first and second lines, thereby also reducing the circuit scale.

[**0032**] Addition and read-out of signals from two pixels at the FD portion **204** can also be realized by changing only the timings of application pulses without changing the circuit arrangement of the first embodiment. **FIG. 4** is a timing chart when signals from two, upper and lower pixels are added. The timings of the transfer clocks ϕtx**11** and ϕtx**12** are shifted to each other by one line in **FIG. 3** showing the non-addition mode, whereas their timings are the same in the addition mode. More specifically, to simultaneously read out signals from the photoelectric conversion elements **1-1** and **1-2**, the clock ϕTN goes high to read out a noise component from a vertical output line. Then, the transfer clocks ϕtx**11** and ϕtx**12** simultaneously go high and low respectively, to transfer signals to the FD portion **204**. Accordingly, the signals from the two, upper and lower photoelectric conversion elements **1** can be added by the FD portion **204** at the same timing.

[**0033**] The first embodiment can easily implement addition function by only changing the timings of the external transfer clocks ϕTX1 and ϕTX2.

[**0034**] The arithmetic processing unit **17** in the first embodiment is made up of AND and NAND gates, but is not limited to this.

[**0035**] **FIG. 11** shows an arrangement of the first embodiment when the arithmetic processing unit is made up of OR and NOR gates. **FIG. 12** is a timing chart showing the operation in this arrangement. This arrangement can also generate a desired clock by processing the vertical scanning timing clock and the clocks ϕRES, ϕSEL, ϕTX1, and ϕTX2 by the arithmetic processing unit. In the pixel layout represented by this arrangement, the number of transistors which constitute gates can be more reduced when the arithmetic processing unit is made up of OR and NOR gates than when it is made up of AND and NAND gates. This can further reduce the circuit scale.

[**0036**] **FIG. 5** is a circuit diagram showing the equivalent circuit of a solid-state image pickup element according to the second embodiment of the present invention. In the second embodiment, four pixels in the Y direction form one pixel block, and one vertical scanning circuit **16** is arranged for every four pixels.

[**0037**] In the second embodiment, sensor read operation can be performed by generating a vertical scanning timing signal only once while controlling the pixel arrays of the four, first to fourth lines. The circuit arrangement of the vertical scanning circuit can be more simplified than in the first embodiment. The scanning circuit can be reduced along with pixel reduction to implement a smaller-size solid-state image pickup element.

[**0038**] A pair of circuits for generating a reset clock ϕres and vertical selection clock ϕsel are arranged for and shared by the four, first to fourth lines, thereby also reducing the circuit scale.

[0039] Addition and read-out of signals from four pixels in the Y direction at an FD portion **204** can also be easily realized by changing only the timings of application pulses without changing the circuit arrangement of the second embodiment.

[0040] **FIG. 6** is a circuit diagram showing the equivalent circuit of a solid-state image pickup element according to the third embodiment of the present invention. In the third embodiment, an arithmetic processing unit **17** is comprised of transfer gates **601** and switch MOS transistors **602**. Reference numeral **603** denotes an inverter which generates the inverted signal of a vertical scanning timing clock.

[0041] The operation of the third embodiment will be explained with reference to the timing chart of **FIG. 3**. Similar to the first embodiment, after photoelectric conversion elements are reset, accumulation operation starts. At the end of the accumulation time, a timing output V**1** from a vertical scanning circuit **16** goes high to turn on transfer gates **601-1** to **601-4**. External clocks ϕSEL, ϕRES, ϕTX**1**, and ϕTX**2** are transferred to pixels via the transfer gates **601-1** to **601-4**, and act as clocks which operate respective pixels at the same timings as those described in the first embodiment. After signals on the first and second lines are read out, the vertical scanning timing clock V**1** goes low to turn on the switch MOS transistors **602**, and the gates of vertical selection MOS transistors **3** and those of transfer MOS transistors **5** corresponding to the first and second lines are fixed to a turn-off potential. The gates of reset MOS transistors **4** are fixed to a turn-on potential.

[0042] The third embodiment also attains the same effects as those of the first and second embodiments. In addition, the third embodiment can reduce the circuit scale of the arithmetic processing unit **17** much more than the first and second embodiments. In the third embodiment, an external clock is directly transferred to the gate of a pixel transistor via the transfer gate **601**. In the first and second embodiments, the clock amplitude is uniquely determined by the power supply voltage of a logic gate. In the third embodiment, the clock amplitude can be freely changed by changing the amplitude of an input external clock. For example, the gate voltage when the transfer MOS transistor is OFF is set slightly higher than the threshold voltage of the MOS during the accumulation period. This setting enables lateral overflow draining of discharging to a power source VDD, through the transfer MOS transistor and reset MOS transistor, excessive charges generated when strong light is incident on a photoelectric conversion element **1**.

[0043] **FIG. 7** is a circuit diagram showing the equivalent circuit of a solid-state image pickup element according to the fourth embodiment of the present invention. In the fourth embodiment, a decoder circuit **701** is arranged between an external clock input portion and an arithmetic processing unit to reduce the number of externally input clocks.

[0044] **FIG. 8** is a circuit diagram showing the decoder circuit, and **FIG. 9** is a timing chart showing its operation. As shown in **FIG. 9**, an external clock ϕTX is distributed to any one of ϕTX**1** to ϕTX**4** in accordance with whether decoder clocks ϕDEC**1** and ϕDEC**2** are high or low, thereby outputting the selected clock. The output clocks ϕTX**1** to ϕTX**4** and vertical scanning timing clocks are ANDed to generate transfer clocks.

[0045] Compared to the second embodiment, the fourth embodiment can reduce the number of external clocks by one by arranging the decoder circuit **701**. In the fourth embodiment, four pixels in the Y direction form one pixel block. For example, when eight pixels form one pixel block, the second embodiment requires eight external transfer clocks, but the fourth embodiment can realize an operation similar to the above-described one by a total of four clocks, i.e., one external transfer clock and three decoder clocks.

[0046] The fourth embodiment can, therefore, obtain new effects: the number of external clocks can be reduced, the solid-state image pickup element can be easily controlled, and the area for laying out clock wires can be reduced.

[0047] The vertical scanning circuit in each of the first to fourth embodiments may be a shift register circuit or decoder circuit. The shift register circuit can reduce the circuit scale more than the decoder circuit. The decoder circuit can freely select the pixel column selection order and can realize various signal read-out orders in comparison with the shift register circuit.

[0048] As has been described above, the first to fourth embodiments can implement a solid-state image pickup element in which the peripheral circuit is downsized, resulting in low cost by downsizing and high yield, a small-size package, a small-size optical system, and a simple external control circuit.

[0049] **FIG. 10** is a schematic view showing an image pickup apparatus such as a digital camera. As shown in **FIG. 10**, image light passing through an optical system **71** and iris **80** forms an image on a CMOS sensor **72**. The optical information is converted into an electrical signal by a pixel array arranged on the CMOS sensor **72**. Noise is removed from the electrical signal, and the resultant signal is output. The output signal undergoes signal conversion processing by a signal processing circuit **73** by a predetermined method, and output. The processed signal is recorded by an information recording device or transferred via a recording and communication system **74**. The recorded or transferred signal is reproduced by a reproducing system **77**. The iris **80**, CMOS sensor **72**, and signal processing circuit **73** are controlled by a timing control circuit **75**, whereas the optical system **71**, timing control circuit **75**, recording and communication system **74**, and reproducing system **77** are controlled by a system control circuit **76**. In this case, the CMOS sensor **72** is a solid-state image pickup element described in each of the first to fourth embodiments.

[0050] Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

What is claimed is:

1. A solid-state image pickup element comprising:

a plurality of pixel blocks each having a plurality of photoelectric conversion elements, a plurality of transfer switches for transferring signals from said respective photoelectric conversion elements, and a common amplifier for receiving signals from said plurality of transfer switches; and

a scanning circuit for outputting a scanning clock for each pixel block.

2. An element according to claim 1, wherein said scanning circuit includes a shift register.

3. An element according to claim 1, wherein said scanning circuit includes a decoder.

4. An element according to claim 1, further comprising an operation processing circuit for receiving a plurality of transfer clocks corresponding to said plurality of transfer switches in said pixel block, performing operation processing for the scanning clock output from said scanning circuit and the plurality of transfer clocks, and supplying processed signals as clocks for driving said plurality of transfer switches.

5. An element according to claim 4, further comprising a decoder for converting one transfer clock input into a plurality of transfer clock inputs corresponding to said plurality of transfer switches in said pixel block and inputting the plurality of transfer clock inputs to said operation processing circuit.

6. An element according to claim 4, wherein said operation processing circuit includes an AND operation processing circuit for receiving the scanning clock and the transfer clock.

7. An element according to claim 5, wherein said operation processing circuit includes an AND operation processing circuit for receiving the scanning clock and the transfer clock.

8. An element according to claim 4, wherein said operation processing circuit includes an OR operation processing circuit for receiving the scanning clock and the transfer clock.

9. An element according to claim 5, wherein said operation processing circuit includes an OR operation processing circuit for receiving the scanning clock and the transfer clock.

10. An element according to claim 4, wherein

when said plurality of transfer switches of said pixel block are set as a plurality of first transfer switches, said operation processing circuit is formed from a plurality of second transfer switches,

the scanning clock is input to gates of said plurality of second transfer switches, and

the transfer clock inputs are supplied to said first transfer switches via said second transfer switches.

11. An element according to claim 5, wherein

when said plurality of transfer switches of said pixel blocks are set as a plurality of first transfer switches, said operation processing circuit is formed from a plurality of second transfer switches,

the scanning clock is input to gates of said plurality of second transfer switches, and

the transfer clock inputs are supplied to said first transfer switches via said second transfer switches.

12. An element according to claim 1, further comprising:

a reset switch arranged in each pixel block to reset a signal input portion; and

an operation processing circuit for receiving a reset clock input, performing arithmetic processing for the scanning clock and the reset clock input, and supplying a processed signal as a clock for driving said reset switch.

13. An element according to claim 1, further comprising:

a selection switch arranged in each pixel block to select said pixel block; and

an operation processing circuit for receiving a selection clock input, performing arithmetic processing for the scanning clock and the selection clock input, and supplying a processed signal as a clock for driving said selection switch.

14. An image pickup apparatus comprising:

said solid-state image pickup element defined in claim 1;

an optical system for forming light into an image on said solid-state image pickup element; and

a signal processing circuit for processing an output signal from said solid-state image pickup element.

* * * * *

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INGHAM, JOHN C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Interview Summary	Application No. 12/178,250	Applicant(s) MORI ET AL.	
	Examiner JOHN C. INGHAM	Art Unit 2814	

All participants (applicant, applicant's representative, PTO personnel):

(1) *JOHN C. INGHAM*. (3)_____.

(2) *RAMYAR FARID*. (4)_____.

Date of Interview: *08 December 2010*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *31,36 and 41*.

Identification of prior art discussed: *Kochi*.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *The proposed amendments overcome the Kochi reference and will require a further search. A new prior art Guidash (US 6,160,281 Fig 5B items 32, 33) was noted by the Examiner for consideration by Applicants*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

/John C Ingham/ Examiner, Art Unit 2814	/Wael M Fahmy/ Supervisory Patent Examiner, Art Unit 2814

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

———

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Case Docket Number: 60188-710 **Customer Number: 20277**

UTILITY PATENT APPLICATION
UNDER 37 CFR 1.53(b)

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Mitsuyoshi MORI, Takumi YAMAGUCHI, Takahiko MURATA
FOR: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

Enclosed are:

- ☒ 39 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☐ Certified copy of _____
- ☒ 10 sheets of formal drawing.
- ☒ An assignment of the invention to MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. and the assignment recordation fee.
- ☒ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☐ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	30	-20	10	$18.00	$180.00
Independent Claims	5	-3	2	$86.00	$172.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$770.00
				Total of Above Calculations	$1,122.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$40.00
				Total Fee	$1,162.00

☒ Please charge my Deposit Account No. 500417 in the amount of $1,162.00. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 500417 . A duplicate copy is enclosed.

☒ Any additional filing fees required under 37 CFR 1.16.

☒ The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 500417. A duplicate copy of this sheet is enclosed.

☒ Any patent application processing fees under 37 CFR 1.17.

☒ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,

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Date: November 14, 2003

SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

BACKGROUND OF THE INVENTION

The present invention relates to a solid state imaging apparatus in which a plurality of photoelectric conversion sections are arranged in an array, a method for driving the solid state imaging apparatus and a camera using the solid state imaging apparatus.

FIG. 10 is a diagram illustrating a general circuit configuration for a MOS type image sensor, i.e., a known solid imaging apparatus (e.g., see M. H. White, D. R. Lange, F. C. Blaha and I. A. Mach, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels", IEEE J. Solid-State Circuits, SC-9, pp. 1-13 (1974)).

As shown in FIG. **10**, a photoelectric conversion cell includes a photodiode (PD) section **101**, a transfer transistor **113**, a reset transistor **122**, a pixel amplifier transistor **123**, a select transistor **152**, a floating diffusion (FD) section **109**, a power supply line **131** and an output signal line **138**.

The PD section **101** of which the anode is grounded is connected to the drain of the transfer transistor **113** at the cathode. The source of the transfer transistor **113** is connected to the respective sources of the FD section **109**, the gate of the pixel amplifier transistor **123** and the source of the reset transistor **122**. The gate of the transfer transistor **113** is connected to a read-out line **134**. The reset transistor **122** which receives a reset signal **137** at the gate includes a drain connected to the drain of the pixel amplifier transistor **123** and the power supply line **131**. The source of the pixel amplifier transistor **123** is connected to the drain of the select transistor **152**. The select transistor **152** receives a selection signal SEL at the gate and includes a source connected to the output signal line **138**.

The output signal line **138** is connected to the source of a load gate **125**. The gate

of the load gate **125** is connected to a load gate line **140** thereof and the drain is connected to a source power supply line **141**.

In this configuration, a predetermined voltage is applied to the load gate line **140** so that the load gate **125** becomes a constant current source, and then the transfer transistor **113** is temporarily turned ON to transfer charge photoelectric-converted in the PD section **101** to the FD section **109**. Then, the potential of the PD section **101** is detected by the pixel amplifier transistor **123**. In this case, by turning the select transistor **152** ON, signal charge can be detected through the output signal line **138**.

However, in the known solid state apparatus, four transistors **113**, **122**, **123** and **152** and five lines **131**, **134**, **137**, **138** and **150** are required for total in each photoelectric conversion cell. Accordingly, the areas of transistor and line sections in a cell are increased. For example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm x 4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD section **101** to the photoelectric conversion cell is only about 5% Therefore, it is difficult to ensure a sufficiently large area of opening of the PD section **101** and also to reduce the size of the photoelectric conversion cell.

SUMMARY OF THE INVENTION

It is an object of the present invention to solve the above-described problems and, to reduce, in a FDA (floating diffusion amplifier) system, the size of a photoelectric conversion cell while increasing an aperture area of a photoelectric conversion section.

To achieve the above-described object, the present invention has been deviced, so that a configuration in which a transistor and an interconnect can be shared by a plurality of photoelectric conversion (PD) sections is used in a solid state imaging apparatus.

Specifically, a first solid sate imaging apparatus includes: a plurality of

photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections which are included in the same row; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. In the apparatus, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

In the first solid imaging apparatus, each said floating diffusion section is shared by ones of the photoelectric conversion sections included in the same row, and furthermore, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections. Thus, the number of read-out lines per photoelectric conversion cell becomes 0.5. As a result, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in the same column. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in the same column can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

Moreover, in the first solid state imaging apparatus, it is preferable that wherein

each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in two adjacent columns, respectively. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in two adjacent columns, respectively, can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by a row which is read out by a transfer transistor connected to one of the read-out line and another row which is adjacent to the read-out row.

It is preferable that the first solid state imaging apparatus further includes: a signal line for outputting a signal from each said pixel amplifier transistor to the outside; and a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line. Thus, charges from one of the photoelectric conversion sections which are included in adjacent rows, respectively, can be detected through a shared signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by photoelectric conversion sections which are adjacent to each other in the row direction or in the column direction. Thus, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that in each said floating diffusion section, a reset section for resetting charge stored in the floating diffusion section is provided. Thus, it is possible to stop, after charge read out from a photoelectric conversion section has been detected by an amplifier, detection of charge by the pixel

amplifier transistor.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction. Thus, a high quality image can be obtained from signals read out from the photoelectric conversion sections.

It is preferable that the first solid state imaging apparatus further includes a signal processing circuit for processing an output signal from each said pixel amplifier transistor. Thus, a high quality image can be obtained.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film. Thus, a power supply line can be formed in a different interconnect layer from an interconnect layer in which an output signal line connected to a pixel amplifier transistor is formed. Therefore, the size of a photoelectric conversion cell can be further reduced and also the aperture area can be increased.

A method for driving a solid state imaging apparatus according to the present invention is directed to a method for driving the first solid state imaging apparatus of the present invention and includes: a first step of transferring, in each said photoelectric conversion cell, by a first read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which are not included in the same row but included in two columns adjacent to each other, respectively, to one of the floating diffusion sections connected to said ones of the photoelectric conversion sections; and a second step of transferring, by a second read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which have not been read out in the first step to the same floating diffusion section connected to said ones of the photoelectric conversion sections as that in the first step.

A second solid state imaging apparatus according to the present invention includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows; a plurality of floating diffusion sections each being connected, via each of a plurality of transfer transistors, to each of ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same column in each said photoelectric conversion cell, and each being shared by said ones of the photoelectric conversion sections; a plurality of read-out lines each being connected to one of the transfer transistors and independently reading out charge from each of said ones of the photoelectric conversion sections to each said floating diffusion section shared by said ones of the photoelectric conversion sections; and a plurality of pixel amplifier transistors each detecting and outputting the potential of the floating diffusion section.

In the second solid state apparatus, each said floating diffusion section is connected to some of the plurality of transfer transistors, is shared by ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same. Furthermore, some of the plurality of read-out lines each independently reading out charge from each of said ones of the photoelectric conversion sections are connected to each said transfer transistor. Thus, a row-select transistor which is usually provided is not needed. As a result, the number of interconnects per photoelectric conversion section is reduced from 5 to 3.5. Therefore, the area of the photoelectric conversion cell itself can be reduced while increasing the area of the photoelectric sections.

It is preferable that the second solid state imaging apparatus further includes a reset transistor for resetting charge stored in each said floating diffusion section and the drain of the reset transistor is connected to the drain of the pixel amplifier transistor so that a drain

is shared by the reset transistor and the pixel amplifier transistor. Thus, an interconnect connecting between the drain of the reset transistor and the drain of the pixel amplifier transistor can be shared. Accordingly, the number of interconnects per the photoelectric conversion cell can be further reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion sections which are adjacent to each other in the row direction in each said photoelectric conversion cell. Thus, the area of floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and a gate of the MIS transistor is arranged in the column direction. Thus, each said the read-out line can be also function as an interconnect of a transfer transistor, so that the area of the read-out lines occupying the photoelectric conversion cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the area of the pixel amplifier transistor per photoelectric conversion cell can be reduced whereas the area of the photoelectric conversion sections can be increased. Therefore, light sensitivity is increased.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor and each said floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect connecting between the pixel amplifier transistor and the floating diffusion section can be shortened, so that the areas of the pixel amplifier transistor and the floating diffusion section per photoelectric conversion

cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between ones of the photoelectric cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so as to have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

Moreover, in the second solid state imaging apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and each said pixel amplifier transistor is arranged between respective gates of the MIS transistor and another MIS transistor. Thus, an empty region located in an area of the cell in which a row and a column intersect to each other can be utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the area of the reset transistors per photoelectric conversion section can be reduced. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said pixel amplifier transistor and the floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect between the floating diffusion section can be omitted and the source of the reset transistor and the floating diffusion section can be connected to each other to be

shared. Therefore, the areas of the reset transistors and the floating diffusion sections per photoelectric conversion cell can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is connected to a line arranged between ones of the photoelectric cells which are adjacent to each other in the row direction. Thus, pitches of the photoelectric sections in row directions can be matched in a simple manner, so that resolution is improved.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so as to have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

In this case, it is preferable that each said transfer transistor is made of an MIS transistor, and each said reset transistor is arranged between respective gate of the MIS transistor and another MIS transistor. Thus, an empty region located in an area of the cell in which a row and a column intersect to each other can be utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, the area of the floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain

distance in at least one of the row direction and the column direction. Thus, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that the line connecting respective drains of the reset transistor and the pixel amplifier transistor also functions as a light-shielding film. Thus, the number of interconnects per photoelectric conversion cell can be reduced. Therefore, the area of the photoelectric sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

It is preferable that each of the first and second solid state imaging apparatus further includes a signal processing circuit for processing an output signal output from each said pixel amplifier transistor. Thus, a high resolution image can be obtained.

A camera according to the present invention includes the first or second solid state imaging apparatus of the present invention. Thus, the camera of the present invention can achieve a high resolution image.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a first embodiment of the present invention.

FIG. 2 is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment.

FIG. 3 is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment.

FIG. 4 is a circuit diagram illustrating an exemplary photoelectric conversion cell

in a solid state imaging apparatus according to a second embodiment of the present invention.

FIG. 5 is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment.

FIG. 6 is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention.

FIG. 7 is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment.

FIG. 8 is a plane view schematically illustrating a layout of the photoelectric conversion cell in the solid state imaging apparatus of the third embodiment.

FIG. 9 is a table showing the aperture ratio of PD sections to a photoelectric conversion cell in each of regions A through E of FIG. 8 where a transistor and the like are arranged.

FIG. 10 is a circuit diagram illustrating a photoelectric conversion cell in a known solid imaging apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

A first embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. 1 is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to the first embodiment of the present invention.

As shown in FIG. 1, for example, photoelectric conversion (PD) sections 1, 2, 3

and 4 each of which is made of a photodiode and converts incident light to electric energy are arranged in this order in the row direction. Furthermore, PD sections 5, 6, 7 and 8 are arranged in this order in the row direction so that the PD sections 5, 6, 7 and 8 are adjacent to the PD sections 1, 2, 3 and 4, respectively, in the column direction.

Here, in this application, the row direction means to be the direction in which a row number increases and the column direction means to be the direction in which a column number increases.

Between the first and 0^{th} rows (not shown), a first floating diffusion (FD) section 9 for storing photoelectric-converted charges from the PD sections 1 and 5 included in the first row and PD sections included in the 0^{th} row is provided. Between the second and third rows, a second floating diffusion section 10 for storing photoelectric-converted charges from the PD sections 2 and 6 included in the second row and the PD sections 3 and 7 included in the third row is provided so as to be surrounded by the PD sections 2, 3, 6 and 7. Between the fourth and fifth rows (not shown), a third floating diffusion section 11 for storing photoelectric-converted charges from the PD sections 4 and 8 included in the fourth row and PD sections included in the fifth row is provided. In this manner, each of the FD sections 9, 10 and 11 is shared by four PD sections.

In this case, a cell including the PD sections 1, 2, 5 and 6 is a first photoelectric conversion cell 91 and a cell including the PD sections 3, 4, 7 and 8 is a second photoelectric conversion cell 92.

In the first photoelectric conversion cell 91, a transfer transistor 13 made of an N channel FET for transferring charge from the PD section 1 to the first FD section 9 is connected between the PD section 1 included in the first row and the first FD section 9, and a transfer transistor 17 made of an N channel FET for transferring charge from the PD section 5 to the first FD section 9 is connected between the PD section 5 and the first FD

section 9.

Moreover, in the first photoelectric conversion cell **91**, a transfer transistor **14** made of an N channel FET for transferring charges from the PD section **2** to the second FD section **10** is connected between the PD section **2** included in the second row and the second FD section **10**, and a transfer transistor **18** made of an N channel FET for transferring charges from the PD section **6** to the second FD section **10** is connected between the PD section **6** and the second FD section **10**.

As a characteristic of the first embodiment, the transfer transistor **13** included in the first row and the transfer transistor **14** included in the second row are connected to a first read-out (READ) line **32** while the transfer transistor **17** included in the first row and the transfer transistor **18** included in the second row are connected to a second READ line **33**.

In the second photoelectric conversion cell **92**, a transfer transistor **15** made of an N channel FET for transferring charge from the PD section **3** to the second FD section **10** is connected between the PD section **3** included in the third row and the second FD section **10**, and a transfer transistor **19** made of an N channel FET for transferring charge from the PD section **7** to the second FD section **10** is connected between the PD section **7** and the second FD section **10**.

Moreover, in the second photoelectric conversion cell **92**, a transfer transistor **16** made of an N channel FET for transferring charges from the PD section **4** to the third FD section **11** is connected between the PD section **4** included in the fourth row and the third FD section **11**, and a transfer transistor **20** made of an N channel FET for transferring charges from the PD section **8** to the third FD section **11** is connected between the PD section **8** and the third FD section **11**.

Also, in this cell, the transfer transistor **15** included in the third row and the transfer transistor **16** included in the fourth row are connected to the third READ line **34** while the

transfer transistor 19 included in the third row and the transfer transistor 20 are connected to the fourth READ line 35.

To the first FD section 9, a first reset transistor 21 made of an N channel FET is connected. The first reset transistor 21 includes a source connected to the first FD section 9, a drain connected to a photoelectric conversion cell power supply (VDDCELL) line 31 and a gate connected to a first reset pulse (RSCELL) line 36. Thus, charge stored in the first FD section 9 is made to flow through the VDDCELL line 31 by a RSCELL signal.

In the same manner, a second reset transistor 22 made of an N channel FET is connected to the second FD section 10. The second reset transistor 22 includes a source connected to the second FD section 10, a drain connected to the VDDCELL line 31 and a gate connected to a second RSCELL line 37. Note that although not shown in FIG. 1, a reset transistor of the same configuration as that of the first reset transistor 21 or the like is provided in the third FD section 11.

To the first FD section 9 and the first reset transistor 21, a first pixel amplifier transistor 23 made of an N channel FET is connected. The first pixel amplifier transistor 23 includes a gate connected to the first FD section 9, a drain connected to the VDDCELL line 31 and a source connected to a first output signal (VO) line 38.

In the same manner, a second pixel amplifier transistor 24 made of an N channel FET is connected to the second FD section 10 and the second reset transistor 22. The second pixel amplifier transistor 24 includes a gate connected to the second FD section 10, a drain connected to the VDDCELL line 31 and a source connected to a second VO line 39.

The first VO line 38 and the second VO line 39 are connected to not only the pixel amplifier transistors 23 and 24, respectively, but also first and second load transistors 25 and 26, respectively. Each of the first and second load transistor 25 and 26 is made of an N channel for constituting a source follower amplifier. A load gate (LGCELL) line 40 is

connected to each of the gates of the first and second load transistors **25** and **26**. A source power supply (SCLL) line **41** is connected to each of the respective drains of first and second load transistors **25** and **26**.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **2** is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment. In this case, a series of operations is completed in a horizontal blanking period (= 1 H).

Moreover, as for the detection order of signal charges from the PD sections **1** through **8** arranged in an array, detection is simultaneously carried out in the first and second rows and then detection is simultaneously carried out in the third and fourth rows.

As shown in FIG. **2**, first, high level voltage is applied to the LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source, and then during a period in which the potential of the VDDCELL line **31** is high level, each of the RSCELL lines **36** and **37** is set to be a high level in a pulse state to temporarily turn each of the reset transistors **21** and **22** ON. Thus, each of charges stored in the first FD section **9** in the first photoelectric conversion cell **91** and in the second FD section **10** in the second photoelectric conversion cell **92** is made to flow through the VDDCELL line **31**. In this case, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is

transferred to the first FD section **9** while charge stored in the PD section **2** is transferred to the second FD section **10**. For charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

Subsequently, when the VDDCELL line **31** is turned to be in a low level OFF state and each of the RSCELL lines **36** and **37** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **10** becomes in the same OFF level state as that of the VDDCELL line **31**. Thus, each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **24** is not operated and thus the vertical line scanning circuit is in a non-select state.

In a subsequent horizontal blanking period **2H**, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at a reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn

transfer transistors 17 and 18 ON. Thus, charge stored in the PD section 5 in the first row is transferred to the first FD section 9 while charge stored in the PD section 6 in the second row is transferred to the second FD section 10.

Thereafter, in the same manner as in the first horizontal blanking period 1H, for respective charges transferred to the first FD section 9 and the second FD section 10, voltage levels of stored signals are detected in the first pixel amplifier transistor 23 and the second pixel amplifier transistor 24, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line 38 and the second VO line 39, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors 23 and 24 can be detected.

In this manner, charges detected during the first horizontal blanking period 1H and charges detected during the second horizontal blanking period 2H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges.

Subsequently, by driving the PD sections in the third and fourth rows in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

Note that in the first embodiment, the circuit configuration and driving method in which after every second column, i.e., every odd-numbered column including the PD sections 1 and 2 have been read out, charges in every even-numbered column including the PD sections 5 and 6 are detected have been described. However, this embodiment is not limited thereto but READ lines can be increased to detect charge in every third column at

the same timing as described above.

In the solid state imaging apparatus of the first embodiment, as shown in the circuit configuration of FIG. 1, for example, four PD sections share a FD section, a pixel amplifier transistor and a reset transistor. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 1.5. The number of interconnects can be reduced from 5 (required in the known solid state imaging apparatus) to 2.5. For example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm x 4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections to the photoelectric conversion cell is about 35%. Therefore, it is possible to reduce the cell sizes of the photoelectric conversion cells **91** and **92** and to largely increase the aperture ratio of the PD section at the same time.

In this connection, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are detected by a READ line at the same timing is applied to the known circuit configuration. If a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm x 4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 10%.

Moreover, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are read out by a READ line, and a FD section and a pixel amplifier transistor included in a row which adjacent to an unread row in a photoelectric conversion cell are shared by two photoelectric sections to detect signal charge is applied to the known circuit configuration. With a driving method in which signal charges are simultaneously detected in the two photoelectric conversion sections, for example, if a photoelectric conversion cell is designed, assuming that the area

of a photoelectric conversion cell is 4.1 μm x 4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 15%.

(Modified Example of First Embodiment)

FIG. 3 is a diagram illustrating a circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment of the present invention. Also, in this modified example, each member also shown in FIG. 1 is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. 3, for example, in the first photoelectric conversion cell 91, the first READ line 32 is connected to the transfer transistor 13 and the transfer transistor 18 included in adjacent columns, respectively, while the second READ line 33 is connected to the transfer transistor 14 and the transfer transistor 17 included in adjacent columns, respectively. Thus, even if connections are made with respect to the PD sections 1, 2, 5 and 6 included in two adjacent rows with the first and second READ lines 32 and 33 interposed between the PD sections 1 and 5 and the PD sections 2 and 6 so that signal charges from the PD sections which are not included in the same columns are transferred, charge can be detected at the same timing as that shown in FIG. 2.

For example, when the first READ line 32 is temporarily turned ON, signal charge is transferred from the PD section 1 to the first FD section 9 via the transfer transistor 13 and, at the same time, signal charge is transferred from the PD section 6 to the second FD section 10 via the transfer transistor 18.

Note that in the modified example of the first embodiment, signal charges from two of the four PD sections included in a photoelectric conversion cell 91 are read out during the horizontal blanking period 1H. However, instead of this, signal charges from all of the

four PD sections may be read out.

Moreover, by performing signal processing to signal charges from all of the photoelectric conversion cells which have been read out during different horizontal blanking periods, a high quality image with a large number of pixels can be obtained.

(Second Embodiment)

Hereinafter, a second embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **4** is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a second embodiment of the present invention. In FIG. **4**, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

First, differences of the solid state imaging apparatus of FIG. **4** from that of the first embodiment shown in FIG. **1** will be described.

In the second embodiment, an configuration in which the first and second pixel amplifier transistors **23** and **24** are connected to the first and second output signal (VO) lines **38** and **39**, respectively, via the first and second select transistors **52** and **53** each of which made of an N channel FET, respectively, is used.

To the respective gates of the first and second select transistors **52** and **53**, first and second select (SO) lines **50** and **51** to which a switching pulse is applied are connected, respectively.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **5** is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment. In this case, a series of operations is completed in a

horizontal blanking period (= 1 H).

As shown in FIG. 5, first, a predetermined voltage is applied to the LGCELL line 40 so that each of the load transistors 25 and 26 becomes a constant current source and the potential of the VDDCELL line 31 is set to be a high level. Subsequently, each of the RSCELL lines 36 and 37 is set to be a high level in a pulse state to temporarily turn each of the reset transistors 21 and 22 ON. Thus, each of charges stored in the first FD section 9 and in the second FD section 10 is made to flow through the VDDCELL line 31. In this case, in each of the pixel amplifier transistors 23 and 24, each of the select transistors 52 and 53 has been turned ON in advance, so that a signal level at a reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines 38 and 39. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor 21 and 22 has been turned OFF, high level voltage is applied in an pulse state to the first READ line 32 to simultaneously turn transfer transistors 13 and 14 ON. Thus, charge stored in the PD section 1 in the first row is transferred to the first FD section 9 while charge stored in the PD section 2 is transferred to the second FD section 10. Thereafter, for charges transferred to the first FD section 9 and the second FD section 10, voltage levels of stored signals are detected in the first pixel amplifier transistor 23 and the second pixel amplifier transistor 24, respectively.

Subsequently, by changing each of the first and second SO lines 50 and 51 to a high level to keep the first and second transistors 52 and 53 ON, stored charge signals of the first pixel amplifier transistor 23 and the second pixel amplifier transistor 24 are introduced to the noise cancellation circuit via the first VO line 38 and the second VO line 39, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit.

Thereafter, each of the first and second SO lines **50** and **51** is set back to be a low level to turn the first and second select transistors **52** and **53** OFF, so that each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** is selected, each of the pixel amplifier transistors **23** and **24** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2H**, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of the FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **17** and **18** ON. Thus, charge stored in the PD section **5** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the second FD section **10**.

Thereafter, in the same manner as in the first horizontal blanking period **1H**, for respective charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the stored signals whose voltage level have been detected selectively conducts the first and second VO lines **38** and **39** and are introduced to the noise cancellation circuit. Then, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and

which are held by the pixel amplifier transistors **23** and **24** can be detected.

Thus, with the first and second select transistors **52** and **53** between the FD section **9** and the first VO line **38** and between the FD section **10** and the second VO line **39**, respectively. Thus, the number of transistors per photoelectric conversion cell is 1.75. Moreover, the number of interconnects is 2.75. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells **91** and **92** and also to largely improve the aperture ratio of PD sections.

Note that also in the second embodiment, as in the modified example of the first embodiment, for example, a configuration in which the transfer transistor **13** and the transfer transistor **18** located diagonally to the transfer transistor **13** are connected to the first READ line **32**, and the transfer transistor **14** and the transfer transistor **17** located diagonally to the transfer transistor **14** are connected to the second READ line **33** may be used.

Moreover, in the photoelectric conversion cell **91**, the PD sections are arranged in two rows and two columns. However, the present invention is not limited thereto, but the PD sections may be arranged in two rows and three columns and, furthermore, may be arranged in three or more rows and three or more columns.

(Third Embodiment)

Hereinafter, a third embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. 6 is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention. In FIG. 6, each member also shown in FIG. 1 is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. **6**, in the solid state imaging apparatus of the third embodiment, first through fourth photoelectric conversion cells **91**, **92**, **93** and **94** are arranged in a matrix.

For example, the first photoelectric conversion cell **91** includes photoelectric conversion (PD) sections **1** and **2** arranged in regions which is located in the first column of an array and the first row and which is located in the first column of and the second rows of the array, respectively. The PD sections **1** and **2** share a first FD section **9** via transfer transistors **13** and **14** each of which is made of an N channel FET, respectively.

To the first FD section **9**, the first reset transistor **21** made of an N channel FET is connected. The first reset transistor **21** includes a source connected to the first FD section **9**, a drain connected to the first FD section **9** and a gate connected to a first RSCELL line **36**. Thus, charge stored in the first FD section **9** is made to flow through a first VDDCELL line **30** by a RSCELL signal.

To the first FD section **9** and the first reset transistor **21**, a first pixel amplifier transistor **23** of an N channel FET is connected. The first pixel amplifier transistor made of an N channel FET includes a gate connected to the first FD section **9**, a drain connected to the first VDDCELL line **30** and a source connected to a first VO line **38**.

In the same manner, PD sections **3** and **4** arranged in regions of an array forming a second photoelectric conversion cell **92** which is located in the first column and the third row and which is located in the first column and the fourth row, respectively, share a second FD section **10** via transfer transistors **15** and **16**, respectively. A second reset transistor **22** selectively conducts the second FD section **10** and the first VDDCELL line **30**. Moreover, a second pixel amplifier transistor **24** which receives the signal potential of the second FD section **10** at the gate and receives the power supply potential of the first VDDCELL line **30** at the drain outputs a detected signal corresponding to a received signal

potential to the first VO line **38**.

PD sections **5** and **6** arranged in regions of an array forming a third photoelectric conversion cell **93** which is located in the second column and the first row and which is located in the second column and the second row, respectively, share a third FD section **11** via transfer transistors **17** and **18**, respectively. A third reset transistor **61** selectively conducts the third FD section **11** and a second VDDCELL line **31**. Moreover, a third pixel amplifier transistor **63** which receives the signal potential of the third FD section **11** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs a detected signal corresponding to a received signal potential to a second VO line **39**.

PD sections **7** and **8** arranged in regions of an array forming a fourth photoelectric conversion cell **94** which is located in the second column and the third row and which is located in the second column and the fourth row, respectively, share a fourth FD section **12** via transfer transistors **19** and **20**, respectively. A fourth reset transistor **62** selectively conducts the fourth FD section **12** and a second VDDCELL line **31**. Moreover, a fourth pixel amplifier transistor **64** which receives the signal potential of the fourth FD section **12** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs a detected signal corresponding to a received signal potential to a second VO line **39**.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **7** is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment. In this case, a series of operations is completed in a horizontal blanking period (= 1 H).

Moreover, as for the detection order of signal charges from the PD sections 1

through 8 arranged in an array, detection is carried out sequentially from the first row to the second row and so on.

As shown in FIG. 7, first, high level voltage is applied to a LGCELL line 40 so that each of the load transistors 25 and 26 becomes a constant current source, and then during a period in which the potentials of the first VDDCELL line 30 and the VDDCELL line 31 are set to be high level, the first RSCELL lines 36 is set to be high level in a pulse state to temporarily turn each of the reset transistors 21 and 61 ON. Thus, charges stored in the first FD section 9 in the first photoelectric conversion cell 91 and in the third FD section 11 in the third photoelectric conversion cell 93 are made to flow through the first VDDCELL line 30 and the VDDCELL line 31, respectively. In this case, in each of the pixel amplifier transistors 23 and 63, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines 38 and 39. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor 21 and 61 has been turned OFF, high level voltage is applied in an pulse state to the first READ line 32 to simultaneously turn transfer transistors 13 and 14 ON. Thus, charge stored in the PD section 1 in the first row is transferred to the first FD section 9 while charge stored in the PD section 5 in the second row is transferred to the third FD section 11. For charges transferred to the first FD section 9 and the third FD section 11, voltage levels of stored signals are detected in the first pixel amplifier transistor 23 and the third pixel amplifier transistor 63, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line 38 and the second VO line 39, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors 23 and 63 can be detected.

Subsequently, when each of the VDDCELL lines **30** and **31** is turned to be in a low level OFF state and the first RSCELL line **36** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **11** becomes in the same OFF level state as that of each of the VDDCELL lines **30** and **31**. Then, each of the pixel amplifier transistors **23** and **63** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL line **36** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **63** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2H**, each of the reset transistors **21** and **61** is temporarily turned ON to reset charges of the FD sections **9** and **11**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **63**, a signal level at the reset time is detected, detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **61** has bee turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **14** and **18** ON. Thus, charge stored in the PD section **2** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the third FD section **11**.

Thereafter, in the same manner as in the first horizontal blanking period **1H**, for respective charges transferred to the first FD section **9** and the third FD section **11**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the third pixel amplifier transistor **63**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise

cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors 23 and 63 can be detected

In this manner, charges detected during the first horizontal blanking period 1H and charges detected during the second horizontal blanking period 2H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges. Thus, in the third embodiment, for example, the power supply potentials which are to be applied to the respective drains of the first reset transistor 21 and the first pixel amplifier transistor 23 vary in the same manner. Therefore, the known row selection transistor 152 is not necessarily provided.

Subsequently, if the PD sections in the third and fourth rows are driven in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

As has been described, the solid state imaging apparatus of the third embodiment has, for example, a configuration in which the two PD sections 1 and 2 share the first FD section 9, the first pixel amplifier transistor 23 and the first reset transistor 21. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 2. Moreover, the number of interconnects can be reduced from 5 (required in the known apparatus) to 3.5. Accordingly, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm x 4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD sections 1 and 2 is about 30%. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells and also to largely improve the aperture ratio of the PD section.

Note that each of the reset transistors **21**, **22**, **61** and **62** is made of an N channel type MOS transistor. However, in each of the reset transistors **21**, **22**, **61** and **62** made of, instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second RSCELL lines **36** and **37**, each of the reset transistors **21**, **22**, **61** and **62** is turned ON.

In the same manner, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is made of an N channel type MOS transistor. However, in each of the pixel amplifier transistors **23**, **24**, **63** and **64** made of, instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second VDDVELL lines **30** and **31**, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is turned ON to be in a potential detection period in which signal potentials from the corresponding FD sections **9**, **10**, **11** and **12** are detected.

Hereinafter, in the layout in which each of the PD sections **1**, **2**, **3**, **5**, **6** and **7** arranged as shown in FIG. **8**, a region of the cell located between the PD sections **1** and **2** is referred to as an "A region"; a region of the cell surrounded by the PD sections **1**, **2**, **5** and **6** is referred to as a "B region"; a region of the cell located between the PD sections **5** and **6** is referred to as a "C region"; a region of the cell located between the PD sections **2** and **6** is referred to as a "D region"; and a region of the cell located between the PD sections **1** and **5** is referred to as an "E region". Then, by arranging the FD sections **9** and **11**, the pixel amplifier transistors **23** and **63**, and the reset transistors **21** and **61** in regions in the cell indicated in the FIG. **9**, respectively, the aperture ratio of the PD sections to the photoelectric conversion cell can be improved in any case, compared to the known solid state imaging apparatus. Moreover, the size of the cell can be reduced.

Furthermore, as also shown in FIG. **9**, if the FD sections **9** and **11** are arranged in the A and C regions, respectively, the aperture of the PD sections can be improved to be

about 30% by arranging in parallel the READ lines **32** and **33** for driving the transfer transistors **13** and **14**, respectively.

Moreover, as shown in FIG. **9**, for example, the aperture of the PD sections can be improved to be about 30% by arranging the first RSCELL line **36** between the PD sections **2** and **3**.

Moreover, as shown in FIG. **8**, by arranging the PD sections so as to be spaced apart from one another by a certain distance at least in one of the row direction and the column direction, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

Moreover, although not shown in the drawings, by using the first VDDCELL line **30** and the second VDDCELL line **31** as light-shielding films for separating the photoelectric conversion cells from one another, the first VO line **38** and the second VO line **39** can be formed in different interconnect layers. Thus, the sizes of the photoelectric conversion cells **91** and **92** can be reduced and also the aperture area of the PD sections can be increased.

Moreover, with the solid state imaging apparatus of any one of the first through third embodiments, a camera which is small-sized and provides a high resolution image can be obtained.

WHAT IS CLAIMED IS:

1. A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns;

a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections which are included in the same row;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section

wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

2. The solid state imaging apparatus of claim 1, wherein each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in the same column.

3. The solid state imaging apparatus of claim 1, wherein each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in two adjacent columns, respectively.

4. The solid state imaging apparatus of claim 1, wherein each said floating

diffusion section and each said pixel amplifier transistor are shared by a row which is read out by a transfer transistor connected to one of the read-out line and another row which is adjacent to the read-out row.

5. The solid state imaging apparatus of claim 1, further comprising:

a signal line for outputting a signal from each said pixel amplifier transistor to the outside; and

a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line.

6. The solid state imaging apparatus of claim 1, wherein each said floating diffusion section and each said pixel amplifier transistor are shared by photoelectric conversion sections which are adjacent to each other in the row direction or in the column direction.

7. The solid state imaging apparatus of claim 1, wherein in each said floating diffusion section, a reset section for resetting charge stored in the floating diffusion section.

8. The solid state imaging apparatus of claim 1, wherein the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction.

9. The solid state imaging apparatus of claim 1, further comprising a signal processing circuit for processing an output signal from each said pixel amplifier transistor.

10. The solid state imaging apparatus of claim 1, wherein the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film.

11. A method for driving a solid state imaging apparatus which includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections which are included in the same row; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section, in which respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections and each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in the same column, respectively, the method comprising the steps of:

a first step of transferring, in each said photoelectric conversion cell, by a first read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which are not included in the same row but included in two columns adjacent to each other, respectively, to one of the floating diffusion sections connected to said ones of the photoelectric conversion sections; and

a second step of transferring, by a second read-out line of the read-out lines, signal

charges from ones of the photoelectric conversion sections which have not been read out in the first step to the same floating diffusion section connected to said ones of the photoelectric conversion sections as that in the first step.

12. A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows;

a plurality of floating diffusion sections each being connected, via each of a plurality of transfer transistors, to each of ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same column in each said photoelectric conversion cell, and each being shared by said ones of the photoelectric conversion sections;

a plurality of read-out lines each being connected to one of the transfer transistors and independently reading out charge from each of said ones of the photoelectric conversion sections to each said floating diffusion section shared by said ones of the photoelectric conversion sections; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of the floating diffusion section.

13. The solid state imaging apparatus of claim 12, further comprising a reset transistor for resetting charge stored in each said floating diffusion section

wherein the drain of the reset transistor is connected to the drain of the pixel amplifier transistor so that a drain is shared by the reset transistor and the pixel amplifier transistor.

14. The solid state imaging apparatus of claim 12, wherein each said floating diffusion section is arranged between ones of the photoelectric conversion sections which are adjacent to each other in the row direction in each said photoelectric conversion cell.

15. The solid state imaging apparatus of claim 12, wherein each said transfer transistor is made of an MIS transistor, and

wherein a gate of the MIS transistor is arranged in the row direction.

16. The solid state imaging apparatus of claim 12, wherein each said pixel amplifier transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell.

17. The solid state imaging apparatus of claim 12, wherein each said pixel amplifier transistor and each said floating diffusion section are arranged between adjacent ones of the read out lines.

18. The solid state imaging apparatus of claim 12, wherein each said pixel amplifier transistor is arranged between ones of the photoelectric cells which are adjacent to each other in the column direction.

19. The solid state imaging apparatus of claim 18, wherein each said transfer transistor is made of an MIS transistor, and

wherein each said pixel amplifier transistor is arranged between respective gates of the MIS transistor and another MIS transistor.

20. The solid state imaging apparatus of claim 13, wherein each said reset transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell.

21. The solid state imaging apparatus of claim 13, wherein each said pixel amplifier transistor and the floating diffusion section are arranged between adjacent ones of the read out lines.

22. The solid state imaging apparatus of claim 13, wherein each said reset transistor is connected to a line arranged between ones of the photoelectric cells which are adjacent to each other in the row direction.

23. The solid state imaging apparatus of claim 13, wherein each said reset transistor is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction.

24. The solid state imaging apparatus of claim 23, wherein each said transfer transistor is made of an MIS transistor, and

wherein each said reset transistor is arranged between respective gate of the MIS transistor and another MIS transistor.

25. The solid state imaging apparatus of claim 12, wherein each said floating diffusion section is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction.

26. The solid state imaging apparatus of claim 12, wherein the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in at least one of the row direction and the column direction.

27. The solid state imaging apparatus of claim 13, wherein the line connecting respective drains of the reset transistor and the pixel amplifier transistor also functions as a light-shielding film.

28. The solid state imaging apparatus of claim 12, further comprising a signal processing circuit for processing an output signal output from each said pixel amplifier transistor.

29. A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns;

a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections which are included in the same row;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section,

wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read

out by different floating diffusion sections.

30. A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows;

a plurality of floating diffusion sections, each being connected, via each of a plurality of transfer transistors, to each of ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same column in each said photoelectric conversion cell, and each being shared by said ones of the photoelectric conversion sections;

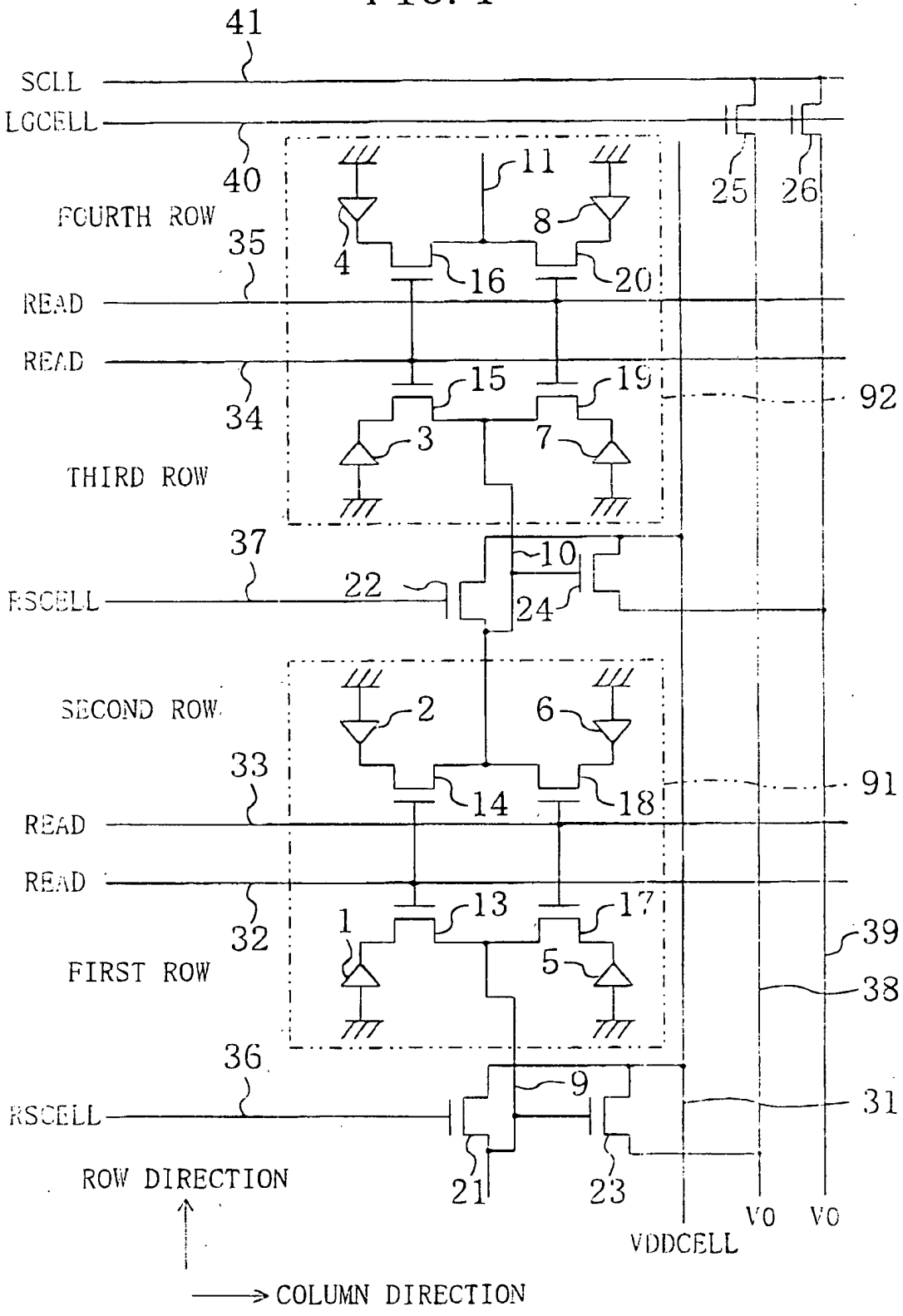
a plurality of read-out lines each being connected to one of the transfer transistors and independently reading out charge from each of said ones of the photoelectric conversion sections to each said floating diffusion section shared by said ones of the photoelectric conversion sections; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of the floating diffusion section.

ABSTRACT OF THE DISCLOSURE

A solid state imaging apparatus includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. Charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

FIG. 1


41
SCLL
LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
33
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
2
6
14
18
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17
1
5
39
38
9
31
21
23
VO
VO
VDDCELL

FIG. 2

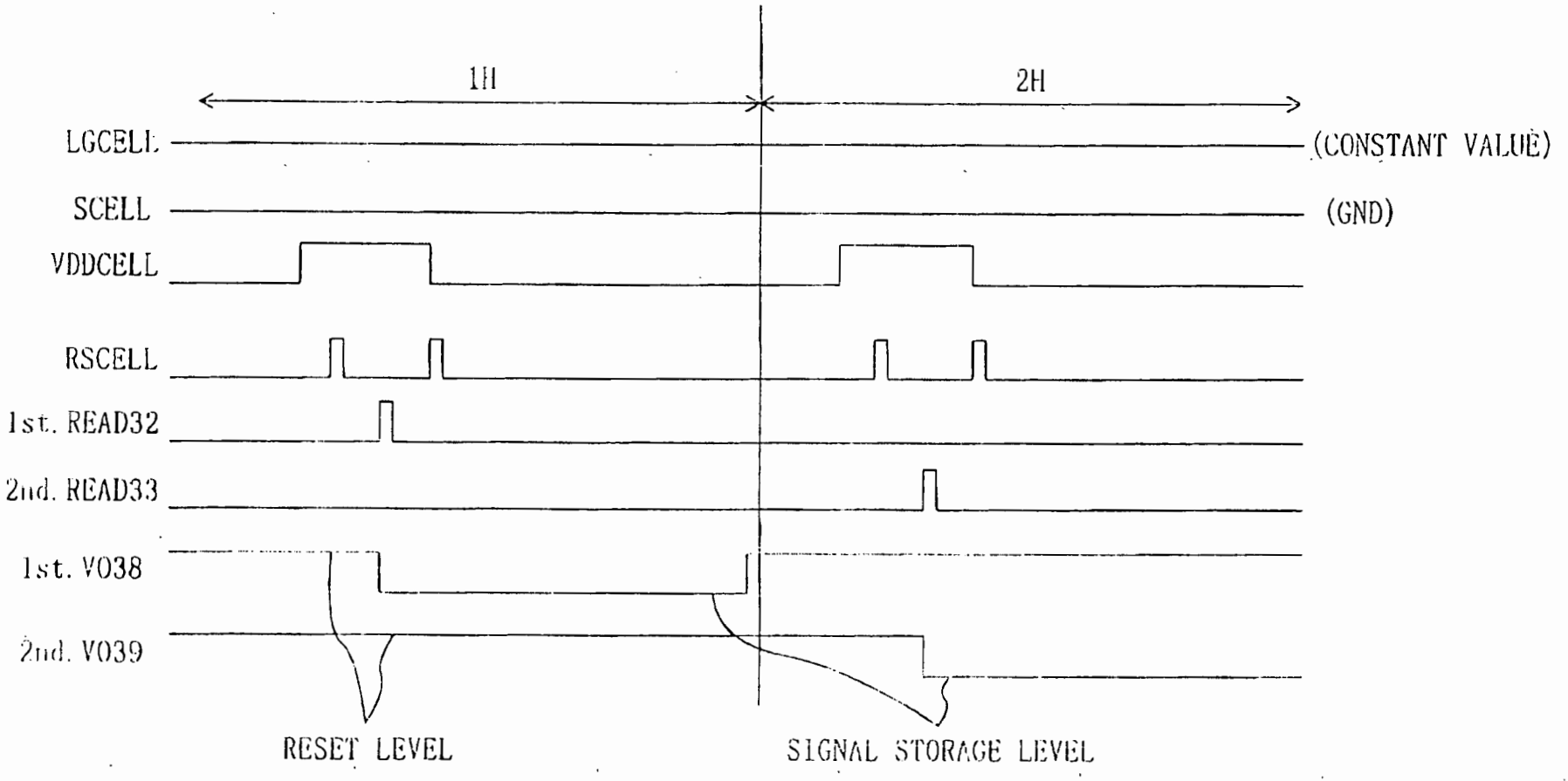
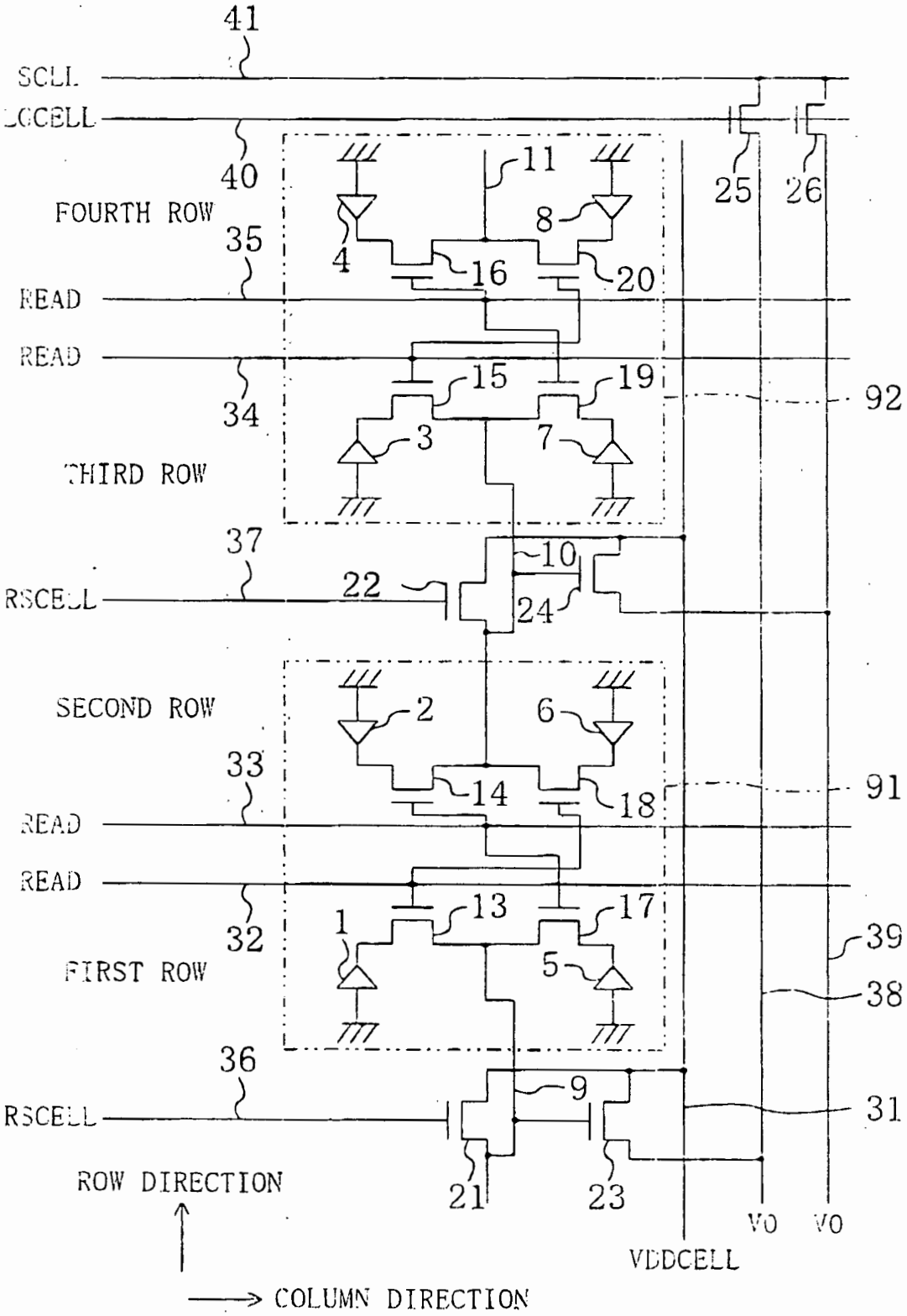

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
RSCELL
1st. READ32
2nd. READ33
1st. VO38
2nd. VO39
RESET LEVEL
SIGNAL STORAGE LEVEL

FIG. 3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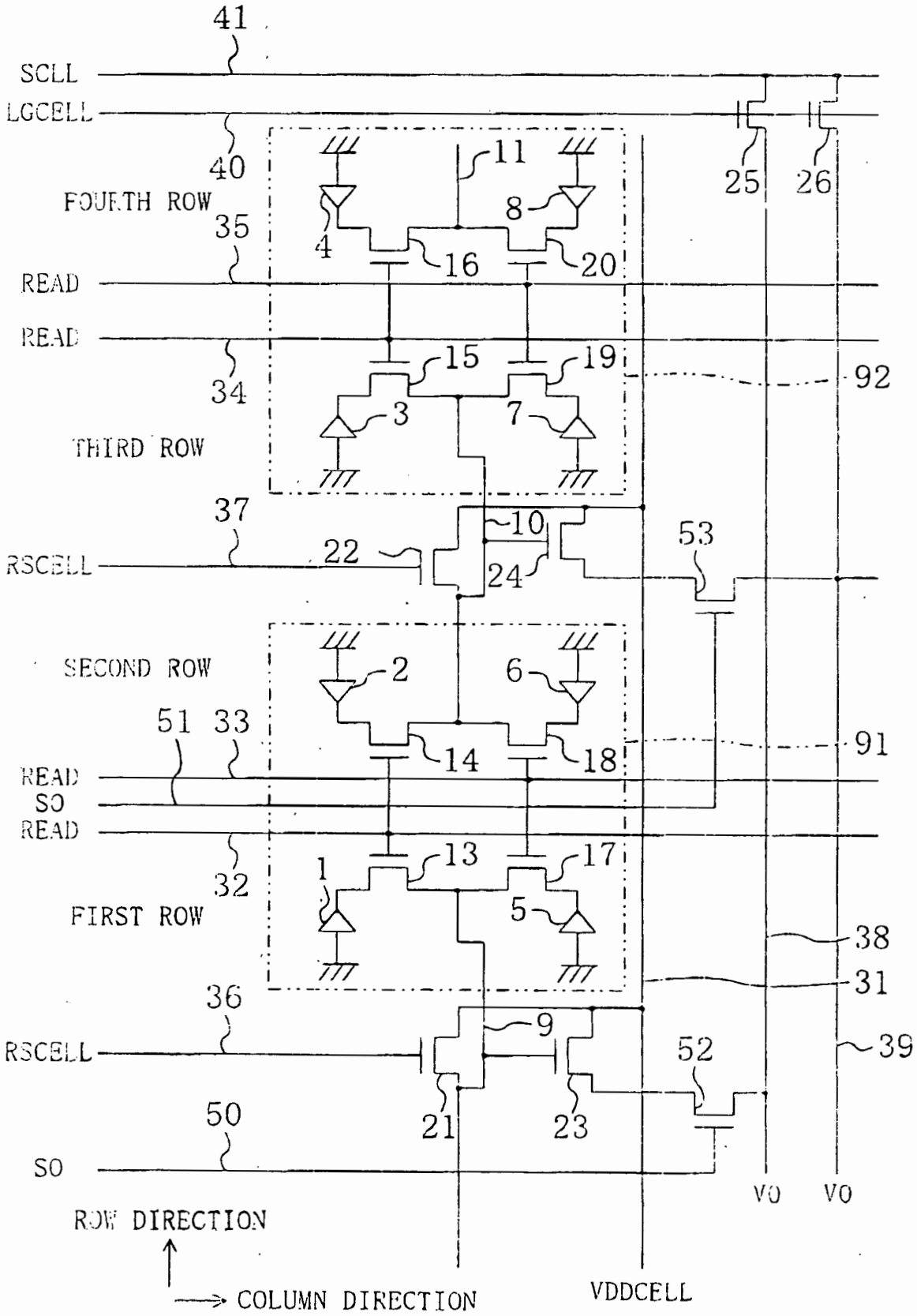
LCCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
33
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
2
6
14
18
91
13
17
1
5
39
38
9
31
21
23
VO
VO
VDDCELL

FIG. 4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SCLL
LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
51
33
READ
SO
READ
32
FIRST ROW
36
RSCELL
50
SO
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
53
2
6
14
18
91
13
17
1
5
38
31
9
52
39
21
23
VO
VO
VDDCELL

FIG. 5

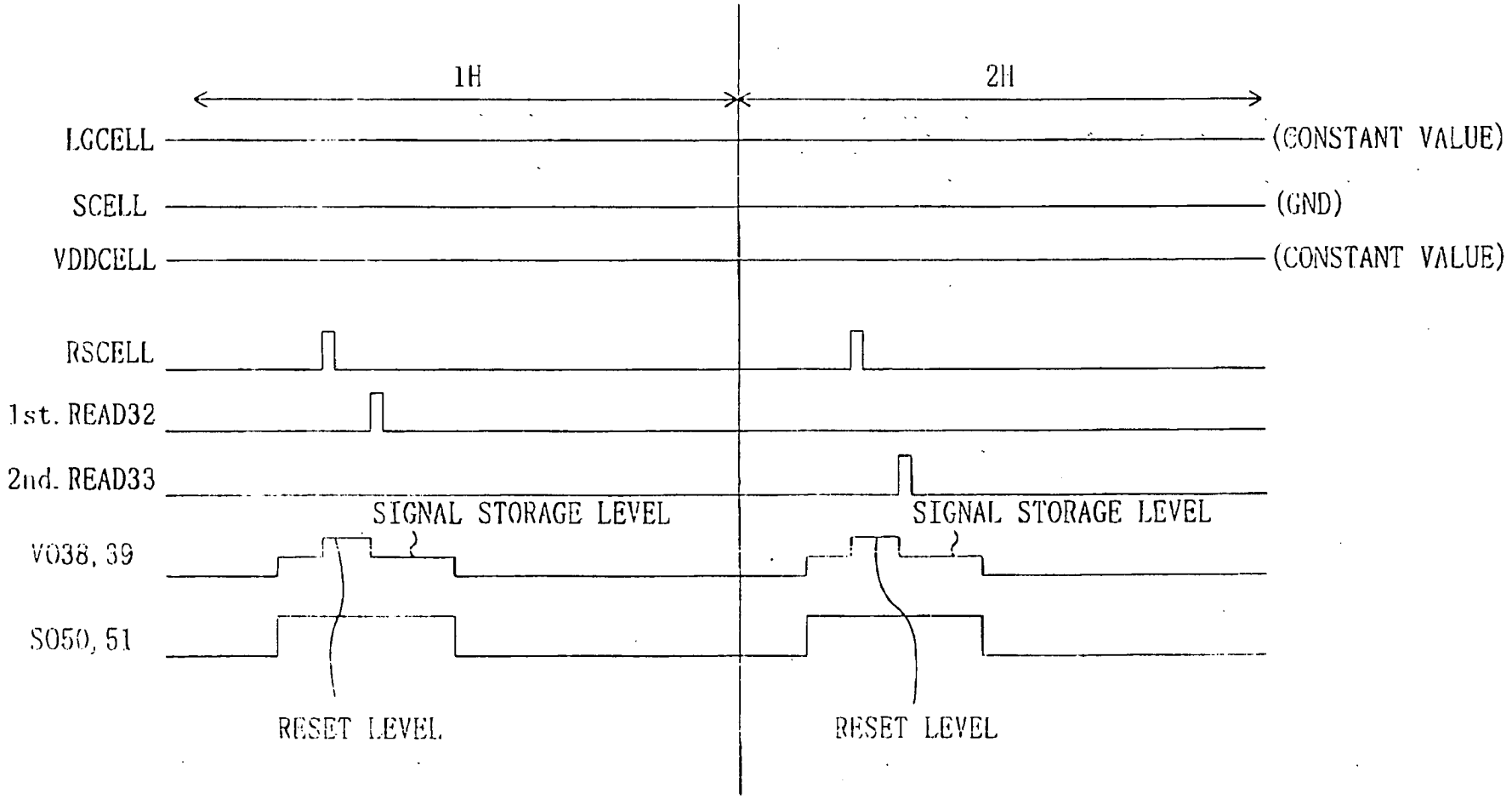
1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
(CONSTANT VALUE)
RSCELL
1st. READ32
2nd. READ33
SIGNAL STORAGE LEVEL
SIGNAL STORAGE LEVEL
V038, 39
S050, 51
RESET LEVEL
RESET LEVEL

FIG. 6

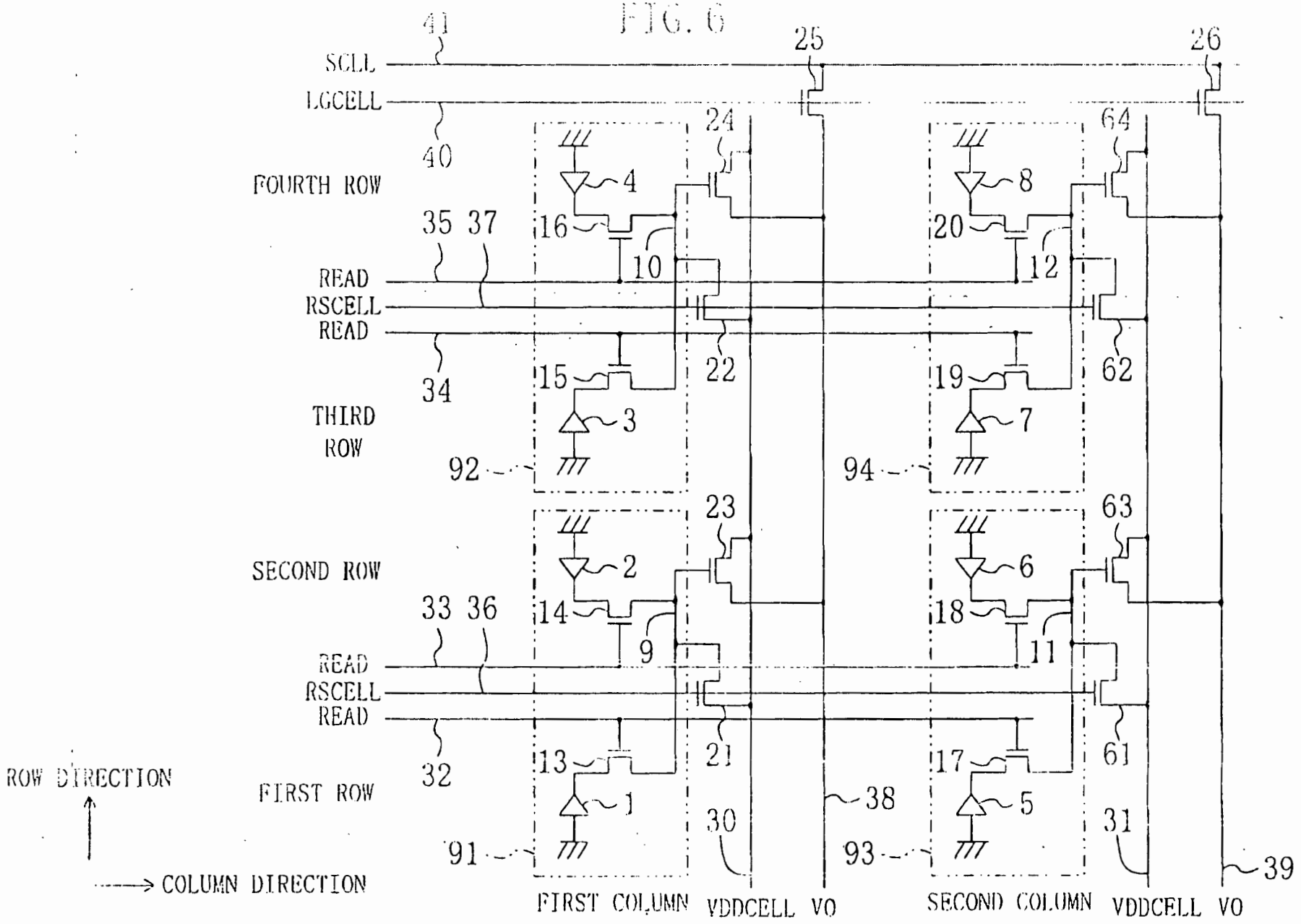

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FIG. 7

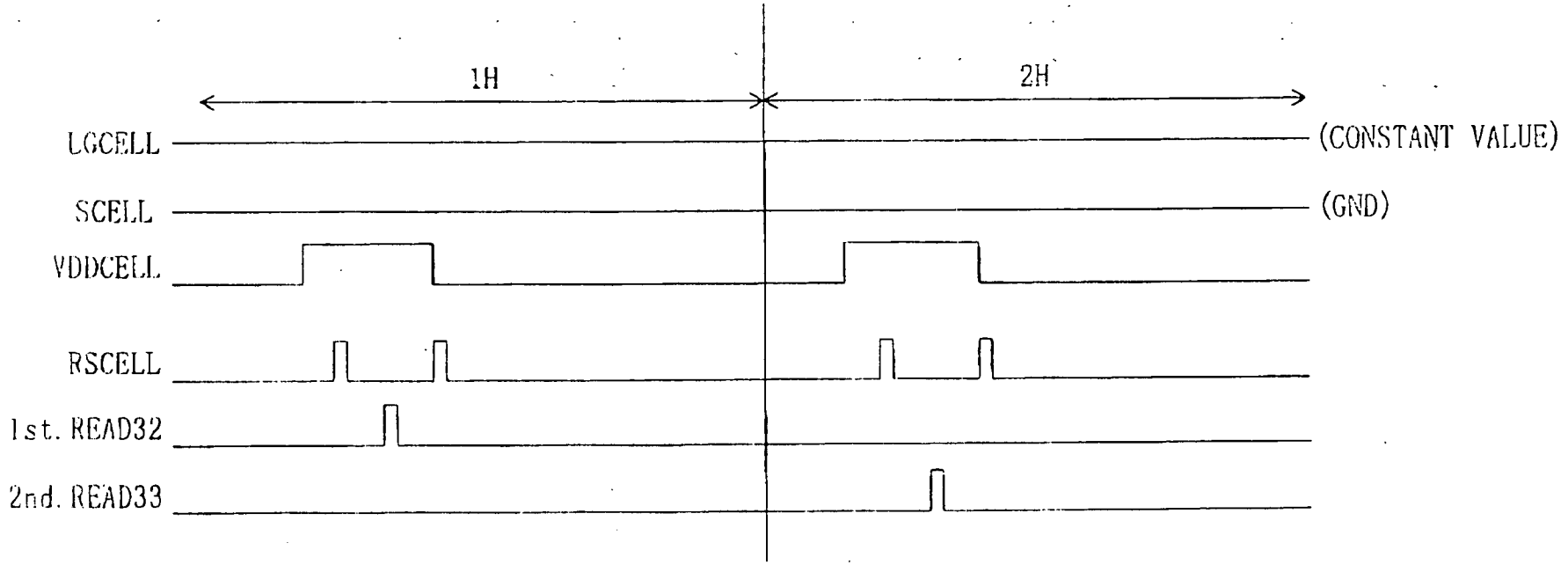

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
RSCELL
1st. READ32
2nd. READ33

FIG. 8

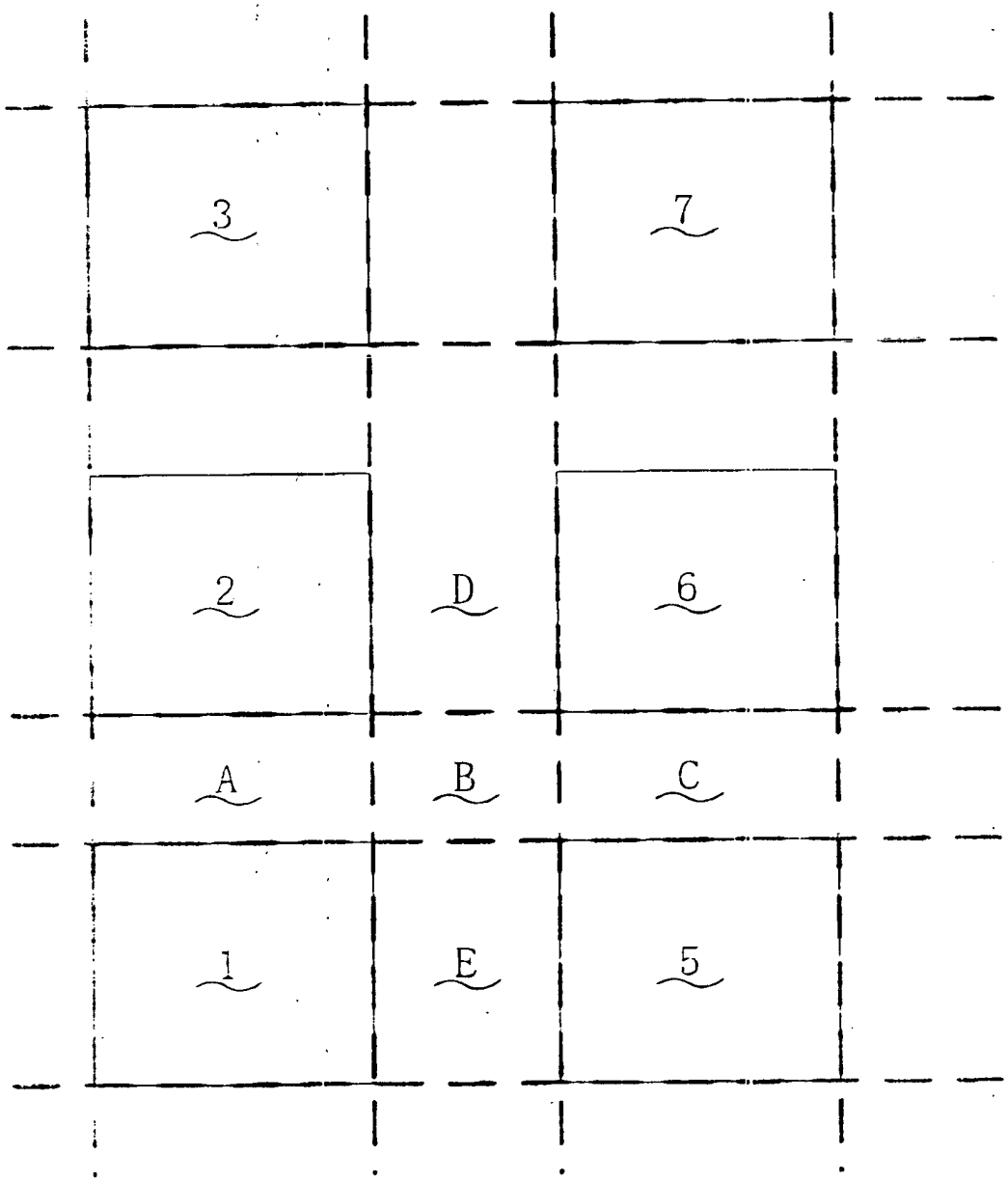
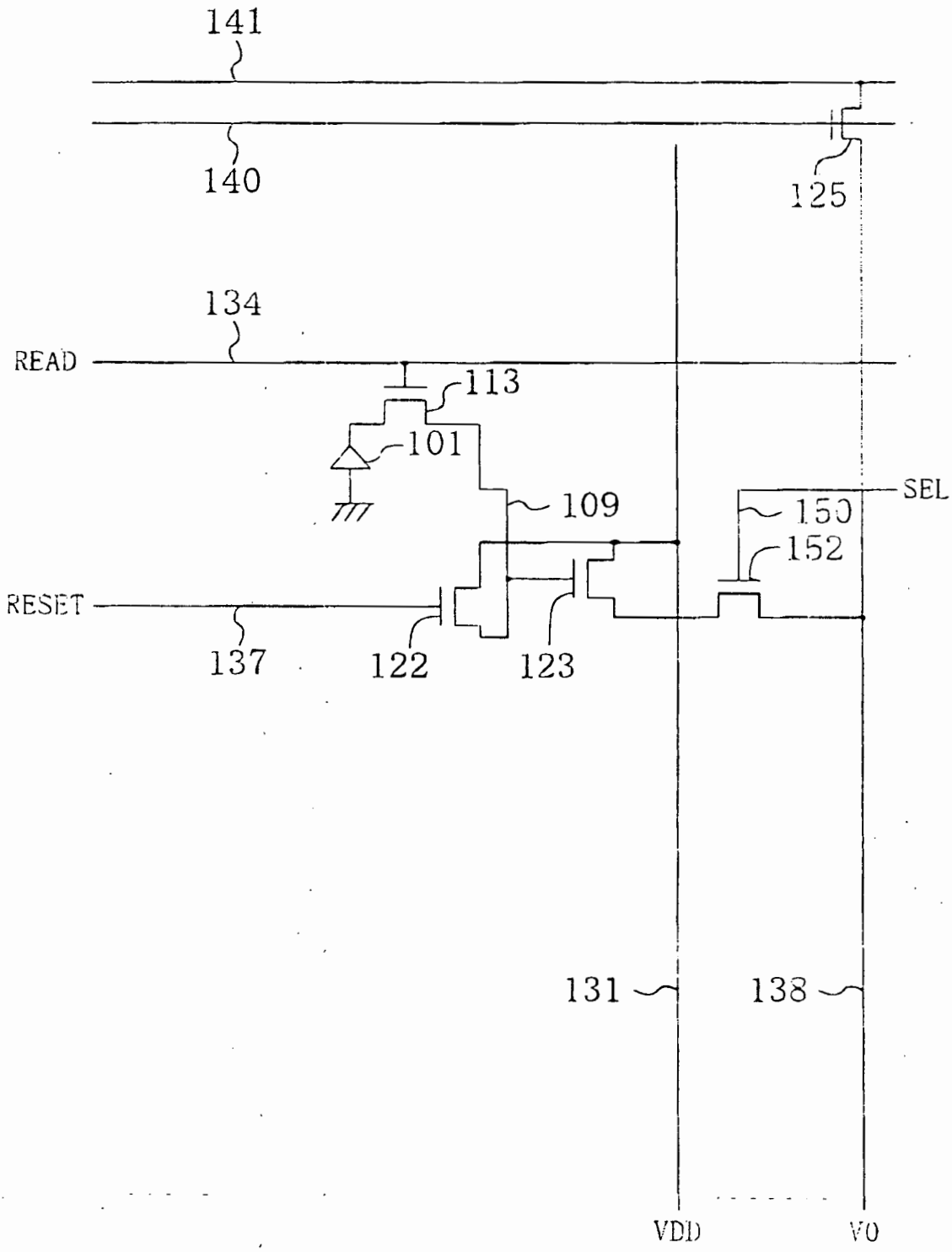


FIG. 9

FD SECTION	PIXEL AMPLIFIER	RESET GATE	APERTURE RATIO
A REGION, B REGION, C REGION	A REGION, B REGION, C REGION	A REGION, B REGION, C REGION	10%
		D REGION, B REGION, E REGION	25%
	D REGION, B REGION, E REGION	A REGION, B REGION, C REGION	20%
		D REGION, B REGION, E REGION	35%
D REGION, B REGION, E REGION	A REGION, B REGION, C REGION	A REGION, B REGION, C REGION	20%
		D REGION, B REGION, E REGION	20%
	D REGION, B REGION, E REGION	A REGION, B REGION, C REGION	20%
		D REGION, B REGION, E REGION	20%

FIG. 10

PRIOR ART



IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

GODO KAISHA IP BRIDGE 1, Plaintiff, v. OMNIVISION TECHNOLOGIES, INC., Defendant.	Case No. 1:16-cv-00290-MN **DECLARATION OF ERIK CARLSON IN SUPPORT OF DEFENDANT OMNIVISION TECHNOLOGIES, INC.'S SURREPLY CLAIM CONSTRUCTION BRIEF**

DECLARATION OF ERIK CARLSON IN SUPPORT OF DEFENDANT OMNIVISION TECHNOLOGIES, INC.'S SURREPLY CLAIM CONSTRUCTION BRIEF

I, Erik Carlson, declare as follows:

1. I am an attorney at Wilson Sonsini Goodrich & Rosati, counsel for Defendant OmniVision Technologies, Inc. ("OmniVision") in the above-referenced action. I submit this declaration in support of OmniVision's Surreply Claim Construction Brief. The matters set forth herein are based upon my personal knowledge, and, if called as a witness, I could and would competently testify thereto.

2. Attached as **Appendix 0660 – 0661** is a true and correct copy of the October 11, 2018 Declaration of Dr. Jack C Lee, Ph.D. In Support of Defendant OmniVision Technologies, Inc.'s Sur-Reply Claim Construction Brief.

3. Attached as **Appendix 0662 – 0722** is a true and correct copy of U.S. Patent No. 6,977,684 to Hashimoto et al.

4. Attached as **Appendix 0723 – 0737** is a true and correct copy of U.S. Pat. App. Pub. No. 2002/0018131 A1 (Kochi).

5. Attached as **Appendix 0738 – 0740** is a true and correct of the Examiner Interview Summary mailed on December 13, 2010 from the file history of U.S. Pat. No. 8,106,431.

6. Attached as **Appendix 0741 – 0791** is a true and correct copy of the November, 11, 2003 Application from the file history of U.S. Pat. No. 7,436,010.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed at Los Angeles, California on October 12, 2018.

/s/ *Erik Carlson*
Erik Carlson