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July 8, 1988

ENERGY RESOURCE CENTER/PGE
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IEEE Standard Dictionary of Electrical and Electronics Terms

Fourth Edition

Library of Congress Catalog Number 88-082198

ISBN: 1-55937-000-9

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November 3, 1988

SH12070

able electric power from the source. *Notes:* (1) The sound pressure apparent at a distance of 1 meter can be found by multiplying the sound pressure observed at a remote point where the sound field is spherically divergent by the number of meters from the effective acoustic center to that point. (2) The available power response is a function not only of the transducer but also of some source impedances, either actual or nominal, the value of which must be specified. *See:* **loudspeaker.** 176

available short-circuit current (at a given point in a circuit) (prospective short-circuit current). The maximum current that the power system can deliver through a given circuit point to any negligible-impedance short-circuit applied at the given point, or at any other point that will cause the highest current to flow through the given point. *Notes:* (1) This value can be in terms of either symmetrical or asymmetrical: peak or root-mean-square current, as specified. (2) In some resonant circuits the maximum available short-circuit current may occur when the short circuit is placed at some other point than the given one where the available current is measured. 103

available short-circuit test current (at the point of test) (prospective short-circuit test current). The maximum short-circuit current for any given setting of a testing circuit that the test power source can deliver at the point of test, with the test circuit short-circuited by a link of negligible impedance at the line terminals of the device to be tested. *Note:* This value can be in terms of either symmetrical or asymmetrical, peak or root-mean-square current, as specified. 103

available signal-to-noise ratio (at a point in a circuit). The ratio of the available signal power at that point to the available random noise power. *See:* **signal-to-noise ratio.** 328

available time (electric drive) (industrial control). The period during which a system has the power turned on, is not under maintenance, and is known or believed to be operating correctly or capable of operating correctly. *See:* **electric drive.** 206

avalanche (gas-filled radiation counter tube). The cumulative process in which charged particles accelerated by an electric field produce additional charged particles through collision with neutral gas molecules or atoms. It is therefore a cascade multiplication of ions. *See:* **amplifier.** 96, 125

avalanche breakdown (of a semiconductor device)(-charged-particle detectors)(germanium gamma-ray detectors). A breakdown that is caused by the cumulative multiplication of charge carriers through field-induced impact ionization. 119,118, 245,528

avalanche impedance (semiconductor). *See:* **breakdown impedance; semiconductor.**

avalanche photodiode (APD)(fiber optics). A photodiode designed to take advantage of avalanche multiplication of photocurrent. *Note:* As the reverse-bias voltage approaches the breakdown voltage, hole-electron pairs created by absorbed photons acquire sufficient energy to create additional hole-electron pairs when they collide with ions; thus a multiplication (signal gain) is achieved. *See:* **photodiode; PIN photodiode.** 433

average absolute burst magnitude (audio and electroacoustics). The average of the instantaneous burst magnitude taken over the burst duration. *See:* figure under **burst duration.** *See:* **burst (audio and electroacoustics).** 176

average absolute pulse amplitude. The average of the absolute value of the instantaneous amplitude taken over the pulse duration. 254

average bundle gradient (overhead-power-line corona and radio noise). For a bundle of two or more subconductors, the arithmetic mean of the average gradients of the individual subconductors. 411

average crossing rate (ACR)(1)(electromagnetic site survey). The average number of crossings in the positive direction of a given level v_1 per unit time. (See Figure "Typical Noise Envelope of a Man-Made Radio-Noise Process".) 457

(2)(control of system electromagnetic compatibility). The average number of pulses crossing a specified level (zero, if not specified) in the positive-going direction per unit time. 495

average current (periodic current). The value of the current averaged over a full cycle unless otherwise specified. *See:* **rectification.** 237, 66

average detector (overhead-power-line corona and radio noise). A detector, the output voltage of which approximates the average value of the envelope of an applied signal or noise. *Notes:* (1) This detector function is often identified on radio noise meters as field intensity (FI). (Field intensity is deprecated; field strength should be used.) (2) Field intensity (FI) (field strength) setting on some radio noise meters produces on the meter scale the average value of the logarithmic detector. 411

average electrode current (electron tube). The value obtained by integrating the instantaneous electrode current over an averaging time and dividing by the averaging time. *See:* **electrode current (electron tube).** 125

average forward-current rating (rectifier circuit element). The maximum average value of forward current averaged over a full cycle, permitted by the manufacturer under stated conditions. 208

average information content (per symbol) (information rate from a source, per symbol). The average of the information content per symbol emitted from a source. *Note:* The term entropy rate is also used to designate average information content. *See:* **information theory.** 61

average inside air temperature (of enclosed switchgear) (power switchgear). The average temperature of the surrounding cooling air which comes in contact with the heated parts of the apparatus within the enclosure. 103

average luminance (illuminating engineering). Luminance is the property of a geometric ray. Luminance as measured by conventional meters is averaged with respect to two independent variables, area and solid

dimension, critical mating (standard connector). Those longitudinal and transverse dimensions assuring nondestructive mating with a corresponding standard connector. 110

diminished-radix complement (mathematics of computing). The complement obtained by subtracting each digit of a given numeral from the largest digit in the numeration system. For example, ones complement in binary notation, nines complement in decimal notation. *See:* **radix complement.** 564

dimming reactor (thyristor). A reactor that may be inserted in a lamp circuit at will for reducing the luminous intensity of the lamp. *Note:* Dimming reactors are normally used to dim headlamps, but may be applied to other circuits, such as gauge lamp circuits. 328

diode (1) (electron tube). A two-electrode electron tube containing an anode and a cathode. *See:* **equivalent diode.** 125

(2) (semiconductor). A semiconductor device having two terminals and exhibiting a nonlinear voltage-current characteristic; in more-restricted usage, a semicondutor device that has the asymmetrical voltage-current characteristic exemplified by a single *p-n* junction. *See:* **semiconductor.** 245

diode characteristic (multielectrode tube). The composite electrode characteristic taken with all electrodes except the cathode connected together. 125

diode equivalent. The imaginary diode consisting of the cathode of a triode or multigrid tube and a virtual anode to which is applied a composite controlling voltage such that the cathode current is the same as in the triode or multigrid tube. 125

diode function generator (analog computers). A function generator that uses the transfer characteristics of resistive networks containing biased diodes. The desired function is approximated by linear segments whose values are manually inserted by means of potentiometers and switches. 9

diode fuses (semiconductor rectifiers). Fuses of special characteristics connected in series with one or more semiconductor rectifier diodes to disconnect the semiconductor rectifier diode in case of failure and protect the other components of the rectifier. *Note:* Diode fuses may also be employed to provide coordinated protection in case of overload or short-circuit. *See:* **semiconductor rectifier stack.** 208

diode laser. *See:* **injection laser diode (ILD).**

dip (electroplating). A solution used for the purpose of producing a chemical reaction upon the surface of a metal. *See:* **electroplating.** 328

diplex operation (data transmission). The simultaneous transmission or reception of two signals using a specified common feature, such as a single antenna or a single carrier. 59

diplex radio transmission. The simultaneous transmission of two signals using a common carrier wave. *See:* **radio transmission.** 111

dip needle. A device for indicating the angle between the magnetic field and the horizontal. *See:* **magnetometer.** 328

dipole. *See:* **dipole antenna; folded dipole antenna; electricdipole; magnetic dipole.**

dipole antenna (1) (antennas). Any one of a class of antennas producing a radiation pattern approximating that of an elementary electric dipole. *Note:* Common usage considers the dipole antenna to be a metal radiating structure which supports a line current distribution similar to that of a thin straight wire so energized that the current has a node only at each end. *Syn:* **doublet antenna.** 111

(2) (data transmission). Any one of a class of antennas producing the radiation pattern approximating that of an elementary electric dipole. *Note:* Common usage considers a dipole antenna to be a metal radiating structure which supports a line current distribution similar to that of a thin straight wire a ½ wavelength long so energized that the current has two nodes, one at each of the far ends. 59

(3) (overhead-power-line corona and radio noise). Any one of a class of antennas having a radiation pattern approximating that of an elementary electric dipole. *Note:* Common usage considers the dipole antenna to be a metal radiating or receiving structure which supports a line-current distribution similar to that of a thin straight wire, a half wavelength long, so that the current has a node at each end of the antenna. 411

dipole molecule. A molecule that possesses a dipole moment as a result of the permanent separation of the centroid of positive charge from the centroid of negative charge for the molecule as a whole. 210

dip plating. *See:* **immersion plating.**

dip soldering (soldered connections). The process whereby assemblies are brought in contact with the surface of molten solder for the purpose of making soldered connections. 284

direct ac converter (cycloconverter)(self-commutated converters). The alternating current (ac) conversion is accomplished directly, without an intermediate link having different power characteristics, such as direct current (dc) or high-frequency ac. 584

direct-acting machine voltage regulator (power switchgear). A machine voltage regulator having a voltage-sensitive element which acts directly without interposing power-operated means to control the excitation of an electric machine. 103

direct-acting overcurrent trip device. *See:* **direct release (series trip); indirect release (trip); overcurrent release (trip).**

direct-acting overcurrent trip device current rating (trip devices for ac and general-purpose dc low-voltage power circuit breakers). The value of current designated by the manufacturer on which trip element calibration marks are based. 560

direct-acting recording instrument. A recording instrument in which the marking device is mechanically connected to, or directly operated by, the primary detector. *See:* **instrument.** 328

direct address (computing systems). An address that specifies the location of an operand. *See:* **one-level address.** 255, 77

ductively connected to it flows in both directions. *Note:* The terms single-way and double-way provide a means for describing the effect of the rectifier circuit on current flow in transformer windings connect to rectifier circuit elements. Most rectifier circuits may be classified into these two general types. Double-way rectifier circuits are also referred to as bridge rectifier circuits. *See:* **rectification; rectifier circuit element; power rectifier; single-way rectifier circuit; bridge rectifier circuit.** 208

double-winding synchronous generator. A generator that has two similar windings, in phase with one another, mounted on the same magnetic structure but not connected electrically, designed to supply power to two independent external circuits. 63

doughnut (electronic device). *See:* **toroid.**

dovetail projection. A tenon, commonly flared; used for example, to fasten a pole to the spider. *See:* **stator.** 63

dovetail slot. (1) A recess along the side of a coil slot into which a coil-slot wedge is inserted. (2) A flaring slot into which a dovetail projection is engaged; used for example, to fasten a pole to the spider. *See:* **stator.** 63

dowel (dowel pin). A pin fitting with close tolerance into a hole in abutting pieces to establish and maintain accurate alignment of parts. Frequently designed to resist a shear load at the interface of the abutting pieces. 63

downconverter (nonlinear, active, and nonreciprocal waveguide components). A heterodyne frequency conversion device that converts an input signal to a lower frequency output signal. 530

down lead (lightning protection). The conductor connecting an overhead ground wire or lightning conductor with the grounding system. *See:* **direct-stroke protection (lightning).** 64

downlight (illuminating engineering). A small direct lighting unit which directs the light downward and can be recessed, surface mounted, or suspended. 167

down link (communication satellite). A transmission link carrying information from a satellite or spacecraft to earth. Typically down links carry telemetry, data and voice. 83

down time. (1) (station control and data acquisition). The time during which a device or system is not capable of meeting performance requirements. 403

(2)(supervisory control, data acquisition, and automatic control). The time during which a device or system is not capable of meeting performance requirements. 570

downward component (illuminating engineering). That portion of the luminous flux from a luminaire which is emitted at angles below the horizontal. 167

downward modulation. Modulation in which the instaneous amplitude of the modulated wave is never greater than the amplitude of the unmodulated carrier. 339

DR. *See:* **dead reckoning.**

draft gauge (navigation aid terms). A hydrostatic instrument installed in vessels to indicate the depth to which a vessel is submerged. 526

drag-in (electroplating). The quantity of solution that adheres to cathodes when they are introduced into a bath. *See:* **electroplating.** 328

drag magnet. *See:* **retarding magnet.**

drag-out (electroplating). The quantity of solution that adheres to cathodes when they are removed from a bath. *See:* **electroplating.** 328

drain (1) (general). The current supplied by a cell or battery when in service. *See:* **battery (primary or secondary).** 328

(2) (metal-nitride-oxide field-effect transistor). Region in the device structure of an insulated-gate field-effect transistor (IGFET) which contains the terminal into which charge carriers flow from the source through the channel. It has the potential which is more attractive than the source for the carriers in the channel. 386

drainage (corrosion). Conduction of current (positive electricity) from an underground metallic structure by means of a metallic conductor. 205

drainage unit (wire-line communication facilities). Center-tapped inductive device designed to relieve conductor-to-conductor and conductor-to-ground voltage stress by draining extraneous currents to ground. It is also designed to serve the purpose of a mutual drainage reactor forcing simultaneous protector-gap operation. 414

drain line (rotating machinery) (bearing oil system). A return pipe line using gravity flow. *See:* **oil cup (rotating machinery).** 63

drawbar pull (cable plowing). The effective pulling force delivered. 52

drawbridge coupler. *See:* **movable-bridge coupler.**

drawdown (power operations). The distance that the water surface of a reservoir is lowered from a given elevation as the result of the withdrawal of water. 516

drawout-mounted device (power switchgear). One having disconnecting devices and in which the removable portion may be removed from the stationary portion without the necessity of unbolting connections or mounting supports. *See:* **stationary-mounted device.** 103

D region (radio wave propagation). The region of the terrestrial ionosphere between about 40 and 90 km altitude responsible for most of the attenuation of radio waves in the range 1 to 100 MHz. 146

drift (1)(navigation aid terms). (A) Drift angle, (B) component of a vehicle's ground speed perpendicular to heading and (C) distance a craft is moved by current and wind. 526

(2) (rotating machinery). A long-time change in synchronous-machine resulting system error resulting from causes such as aging of components, self-induced temperature changes, and random phenomena. *Note:* Maximum acceptable drift is normally a specified change for a specified period of time, for specified conditions. 63

(3) (industrial control). An undesired but relatively

point

S_s = sound pressure in newtons per square meter per volt applied at the input terminals produced at a distance δ meters from the arbitrary reference point

f = frequency in hertz

ρ = density of the medium in kilograms per cubic meter

δ = distance in meters from the arbitrary reference point on or near the transducer to the point in which the sound pressure established by the transducer when emitting is evaluated.

See: **loudspeaker.** 176

electroacoustic transducer (electric system). A transducer for receiving waves and delivering waves to an acoustic system, or vice versa. *See:* **loudspeaker; transducer.** 176

electrobiology. The study of electrical phenomena in relation to biological systems. 192

electrocardiogram. The graphic record of the variation with time of the voltage associated with cardiac activity. *See:* **electrocorticogram (electrobiology); electrodermogram (electrobiology); Galvani's experiment (electrobiology); spindle wave (electrobiology); vector electrocardiogram (electrobiology).** 192

electrocardiographic waves, P, Q, R, S, and, T (medical electronics)(in electrocardiograms obtained from differential electrodes placed on the right arm and left leg). The characteristic tracing consists of five consecutive waves: *P*, a prolonged, low, positive wave: *Q*, brief, low, negative: *R*, brief, high, positive: *S*, brief, low, negative, and *T*, prolonged, low, positive. 192

electrocautery (electrotherapy). An instrument for cauterizing the tissues by means of a conductor brought to a high temperature by an electric current. *See:* **electrotherapy.** 192

electrochemical cell. A system consisting of an anode, cathode, and an electrolyte plus such connections (electric and mechanical) as may be needed to allow the cell to deliver or receive electric energy. 223, 186

electrochemical equivalent (element, compound, radical, or ion) (1) (general). The weight of that substance involved in a specified electrochemical reaction during the passage of a specified quantity of electricity, such as a faraday, ampere-hour, or coulomb. 328
(2) (oxidation). The weight of an element or group of elements oxidized or reduced at 100-percent efficiency by a unit quantity of electricity. *See:* **electrochemistry.** 205

electrochemical recording (facsimile). Recording by means of a chemical reaction brought about by the passage of signal-controlled current through the sensitized portion of the record sheet. *See:* **recording (facsimile).** 12

electrochemical series. *See:* **electromotive series.**

electrochemical valve. An electric valve consisting of a metal in contact with a solution or compound across the boundary of which current flows more readily in one direction than in the other direction and in which the valve action is accompanied by chemical changes. 328

electrochemical valve metal. A metal or alloy having properties suitable for use in an electrochemical valve. *See:* **electrochemical valve.** 328

electrochemistry. That branch of science and technology that deals with interrelated transformations of chemical and electric energy. 328

electrocoagulation (medical electronics). The clotting of tissue by heat generated within the tissue by impressed electric currents. 192

electrocorticogram (medical electronics). A graphic record of the variation with time of voltage taken from exposed cortex cerebra. 192

electroculture (medical electronics). The stimulation of growth, flowering, or seeding by electric means. 192

electrocution. The destruction of life by means of electric current. 192

electrode (1) (electrochemistry). An electric conductor for the transfer of charge between the external circuit and the electroactive species in the electrolyte. *Note:* Specifically, in an electrolytic cell, an electrode is a conductor at the surface of which a change occurs from conduction by electrons to conduction by ions or colloidal ions. *See:* **electrolytic cell; electrochemical cell.** 186
(2) (electron tube). A conducting element that performs one or more of the functions of emitting, collecting, or controlling by an electric field the movements of electrons or ions. 125
(3) (biological electronics) (reference, inactive, diffuse, dispersive, indifferent electrode). (A) A pickup electrode that, because of averaging, shunting, or other aspects of the tissue-current pattern to which it connects, shows potentials not characteristic of the region near the active electrode. (B) Any electrode, in a system of stimulating electrodes, at which due to its dispersive action, excitation is not produced. (C) An electrode of relatively large area applied to some inexcitable or distant tissue in order to complete the circuit with the active electrode that is used for stimulation. 192

electrode, accelerating (electron-beam tube). *See:* **accelerating electrode.**

electrode admittance (*j*th electrode of an *n*-electrode electron tube). The short-circuit driving-point admittance between the *jth* electrode and the reference point measured directly at the *jth* electrode. *Note:* To be able to determine the intrinsic electronic merit of an electron tube, the driving-point and transfer admittances must be defined as if measured directly at the electrodes inside the tube. The definitions of electrode admittance and electrode impedance are included for this reason. *See:* **electron-tube admittances.** 125

electrode alternating-current resistance (electron device). The real component of the electrode impedance. *See:* **self-impedance.** 190

electrode bias (electron tubes). The voltage at which an electrode is stabilized under operating conditions with no incoming signal, but taking into account the

gas-oil sealed system (power and distribution transformer). A system in which the interior of the tank is sealed from the atmosphere, over the temperature range specified, by means of an auxiliary tank or tanks to form a gas-oil seal operating on the manometer principle. 53

gasoline dispensing and service station (National Electrical Code). A location where gasoline or other volatile flammable liquids or liquified flammable gases are transferred to the fuel tanks (including auxiliary fuel tanks) of self-propelled vehicles. 256

gasoline-electric drive. *See:* **gas-electric drive.**

gas-pressure relay (power switchgear). A relay so constructed that it operates by the gas pressure in the protected equipment. 103

gasproof. So constructed or protected that the specified gas will not interfere with successful operation. 103

gasproof or vaporproof (rotating machinery). So constructed that the entry of a specified gas or vapor under prescribed conditions cannot interfere with satisfactory operating of the machine. *See:* **asynchronous machine.** 63

gas ratio. The ratio of the ion current in a tube to the electron current that produces it. *See:* **electrode current.** 190

gas seal (rotating machinery). A sealing arrangement intended to minimize the leakage of gas to or from a machine along a shaft. *Note:* It may be incorporated into a ball or roller bearing assembly. 63

gassing. The evolution of gases from one or more of the electrodes during electrolysis. *See:* **electrolytic cell.** 328

gas system (rotating machinery). The combination of parts used to ventilate a machine with any gas other than air, including facilities for charging and purging the gas in the machine. 63

gastight (1) (lightning protection). So constructed that gas or air can neither enter nor leave the structure except through vents or piping provided for the purpose. 297

(2) (power switchgear). So constructed that the specified gas will not enter the enclosing case under specified pressure conditions. 103

gas tube. An electron tube in which the pressure of the contained gas or vapor is such as to affect substantially the electrical characteristics of the tube. 190

gas-tube relaxation oscillator (arc-tube relaxation oscillator). A relaxation oscillator in which the abrupt discharge is provided by the breakdown of a gas tube. *See:* **oscillatory circuit.** 328

gas-tube surge arrester (gas-tube protective devices). A gap, or gaps, in an enclosed discharge medium, other than air at atmospheric pressure, designed to protect apparatus or personnel, or both, from high transient voltages. 490

gas-turbine-electric drive. A self-contained system of power generation and application in which the power generated by a gas turbine is transmitted electrically by means of a generator and a motor (or multiples of these) for propulsion purposes. *Note:* The prefix gas-turbine-electric is applied to ships, locomotives, cars, buses, etcetera, that are equipped with this drive. *See:* **electric locomotive.** 328

gate (1)(microwave)(nonlinear, active, and nonreciprocal waveguide components). In elementary form, a two-port switch having a single-pole, single-throw function. *See:* **bang snuffer.** 530

(2)(X-ray energy spectrometers). A device or element that, depending upon one or more specified inputs, has the ability to permit or inhibit the passage of a signal. 471

(3) (electronic computers). (A) A device having one output channel and one or more input channels, such that the output channel state is completely determined by the contemporaneous input channel states, except during switching transients. (B) A combinational logic element having at least one input channel. (C) An AND gate. (D) An OR gate. 235

(4) (cryotron). An output element of a cryotron. *See:* **superconductivity.** 191

(5) (navigation systems). (A) An interval of time during which some portion of the circuit or display is allowed to be operative, or (B) the circuit which provides gating. *See:* **navigation.** 187, 13

(6) (metal-nitride-oxide field-effect transistor). This structural element of an insulated-gate field-effect transistor (IGFET) controls the current between source and drain by a voltage applied to its terminal. 386

gate-controlled delay time (thyristor). The time interval, between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped (risen) to a specified value near its initial value during switching of a thyristor from the OFF state to the ON state by a gate pulse. *See:* **principal voltage-current characteristic.** 243, 66, 208, 191

gate-controlled rise time (thyristor). The time interval between the instants at which the principal voltage (current) has dropped (risen) from a specified value near its initial value to a specified low (high) value, during switching of a thyristor from the OFF state to the ON state by a gate pulse. *Note:* This time interval will be equal to the rise time of the ON state current only for pure resistive loads. *See:* **principal voltage-current characteristic.** 243, 66, 208, 191

gate-controlled turn-off time (turn-off thyristor). The time interval, between a specified point at the beginning of the gate pulse and the instant when the principal current has decreased to a specified value, during switching from the ON state to the OFF state by a gate pulse. *See:* **principal voltage-current characteristic.** 243, 66, 208, 191

gate-controlled turn-on time (thyristor). The time interval, between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped (risen) to a specified low (high) value during switching of a thyristor from the OFF state to the ON state by a gate pulse. Turn-on time is the sum of delay time and rise time. *See:* **principal voltage-current characteristic; delay time; rise time.** 243, 204, 208, 191

reference has the polar axis vertical and the origin at or near the antenna. Under these conditions, a vertical dipole will radiate only theta (j) polarization, and a horizontal loop will radiate only phi (Φ) polarization. *See:* **antenna.** 111, 246

Philips gauge. A vacuum gauge in which the gas pressure is determined by measuring the current in a glow discharge. *See:* **instrument.** 328

phon. The unit of loudness level as specified in the definition of loudness level. *See:* **loudspeaker.** 176

phonograph pickup (mechanical reproducer). A mechanoelectrical transducer that is actuated by modulations present in the groove of the recording medium and that transforms this mechanical input into an electric output. *Note:* (1) Where no confusion is likely the term **phonograph pickup** may be shortened to **pickup.** (2) A phonograph pickup generally includes a pivoted mounting arm and the transducer itself (the pickup cartridge). 176

phosphene (electrical) (electrotherapy). A visual sensation experienced by a human subject during the passage of current through the eye. *See:* **electrotherapy.** 192

phosphor. A substance capable of luminescence. *See:* **cathode-ray tube; fluorescent lamp; radio navigation; television.** 328

phosphor decay. A phosphorescence curve describing energy emitted versus time. *See:* **oscillograph.** 185

phosphorescence (illuminating engineering). The emission of light as the result of the absorption of radiation, and continuing for a noticeable length of time after excitation. 167

phosphor screen. All the visible area of the phosphor on the cathode-ray tube faceplate. *See:* **oscillograph.** 185

phot (ph) (illuminating engineering). A unit of illuminance equal to one lumen per square centimeter. The use of this unit is deprecated. 167

photocathode. An electrode used for obtaining a photoelectric emission when irradiated. *See:* **electrode (electron tube); phototube.** 117

photocathode blue response. The photoemission current produced by a specified luminous flux from a tungsten filament lamp at 2854 kelvins color temperature when the flux is filtered by a CS 5-58 blue filter of half stock thickness (1.75—2.25 mm). This parameter is useful in characterizing response to scintillation counting sources. 117

photocathode luminous sensitivity. *See:* **sensitivity, cathode luminous.**

photocathode response (diode-type camera tube). The response of a photocathode is the current emitted into vacuum per incident radiant power of specified spectral distribution. It is expressed in amperes watt^{-1} (AW^{-1}). 380

photocathode, semitransparent. *See:* **semitransparent photocathode.**

photocathode spectral quantum efficiency (diode-type camera tube). The ratio of the average number of electrons emitted to the number of photons in the input signal irradiance on the photocathode face as a function of the photon energy, frequency, or wavelength. 380

photocathode spectral-sensitivity characteristic. *See:* **spectral-sensitivity characteristic photocathode.**

photocathode transit time. That portion of the photomultiplier transit time corresponding to the time for photoelectrons to travel from the photocathode to the first dynode. 117

photocathode transit-time difference. The difference in transit time between electrons leaving the center of the photocathode and electrons leaving the photocathode at some specified point on a designated diameter. 117

photocell (photoelectric cell). (1) A solid-state photosensitive electron device in which use is made of the variation of the current-voltage characteristic as a function of incident radiation. *See:* **phototube.** 117

(2) A device exhibiting photovoltaic or photoconductive effects. *See:* **phototube.** 244, 190

photochemical radiation (illuminating engineering). Energy in the ultraviolet, visible and infrared regions to produce chemical changes in materials. *Note:* Examples of photochemical processes are accelerated fading tests, photography, photoreproduction and chemical manufacturing. In many such applications a specific spectral region is of importance. 167

photoconductive cell. A photocell in which the photoconductive effect is utilized. *See:* **phototube.** 244, 190

photoconductive effect (photoconductivity). A photoelectric effect manifested as a change in the electric conductivity of a solid or a liquid and in which the charge carriers are not in thermal equilibrium with the lattice. *Note:* Many semiconducting metals and their compounds (notably selenium, selenides, and tellurides) show a marked increase in electric conductance when electromagnetic radiation is incident on them. *See:* **photoelectric effect; phototube; photovoltaic effect; photoemissive effect.** 210, 190

photoconductivity (fiber optics). The conductivity increase exhibited by some nonmetallic materials, resulting from the free carriers generated when photon energy is absorbed in electronic transitions. The rate at which free carriers are generated, the mobility of the carriers,and the length of time they persist in conducting states (their lifetime) are some of the factors that determine the amount of conductivity change. *See:* **photoelectric effect.** 433

photocurrent (fiber optics). The current that flows through a photosensitive device (such as a photodiode) as the result of exposure to radiant power. Internal gain, such as that in an avalanche photodiode, may enhance or increase the current flow but is a distinct mechanism. *See:* **dark current; photodiode.** 433

photodiode (fiber optics). A diode designed to produce photocurrent by absorbing light. Photodiodes are used for the detection of optical power and for the conversion of optical power to electrical power. *See:* **ava-**

lanche photodiode (APD); photocurrent; PIN photodiode. 433

photoelectric beam-type smoke detector (fire protection devices). A device which consists of a light source which is projected across the area to be protected into a photosensing cell. smoke between the light source and the receiving photosensing cell reduces the light reaching the cell, causing actuation. 71

photoelectric cathode. *See:* **photocathode.**

photoelectric color-register controller. A photoelectric control system used as a longitudinal position regulator for a moving material or web to maintain a preset register relationship between repetitive register marks in the first color and reference positions of the printing cylinders of successive colors. *See:* **photoelectric control.** 206

photoelectric control (industrial control). Control by means of which a change in incident light effects a control function. 206

photoelectric counter (industrial control). A photoelectrically actuated device used to record the number of times a given light path is intercepted by an object. *See:* **photoelectric control.** 206

photoelectric current. The current due to a photoelectric effect. *See:* **photoelectric effect.** 244, 206

photoelectric cutoff register controller (industrial control). A photoelectric control system used as a longitudinal position regulator that maintains the position of the point of cutoff with respect to a repetitively referenced pattern on a moving material. *See:* **photoelectric control.** 206

photoelectric directional counter. A photoelectrically actuated device used to record the number of times a given light path is intercepted by an object moving in a given direction. *See:* **photoelectric control.** 204

photoelectric door opener. A photoelectric control system used to effect the opening and closing of a power-operated door. *See:* **photoelectric control.** 204

photoelectric effect (fiber optics). (1) External photoelectric effect: The emission of electrons from the irradiated surface of a material. *Syn:* **photoemissive effect.** (2) Internal photoelectric effect: photoconductivity. 433

photoelectric emission (electron tube). The ejection of electrons from a solid or liquid by electromagnetic radiation. *See:* **field-enhanced photoelectric emission.** 125

photoelectric flame detector (fire protection devices). A device whose sensing element is a photocell which either changes its electrical conductivity or produces an electrical potential when exposed to radiant energy. 71

photoelectric lighting controller. A photoelectric relay actuated by a change in illumination to control the illumination in a given area or at a given point. *See:* **photoelectric control.** 206

photoelectric loop control (industrial control). A photoelectric control system used as a position regulator for a strip processing line that matches the average linear speed in one section to the speed in an adjacent section to maintain the position of the loop located between the two sections. *See:* **photoelectric control.** 206

photoelectric pinhole detector. A photoelectric control system that detects the presence of minute holes in an opaque material. *See:* **photoelectric control.** 204

photoelectric power system. *See:* **photovoltaic power system.**

photoelectric pyrometer (industrial control). An instrument that measures the temperature of a hot object by means of the intensity of radiant energy exciting a phototube. *See:* **electronic control.** 206

photoelectric relay. A relay that functions at predetermined values of incident light. *See:* **photoelectric control.** 206

photoelectric scanner (industrial control). A single-unit combination of a light source and one or more phototubes with a suitable optical system. *See:* **photoelectric control.** 206

photoelectric side-register controller (industrial control). A photoelectric control system used as a lateral position regulator that maintains the edge of, or a line on, a moving material or web at a fixed position. *See:* **photoelectric control.** 206

photoelectric smoke-density control. A photoelectric control system used to measure, indicate, and control the density of smoke in a flue or stack. *See:* **photoelectric control.** 206

photoelectric smoke detector (industrial control). A photoelectric relay and light source arranged to detect the presence of more than a predetermined amount of smoke in air. *See:* **photoelectric control.** 206

photoelectric spot-type smoke detector (fire protection devices). A device which contains a chamber with either overlapping or porous covers which prevent the entrance of outside sources of light but which allow the entry of smoke. The unit contains a light source and a special photosensitive cell in the darkened chamber. The cell is either placed in the darkened area of the chamber at an angle different from the light path or has the light blocked from it by a light stop or shield placed between the light source and the cell. With the admission of smoke particles, light strikes the particles and is scattered and reflected into the photosensitive cell. This causes the photosensing circuit to respond to the presence of smoke particles in the smoke chamber. 71

photoelectric system (protective signaling). An assemblage of apparatus designed to project a beam of invisible light onto a photoelectric cell and to produce an alarm condition in the protection circuit when the beam is interrupted. *See:* **protective signaling.** 328

photoelectric tube. An electron tube, the functioning of which is determined by the photoelectric effect. *See:* **phototube.** 190

photo-electron. An electron liberated by the photoemissive effect. *See:* **photoelectric effect.** 190

photo-electron irradiation dark current increase (diode-type camera tube). That irreversible dark current increase which is caused by bombardment of the charge storage target by photo- electrons. 380

plates perpendicular to the cylinder, spaced less than one wavelength apart. *Syn:* **cheese antenna.** 111

pilot (transmission system). A signal wave, usually a single frequency, transmitted over the system to indicate or control its characteristics. 328

pilotage (navigation aid terms). The process of directing a vehicle by reference to recognizable landmarks or soundings, or to electronic or other aids to navigation. Observations may be by any means including optical, aural, mechanical, or electronic. 526

pilot cell (storage battery). A selected cell whose condition is assumed to indicate the condition of the entire battery. *See:* **battery (primary or secondary).** 328

pilot channel. A channel over which a pilot is transmitted. 328

pilot circuit (industrial control). The portion of a control apparatus or system that carries the controlling signal from the master switch to the controller. *See:* **control.** 206

pilot director indicator. A device that indicates to the pilot information as to whether or not the aircraft has departed from the target track during a bombing run. 328

pilot exciter (1)(excitation systems for synchronous machines). The equipment providing the field current for the excitation of another exciter. 507
(2)(rotating machinery) (electric installations on shipboard). The source of all or part of the field current for the excitation of another exciter. 63, 3

pilot fit (spigot fit) (rotating machinery). A clearance hole and mating projection used to guide parts during assembly. 63

pilot house control (illuminating engineering). A mechanical means for controlling the elevation and train of a searchlight from a position on the other side of the bulkhead or deck on which it is mounted. 167

pilot lamp. A lamp that indicates the condition of an associated circuit. In telephone switching, a pilot lamp is a switchboard lamp that indicates a group of line lamps, one of which is or should be lit. 328

pilot light. A light, associated with a control, that by means of position or color indicates the functioning of the control. 328

pilot line (conductor stringing equipment). A lightweight line, normally synthetic fiber rope, used to pull heavier pulling lines which in turn are used to pull the conductor. Pilot lines may be installed with the aid of finger lines or by helicopter when the insulators and travelers are hung. *Syn:* **lead line; leader; P-line; straw line.** 431

pilot line winder (conductor stringing equipment). A device designed to payout and rewind pilot lines during stringing operations. It is normally equipped with its own engine which drives a drum or a supporting shaft for a reel mechanically, hydraulically or through a combination of both. These units are usually equipped with multiple drums or reels, depending upon the number of pilot lines required. The pilot line is payed out from the drum or reel, pulled through the travelers in the sag section, and attached to the pulling line on the reel stand or drum puller. It is then rewound to pull the pulling line through the travelers. 431

pilot protection (power switchgear). A form of line protection that uses a communication channel as a means to compare electrical conditions at the terminals of a line. 103

pilot streamer (lightning). The initial low-current discharge that begins when the voltage gradient exceeds the breakdown voltage of air. *See:* **direct-stroke protection (lightning).** 64

pilot wire. An auxiliary conductor used in connection with remote measuring devices or for operating apparatus at a distant point. *See:* **center of distribution.** 64

pilot-wire-controlled network. A network whose switching devices are controlled by means of pilot wires. *See:* **alternating-current distribution.** 64

pilot wire protection (power switchgear). Pilot protection in which a metallic circuit is used for the communicating means between relays at the circuit terminals. *See:* **wire-pilot protection.** 103

pilot-wire regulator. An automatic device for controlling adjustable gains or losses associated with transmission circuits to compensate for transmission changes caused by temperature variations, the control usually depending upon the resistance of a conductor or pilot wire having substantially the same temperature conditions as the conductors of the circuits being regulated. *See:* **transmission regulator.** 328

pinboard. A perforated board that accepts manually inserted pins to control the operation of equipment. 255, 77, 54

pinch (electron tubes). The part of the envelope of an electron tube or valve carrying the electrodes and through which pass the connections to the electrodes. *See:* **electron tube.** 244, 190

pinch effect (1) (rheostriction). The phenomenon of transverse contraction and sometimes momentary rupture of a fluid conductor due to the mutual attraction of the different parts carrying currents. *See:* **electrothermics; induction heating.** 210
(2) (disk recording). A pinching of the reproducing stylus tip twice each cycle in the reproduction of lateral recordings due to a decrease of the groove angle cut by the recording stylus when it is moving across the record as it swings from a negative to a positive peak. 176
(3) (induction heating). The result of an electromechanical force that constricts, and sometimes momentarily ruptures, a molten conductor carrying current at high density. *See:* **motor effect; skin effect.** 14

p-i-n detector (charged-particle detectors)(germanium gamma-ray detectors)(semiconductor radiation detectors)(X-ray energy spectrometers). A detector consisting of an intrinsic or nearly intrinsic region between a p and n region. 528, 23, 471

PIN diode (fiber optics). A diode with a large intrinsic region sandwiched between p- and n-doped semiconducting regions. Photons absorbed in this region create electron-hole pairs that are then separated by an

electric field, thus generating an electric current in a load circuit. 433

p-i-n diode attenuator (nonlinear, active, and nonreciprocal waveguide components). A device that provides a predetermined value of attenuation in a transmission line in response to a precise value of bias. 530

p-i-n diode limiter (nonlinear, active, and nonreciprocal waveguide components). A passive microwave power limiter that utilizes the nonlinear conductivity of p-i-n diodes. 530

pin insulator. A complete insulator, consisting of one insulating member or an assembly of such members without tie wires, clamps, thimbles, or other accessories, the whole being of such construction that when mounted on an insulator pin it will afford insulation and mechanical support to a conductor that has been properly attached with suitable accessories. *See:* **insulator; tower.** 64

pin jack. A single-conductor jack having an opening for the insertion of a plug of very small diameter. 341

pink noise (speech quality measurements). A random noise whose spectrum level has a negative slope of 10 decibels per decade. 126

pins (electron tube or valve). Metal pins connected to the electrodes that plug into the holder. They ensure the electric connection between the electrodes and the external circuit and also mechanically fix the tube in its holder. *See:* **electron tube.** 244, 190

pip. A popular term for a sharp deflection in a visible trace. *See:* **radar.** 328

pipe cable. A pressure cable in which the container for the pressure medium is a loose-fitting rigid metal pipe. *See:* **pressure cable; oil-filled pipe cable; gas-filled pipe cable.** 64

pipe guide. A component of a switch operating mechanism designed to maintain alignment of a vertical rod or shaft. 27

pipeline (National Electrical Code)(electrical heating systems). A length of pipe including pumps, valves, flanges, control devices, strainers and/or similar equipment for conveying fluids. 256, 476

pipelined transfer (FASTBUS acquisition and control). The portion of a FASTBUS operation in which a master either sends data to or causes data to be sent by an attached slave on every transition of data sync. The slave acknowledges receipt of or sends data with every transition of data acknowledge. The master does not wait for an acknowledge signal from the slave before causing another data sync transition. 480

pipe-ventilated (rotating machinery). *See:* **duct-ventilated.**

pip-matching display (navigation)(navigation aid terms). A display in which the received signal appears as a pair of blips, the comparison of the characteristics of which provides a measure of the desired quantity. 526

Pirani gauge. A bolometric vacuum gauge that depends for its operation on the thermal conduction of the gas present: pressure being measured as a function of the resistance of a heated filament ordinarily over a pressure range of 10^{-1} to 10^{-4} conventional millimeter of mercury. *See:* **instrument.** 328

piston (high-frequency communication practice) (plunger). A conducting plate movable along the inside of an enclosed transmission path and acting as a short-circuit for high-frequency currents. *See:* **waveguide.** 328

piston attenuator (waveguide). A variable cutoff attenuator in which one of the coupling devices is carried on a sliding member like a piston. *See:* **waveguide.** 244, 179

pistonphone. A small chamber equipped witha reciprocating piston of measurable displacement that permits the establishment of a known sound pressure in the chamber. *See:* **loudspeaker.** 176

pit (rotating machinery). A depressed area in a foundation under a machine. 63

pitch (acoustics) (audio and electroacoustics). The attribute of auditory sensation in terms of which sounds may be ordered on a scale extending from low to high, such as a musical scale. *Notes:* (1) Pitch depends primarily upon the frequency of the sound stimulus, but it also depends upon the sound pressure and wave form of the stimulus. (2) The pitch of a sound may be described by the frequency of that simple tone, having a specified sound pressure or loudness level, that seems to the average normal ear to produce the same pitch. (3) The unit of pitch is the mel. 176

pitch angle. *See:* **pitch attitude.**

pitch attitude (navigation aid terms). The angle between the longitudinal axis of the vehicle and the horizontal. *Syn:* **pitch angle.** 526

pitch factor (rotating machinery). The ratio of the resultant voltage induced in a coil to the arithmetic sum of the magnitudes of the voltages induced in the two coil sides. *See:* **armature.** 63

pits. Depressions produced in metal surfaces by nonuniform electrodeposition or from electrodissolution: for example, corrosion. *See:* **electrodeposition.** 328

pitting (corrosion). Localized corrosion taking the form of cavities at the surface. 205

pitting factor (corrosion). The depth of the deepest pit resulting from corrosion divided by the average penetration as calculated from weight loss. 205

PIV. *See:* **peak inverse voltage; peak reverse voltage (semiconductor rectifier).**

pivot-friction error. Error caused by friction between the pivots and the jewels: it is greatest when the instrument is mounted with the pivot axis horizontal. *Note:* This error is included with other errors into a combined error defined in **repeatability.** *See:* **moving element (instrument).** 280

pixel. *See:* **picture element.**

place. In positional notation, a position corresponding to a given power of the base, a given cumulated product, or a digit cycle of a given length. It can usually be specified as the *nth* character from one end of the numerical expression. 235

plain conductor. A conductor consisting of one metal only. *See:* **conductors.** 64

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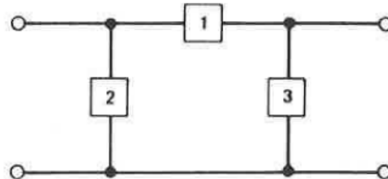
pi (π) mode (magnetrons). The mode of operation f(which the phases of the fields of successive anode openings facing the interaction space differ by p radians. *See:* **magnetrons.** 125

pi (π) network. A network composed of three branches connected in series with each other to form a mesh, the three junction points forming an input terminal, an output terminal, and a common input and output terminal, respectively. See accompanying figure. *See:* **network analysis.** 210



pi network. The junction point between branches 1 and 2 forms an input terminal, that between branches 1 and 3 forms an output terminal, and that between branches 2 and 3 forms a common input and output terminal.

pi (π) point. A frequency at which the insertion phase shift of an electric structure is 180 degrees or an integral multiple thereof. 328

pickle (corrosion) (electroplating). A solution or process used to loosen or remove corrosion products such as oxides, scale, and tarnish from a metal. *See:* **electroplating.** 205

pickling (electroplating) (1) (chemical). The removal of oxides or other compounds from a metal surface by means of a solution that acts chemically upon the compounds.

(2) (electrolytic). Pickling during which a current is passed through the pickling solution to the metal (cathodic pickling) or from the metal (anodic pickling). *See:* **electroplating.** 328

pickoff (1) (gyro; accelerometer). A device which produces a signal output, generally a voltage, as a function of the relative linear or angular displacement between two elements. 46

(2) (test, measurement and diagnostic equipment). A sensing device that responds to movement to create a signal or to effect some type of control. 54

pickoff axis (dynamically tuned gyro) (inertial sensor). The axis of angular displacement between the rotor and the case that results in the maximum signal per unit of rotation from the pickoff. 46

pickup (1) (of a relay) (power switchgear). The action of a relay as it makes designated response to progressive increase of input. As a qualifying term, the state of a relay when all response to progressive increase of input has been completed. Also used to identify the minimum value of an input quantity reached by progressive increases which will cause the relay to reach the pickup state from reset. *Note:* In describing the performance of relays having multiple inputs, [illegible] has been used to denote contact operation, in which case pickup value of any input is meaningful only when related to all other inputs. 103

(2) (electronics). A device that converts a sound, scene, or other form of intelligence into corresponding electric signals (for example, a microphone, a television camera, or a phonograph pickup). *See:* **microphone; phonograph pickup; television.** 178, 54

pickup and seal voltage (magnetically operated device) (industrial control). The minimum voltage at which the device moves from its deenergized into its fully energized position. *See:* **initial contact pressure.** 302

pickup current. *See:* **pickup value.**

pick-up factor (DF [direction finder] antenna system)(navigation aid terms). An index of merit expressed as the voltage across the receiver input impedance divided by the signal field strength to which the antenna system is exposed, the direction of arrival and polarization of the wave being such as to give maximum response. 526

pickup factor, direction-finder antenna system. An index of merit expressed as the voltage across the receiver input impedance divided by the signal field strength to which the antenna system is exposed, the direction of arrival and polarization of the wave being such as to give maximum response. *See:* **navigation.** 278, 187, 13

pickup spectral characteristic (color television). The set of spectral responses of the device, including the optical parts, that converts radiation to electric signals, as measured at the output terminals of the pickup tubes. *Note:* Because of nonlinearity, the spectral characteristics of some kinds of pickup tubes depend upon the magnitude of radiance used in the measurement. 18

pickup tube. *See:* **camera tube.**

pickup value. The minimum input that will cause a device to complete contact operation or similar designated action. *Note:* In describing the performance of devices having multiple inputs, the pickup value of an input is meaningful only when related to all other inputs. 103

pickup voltage (or current) (magnetically operated device). The voltage (or current) at which the device starts to operate when its operating coil is energized under conditions of normal operating temperature. *See:* **contactor.** 1, 206

pico (p)(mathematics of computing). A prefix indicating 10^{-12}. 564

pictorial format (pulse measurement). A graph, plot, or display in which a waveform is presented for observation or analysis. Any of the waveform formats defined in the following subsections may be presented in the pictorial format. 15

picture element (pixel). The smallest area of a television picture capable of being delineated by an electric signal passed through the system or part thereof. *Note:* It has three important properties, namely P_v, the vertical height of the picture element: P_h, the horizontal length of the picture element, and P_a, the aspect ratio

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semiconductor. An electronic conductor, with resistivity in the range between metals and insulators, in which the electric-charge-carrier concentration increases with increasing temperature over some temperature range. *Note:* Certain semiconductors possess two types of carriers, namely, negative electrons and positive holes. 245

semiconductor, compensated. A semiconductor in which one type of impurity or imperfection (for example, donor) paritally cancels the electric effects of the other type of impurity or imperfection (for example, acceptor). *See:* **semiconductor.** 245, 23

semiconductor controlled rectifier (SCR). An alternative name used for the reverse-blocking triode-thyristor. *Note:* The name of the actual semiconductor material (selenium, silicon, etcetera) may be substituted in place of the word **semiconductor** in the name of the components. *See:* **thyristor.** 245

semiconductor converters, classification. The following designations are intended to describe the functional characteristics of converters, but not necessarily the circuits or components used. *Note:* Forms A through D refer only to the converters. Rotational direction of motors may be changed by field or armature reversal.
(1) form A converter. A single converter unit in which the direct current can flow in one direction only and which is not capable of inverting energy from the load to the ac supply. Operates in quadrant I only (semiconverter).
(2) form B converter. A double converter unit in which the direct current can flow in either direction but which is not capable of inverting energy from the load to the ac supply. Operates in quadrants I and III only.
(3) form C converter. A single converter unit in which the direct current can flow in one direction only and which is capable of inverting energy from the load to the ac supply. Operates in quadrant I and IV.
(4) form D converter. A double converter unit in which the direct current can flow in either direction and which is capable of inverting energy from the load to the ac supply. Operates in quadrant I, II, III, and IV. 121

semiconductor device An electron device in which the characteristic distinguishing electronic conduction takes place within a semiconductor. *See:* **semiconductor.** 210

semiconductor device circuit breaker (thyristor). A circuit breaker of special characteristics used to isolate or protect semiconductor devices from overcurrent. 445

semiconductor device fuse (thyristor). A fuse of special characteristics connected in series with one or more semiconductor devices to isolate or protect the semiconductor. 445

semiconductor device lead inductance (nonlinear, active, and nonreciprocal waveguide components). The inductance of a semiconductor device associated with the strap, mesh, or wire connections used to contact the semiconductor chip. In general, a larger cross-sectional contacting area results in decreased lead inductance. 530

semiconductor diode (circuits and systems). A two-terminal device formed of a semiconductor junction having a nonlinear characteristic which will conduct electric current more in one direction than in the other. 267

semiconductor-diode parametric amplifier. A parametric amplifier using one or more varactors. *See:* **parametric device.** 191

semiconductor, extrinsic (1) (general). A semiconductor with charge-carrier concentration dependent upon impurities. *See:* **semiconductor.** 245
(2) (power semiconductor). A semiconductor in which the concentrations of holes and electrons are unbalanced by the introduction of impurities. 266

semiconductor frequency changer. A complete equipment employing semiconductor devices for changing from one alternating-current frequency to another. *See:* **semiconductor rectifier stack.** 208

semiconductor, intrinsic (1) (general). A semiconductor whose charge-carrier concentration is substantially the same as that of the ideal crystal. *See:* **semiconductor.** 245
(2) (power semiconductor). A semiconductor in which holes and electrons are created solely by thermal excitation across the energy gap. In an intrinsic semiconductor the concentration of holes and electrons must always be the same. 266

semiconductor junction (light emitting diodes). A region of transition between semiconductor regions of different electrical properties. 162

semiconductor laser. *See:* **injection laser diode (ILD).**

semiconductor, *n*-type. An extrinsic semiconductor in which the conduction electron concentration exceeds the mobile hole concentration.*Note:* It is implied that the net ionized impurity concentration is donor type. *See:* **semiconductor.** 245

semiconductor, *n*-type. An *n*-type semiconductor in which the excess conduction electron concentration is very large.*See:* **semiconductor.** 245

semiconductor, n^+-type. An *n*-type semiconductor in which the excess conduction electron concentration is very large. *See:* **semiconductor.** 245

semiconductor, p^+-type. A *p*-type semiconductor in which the excess mobile hole concentration is very large.*See:* **semiconductor.** 245

semiconductor, *p*-type. An extrinsic semiconductor in which the mobile hole concentration exceeds the conduction electron concentration.*Note:* It is implied that the net ionized impurity concentration is acceptor type. *See:* **semiconductor.** 245

semiconductor power converter. A complete equipment employing semiconductor devices for the transformation of electric power. *See:* **semiconductor rectifier stack.** 208

semiconductor radiation detector (1)(germanium gamma-ray detectors). A semiconductor device that utilizes the production and motion of excess free charge carriers in the semiconductor for the detection and measurement of particles or photons of incident radiation. 528

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sound power level, *A*-weighted (airborne sound measurements on rotating electric machinery). The *A*-weighted sound power level, in decibels, is equal to the sound power level determined by weighting each of the frequency bands. 129

sound pressure (1)(power station noise control). The instantaneous pressure measured in a sound wave, that is, the variation in atmospheric pressure. 500
(2)(transmission performance of telephone sets). The sound pressure at a point, is the total instantaneous pressure at that point, in the presence of a sound wave, minus the static pressure at that point. 491

sound pressure, effective (root-mean-square sound pressure). At a point over a time interval, the root-mean-square value of the instantaneous sound pressure at the point under consideration. In the case of periodic sound pressures, the interval must be an integral number of periods or an interval long compared to a period. In the case of nonperiodic sound pressures, the interval should be long enough to make the value obtained essentially independent of small changes in the length of the interval. *Note:* The term **effective sound pressure** is frequently shortened to **sound pressure.** 176

sound pressure, instantaneous (at a point). The total instantaneous pressure at that point minus the static pressure at that point. *Note:* The commonly used unit is the newton per square meter. 176

sound pressure level (1)(SPL)(measurement of sound pressure levels of ac power circuit breakers). Twenty times the logarithm to the base 10 of the ratio of the pressure of a sound to the reference sound pressure. Unless otherwise specified, the effective root-mean-square (rms) pressure is used. The reference sound pressure is 20 μPa. Unit: decibel (dB). 552
(2)(transmission performance of telephone sets). The sound pressure level, in decibels, of a sound is 20 times the logarithm to the base 10 of the ratio of the pressure of this sound to the reference pressure. The reference is one pascal (Pa). 491

sound probe. A device that responds to some characteristic of an acoustic wave (for example, sound pressure, particle velocity) and that can be used to explore and determine this characteristic in a sound field without appreciably altering the field. *Note:* A sound probe may take the form of a small microphone or a small tubular attachment added to a conventional microphone. *See:* instrument. 176

sound recording system. A combination of transducing devices and associated equipment suitable for storing sound in a form capable of subsequent reproduction. *See:* **phonograph pickup.** 176

sound reflection coefficient (surface). The ratio of the sound reflected by the surface to the sound incident upon the surface. Unless otherwise specified, reflection of sound energy in a diffuse sound field is assumed. 176

sound reproducing system. A combination of transducing devices and associated equipment for reproducing recorded sound. *See:* **loudspeaker.** 176

sound spectrum analyzer (sound analyzer). A device or system for measuring the band pressure level of a sound as a function of frequency. 176

sound tract (electroacoustics). A band that carries the sound record. In some cases, a plurality of such bands may be used. In sound film recording, the band is usually along the margin of the film. *See:* **phonograph pickup.** 176

sound transmission coefficient (interface or partition). The ratio of the transmitted to incident sound energy. Unless otherwise specified, transmission of sound energy between two diffuse sound fields is assumed. 176

source (1) (laser-maser). Taken to mean either laser of laser-illuminated reflecting surface. 363
(2) (metal-nitride-oxide field-effect transistor). Region in the device structure of an insulated-gate-field-effect transistor (IGFET) which contains the terminal from which charge carries flow into channel toward the drain. It has the potential which is less attractive than the drain for the carriers in the channel. 386

source efficiency (fiber optics). The ratio of emitted optical power of a source to the input electrical power. 433

source ground (signal-transmission system). Potential reference at the physical location of a source, usually the signal source. *See:* **signal.** 188

source impedance. *See:* **impedance, source; self-impedance.**

source language (software). (A) A language used to write source programs. (B) A language from which statements are translated. *See:* **source programs; target language.** 434

source/load impedance (loudness ratings of telephone connections). For the purposes of IEEE Std 661-1979 the source/load impedance used for determining loudness ratings (see 3.6-3.9) is considered to be 900 Ω resistive. *See:* **impedance matching network; source/ load impedance other than 900 Ω.** 409

source node (network analysis). A node having only outgoing branches. 282

source program (software). (1) A computer program that must be compiled, assembled, or interpreted before being executed by a computer. (2) A computer program expressed in a source language. *See:* **assemble; compile; computer; computer program; interpret; object program; source language.** 434

source resistance. The resistance presented to the input of a device by the source. *See:* **measurement system.** 295

source resistance rating. The value of source resistance that, when injected in an external circuit having essentially zero resistance, will either (1) double the dead band, or (2) shift the dead band by one-half its width. *See:* **measurement system.** 295

space (1) (data transmission). One of the two possible conditions of an element (bit); an open line in a neutral circuit. In Morse code, a duration of two unit intervals between characters and six unit intervals between words. 59

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tions of change and is generally given in the form of a curve as a function of the duration of an applied pulse. *See:* **principal voltage-current characteristic (principal characteristic); semiconductor rectifier stack.** 191

transient voltage capability (thyristor). Rated nonrepetitive peak reverse voltage. The maximum instantaneous value of any nonrepetitive transient reverse voltage which may occur across a thyristor without damage. 445

transimpedance (of a magnetic amplifier). The ratio of differential output voltage to differential control current. 171

transinformation (of an output symbol about an input symbol) (information theory). The difference between the information content of the input symbol and the conditional information content of the input symbol given the output symbol. *Notes:* (1) If x_i is an input symbol and y_j is an output symbol, the transinformation is equal to

$$[-\log p(x_i)] - [-\log p(x_i|y_j)] = \log \frac{p(x_i|y_j)}{p(x_i)} = \log \frac{p(x_i,y_j)}{p(x_i)p(y_j)}$$

where $p(x_i|y_j)$ is the conditional probability that x_i was transmitted when y_j is received, and $p(x_{i,yj})$ is the joint probability of x_i and y_j (2) This quantity has been called **transferred information, transmitted information,** and **mutual information.** *See:* **information theory.** 415

transistor. An active semiconductor device with three or more terminals. It is an analog device. 245

transistor, conductivity-modulation. A transistor in which the active properties are derived from minority-carrier modulation of the bulk resistivity of a semiconductor. *See:* **semiconductor; transistor.** 245

transistor, filamentary. A conductivity-modulation transistor with a length much greater than its transverse dimensions. *See:* **semiconductor; transistor.** 245

transistor, junction. A transistor having a base electrode and two or more junction electrodes. *See:* **transistor.** 245

transistor, point-contact. A transistor having a base electrode and two or more point-contact electrodes. *See:* **semiconductors; transistor.** 245

transistor, point-junction. A transistor having a base electrode and both point-contact and junction electrodes. *See:* **transistor.** 328

transistor reset preamplifier (germanium gamma-ray detectors). A charge-sensitive preamplifier in which the charge that accumulates on the feedback capacitor is periodically discharged through a suitably located transistor. 528

transistor, unipolar. A transistor that utilizes charge carriers of only one polarity. *See:* **semiconductor; transistor.** 245

transit (1)(navigation aid terms). A radio navigation system using low orbit satellites to provide world-wide coverage, with transmissions from the satellites at vhf (very high frequency) and uhf (ultra high frequency), in which fixes are determined from measurements of the Doppler shift of the continuous wave signal received from the moving satellite. 526

(2) (conductor stringing equipment). An instrument primarily used during construction of a line to survey the route, set hubs and point on tangent (POT) locations, plumb structures, determine downstrain angles for locations of anchors at the pull and tension sites, and to sag conductors. *Syn:* **level; scope; site marker.** 431

transit angle. The product of angular frequency and the time taken for an electron to traverse a given path. *See:* **electron emission.** 190, 125

transition (1) (data transmission). (A) (signal transmission). The change from one circuit condition to the other, that is, to change from mark to space or from space to mark. (B) (waveform) (pulse techniques). A change of the instantaneous amplitude from one amplitude to another amplitude level. (C) (transition frequency) (disk recording system) (crossover frequency) (turnover frequency). The frequency corresponding to the point of intersection of the asymptotes to the constant-amplitude and the constant-velocity portions of its frequency response curve. This curve is plotted with output voltage ratio in decibels as the ordinate and the logarithm of the frequency as the abscissa. 59

(2) (pulse terms). A portion of a wave or pulse between a first nominal state and a second nominal state. Throughout the remainder of this document the term transition is included in the term pulse and wave.

transitional mode (seismic testing of relays). The change from the nonoperating to the operating mode, caused by switching the input to the relay from the nonoperating to the operating input, or vice versa. 392

transition duration (pulse terms). The duration between the proximal point and the distal point on a transition waveform. 254

transition frequency (disk recording system) (crossover frequency) (turnover frequency). The frequency corresponding to the point of intersection of the asymptotes to the constant-amplitude and the constant-velocity portions of its frequency response curve. This curve is plotted with output voltage ratio in decibels as the ordinate and the logarithm of the frequency as the abscissa. *See:* **phonograph pickup.** 176

transition joint (power cable joint). A cable joint which connects two different types of cable. 34

transition load (rectifier circuit). The load at which a rectifier unit changes from one mode of operation to another. *Note:* The load current corresponding to a transition load is determined by the intersection of extensions of successive portions of the direct-current voltage-regulation curve where the curve changes shape or slope. *See:* **rectification; rectifier circuit element.** 66

transition loss (1) (wave propagation). (A) At a transition or discontinuity between two transmission media,

Dictionary of Electrical and Computer Engineering

The McGraw·Hill Companies

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1 2 3 4 5 6 7 8 9 0 DOC/DOC 0 9 8 7 6 5 4

ISBN 0-07-144210-3

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This book was set in Helvetica Bold and Novarese Book by TechBooks, Fairfax, Virginia. It was printed and bound by RR Donnelley, The Lakeside Press.

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Library of Congress Cataloging-in-Publication Data

McGraw-Hill dictionary of electrical and computer engineering.
p. cm.
ISBN 0-07-144210-3
1. Computer engineering—Dictionaries. 2. Electric engineering—Dictionaries.

TK7885.A2M37 2004
004'.03—dc22 2004049888

rence |COMMUN| A :he same frequency as er in a color television iase with respect to the ie reference with which ce signal is compared dulation or demodu- ırominance-subcarrier reference; color- 'krō·mə·nəns ¦kar·ē·ər

OMMUN| Any path that rominance signal in an stem. { 'krō·mə·nəns

|ELECTR| A demodu- olor television receiver Q components of the he chrominance signal carrier frequency. Also ıbcarrier demodulator. id·ər }

|COMMUN| The fre- ınce subcarrier, equal { 'krō·mə·nəns ,frē·

|ELECTR| Variable re- l blue matrix channels rimary signal levels in r. { 'krō·mə·nəns 'gān

|ELECTR| A modulator olor television trans- chrominance signal y chrominance compo- ıance subcarrier. Also -subcarrier modulator. ·ər }

MMUN| One of the two I signal and Q signal, oduce the total chromi- ng color television sys- ier chrominance signal.

ier |COMMUN| The rier whose modulation the monochrome signal tion in an analog color known as chrominance or subcarrier; subcarrier. ər }

modulator *See* chromi- 'krō·mə·nəns səb'kar·ē·

modulator *See* chro- 'krō·mə·nəns səb'kar·ē·

scillator *See* chroma osc- səb'kar·ē·ər 'äs·ə,lād·ər }
reference *See* chromi- . { 'krō·mə·nəns səb

chrominance video signal |ELECTR| Voltage output from the red, green, or blue section of a color television camera or receiver matrix. { 'krō·mə·nəns 'vid·ē·ō ,sig·nəl }

chromium dioxide tape |ELECTR| A magnetic recording tape developed primarily to improve quality and brilliance of reproduction when used in cassettes operated at 1⅞ inches per second (4.76 centimeters per second); requires special recorders that provide high bias. { 'krō·mē·əm dī'äk,sīd 'tāp }

chromium-gold metallizing |ELECTR| A metal film used on a silicon or silicon oxide surface in semiconductor devices because it is not susceptible to purple plague deterioration; a layer of chromium is applied first for adherence to silicon, then a layer of chromium-gold mixture and finally a layer of gold to which bonding contacts can be applied. { ¦krō·mē·əm ¦gōld 'med·əl·īz·iŋ }

chronistor |ELECTR| A subminiature elapsed-time indicator that uses electroplating principles to totalize operating time of equipment up to several thousand hours. { krə'nis·tər }

chronometric encoder |ELECTR| An encoder that uses an electronic counter to time or count electrical events and deliver in digital form a number equivalent to the input magnitude. { 'krän·ə,me·trik en'kōd·ər }

chronopher |ELECTR| Instrument for emitting standard time signal impulses from a standard clock or timing device. { 'krän·ə·fər }

chronotron |ELECTR| A device that measures millimicrosecond time intervals between pulses on a transmission line to determine the time between the events which initiated the pulses. { 'krän·ə ,trän }

chute blades |COMPUT SCI| Thin metal bands which form channels to the various pockets of a sorter. { 'shüt ,blādz }

C³I *See* command, control, communications, and intelligence. { 'sē 'thrē'ī }

CID *See* charge-injection device.

CIM *See* computer input from microfilm; computer-integrated manufacturing.

cinching |COMPUT SCI| Creases produced in magnetic tape when the supply reel is wound at low tension and suddenly stopped during playback. { 'sin·chiŋ }

C-indicator *See* C-display. { 'sē ,in·də,kād·ər }

cipher |COMMUN| A transposition or substitution code for transmitting secret messages. { 'sī·fər }

cipher block chaining |COMMUN| A technique for block chaining in which each block of ciphertext is produced by adding, through the EXCLUSIVE OR operation, the previous block of ciphertext to the current block of plaintext. Abbreviated CBC. { 'sī·fər ,bläk ,chān·iŋ }

cipher feedback |COMMUN| An implementation of ciphertext autokey cipher in which the leftmost *n* bits of the data encryption standard (DES) output are added by the EXCLUSIVE OR operation to N bits of plaintext to produce N bits of ciphertext (where N is the number of bits enciphered at one time), and these N bits of ciphertext are fed back into the algorithm by first shifting the current DES input N bits to the left, and then appending the N bits of ciphertext to the right-hand side of the shifted input to produce a new DES input used for the next iteration of the algorithm. { ¦sī·fər ¦fēd,bak }

cipher machine |COMMUN| Mechanical or electrical apparatus for enciphering and deciphering. { 'sī·fər mə'shēn }

ciphertext |COMMUN| A message which has been transformed by a cipher so that it can be read only by those privy to the secrets of the cipher. { 'sī·fər,tekst }

ciphertext autokey cipher |COMMUN| A stream cipher in which the cryptographic bit stream generated at a given time is determined by the ciphertext generated at earlier times. { 'sī·fər ,tekst 'ȯd·ō,kē ,sī·fər }

ciphony |COMMUN| A technique by which security is accomplished by converting speech into a series of on-off pulses and mixing these with the pulses supplied by a key generator; to recover the original speech, the identical key must be subtracted and the resultant on-off pulses reconverted into the original speech pattern; unauthorized listeners are unable to reconstruct the plain text unless they have an identical key generator and the daily key setting. { 'sī·fə·nē }

ciphony equipment |ELECTR| Any equipment attached to a radio transmitter, radio receiver, or telephone for scrambling or unscrambling voice messages. { 'sī·fə·nē i,kwip·mənt }

circle diagram |ELEC| A diagram which gives a graphical solution of equations for a transmission line, giving the input impedance of the line as a function of load impedance and electrical length of the line. { ¦sər·kəl ¦dī·ə,gram }

circle-dot mode |ELECTR| Mode of cathode-ray storage of binary digits in which one kind of digit is represented by a small circle of excitation of the screen, and the other kind by a similar circle with a concentric dot. { ¦sər·kəl ¦dät ,mōd }

circuit |ELEC| *See* electric circuit. |ELECTROMAG| A complete wire, radio, or carrier communications channel. { 'sər·kət }

circuit analyzer *See* volt-ohm-milliammeter. { 'sər·kət ,an·ə,līz·ər }

circuit board *See* printed circuit board. { 'sər·kət ,bȯrd }

circuit breaker |ELEC| An electromagnetic device that opens a circuit automatically when the current exceeds a predetermined value. { 'sər·kət ,brāk·ər }

circuit capacity |COMMUN| Number of communications channels which can be handled by a given circuit at the same time. { 'sər·kət kə'pas·əd·ē }

circuit conditioning |ELECTR| Test, analysis, engineering, and installation actions to upgrade a communications circuit to meet an operational requirement; includes the reduction of noise, the equalization of phase and level stability and frequency response, and the correction of impedance discontinuities, but does not include normal maintenance and repair activities. { 'sər·kət kən'dish·ə·niŋ }

circuit design |ELEC| The art of specifying the components and interconnections of an electrical network. { 'sər·kət də'zīn }

circuit diagram |ELEC| A drawing, using standardized symbols, of the arrangement and interconnections of the conductors and components of an electrical or electronic device or installation. Also known as schematic circuit diagram; wiring diagram. { 'sər·kət ,dī·ə,gram }

circuit efficiency |ELECTR| Of an electron tube, the power delivered to a load at the output terminals of the output circuit at a desired frequency divided by the power delivered by the electron stream to the output circuit at that frequency. { 'sər·kət i'fish·ən·sē }

circuit element *See* component. { 'sər·kət ¦el·ə·mənt }

circuit grade |COMMUN| A circuit rating defining the ability to carry information; grades include telegraph, voice, and broad-band. { 'sər·kət ,grād }

circuit interrupter |ELEC| A device in a circuit breaker to remove energy from an arc in order to extinguish it. { 'sər·kət ,in·tə,rəp·tər }

circuit loading |ELEC| Power drawn from a circuit by an electric measuring instrument, which may alter appreciably the quantity being measured. { 'sər·kət ,lōd·iŋ }

circuit noise |COMMUN| In telephone practice, the noise which is brought to the receiver electrically from a telephone system, excluding noise picked up acoustically by telephone transmitters. { 'sər·kət ,nȯiz }

circuit noise level |COMMUN| Ratio of the circuit noise at that point to some arbitrary amount of circuit noise chosen as a reference; usually expressed in decibels above reference noise, signifying the reading of a circuit noise meter, or in adjusted decibels, signifying circuit noise meter reading adjusted to represent interfering effect under specified conditions. { 'sər·kət ,nȯiz ,lev·əl }

circuit protection |ELECTR| Provision for automatically preventing excess or dangerous temperatures in a conductor and limiting the amount of energy liberated when an electrical failure occurs. { 'sər·kət prə'tek·shən }

circuit reliability |COMMUN| The percent of time a circuit was available to the user during a specified period of time. { 'sər·kət ri,lī·ə'bil·əd·ē }

circuitron |ELECTR| Combination of active and passive components mounted in a single envelope like that used for tubes, to serve as one or more complete operating stages. { 'sər·kyə ,trän }

circuitry |ELEC| The complete combination of circuits used in an electrical or electronic system or piece of equipment. { 'sər·kə·trē }

circuit shift *See* cyclic shift. { 'sər·kət ,shift }

circuit switching |COMMUN| **1.** The method of providing communication service through a switching facility, either from local users or from other switching facilities. **2.** A method of

dimension [COMPUT SCI] A declarative statement that specifies the width and height of an array of data items. { də'men·chən }

dimension declaration statement [COMPUT SCI] A FORTRAN statement identifying arrays and specifying the number and bounds of the subscripts. { də'men·chən·əl dek·lə'rā·shən ,stāt·mənt }

diminution [COMPUT SCI] Limiting the negative effect of an attack on a computer system. { ,dim·ə'nü·shən }

DIMM [COMPUT SCI] A small circuit board that holds semiconductor memory chips with two independent rows of input/output contacts. Derived from dual in-line memory module.

dimmer [ELEC] An electrical or electronic control for varying the intensity of a lamp or other light source. { 'dim·ər }

dina [ELECTR] An airborne radar-jamming transmitter operating in the band from 92 to 210 megahertz with an output of 30 watts, radiating noise in one side band for spot or barrage jamming; the carrier and the other side band are suppressed. { 'dī·nə }

D-indicator *See* D-display. { 'dē ,in·də,kād·ər }

diode [ELECTR] **1.** A two-electrode electron tube containing an anode and a cathode. **2.** *See* semiconductor diode. { 'dī,ōd }

diode alternating-current switch *See* trigger diode. { 'dī,ōd ¦ȯl·tər,nād·iŋ ¦kər·ənt ,swich }

diode amplifier [ELECTR] A microwave amplifier using an IMPATT, TRAPATT, or transferred-electron diode in a cavity, with a microwave circulator providing the input/output isolation required for amplification; center frequencies are in the gigahertz range, from about 1 to 100 gigahertz, and power outputs are up to 20 watts continuous-wave or more than 200 watts pulsed, depending on the diode used. { 'dī,ōd 'am·plə ,fī·ər }

diode bridge [ELECTR] A series-parallel configuration of four diodes, whose output polarity remains unchanged whatever the input polarity. { 'dī,ōd ,brij }

diode-capacitor transistor logic [ELECTR] A circuit that uses diodes, capacitors, and transistors to provide logic functions. { ¦dī,ōd kə¦pas·əd·ər tran'zis·tər ,läj·ik }

diode characteristic [ELECTR] The composite electrode characteristic of an electron tube when all electrodes except the cathode are connected together. { 'dī,ōd ,kar·ik·tə·'ris·tik }

diode clamp *See* diode clamping circuit. { 'dī,ōd ,klamp }

diode clamping circuit [ELECTR] A clamping circuit in which a diode provides a very low resistance whenever the potential at a certain point rises above a certain value in some circuits or falls below a certain value in others. Also known as diode clamp. { ¦dī,ōd 'klamp·iŋ ,sər·kət }

diode clipping circuit [ELECTR] A clipping circuit in which a diode is used as a switch to perform the clipping action. { ¦dī,ōd 'klip·iŋ ,sər·kət }

diode-connected transistor [ELECTR] A bipolar transistor in which two terminals are shorted to give diode action. { 'dī,ōd kə¦nek·təd tran'zis·tər }

diode demodulator [ELECTR] A demodulator using one or more diodes to provide a rectified output whose average value is proportional to the original modulation. Also known as diode detector. { 'dī,ōd dē'mäj·ə,lād·ər }

diode detector *See* diode demodulator. { 'dī,ōd di'tek·tər }

diode drop *See* diode forward voltage. { 'dī,ōd ,dräp }

diode forward voltage [ELECTR] The voltage across a semiconductor diode that is carrying current in the forward direction; it is usually approximately constant over the range of currents commonly used. Also known as diode drop; diode voltage; forward voltage drop. { 'dī,ōd ¦fȯr·wərd 'vōl·tij }

diode function generator [ELECTR] A function generator that uses the transfer characteristics of resistive networks containing biased diodes; the desired function is approximated by linear segments. { 'dī,ōd 'fəŋk·shən ,jen·ə,rād·ər }

diode gate [ELECTR] An AND gate that uses diodes as switching elements. { 'dī,ōd ,gāt }

diode laser *See* semiconductor laser. { 'dī,ōd ,lāz·ər }

diode limiter [ELECTR] A peak-limiting circuit employing a diode that becomes conductive when signal peaks exceed a predetermined value. { ,dī,ōd 'lim·əd·ər }

diode logic [ELECTR] An electronic circuit using current-steering diodes, such that the relations between input and output voltages correspond to AND or OR logic functions. { 'dī,ōd ,läj·ik }

diode matrix [ELECTR] A two-dimensional array of diodes used for a variety of purposes such as decoding and read-only memory. { 'dī,ōd ,mā·triks }

diode mixer [ELECTR] A mixer that uses a crystal or electron tube diode; it is generally small enough to fit directly into a radio-frequency transmission line. { 'dī,ōd ,mik·sər }

diode modulator [ELECTR] A modulator using one or more diodes to combine a modulating signal with a carrier signal; used chiefly for low-level signaling because of inherently poor efficiency. { 'dī,ōd 'mäj·ə,lād·ər }

diode pack [ELECTR] Combination of two or more diodes integrated into one solid block. { dī,ōd ,pak }

diode peak detector [ELECTR] Diode used in a circuit to indicate when peaks exceed a predetermined value. { 'dī,ōd 'pēk di,tek·tər }

diode-pentode [ELECTR] Vacuum tube having a diode and a pentode in the same envelope. { ¦dī ,ōd ¦pen,tōd }

diode rectifier [ELECTR] A half-wave rectifier of two elements between which current flows in only one direction. { 'dī,ōd 'rek·tə,fī·ər }

diode rectifier-amplifier meter [ELECTR] The most widely used vacuum tube voltmeter for measurement of alternating-current voltage;

the carrier and modulation frequencies. { ¦dəb·əl ¦sīd,band tranz'mish·ən }

double-sideband transmitted-carrier modulation *See* double-sideband modulation. { ¦dəb·əl ¦sīd ,band tranz¦mid·əd ¦kar·ē·ər ,mäj·ə'lā·shən }

double-sided board [ELECTR] A printed wiring board that contains circuitry on both external layers. { ¦dəb·əl ,sīd·əd 'bȯrd }

double-sided disk [COMPUT SCI] A diskette that can be written on both of its sides. { ¦dəb·əl ¦sīd·əd 'disk }

double-stream amplifier [ELECTR] Microwave traveling-wave amplifier in which amplification occurs through interaction of two electron beams having different average velocities. { ¦dəb·əl ,strēm 'am·plə,fī·ər }

double-stub tuner [ELECTROMAG] Impedance-matching device, consisting of two stubs, usually fixed three-eighths of a wavelength apart, in parallel with the main transmission lines. { ¦dəb·əl ,stəb 'tün·ər }

double-superheterodyne reception [COMMUN] Method of reception in which two frequency converters are employed before final detection. Also known as triple detection. { ¦dəb·əl ,sü·pər¦het·rə,dīn ri'sep·shən }

doublet antenna *See* dipole antenna. { 'dəb·lət an'ten·ə }

double-throw circuit breaker [ELEC] Circuit breaker by means of which a change in the circuit connections can be obtained by closing either of two sets of contacts. { ¦dəb·əl ,thrō 'sər·kət ,brāk·ər }

double-throw switch [ELEC] A switch that connects one set of two or more terminals to either of two other similar sets of terminals. { ¦dəb·əl ,thrō 'swich }

double-track tape recorder [ENG ACOUS] A tape recorder with a recording head that covers half the tape width, so two parallel tracks can be recorded on one tape. Also known as dual-track tape recorder; half-track tape recorder. { ¦dəb·əl ,trak 'tāp ri,kȯrd·ər }

double triode [ELECTR] An electron tube having two triodes in the same envelope. Also known as duotriode. { ¦dəb·əl 'trī,ōd }

doublet trigger [ELECTR] A trigger signal consisting of two pulses spaced a predetermined amount for coding purposes. { 'dəb·lət ,trig·ər }

double-tuned amplifier [ELECTR] Amplifier of one or more stages in which each stage uses coupled circuits having two frequencies of resonance, to obtain wider bands than those obtainable with single tuning. { ¦dəb·əl ,tünd 'am·plə,fī·ər }

double-tuned circuit [ELECTR] A circuit that is resonant to two adjacent frequencies, so that there are two approximately equal values of peak response, with a dip between. { ¦dəb·əl ,tünd 'sər·kət }

double-tuned detector [ELECTR] A type of frequency-modulation discriminator in which the limiter output transformer has two secondaries, one tuned above the resting frequency and the other tuned an equal amount below. { ¦dəb·əl ,tünd di'tek·tər }

double-winding synchronous generator [ELEC] Synchronous generator which has two similar windings, in phase with one another, mounted on the same magnetic structure but not connected electrically, designed to supply power to two independent external circuits. { ¦dəb·əl ¦wīnd·iŋ ¦siŋ·krə·nəs 'jen·ə,rād·ər }

double word [COMPUT SCI] A unit containing twice as many bits as a word. { ¦dəb·əl 'wərd }

double-word addressing [COMPUT SCI] An addressing mode in computers with short words (less than 16 bits) in which the second of two consecutive instruction words contains the address of a location. { ¦dəb·əl ,wərd 'a ,dres·iŋ }

doubly linked ring [COMPUT SCI] A cycle arrangement of data elements in which searches are possible in both directions. { ¦dəb·lē ¦liŋkt 'riŋ }

do-until structure [COMPUT SCI] A set of program statements that is executed once, and may then be executed repeatedly, depending on the results of a test specified in the first statement. { 'dü ən'til ,strək·chər }

do-while structure [COMPUT SCI] A set of program statements that is executed repeatedly, as long as some condition, specified in the first statement, remains in effect. { 'dü 'wīl ,strək·chər }

down-lead *See* lead-in. { 'dau̇n ,lēd }

downlink [COMMUN] The radio or optical transmission path downward from a communications satellite to the earth or an aircraft, or from an aircraft to the earth. { 'dau̇n,liŋk }

download [COMPUT SCI] To transfer a program or data file from a central computer to a remote computer or to the memory of an intelligent terminal. { 'dau̇n,lōd }

downward compatibility [COMPUT SCI] The ability of an older or smaller computer to accept programs from a newer or larger one. Also known as backward compatibility. { 'dau̇n·wərd kəm ,pad·ə'bil·əd·ē }

Dow oscillator *See* electron-coupled oscillator. { ¦dau̇ 'äs·ə,lād·ər }

DPCM *See* differential pulse-code modulation.

dpdt switch *See* double-pole double-throw switch. { ¦dē¦pē¦dē'tē ,swich }

DPMS *See* display power management signaling.

dpst switch *See* double-pole single-throw switch. { ¦dē¦pē¦es'tē ,swich }

drag [COMPUT SCI] To move an object across a screen by moving a pointing device while holding down the control button. { drag }

drag and drop [COMPUT SCI] A feature whereby operations are performed on objects, such as icons or blocks of text, by dragging them across the screen to a particular spot. { ¦drag ən 'dräp }

drag-cup motor [ELEC] An induction motor having a cup-shaped rotor or conducting material, inside of which is a stationary magnetic core. { 'drag ,kəp 'mōd·ər }

drain [ELEC] *See* current drain. [ELECTR] The region into which majority carriers flow in a field-effect transistor; it is comparable to the collector of a bipolar transistor and the anode of an electron tube. { drān }

cell that includes one or more electrochromic materials and an electrolyte. { i,lek·trə¦krōm·ik di'vīs }

electrochromic display [ELECTR] A solid-state passive display that uses organic or inorganic insulating solids which change color when injected with positive or negative charges. { i¦lek·trō¦krō·mik di'splā }

electrode [ELEC] An electric conductor through which an electric current enters or leaves a medium, whether it be an electrolytic solution, solid, molten mass, gas, or vacuum. { i'lek ,trōd }

electrode admittance [ELECTR] Quotient of dividing the alternating component of the electrode current by the alternating component of the electrode voltage, all other electrode voltages being maintained constant. { i'lek,trōd ad'mit·əns }

electrode capacitance [ELECTR] Capacitance between one electrode and all the other electrodes connected together. { i'lek,trōd kə'pas·əd·əns }

electrode characteristic [ELECTR] Relation between the electrode voltage and the current to an electrode, all other electrode voltages being maintained constant. { i'lek,trōd ,kar·ik·tə'ris·tik }

electrode conductance [ELECTR] Quotient of the inphase component of the electrode alternating current by the electrode alternating voltage, all other electrode voltage being maintained constant; this is a variational and not a total conductance. Also known as grid conductance. { i'lek,trōd kən'dək·təns }

electrode couple [ELEC] The pair of electrodes in an electric cell, between which there is a potential difference. { i'lek,trōd ,kə·pəl }

electrode current [ELECTR] Current passing to or from an electrode, through the interelectrode space within a vacuum tube. { i'lek,trōd ,kə·rənt }

electrode dark current [ELECTR] The electrode current that flows when there is no radiant flux incident on the photocathode in a phototube or camera tube. Also known as dark current. { i'lek ,trōd ¦därk 'kə·rənt }

electrode dissipation [ELECTR] Power dissipated in the form of heat by an electrode as a result of electron or ion bombardment. { i'lek,trōd ,dis·ə'pā·shən }

electrode drop [ELECTR] Voltage drop in the electrode due to its resistance. { i'lek,trōd ,dräp }

electrode impedance [ELECTR] Reciprocal of the electrode admittance. { i'lek,trōd im'pēd·əns }

electrode inverse current [ELECTR] Current flowing through an electrode in the direction opposite to that for which the tube is designed. { i'lek ,trōd 'in·vərs ,kə·rənt }

electrodeless discharge [ELECTR] An electric discharge generated by placing a discharge tube in a strong, high-frequency electromagnetic field. { i¦lek,trōd·ləs 'dis,chärj }

electrodeless lamp [ELECTR] A lamp based on an electrodeless discharge. { i¦lek,trōd·ləs 'lamp }

electrode potential [ELECTR] The instantaneous voltage of an electrode with respect to the cathode of an electron tube. Also known as electrode voltage. { i'lek,trōd pə'ten·chəl }

electrode resistance [ELECTR] Reciprocal of the electrode conductance; this is the effective parallel resistance and is not the real component of the electrode impedance. { i'lek,trōd ri'zis·təns }

electrode voltage *See* electrode potential. { i'lek ,trōd ,vōl·tij }

electrodynamic ammeter [ENG] Instrument which measures the current passing through a fixed coil and a movable coil connected in series by balancing the torque on the movable coil (resulting from the magnetic field of the fixed coil) against that of a spiral spring. { i,lek·trō·dī'nam·ik 'a,mēd·ər }

electrodynamic instrument [ENG] An instrument that depends for its operation on the reaction between the current in one or more movable coils and the current in one or more fixed coils. Also known as electrodynamometer. { i,lek·trō·dī'nam·ik 'in·strə·mənt }

electrodynamic loudspeaker [ENG ACOUS] Dynamic loudspeaker in which the magnetic field is produced by an electromagnet, called the field coil, to which a direct current must be furnished. { i,lek·trō·dī'nam·ik 'laüd,spēk·ər }

electrodynamic machine [ELEC] An electric generator or motor in which the output load current is produced by magnetomotive currents generated in a rotating armature. { i,lek·trō·dī'nam·ik mə'shēn }

electrodynamic wattmeter [ENG] An electrodynamic instrument connected as a wattmeter, with the main current flowing through the fixed coil, and a small current proportional to the voltage flowing through the movable coil. Also known as moving-coil wattmeter. { i,lek·trō·dī'nam·ik 'wät,mēd·ər }

electrodynamometer *See* electrodynamic instrument. { i,lek·trō,dī·nə'mäm·əd·ər }

electroexplosive [ENG] An initiator or a system in which an electric impulse initiates detonation or deflagration of an explosive. { i,lek·trō·ik 'splō·siv }

electrogram [ELECTR] A record of an image of an object made by sparking, usually on paper. { i'lek·trə,gram }

electrograph [ENG] Any plot, graph, or tracing produced by the action of an electric current on prepared sensitized paper (or other chart material) or by means of an electrically controlled stylus or pen. { i'lek·trə,graf }

electrographic pencil [ELECTR] A pencil used to make a conductive mark on paper, for detection by a conductive-mark sensing device. { i'lek·trə ,graf·ik 'pen·səl }

electrokinetic transducer [ELEC] An instrument which converts dynamic physical forces, such as vibration and sound, into corresponding electric signals by measuring the streaming potential generated by passage of a polar fluid through a permeable refractory-ceramic or fritted-glass member between two chambers. { i¦lek·trō·kə'ned·ik tranz'dü·sər }

insulation and keep out moisture. { 'gas ,fild 'kā·bəl }

gas-filled diode |ELECTR| A gas tube which is a diode, such as a cold-cathode rectifier or phanotron. { 'gas ,fild 'dī,ōd }

gas-filled rectifier *See* cold-cathode rectifier. { 'gas ,fild 'rek·tə,fī·ər }

gas-filled triode |ELECTR| A gas tube which has a grid or other control element, such as a thyratron or ignitron. { 'gas ,fild 'trī,ōd }

gas focusing |ELECTR| A method of concentrating an electron beam by utilizing the residual gas in a tube; beam electrons ionize the gas molecules, forming a core of positive ions along the path of the beam which attracts beam electrons and thereby makes the beam more compact. Also known as ionic focusing. { 'gas ,fō·kəs·iŋ }

gas-insulated substation |ELEC| An electric power substation in which all live equipment and busbars are housed in grounded metal enclosures sealed and filled with sulfur hexafluoride gas. { 'gas ,in·sə,lād·əd 'səb,stā·shən }

gas ionization |ELECTR| Removal of the planetary electrons from the atoms of gas filling an electron tube, so that the resulting ions participate in current flow through the tube. { ¦gas ,ī·ə·nə'zā·shən }

gas magnification |ELECTR| Increase in current through a phototube due to ionization of the gas in the tube. { ¦gas ,mag·nə·fə'kā·shən }

gas phototube |ELECTR| A phototube into which a quantity of gas has been introduced after evacuation, usually to increase its sensitivity. { ¦gas 'fōd·ō,tüb }

gas scattering |ELECTR| The scattering of electrons or other particles in a beam by residual gas in the vacuum system. { 'gas ,skad·ə·riŋ }

gas-sensitive field-effect transistor |ELECTR| A field-effect transistor whose gate electrode is composed of a material, such as palladium, that is sensitive to a particular gas, such as hydrogen, so that the gain of the transistor depends on the concentration of this gas. { 'gas ¦sen·səd·iv 'fēld i,fekt tran,zis·tər }

gassiness |ELECTR| Presence of unwanted gas in a vacuum tube, usually in relatively small amounts, caused by the leakage from outside or evolution from the inside walls or elements of the tube. { 'gas·ē·nəs }

gassing |ELEC| The evolution of gas in the form of small bubbles in a storage battery when charging continues after the battery has been completely charged. { 'gas·iŋ }

gassy tube |ELECTR| A vacuum tube that has not been fully evacuated or has lost part of its vacuum due to release of gas by the electrode structure during use, so that enough gas is present to impair operating characteristics appreciably. Also known as soft tube. { ¦gas·ē 'tüb }

gas tetrode *See* tetrode thyratron. { ¦gas 'te,trōd }

gas thermostatic switch |ELEC| A thermostatic switch in which heat causes the pressure of gas in a sealed metal bellows to increase, thereby moving the bellows and closing the contacts of a switch. { ¦gas 'thər·mə,stad·ik 'swich }

gas tube |ELECTR| An electron tube into which a small amount of gas or vapor is admitted after the tube has been evacuated; ionization of gas molecules during operation greatly increases current flow. { 'gas ,tüb }

gas vacuum breakdown |ELECTR| Ionization of residual gas in a vacuum, causing reverse conduction in an electron tube. { ¦gas ¦vak·yəm 'brāk ,daùn }

gate |ELECTR| **1.** A circuit having an output and a multiplicity of inputs and so designed that the output is energized only when a certain combination of pulses is present at the inputs. **2.** A circuit in which one signal, generally a square wave, serves to switch another signal on and off. **3.** One of the electrodes in a field-effect transistor. **4.** To control the passage of a pulse or signal. **5.** In radar, an electric waveform which is applied to the control point of a circuit to alter the mode of operation of the circuit at the time when the waveform is applied. Also known as gating waveform. **6.** In radar, an electronic waveform applied to a circuit or a timing cue applied to logic to alter the operation of the circuit or logic at the appropriate time; generally used in anticipation of an input of particular interest. { gāt }

gate-array device |ELECTR| An integrated logic circuit that is manufactured by first fabricating a two-dimensional array of logic cells, each of which is equivalent to one or a few logic gates, and then adding final layers of metallization that determine the exact function of each cell and interconnect the cells to form a specific network when the customer orders the device. { 'gāt ə ,rā di,vīs }

gate-controlled rectifier |ELECTR| A three-terminal semiconductor device, such as a silicon controlled rectifier, in which the unidirectional current flow between the rectifier terminals is controlled by a signal applied to a third terminal called the gate. { 'gāt kən,trōld 'rek·tə,fī·ər }

gate-controlled switch |ELECTR| A semiconductor device that can be switched from its nonconducting or "off" state to its conducting or "on" state by applying a negative pulse to its gate terminal and that can be turned off at any time by applying reverse drive to the gate. Abbreviated GCS. { 'gāt kən,trōld 'swich }

gated-beam tube |ELECTR| A pentode electron tube having special electrodes that form a sheet-shaped beam of electrons; this beam may be deflected away from the anode by a relatively small voltage applied to a control electrode, thus giving extremely sharp cutoff of anode current. { ¦gād·əd ¦bēm ,tüb }

gated sweep |ELECTR| Sweep in which the duration as well as the starting time is controlled to exclude undesired echoes from the indicator screen. { ¦gād·əd 'swēp }

gate equivalent circuit |ELECTR| A unit of measure for specifying relative complexity of digital circuits, equal to the number of individual logic gates that would have to be interconnected to

photocomposition [COMPUT SCI] Composition of type using electrophotographic techniques such as phototypesetters and laser printers. { ,fōd·ō ,käm·pə'zish·ən }

photoconduction [SOLID STATE] An increase in conduction of electricity resulting from absorption of electromagnetic radiation { ¦fōd·ō·kən'dək·shən }

photoconductive cell [ELECTR] A device for detecting or measuring electromagnetic radiation by variation of the conductivity of a substance (called a photoconductor) upon absorption of the radiation by this substance. Also known as photoresistive cell; photoresistor. { ¦fōd·ō·kən'dək·tiv 'sel }

photoconductive device [ELECTR] A photoelectric device which utilizes the photoinduced change in electrical conductivity to provide an electrical signal. { fōd·ō·kən'dək·tiv di'vīs }

photoconductive film [ELECTR] A film of material whose current-carrying ability is enhanced when illuminated. { fōd·ō·kən'dək·tiv 'film }

photoconductive gain factor [ELECTR] The ratio of the number of electrons per second flowing through a circuit containing a cube of semiconducting material, whose sides are of unit length, to the number of photons per second absorbed in this volume. { fōd·ō·kən'dək·tiv 'gān ,fak·tər }

photoconductive meter [ELECTR] An exposure meter in which a battery supplies power through a photoconductive cell to a milliammeter. { fōd·ō·kən'dək·tiv 'med·ər }

photoconductivity [SOLID STATE] The increase in electrical conductivity displayed by many nonmetallic solids when they absorb electromagnetic radiation. { ¦fōd·ō·,kän,dək'tiv·əd·ē }

photoconductivity gain [ELECTR] The number of charge carriers that circulate through a circuit involving a photoconductor for each charge carrier generated by light. { fōd·ō,kän,dək'tiv·əd·ē ,gān }

photoconductor [SOLID STATE] A nonmetallic solid whose conductivity increases when it is exposed to electromagnetic radiation. { ¦fōd·ō·kən'dək·tər }

photoconductor diode *See* photodiode. { fōd·ō·kən'dək·tər 'dī,ōd }

photocoupler *See* optoisolator. { ¦fōd·ō'kəp·lər }

photodarlington [ELECTR] A Darlington amplifier in which the input transistor is a phototransistor. { ¦fōd·ō'där·liŋ·tən }

photodetector [ELECTR] A detector that responds to radiant energy; examples include photoconductive cells, photodiodes, photoresistors, photoswitches, phototransistors, phototubes, and photovoltaic cells. Also known as light-sensitive cell; light-sensitive detector; light sensor photodevice; photodevice; photoelectric detector; photosensor. { ¦fōd·ō·di'tek·tər }

photodevice *See* photodetector. { ¦fōd·ō·di,vīs }

photodiffusion effect *See* Dember effect. { ¦fōd·ō·di'fyü·zhən i,fekt }

photodiode [ELECTR] A semiconductor diode in which the reverse current varies with illumination; examples include the alloy-junction photocell and the grown-junction photocell. Also known as photoconductor diode. { ¦fōd·ō'dī ,ōd }

photoelectric [ELECTR] Pertaining to the electrical effects of light, such as the emission of electrons, generation of voltage, or a change in resistance when exposed to light. { ¦fōd·ō·i 'lek·trik }

photoelectric absorption [ELECTR] Absorption of photons in one of the several photoelectric effects. { ¦fōd·ō·i'lek·trik əb'sörp·shən }

photoelectric cell *See* photocell. { ¦fōd·ō·i'lek·trik 'sel }

photoelectric constant [ELECTR] The ratio of the frequency of radiation causing emission of photoelectrons to the voltage corresponding to the energy absorbed by a photoelectron; equal to Planck's constant divided by the electron charge. { ¦fōd·ō·i'lek·trik 'kän·stənt }

photoelectric control [ELECTR] Control of a circuit or piece of equipment by changes in incident light. { ¦fōd·ō·i'lek·trik kən'trōl }

photoelectric counter [ELECTR] A photoelectrically actuated device used to record the number of times a given light path is intercepted by an object. { ¦fōd·ō·i'lek·trik 'kaùnt·ər }

photoelectric cutoff register control [ELECTR] Use of a photoelectric control system as a longitudinal position regulator to maintain the position of the point of cutoff with respect to a repetitive pattern of moving material. { ¦fōd·ō·i'lek·trik ¦kət,ȯf ¦rej·ə·stər kən,trōl }

photoelectric detector *See* photodetector. { ¦fōd·ō·i'lek·trik di'tek·tər }

photoelectric device [ELECTR] A device which gives an electrical signal in response to visible, infrared, or ultraviolet radiation. { ¦fōd·ō·i'lek·trik di¦vīs }

photoelectric effect *See* photoelectricity. { ¦fōd·ō·i'lek·trik i,fekt }

photoelectric electron-multiplier tube *See* multiplier phototube. { ¦fōd·ō·i'lek·trik ¦i'lek,trän 'məl·tə,plī·ər ,tüb }

photoelectric infrared radiation *See* near-infrared radiation. { ¦fōd·ō·i'lek·trik ¦in·frə¦red ,rā·dē'ā·shən }

photoelectric intrusion detector [ELECTR] A burglar-alarm system in which interruption of a light beam by an intruder reduces the illumination on a phototube and thereby closes an alarm circuit. { ¦fōd·ō·i'lek·trik in'trü·zhən di,tek·tər }

photoelectricity [ELECTR] The liberation of an electric charge by electromagnetic radiation incident on a substance; includes photoemission, photoionization, photoconduction, the photovoltaic effect, and the Auger effect (an internal photoelectric process). Also known as photoelectric effect; photoelectric process. { ¦fōd·ō,i ,lek'tris·əd·ē }

photoelectric lighting control [ELECTR] Use of a photoelectric relay actuated by a change in illumination in a given area or at a given point. { ¦fōd·ō·i'lek·trik 'līd·iŋ kən,trōl }

photomultiplier counter [ELECTR] A scintillation counter that has a built-in multiplier phototube. { ¦fōd·ō'məl·tə,plī·ər ¦kaunt·ər }

photomultiplier tube *See* multiplier phototube. { ¦fōd·ō'məl·tə,plī·ər ¦tüb }

photon coupled isolator [ELECTR] Circuit coupling device, consisting of an infrared emitter diode coupled to a photon detector over a short shielded light path, which provides extremely high circuit isolation. { 'fō,tän ¦kəp·əld 'ī·sə,lād·ər }

photon coupling [ELECTR] Coupling of two circuits by means of photons passing through a light pipe. { 'fō,tän ,kəp·liŋ }

photonegative [ELECTR] Having negative photoconductivity, hence decreasing in conductivity (increasing in resistance) under the action of light; selenium sometimes exhibits photonegativity. { ¦fōd·ō'neg·ə·tiv }

photonics [ELECTR] The electronic technology involved with the practical generation, manipulation, analysis, transmission, and reception of electromagnetic energy in the visible, infrared, and ultraviolet portions of the light spectrum. It contributes to many fields, including astronomy, biomedicine, data communications and storage, fiber optics, imaging, optical computing, optoelectronics, sensing, and telecommunications. Also known as optoelectronics. { fō'tän·iks }

photopositive [ELECTR] Having positive photoconductivity, hence increasing in conductivity (decreasing in resistance) under the action of light; selenium ordinarily has photopositivity. { ¦fōd·ō'päz·əd·iv }

photoresistive cell *See* photoconductive cell. { ¦fōd·ō·ri'zis·tiv 'sel }

photoresistor *See* photoconductive cell. { ¦fōd·ō·ri'zis·tər }

photo-SCR *See* light-activated silicon controlled rectifier. { ¦fōd·ō ¦es¦sē'är }

photosensitive *See* light-sensitive. { ¦fod·ō'sen·səd·iv }

photosensor *See* photodetector. { ¦fōd·ō'sen·sər }

phototelegraphy *See* facsimile. { ¦fōd·ō·tə'leg·rə·fē }

photothyristor *See* light-activated silicon controlled rectifier. { ¦fōd·ō·thī'ris·tər }

phototransistor [ELECTR] A junction transistor that may have only collector and emitter leads or also a base lead, with the base exposed to light through a tiny lens in the housing; collector current increases with light intensity, as a result of amplification of base current by the transistor structure. { ¦fōd·ō·tran'zis·tər }

phototronic photocell *See* photovoltaic cell. { ¦fōd·ə¦trän·ik 'fōd·ə,sel }

phototube [ELECTR] An electron tube containing a photocathode from which electrons are emitted when it is exposed to light or other electromagnetic radiation. Also known as electric eye; light-sensitive tube; photoelectric tube. { 'fōd·ō ,tüb }

phototube cathode [ELECTR] The photoemissive surface which is the most negative element of a phototube. { 'fōd·ō,tüb 'kath,ōd }

phototube relay [ELECTR] A photoelectric relay in which a phototube serves as the light-sensitive device. { 'fōd·ō,tüb 'rē,lā }

photovaristor [ELECTR] Varistor in which the current-voltage relation may be modified by illumination, for example, one in which the semiconductor is cadmium sulfide or lead telluride. { ¦fōd·ō·və'ris·tər }

photovoltaic [ELECTR] Capable of generating a voltage as a result of exposure to visible or other radiation. { ¦fod·o·vōl'tā·ik }

photovoltaic cell [ELECTR] A device that detects or measures electromagnetic radiation by generating a potential at a junction (barrier layer) between two types of material, upon absorption of radiant energy. Also known as barrier-layer cell; barrier-layer photocell; boundary-layer photocell; photronic photocell. { ¦fōd·ō·vōl'tā·ik ,sel }

photovoltaic effect [ELECTR] The production of a voltage in a nonhomogeneous semiconductor, such as silicon, or at a junction between two types of material, by the absorption of light or other electromagnetic radiation. { ¦fōd·ō·vōl'tā·ik i ,fekt }

photovoltaic meter [ELECTR] An exposure cell in which a photovoltaic cell produces a current proportional to the light falling on the cell, and this current is measured by a sensitive microammeter. { ¦fōd·ō·vōl'tā·ik ,mēd·ər }

photox cell [ELECTR] Type of photovoltaic cell in which a voltage is generated between a copper base and a film of cuprous oxide during exposure to visible or other radiation. { 'fō,läks ,sel }

photronic cell [ELECTR] Type of photovoltaic cell in which a voltage is generated in a layer of selenium during exposure to visible or other radiation. { fō'trän·ik ,sel }

photronic photocell *See* photovoltaic cell. { fō'trän·ik 'fōd·ə,sel }

phrase name *See* metavariable. { 'frāz ,nām }

physical data independence [COMPUT SCI] A file structure such that the physical structure of the data can be modified without changing the logical structure of the file. { 'fiz·ə·kəl ¦dad·ə ,in·di'pen·dəns }

physical data structure [COMPUT SCI] The manner in which data are physically arranged on a storage medium, including various indices and pointers. { 'fiz·ə·kəl 'dad·ə ,strək·chər }

physical device table [COMPUT SCI] A table associated with a physical input/output unit containing such information as the device type, an indication of data paths that may be used to transfer information to and from the device, status information on whether the device is busy, the input/output operation currently pending on the device, and the availability of any storage contained in the device. { 'fiz·ə·kəl di¦vīs ,tā·bəl }

physical drive [COMPUT SCI] An operational hard disk, which may be formatted to include more than one logical drive. { 'fiz·i·kəl ¦drīv }

physical electronics [ELECTR] The study of physical phenomena basic to electronics, such as discharges, thermionic and field emission,

pilot lamp [ELEC] A small lamp used to indicate that a circuit is energized. Also known as pilot light. { 'pī·lət ,lamp }

pilot light *See* pilot lamp. { 'pī·lət ,līt }

pilot motor [ELEC] A small motor used in the automatic control of an electric current. { 'pī·lət ,mōd·ər }

pilot relaying [ELEC] A system for protecting transmission consisting of protective relays at line terminals and a communication channel between relays which is used by the relays to determine if a fault is within the protected line section, in which case all terminals are tripped simultaneously at high speed, or outside it, in which case tripping is blocked. { 'pī·lət rē,lā·iŋ }

pilot system [COMPUT SCI] A system for evaluating new procedures for handling data in which a sample that is representative of the data to be handled is processed. { 'pī·lət ,sis·təm }

pilot test [COMPUT SCI] A test of a computer system under operating conditions and in the environment for which the system was designed. { 'pī·lət ,test }

pilot tone [COMMUN] Single frequency transmitted over a channel to operate an alarm or automatic control. { 'pī·lət ,tōn }

pilot wire regulator [CONT SYS] Automatic device for controlling adjustable gains or losses associated with transmission circuits to compensate for transmission changes caused by temperature variations, the control usually depending upon the resistance of a conductor or pilot wire having substantially the same temperature conditions as the conductors of the circuits being regulated. { 'pī·lət ¦wīr 'reg·yə,lād·ər }

PIM *See* personal information manager. { ¦pē¦ī'em *or* pim }

pi mode [ELECTR] Of a magnetron, the mode of operation for which the phases of the fields of successive anode openings facing the interaction space differ by pi radians. { 'pī ,mōd }

pin [ELECTR] A terminal on an electron tube, semiconductor, integrated circuit, plug, or connector. Also known as base pin; prong. { pin }

pinch effect [ELEC] Manifestation of the magnetic self-attraction of parallel electric currents, such as constriction of ionized gas in a discharge tube, or constriction of molten metal through which a large current is flowing. Also known as cylindrical pinch; magnetic pinch; rheostriction. { 'pinch i,fekt }

pinch-off voltage [ELECTR] Of a field-effect transistor, the voltage at which the current flow between source and drain is blocked because the channel between these electrodes is completely depleted. { 'pinch,ȯf ,vōl·tij }

pinch resistor [ELECTR] A silicon integrated-circuit resistor produced by diffusing an *n*-type layer over a *p*-type resistor; this narrows or pinches the resistive channel, thereby increasing the resistance value. { 'pinch ri'zis·tər }

pinch roller [ELECTR] A small, freely turning wheel that presses the magnetic tape against the capstan in order to move the tape. { 'pinch ,rō·lər }

pincushion distortion [ELECTR] Distortion in which all four sides of a video image are concave (curving inward). { 'pin,ku̇sh·ən di,stȯr·shən }

pin diode [ELECTR] A diode consisting of a silicon wafer containing nearly equal *p*-type and *n*-type impurities, with additional *p*-type impurities diffused from one side and additional *n*-type impurities from the other side; this leaves a lightly doped intrinsic layer in the middle, to act as a dielectric barrier between the *n*-type and *p*-type regions. Also known as power diode. { 'pin 'dī,ōd }

pine-tree array [ELECTROMAG] Array of dipole antennas aligned in a vertical plane known as the radiating curtain, behind which is a parallel array of dipole antennas forming a reflecting curtain. { 'pīn ,trē ə,rā }

pi network [ELEC] An electrical network which has three impedance branches connected in series to form a closed circuit, with the three junction points forming an output terminal, an input terminal, and a common output and input terminal. { 'pī ,net,wərk }

pin-feed printer [COMPUT SCI] A computer printer in which the paper is aligned and advanced by protrusions on two wheels which engage evenly spaced holes along the edges of the paper. Also known as tractor-feed printer. { 'pin ¦fēd 'print·ər }

ping [ELECTR] A sonic or ultrasonic pulse sent out by an echo-ranging sonar. { piŋ }

pinger [ENG ACOUS] A battery-powered, low-energy source for an echo sounder. { 'piŋ·ər }

ping-pong [COMMUN] To switch a transmission so that it travels in the opposite direction. [COMPUT SCI] The programming technique of using two magnetic tape units for multiple reel files and switching automatically between the two units until the complete file is processed. { 'piŋ,päŋ }

pin jack [ELEC] Single conductor jack having an opening for the insertion of a plug of very small diameter. { 'pin ,jak }

pin junction [ELECTR] A semiconductor device having three regions: *p*-type impurity, intrinsic (electrically pure), and *n*-type impurity. { 'pin ,jəŋk·shən }

pinout [ELECTR] A graphic or text description of the function of electronic signals transmitted through each pin and receptacle in a connector. { 'pin,au̇t }

PIOCS [COMPUT SCI] An extension of the hardware, constituting an interface between programs and data channels; opposed to LIOCS, logical input/output control system. Derived from physical input/output control system. { 'pī,äks }

pip *See* blip. { pip }

pipe [COMPUT SCI] Any software-controlled technique for transfering data from one program or task to another during processing. { pīp }

pipelining [COMPUT SCI] A procedure for processing instructions in a computer program more rapidly, in which each instruction is divided into numerous small stages, and a population of instructions are in various stages at any given time. { 'pīp,līn·iŋ }

pipe-to-soil potential [ELEC] The voltage potential (emf) generated between a buried pipe and its surrounding soil, the result of electrolytic action and a cause of electrolytic corrosion of the pipe. { 'pīp tə ¦sȯil pə,ten·chəl }

pi point [ELEC] Frequency at which the insertion phase shift of an electric structure is 180° or an integral multiple of 180° { 'pī ,pȯint }

pi section filter [ELEC] An electric filter made of several pi networks connected in series. { 'pī ,sek·shən ,fil·tər }

piston [ELECTROMAG] A sliding metal cylinder used in waveguides and cavities for tuning purposes or for reflecting essentially all of the incident energy. Also known as plunger; waveguide plunger. { 'pis·tən }

piston attenuator [ELECTROMAG] A microwave attenuator inserted in a waveguide to introduce an amount of attenuation that can be varied by moving an output coupling device along its longitudinal axis. { 'pis·tən ə'ten·yə,wād·ər }

pitch [COMPUT SCI] The distance between the centerlines of adjacent rows of hole positions in punched paper tape. { pich }

pitch-row [COMPUT SCI] The distance between two adjacent holes in a paper tape. { 'pich ,rō }

pi-T transformation *See* Y-delta transformation. { ¦pī 'tē ,tranz·fər,mā·shən }

pixel [COMPUT SCI] The smallest part of an electronically coded picture image. [ELECTR] The smallest addressable element in an electronic display; a short form for picture element. Also known as pel. { pik'sel }

PL/1 [COMPUT SCI] A multipurpose programming language, developed by IBM for the Model 360 systems, which can be used for both commercial and scientific applications. { ¦pē¦el'wən }

PLA *See* programmed logic array.

placeholder [COMPUT SCI] A section of computer storage reserved for information that will be provided later. { 'plās,hōl·dər }

plaintext [COMMUN] The form of a message in which it can be generally understood, before it has been transformed by a code or cipher into a form in which it can be read only by those privy to the secrets of the cipher. [COMPUT SCI] Data that are to be encrypted. { 'plān,tekst }

plain vanilla *See* vanilla. { 'plān və'nil·ə }

planar area [COMPUT SCI] In computer graphics, an object with boundaries, such as a circle or polygon. { 'plān ər ,ėr·ē ə }

planar array [ELECTR] An array of ultrasonic transducers that can be mounted in a single plane or sheet, to permit closer conformation with the hull design of a sonar-carrying ship. { 'plā·nər ə¦rā }

planar-array antenna [ELECTROMAG] An array antenna in which the centers of the radiating elements are all in the same plane. { 'plā·nər ə¦rā an'ten·ə }

planar ceramic tube [ELECTR] Electron tube having parallel planar electrodes and a ceramic envelope. { 'plā·nər sə¦ram·ik 'tüb }

planar device [ELECTR] A semiconductor device having planar electrodes in parallel planes, made by alternate diffusion of *p*- and *n*-type impurities into a substrate. { 'plā·nər di,vīs }

planar diode [ELECTR] A diode having planar electrodes in parallel planes. { 'plā nər 'dī,ōd }

planar photodiode [ELECTR] A vacuum photodiode consisting simply of a photocathode and an anode; light enters through a window sealed into the base, behind the photocathode. { 'plā nər ¦fōd·ō'dī,ōd }

planar process [ENG] A silicon-transistor manufacturing process in which a fractional-micrometer-thick oxide layer is grown on a silicon substrate; a series of etching and diffusion steps is then used to produce the transistor inside the silicon substrate. { 'plā·nər ,prä·səs }

planar transistor [ELECTR] A transistor constructed by an etching and diffusion technique in which the junction is never exposed during processing, and the junctions reach the surface in one plane; characterized by very low leakage current and relatively high gain. { 'plā·nər tran'zis·tər }

plane [ELECTR] Screen of magnetic cores; planes are combined to form stacks. { plān }

plane earth [ELECTROMAG] Earth that is considered to be a plane surface as used in ground-wave calculations. { 'plān ,ərth }

plane-earth attenuation [ELECTROMAG] Attenuation of an electromagnetic wave over an imperfectly conducting plane earth in excess of that over a perfectly conducting plane. { 'plān ,ərth ə,ten·yə'wā·shən }

plane of polarization [ELECTROMAG] Plane containing the electric vector and the direction of propagation of electromagnetic wave. { 'plān əv ,pō·lə·rə'zā·shən }

plane polarization *See* linear polarization. { 'plān ,pō·lə·rə'zā·shən }

plane-polarized wave [ELECTROMAG] An electromagnetic wave whose electric field vector at all times lies in a fixed plane that contains the direction of propagation through a homogeneous isotropic medium. { 'plān ¦pō·lə,rīzd ,wāv }

plane reflector *See* passive reflector. { 'plān ri ¦flek·tər }

planetary wave *See* long wave. { 'plan·ə,ter·ē 'wāv }

planigraphy *See* sectional radiography. { plə 'nig·rə·fē }

planoconvex spotlight [ELEC] A light that can be used as a sharply defined spotlight or for soft-edged lighting; ranges in power from 100 to 2000 watts. { ¦plā·nō'kän,veks 'spät,līt }

plan position indicator [ELECTR] A radar display in which echoes from various targets appear as bright spots at the same locations as they would on a circular map of the area being scanned, the radar antenna being at the center of the map. Variations of the plan position indicator format include limited-sector display with the radar location offset from the center appropriately, the orientation to true or magnetic north or the radar-vehicle heading at the top, and so on. Abbreviated PPI. { 'plan pə'zish·ən 'in·də,kād·ər }

plan position indicator repeater [ELECTR] Unit which repeats a plan position indicator (PPI)

self-steering microwave array [ELECTROMAG] An antenna array used with electronic circuitry that senses the phase of incoming pilot signals and positions the antenna beam in their direction of arrival. { 'self ¦stir·iŋ 'mī·krō,wāv ə'rā }

self-synchronous device See synchro. { ¦self ¦siŋ·krə·nəs di'vīs }

self-synchronous repeater See synchro. { ¦self ¦siŋ·krə·nəs ri'pēd·ər }

self-test See self-diagnostic routine. { 'self ¦test }

self-triggering program [COMPUT SCI] A computer program which automatically commences execution as soon as it is fed into the central processing unit. { ¦self ¦trig·ə·riŋ 'prō·grəm }

self-tuning regulator [CONT SYS] A type of adaptive control system composed of two loops, an inner loop which consists of the process and an ordinary linear feedback regulator, and an outer loop which is composed of a recursive parameter estimator and a design calculation, and which adjusts the parameters of the regulator. Abbreviated STR. { ¦self ¦tün·iŋ 'reg·yə,lād·ər }

selsyn See synchro. { 'sel·sin }

selsyn generator See synchro transmitter. { 'sel·sin ,jen·ə,rād·ər }

selsyn motor See synchro receiver. { 'sel·sin ,mōd·ər }

selsyn receiver See synchro receiver. { 'sel·sin ri,sē·vər }

selsyn system See synchro system. { 'sel·sin ,sis·təm }

selysn transmitter See synchro transmitter. { 'sel·sin tranz,mid·ər }

SEM See scanning electron microscope.

semantic analysis [COMPUT SCI] A phase of natural language processing, following parsing, that involves extraction of context-independent aspects of a sentence's meaning, including the semantic roles of entities mentioned in the sentence, and quantification information, such as cardinality, iteration, and dependency. { si'man·tik ə'nal·ə·səs }

semantic error [COMPUT SCI] The use of an incorrect symbolic name in a computer program. { si'man·tik 'er·ər }

semantic extension [COMPUT SCI] An extension mechanism which introduces new kinds of objects into an extensible language, such as additional data types or operations. { si'man·tik ik'sten·shən }

semantic gap [COMPUT SCI] The difference between a data or language structure and the objects that it models. { si'man·tik 'gap }

semaphore [COMPUT SCI] A memory cell that is shared by two parallel processes which rely on each other for their continued operation, and that provides an elementary form of communication between them by indicating when significant events have taken place. { 'sem·ə,fōr }

semialgorithm [COMPUT SCI] A procedure for solving a problem that will continue endlessly if the problem has no solution. { ,sem·ē'al·gə ,rith·əm }

semiautomatic telephone system [COMMUN] Telephone system that limits automatic dialing to only those subscribers who are served by the same exchange as the calling subscriber. { ¦sem·ē,ȯd·ə'mad·ik 'tel·ə,fōn ,sis·təm }

semiconducting compound [SOLID STATE] A compound which is a semiconductor, such as copper oxide, mercury indium telluride, zinc sulfide, cadmium selenide, and magnesium iodide. { ¦sem·i·kən¦dək·tiŋ 'käm,paund }

semiconducting crystal [SOLID STATE] A crystal of a semiconductor, such as silicon, germanium, or gray tin. { ¦sem·i·kən¦dək·tiŋ ¦krist·əl }

semiconductor [ELECTR] A solid crystalline material whose conductivity is intermediate between that of a metal and an insulator and may depend on temperature or voltage; by making suitable contacts to the material or by making the material suitably inhomogenous, electrical rectification and amplification may be obtained. { ¦sem·i·kən¦dək·tər }

semiconductor device [ELECTR] Electronic device in which the characteristic distinguishing electronic conduction takes place within a semiconductor. { ¦sem·i·kən¦dək·tər di,vīs }

semiconductor diode [ELECTR] **1.** A two-electrode semiconductor device that utilizes the rectifying properties of a *pn* junction or a point contact. **2.** More generally, any two-terminal electronic device that utilizes the properties of the semiconductor from which it is constructed. Also known as crystal diode; crystal rectifier; diode. { ¦sem·i·kən¦dək·tər 'dī,ōd }

semiconductor-diode parametric amplifier [ELECTR] Parametric amplifier using one or more varactors. { ¦sem·i·kən¦dək·tər ¦dī,ōd ¦par·ə¦me·trik 'am·plə ,fī·ər }

semiconductor disk [COMPUT SCI] A large semiconductor memory that imitates a disk drive in that the operating system can read and write to it as though it were an ordinary disk, but at a much faster rate. Also known as nonrotating disk. { 'sem·i·kən,dək·tər ,disk }

semiconductor doping See doping. { ¦sem·i·kən ¦dək·tər 'dōp·iŋ }

semiconductor heterostructure [ELECTR] A structure of two different semiconductors in junction contact having useful electrical or electrooptical characteristics not achievable in either conductor separately; used in certain types of lasers and solar cells. { ¦sem·i·kən¦dək·tər 'hed·ə·rō,strək·chər }

semiconductor junction [ELECTR] Region of transition between semiconducting regions of different electrical properties, usually between *p*-type and *n*-type material. { ¦sem·i·kən¦dək·tər ,jəŋk·shən }

semiconductor laser [OPTICS] A laser in which stimulated emission of coherent light occurs at a *pn* junction when electrons and holes are driven into the junction by carrier injection, electron-beam excitation, impact ionization, optical excitation, or other means; used as light transmitters

SOS [COMMUN] The distress signal in radiotelegraphy, consisting of the letters S, O, and S of the international Morse code.

sound analyzer [ENG] An instrument which measures the amount of sound energy in various frequency bands; it generally consists of a set of fixed electrical filters or a tunable electrical filter, along with associated amplifiers and a meter which indicates the filter output. { 'saůnd ,an·ə ,līz·ər }

sound board [COMPUT SCI] An adapter which provides a computer with the capability of reproducing and recording digitally encoded sound. Also known as audio adapter; sound card. { 'saůn ,bȯrd }

sound card *See* sound board. { 'saůn kärd }

sound carrier [COMMUN] The analog television carrier that is frequency-modulated by the sound portion of a television program; the unmodulated center frequency of the sound carrier is 4.5 megahertz higher than the video carrier frequency for the same television channel. { 'saůnd ,kar·ē·ər }

sound channel [ELECTR] The series of stages that handles only the sound signal in a television receiver. { 'saůnd ,chan·əl }

sound filmstrip [ENG ACOUS] A filmstrip that has accompanying sound on a separate disk or tape, which is manually or automatically synchronized with projection of the pictures in the strip. { 'saůnd 'film,strip }

sound gate [ENG ACOUS] The gate through which film passes in a sound-film projector for conversion of the sound track into audio-frequency signals that can be amplified and reproduced. { 'saůnd ,gāt }

sound head [ENG ACOUS] **1.** The section of a sound motion picture projector that converts the photographic or magnetic sound track to audible sound signals. **2.** In a sonar system, the cylindrical container for the transmitting projector and the receiving hydrophone. { 'saůnd ,hed }

sound-level meter [ENG] An instrument used to measure noise and sound levels in a specified manner; the meter may be calibrated in decibels or volume units and includes a microphone, an amplifier, an output meter, and frequency-weighting networks. { 'saůnd ¦lev·əl ,mēd·ər }

sound navigation and ranging *See* sonar. { 'saůnd ,nav·ə'gā·shən ən 'rānj·iŋ }

sound-powered telephone [ENG ACOUS] A telephone operating entirely on current generated by the speaker's voice, with no external power supply; sound waves cause a diaphragm to move a coil back and forth between the poles of a powerful but small permanent magnet, generating the required audio-frequency voltage in the coil. { 'saůnd ¦paů·ərd 'tel·ə,fōn }

sound production [ENG ACOUS] Conversion of energy from mechanical or electrical into acoustical form, as in a siren or loudspeaker. { 'saůnd prə,dək·shən }

sound reception [ENG ACOUS] Conversion of acoustical energy into another form, usually electrical, as in a microphone. { 'saůnd ri,sep·shən }

sound recording [ENG ACOUS] The process of recording sound signals so they may be reproduced at any subsequent time, as on a disk, sound track, or magnetic tape. { 'saůnd ri,kȯrd·iŋ }

sound-reinforcement system [ENG ACOUS] An electronic means for augmenting the sound output of a speaker, singer, or musical instrument in cases where it is either too weak to be heard above the general noise or too reverberant; basic elements of such a system are microphones, amplifiers, volume controls, and loudspeakers. Also known as public address system. { 'saůnd ,rē·in'fȯrs·mənt ,sis·təm }

sound-reproducing system [ENG ACOUS] A combination of transducing devices and associated equipment for picking up sound at one location and time and reproducing it at the same or some other location and at the same or some later time. Also known as audio system; reproducing system; sound system. { 'saůnd ,rē·prə'düs·iŋ ,sis·təm }

sound spectrograph [ENG ACOUS] An instrument that records and analyzes the spectral composition of audible sound. { 'saůnd 'spek·trə ,graf }

soundstripe [ENG ACOUS] A longitudinal stripe of magnetic material placed on some motion picture films for recording a magnetic sound track. { 'saůnd,strīp }

sound system *See* sound-reproducing system. { 'saůnd ,sis·təm }

sound track [ENG ACOUS] A narrow band, usually along the margin of a sound film, that carries the sound record; it may be a variable-width or variable-density optical track or a magnetic track. { 'saůnd ,trak }

sound transducer *See* electroacoustic transducer. { 'saůnd tranz,düs·ər }

sound trap [ELECTR] A wave trap in an analog television receiver circuit that prevents sound signals from entering the picture channels. { 'saůnd ,trap }

source [ELEC] The circuit or device that supplies signal power or electric energy or charge to a transducer or load circuit. [ELECTR] The terminal in a field-effect transistor from which majority carriers flow into the conducting channel in the semiconductor material. { sȯrs }

source address [COMPUT SCI] The first address of a two-address instruction (the second address is known as the destination address). { 'sȯrs 'ad,res }

source code [COMPUT SCI] The statements in which a computer program is initially written before translation into machine language. { 'sȯrs ,kōd }

source data automation equipment [COMPUT SCI] Equipment (except paper tape and magnetic tape cartridge typewriters acquired separately and not operated in support of a computer) which, as a by-product of its operation, produces a record in a medium which is acceptable by automatic data-processing equipment. { 'sȯrs ¦dad·ə ,ȯd·ə'mā·shən i,kwip·mənt }

source data capture [COMPUT SCI] The procedures for entering source data into a computer system. { 'sȯrs 'dad·ə ,kap·chər }

frequency measured across a hybrid circuit joined to a given two-wire termination and balancing network. { ¦tranz¦hī·brəd 'lȯs }

transient |PHYS| A pulse, damped oscillation, or other temporary phenomenon occurring in a system prior to reaching a steady-state condition. { 'tranch·ənt }

transient analyzer |ELECTR| An analyzer that generates transients in the form of a succession of equal electric surges of small amplitude and adjustable waveform, applies these transients to a circuit or device under test, and shows the resulting output waveforms on the screen of an oscilloscope. { 'tranch·ənt ,an·ə,līz·ər }

transient distortion |ELECTR| Distortion due to inability to amplify transients linearly. { 'tranch·ənt di,stȯr·shən }

transient phenomena |ELEC| Rapidly changing actions occurring in a circuit during the interval between closing of a switch and settling to a steady-state condition, or any other temporary actions occurring after some change in a circuit. { 'tranch·ənt fə,näm·ə·nä }

transient program |COMPUT SCI| A computer program that is stored in a computer's main memory only while it is being executed. { 'tranch·ənt 'prō·grəm }

transient suppressor *See* surge suppressor. { 'tranch·ənt sə'pres·ər }

transistance |ELECTR| The characteristic that makes possible the control of voltages or currents so as to accomplish gain or switching action in a circuit; examples of transistance occur in transistors, diodes, and saturable reactors. { tran'zis·təns }

transistor |ELECTR| An active component of an electronic circuit consisting of a small block of semiconducting material to which at least three electrical contacts are made, usually two closely spaced rectifying contacts and one ohmic (nonrectifying) contact; it may be used as an amplifier, detector, or switch. { tran'zis·tər }

transistor amplifier |ELECTR| An amplifier in which one or more transistors provide amplification comparable to that of electron tubes. { tran'zis·tər ,am·plə,fī·ər }

transistor biasing |ELECTR| Maintaining a direct-current voltage between the base and some other element of a transistor. { tran'zis·tər ,bī·əs·iŋ }

transistor characteristics |ELECTR| The values of the impedances and gains of a transistor. { tran'zis·tər ,kar·ik·tə,ris·tiks }

transistor chip |ELECTR| An unencapsulated transistor of very small size used in microcircuits. { tran'zis·tər ,chip }

transistor circuit |ELECTR| An electric circuit in which a transistor is connected. { tran'zis·tər ,sər·kət }

transistor clipping circuit |ELECTR| A circuit in which a transistor is used to achieve clipping action; the bias at the input is set at such a level that output current cannot flow during a portion of the amplitude excursion of the input voltage or current waveform. { tran'zis·tər 'klip·iŋ ,sər·kət }

transistor gain |ELECTR| The increase in signal power produced by a transistor. { tran'zis·tər ,gān }

transistor input resistance |ELECTR| The resistance across the input terminals of a transistor stage. Also known as input resistance. { tran'zis·tər 'in,pu̇t ri,zis·təns }

transistor magnetic amplifier |ELECTR| A magnetic amplifier together with a transistor preamplifier, the latter used to make the signal strong enough to change the flux in the core of the magnetic amplifier completely during a half-cycle of the power supply voltage. { tran'zis·tər mag'ned·ik 'am·plə,fī·ər }

transistor memory *See* semiconductor memory. { tran'zis·tər ,mem·rē }

transistor radio |ELECTR| A radio receiver in which transistors are used in place of electron tubes. { tran'zis·tər ,rād·ē·ō }

transistor-transistor logic |ELECTR| A logic circuit containing two transistors, for driving large output capacitances at high speed. Abbreviated T^2L; TTL. { tran'zis·tər tran'zis·tər 'läj·ik }

transition |COMMUN| Change from one circuit condition to the other; for example, the change from mark to space or from space to mark. { tran'zish·ən }

transition element |ELECTROMAG| An element used to couple one type of transmission system to another, as for coupling a coaxial line to a waveguide. { tran'zish·ən ,el·ə·mənt }

transition factor *See* reflection factor. { tran'zish·ən ,fak·tər }

transition function |COMPUT SCI| A function which determines the next state of a sequential machine from the present state and the present input. { tran'zish·ən ,fəŋk·shən }

transition loss |ELEC| At a junction between a source and a load, the ratio of the available power to the power delivered to the load. { tran'zish·ən ,lȯs }

transition point |ELECTROMAG| A point at which the constants of a circuit change in such a way as to cause reflection of a wave being propagated along the circuit. { tran'zish·ən ,pȯint }

transitron |ELECTR| Thermionic-tube circuit whose action depends on the negative transconductance of the suppressor grid of a pentode with respect to the screen grid. { 'tran·sə,trän }

transitron oscillator |ELECTR| A negative-resistance oscillator in which the screen grid is more positive than the anode, and a capacitor is connected between the screen grid and the suppressor grid; the suppressor grid periodically divides the current between the screen grid and the anode, thereby producing oscillation. { 'tran·sə,trän 'äs·ə,lād·ər }

transit time |ELECTR| The time required for an electron or other charge carrier to travel between two electrodes in an electron tube or transistor. { 'trans·ət ,tīm }

transit-time microwave diode |ELECTR| A solid-state microwave diode in which the transit time of charge carriers is short enough to permit operation in microwave bands. { 'trans·ət ,tīm 'mī·krə,wāv 'dī,ōd }

transit-time mode |ELECTR| A mode of operation of a Gunn diode in which a charge dipole,

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

GODO KAISHA IP BRIDGE 1,	)	
	)	
Plaintiff,	)	
	)	
v.	)	C.A. No. 16-290 (MN)
	)	
OMNIVISION TECHNOLOGIES, INC.	)	
	)	
Defendant.	)	

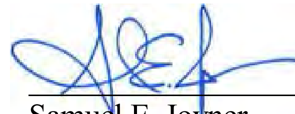
DECLARATION OF SAMUEL E. JOYNER

I, Samuel E. Joyner, make this declaration in support of IP Bridge's Opening Claim Construction Brief and certify as follows:

1. My name is Samuel E. Joyner. I am more than twenty-one years old, of sound mind, and fully capable of making this declaration. I am a graduate of the U.S. Military Academy at West Point, New York. Before attending law school, I served in the U.S. Army as an Airborne Infantry Ranger. I was honorably discharged from active duty service as a Captain. I have never been convicted of a felony or misdemeanor involving moral turpitude. I was conferred the degree of Doctor of Jurisprudence from The University of Tulsa College of Law in 2002, and I received my license from the State Bar of Texas in November 2002. I am a partner at the law firm of Shore Chan DePumpo LLP in Dallas, Texas, and counsel of record for plaintiff Godo Kaisha IP Bridge 1 in an action styled *Godo Kaisha IP Bridge 1 v. Omni Vision Technologies, Inc.*, No. 1:16-cv-00290-MN-SRF, in the United States District Court for the District of Delaware. I have personal knowledge of the facts set forth in this declaration and am competent to testify thereto.

2. A true and correct copy of each document identified in Exhibit A (attached hereto) is included in the Appendix in Support of IP Bridge's Opening Claim Construction Brief.

I declare under penalty of perjury pursuant to 28 U.S.C. § 1746 the foregoing is true and correct to the best of my knowledge. Executed on September 14, 2018.



Samuel E. Joyner

Exhibit A

Description	App.
US Patent No. 8,084,796 B2 to Mori, et al.	App. 0001-0021
April 6, 2011 Amendment in '796 patent file history	App. 0022-0029
September 11, 2011 Notice of Allowability in '796 patent file history	App. 0030-0032
US Patent No. 8,106,431 B2 to Mori, et al.	App. 0033-0053
December 15, 2010 Amendment in '431 patent file history	App. 0054-0063
May 12, 2010 Amendment in '431 patent file history	App. 0064-0073
September 30, 2011 Notice of Allowability in '431 patent file history	App. 0074-0076
US Patent No. 8,378,401 B2 to Mori, et al.	App. 0077-0099
August 27, 2012 Amendment in '401 patent file history	App. 0100-0112
November 14, 2012 Notice of Allowability in '401 patent file history	App. 0113-0115
US Patent No. 7,436,010 B2 to Mori, et al.	App. 0116-0137
May 8, 2006 Amendment in '010 patent file history	App. 0138-0156
October 24, 2006 Amendment in '010 patent file history	App. 0157-0174
March 29, 2007 Amendment in '010 patent file history	App. 0175-0187
September 24, 2007 Amendment in '010 patent file history	App. 0188-0201
March 21, 2008 Amendment in '010 patent file history	App. 0202-0212
US Patent No. 6,160,281 to Guidash	App. 0213-0227
US Patent No. 6,310,366 B1 to Rhodes, et al.	App. 0228-0243
US Patent No. 6,794,677 to Tamaki, et al.	App. 0244-0264
January 22, 2004 Amendment in '677 patent file history	App. 0265-0269
US Patent No. 6,709,950 B2 to Segawa, et al.	App. 0270-0308
January 15, 2003 Amendment in '950 patent file history	App. 0309-0326
October 24, 2003 Amendment in '950 patent file history	App. 0327-0338

November 6, 2003 Notice of Allowability in ’950 patent file history	App. 0339-0340
US Patent No. 6,538,324 B1 to Tagami, et al.	App. 0341-0371
January 28, 2002 Amendment in ’324 patent file history	App. 0372-0378
June 11, 2002 Response/Remarks in ’324 patent file history	App. 0379-0382
August 9, 2002 Amendment in ’324 patent file history	App. 0383-0390
September 10, 2002 Notice of Allowability in ’324 patent file history	App. 0391-0393
IEEE Standard Dictionary of Electrical and Electronics Terms, 1988	App. 0394-0409
McGraw-Hill Dictionary of Electrical and Computer Engineering, 2004	App. 0410-0423
Declaration of Samuel E. Joyner	App. 0424-0427

TK
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HIGH-DENSITY SOLID-STATE IMAGE SENSORS

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Abstract

The most highly developed of solid-state sensors are visible image sensors. Visible image sensor arrays with more than a million picture elements and with noise levels in the tens of electrons have been developed. In this paper the architectures of image sensors are reviewed, and the key issues are discussed. As an example of the present status of sensor technology, results on a 360,000-pixel charge-coupled image sensor are presented.

Sensor Architectures

The first visible image sensor array was reported in 1967 [1]. However, the development of present-day sensors occurred after the discovery of the charge-coupled device (CCD) in 1970 [2]. The first applications for solid-state sensors were in military and commercial systems. Most of these sensors were linear arrays. More recently, area arrays have been developed for consumer applications. Owing to the continuing development of process technology for silicon integrated circuits, the cost of solid-state imagers is rapidly becoming competitive with the electron-beam-scanned camera tubes such as the saticon. Sensor arrays with 180,000 pixels are in production, and arrays with 360,000 pixels are in advanced development. The advances in silicon VLSI technology that made large-area arrays feasible have also made possible linear arrays with up to 5732 elements [3,4], high-sensitivity time-delay-and-integrate (TDI) scanners [5], very high-frame-rate imaging arrays for high-speed video photography [6], and very high-resolution arrays for astronomy [7].

An image sensor consists of photosensitive elements that convert the incoming light to charge and readout structures that transfer the charge to the output. Three major classes of photosensitive elements are in wide-spread use: the photodiode, the photocapacitor, and the photoconductor. The structure and band diagrams for these photosensitive elements are illustrated in Fig. 1. The photodiode consists of a p-n junction. Usually the implantation for the photodiode is tailored to yield a high electric field from the surface to aid in collection of photoelectrons generated near the surface, giving a high blue sensitivity. Owing to the low capacitance of the diode structure, the charge storage capacity of the photodiode is usually small. For image sensor array applications, the diode is usually fabricated in a p-well to reduce crosstalk and blooming. A variant on the photodiode is the p^+-n-p photodiode [8], in which a heavily doped p^+ layer is placed near the surface and the n-type layer is lightly doped and is fully depleted during operation. The p^+n front junction results in a factor of 5 or more charge capacity, as compared to the normal photodiode, as well as reduced image lag.

The photocapacitor consists of a thin polysilicon gate above an oxide. Owing to the high optical absorption of the polysilicon, the quantum efficiency is lower than in the photodiode, particularly in the blue. The photocapacitor is used most widely in the form of a frame-transfer CCD or the CID, although photocapactor arrays have been used for very high-speed applications [6]. Owing to the high capacitance of the MOS structure, the photocapacitor has the highest charge of all the photosensitive elements.

Recently, there has been great excitement over the development of photoconductive films such as hydrogenated amorphous silicon (α-Si:H) [9]. These films, deposited on top of an interline or X-Y-addressed diode array, result in a vertical integration of sensors. The α-Si:H photoconductors consist of a back contact (such as aluminum) that contacts the diode in the underlying array, an α-Si:H layer $\sim 1\,\mu m$ thick, and a transparent top electrode. The photoconductor is biased to complete depletion. Photogenerated carriers are swept out of the photoconductor and stored in the underlying diode. The photoconductor offers high quantum efficiency, very high area utilization, and internal antiblooming.

The major classes of readout architectures for image sensors are the frame-transfer CCD [10,12], the interline-transfer CCD [13-16], and various X-Y-addressed MOS photodiode arrays [6,9,17-20] (Fig. 2). The frame-transfer CCD consists of an illuminated imaging area with vertical registers to integrate and transfer the charge, a storage register to store the charge during readout, and a horizontal transfer register. For television applications both the image and storage areas store one field (242 lines for NTSC television). Vertical interlacing is accomplished by integrating under different electrodes during the two fields, accomplishing a half-pixel shift in the relative position of the pixel. Frame-transfer CCD's have been constructed with two and three levels of polysilicon as well as with one level of polysilicon in virtual-phase CCD's [10]. Since the entire pixel area is photosensitive, the quantum efficiency is very high. However, absorption of blue light in the polysilicon electrodes reduces the blue efficiency. At the end of each field, the integrated charge must be transferred from the image to the storage register. This transfer, which typically requires almost a millisecond, results in some vertical image smearing owing to the very low capacitance of the CCD output (<40 fF); the CCD has very low noise and hence very good low-light-level performance. Output noise values of <50 rms electrons at video rates have been reported.

The interline CCD imager consists of vertical CCD registers used for charge transfer and photodiodes for light sensing and charge storage. For NTSC television there would be 484 diodes vertically and 242 stages of the CCD shift register. At the end of one field the charge from the top diode in each stage is transferred onto the vertical CCD register, while in the other field the charge from the bottom diode is transferred. The vertical registers are optically shielded with aluminum. Owing to the separation of light-sensing and charge-transfer functions, the photodiode typically occupies only 25-40% of the cell area. This results in a lower overall quantum efficiency as compared to the frame-transfer CCD. However, use of photoconductive layers overlying the sensor could greatly reduce this disadvantage.

The unit cell of MOS X-Y-addressed imagers consists of a photodiode (or photocapacitor), a transfer

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gate, and a diffusion contacted by a metal signal line. The transfer gates are addressed by a vertical scan generator, usually a dynamic shift register, which addresses each row sequentially. Horizontal charge readout may be accomplished with horizontal signal lines connected to the vertical signal lines by FET switches controlled by a horizontal scanner. Other X-Y-addressed arrays utilize a CCD for horizontal readout. Owing to the use of a metal signal line instead of a CCD for vertical transfer, the MOS array has a larger fraction of each pixel devoted to the photodiode, resulting in higher quantum efficiency. The MOS array is also simpler to manufacture. However, the sensitivity of the MOS imager at low light levels is severely constrained by the KTC and the pattern noise of the high-capacitance horizontal and vertical signal lines. Although the use of a horizontal CCD reduces the horizontal readout noise, the KTC noise of the vertical signal lines results in a factor of 10 higher noise than the interline CCD readout.

A 360,000-Pixel Solid-State Image Sensor

Sensor Design

As an example of the performance of present solid-state sensors, a 360,000-pixel charge-coupled image sensor will be described [11]. The sensor is used for imaging color photographic negatives on television, which places some unique demands on a solid-state sensor. These include wide dynamic range, low pattern noise, high resolution, and excellent color reproduction.

The sensor architecture is shown in Fig. 3a. The sensor consists of a four-phase CCD image area, dual two-phase horizontal registers, and separate output amplifiers for each of the three colors. During the vertical retrace interval the photographic negative is illuminated. The vertical clocks are held constant to integrate the signal charge. At the end of the vertical retrace interval the signal is read out. A row at a time is transferred into the horizontal registers. The charge from columns with green color filters is transferred to the top register, while the charge from the alternate columns with red and blue color filters is transferred to the bottom register. The dual horizontal register design was required to achieve the 12-μm horizontal column spacing without a third level of polysilicon. The horizontal registers are read out at a 7.15 MHz pixel rate. The charge is sensed by floating diffusion outputs and buffered by dual-stage buried-channel source followers. The use of dual-stage source followers allowed optimization of the first stage for low input capacitance and the second stage for high drive current. The use of the buried-channel FET design reduced low-frequency (1/f) noise.

A photomicrograph of the image sensor is shown in Fig. 3b. The image area is 8.8 mm (H) x 6.6 mm (V). A schematic of the pixel is shown in Fig. 3c. The channel-stop region is 2 μm wide, and the buried channel is 10 μm wide. The gate oxide under both the first and second polysilicon electrodes was 1600 Å thick, to maximize optical transmission in the blue. The polysilicon layers were both 1700 Å thick. Source-drain regions were formed by shallow arsenic implantation to minimize short-channel effects in the output structure.

Spectral Response

In a color image sensor in which the photosensitive area is fully covered by polysilicon, careful choice of the polysilicon thickness is required to achieve adequate transmission in the blue while maintaining sufficiently low resistance to transfer charge vertically. Figure 4a shows the optical absorption coefficient of polysilicon as a function of wavelength. Figure 4b shows the measured spectral response of the sensor along with the response calculated from the known layer thicknesses and the optical constants. At wavelengths below 500 nm the response is dominated by optical absorption in the polysilicon electrodes. Between 500 and 800 nm the response is dominated by structure due to optical interference within the polysilicon and the gate oxide. Beyond 800 nm the light is absorbed well below the silicon surface, and the spectral response decreases, owing to recombination of the photogenerated electrons.

Organic color filter arrays are fabricated on top of the sensor in an R-G-B-G stripe geometry. The color filter arrays are processed by sequential coating, patterning, and dyeing of special photoresists developed for this application. Owing to the narrow (2 μm) light-shield width, extreme resolution and sharpness requirements are placed on the resist materials. The dyes for this color filter array were specifically designed for imaging photographic negatives.

Charge Capacity

Because of the large density range of photographic negatives, a wide dynamic range is required in the sensor. There are two limitations to charge capacity in a buried-channel CCD: (1) the interaction between electrons and interface states at the $Si\text{-}SiO_2$ surface and (2) the potential difference between well and barrier electrodes. Figure 5a illustrates the first limitation. The electrostatic potential and the electron density are shown as a function of depth for three different quantities of charge in the channel. As more electrons are added to the channel, the barrier to the surface decreases and the electron concentration at the surface increases. Electrons can be captured at interface states when electrons come in contact with the surface.

Owing to the narrow channel width, two-dimensional effects significantly reduce charge capacity. Figure 5b shows the electrostatic potential and electron distribution in two dimensions calculated by finite-difference techniques. The electron distribution is shown at the transition between buried- and surface-channel operation ($\phi_{CH} - \phi_S$ = 300 mV) for a 1 x 10^{12} cm^{-2} buried-channel dose. The electrons occupy only the center 4 μm of the 10-μm channel. For a 2 x 10^{12} cm^{-2} buried-channel dose with a significantly larger barrier between channel and surface, the electrons occupy the center 7 μm of the 10-μm channel. The barrier between the electrons in the channel calculated as a function of the electron density is shown in Fig. 5c for two buried-channel doses using one- and two-dimensional models. Figure 6 shows the experimentally measured differential charge-transfer inefficiency for the image area as a function of the number of electrons per pixel for the two buried-channel doses. The 1 x 10^{12} cm^2 dose yields a capacity of 100,000 electrons per pixel, and the 2 x 10^{12} cm^2 dose 800,000 electrons, in good agreement with the two-dimensional model.

Noise

The noise sources in this sensor include pattern and shot noise from dark current, output amplifier noise, and photosensitivity pattern noise due to the sensor and the color filter array.

The dark current in better sensors at room temperature was 5 nA/cm^2 or 1600 electrons per pixel. Measurements of the dark current in test structures adjacent to the sensor as a function of gate voltage showed that surface generation accounted for 2.5 nA/cm^2, generation in the buried-channel implanted region for 1 nA/cm^2, generation in the unimplanted portion of the depletion layer for 0.5 nA/cm^2, and diffusion current for 0.1 nA/cm^2. Comparison of test structures with and without channel stops indicated that the channel stops contributed an additional 1 nA/cm^2 to the overall dark current. Subsequent analysis by transmission electron microscopy revealed dislocation loops 100 Å in diameter in the implanted region of the channel and precipitates 50 Å in diameter in the channel-stop regions.

The largest random noise source is the output amplifier at 200 rms electrons per pixel in a 3.5-MHz bandwidth. The output amplifiers are two-stage buried-channel source followers with sensitivity of 2 μV/electron. Owing to the use of buried-channel transistors in the source follower and to double correlated sampling in the signal processing, the output amplifier noise is almost entirely a result of thermal noise in these transistors.

In Fig. 7 the signal and the noise from various sources are plotted as a function of the density of the photographic negative. The largest noise source is the output amplifier noise at 200 rms electrons per pixel. The dynamic range of the sensor is 70 dB. This exceeds the dynamic range required for imaging photographic negatives.

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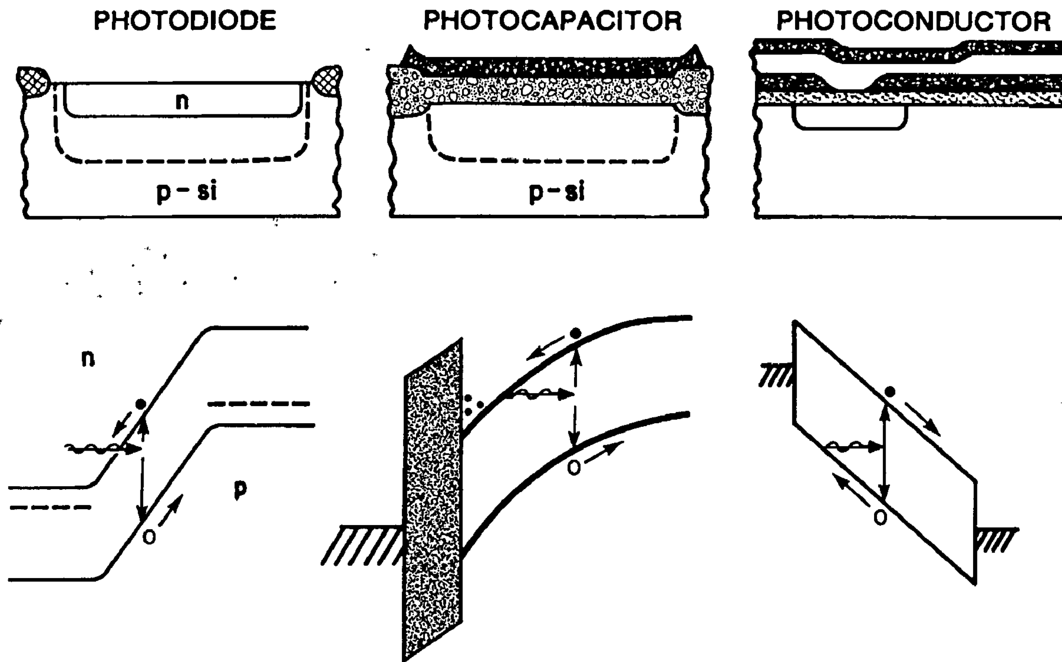


Fig. 1 Cross-sections and band diagrams of photosensitive elements: (a) photodiode, (b) photocapacitor, (c) photoconductor

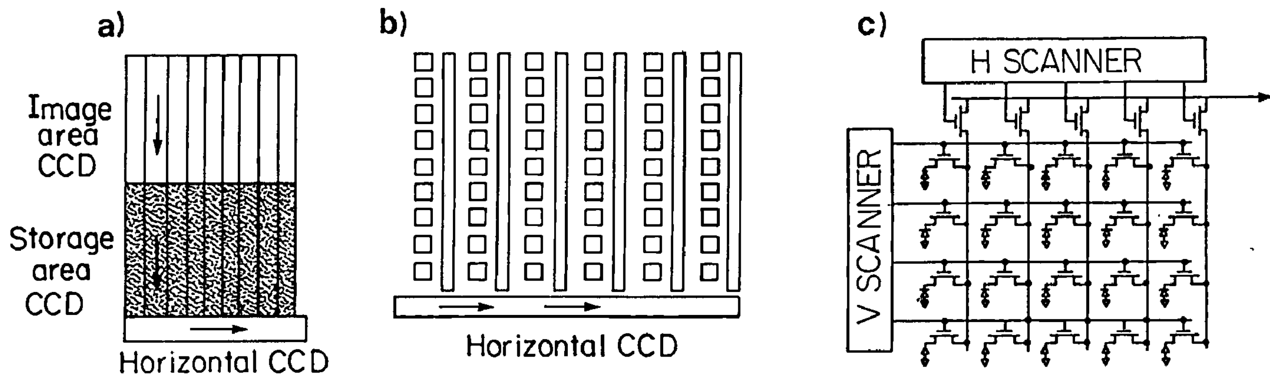
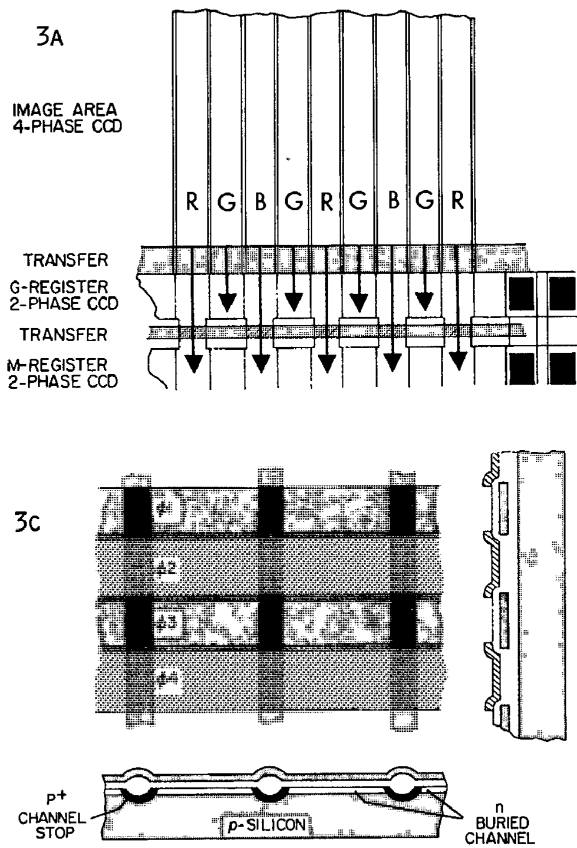


Fig. 2 Architectures of major sensor designs: (a) frame-transfer CCD, (b) interline-transfer CCD, (c) MOS diode array



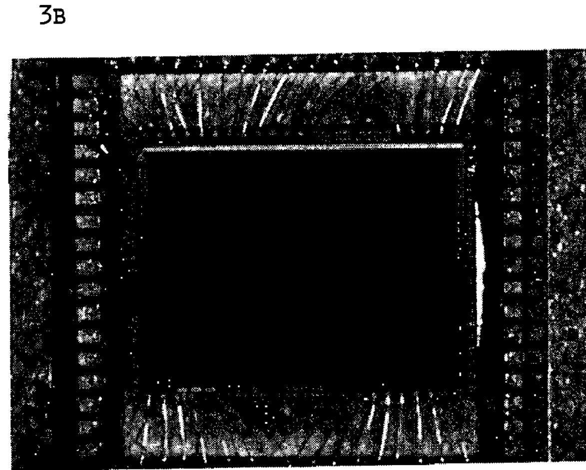
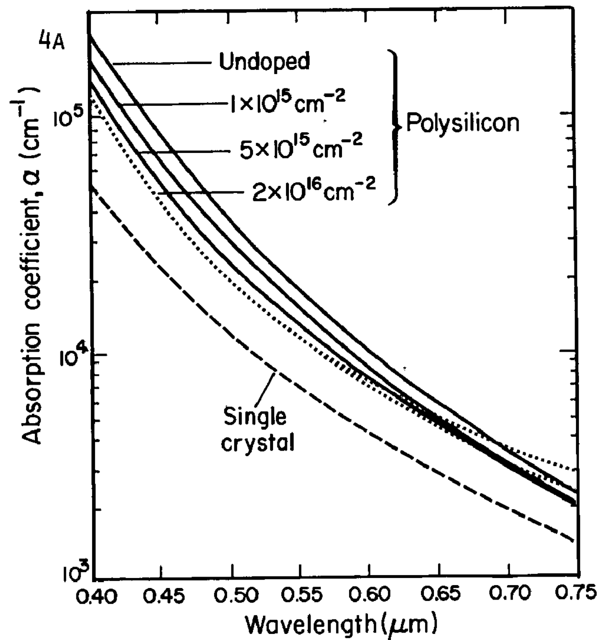


Fig. 3. (a) Design of image sensor. Sensor has 740 columns horizontally with R-G-B-G stripe color filter pattern. Vertical registers are four-phase C.C.D.'s; horizontal registers are two-phase.

(b) Photograph of sensor chip. Image area is 8.8 mm (H) x 6.6 mm (V).

(c) Design of image area. Width of column is 12 μm, including 2 μm channel stops.



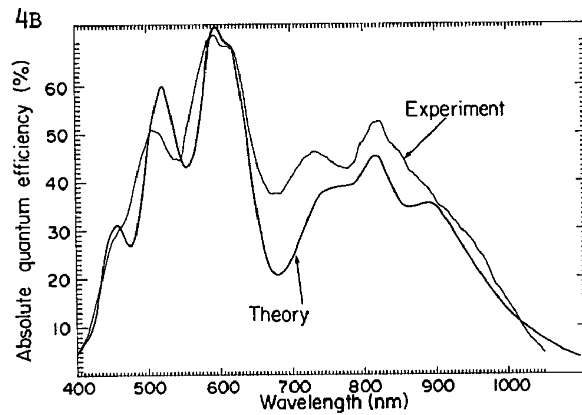
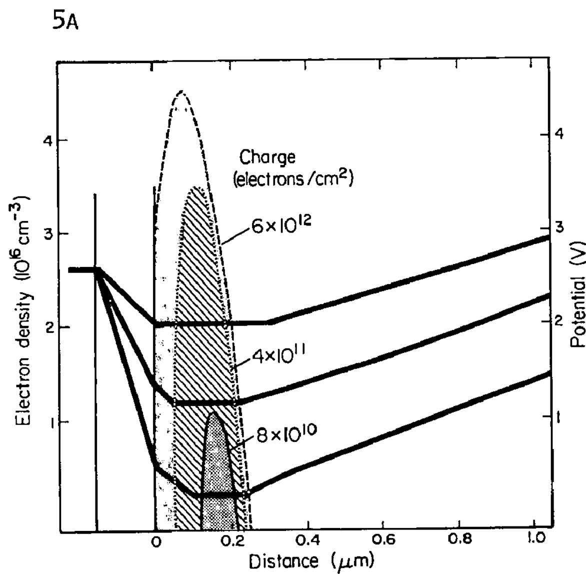


Fig. 4. (a) Absorption coefficient of polysilicon phosphorus doped at various concentrations.

(b) Measured and calculated spectral response of sensor.

5A



5C

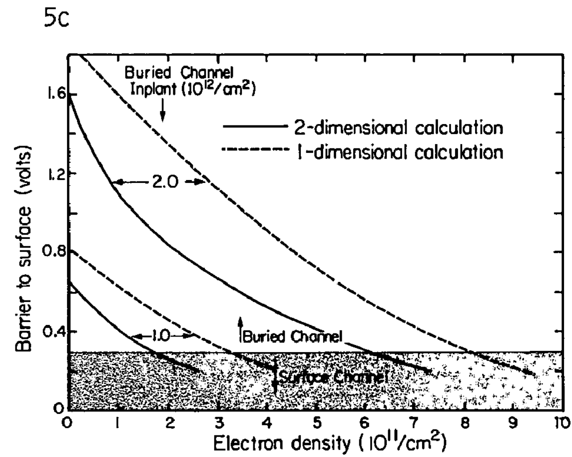
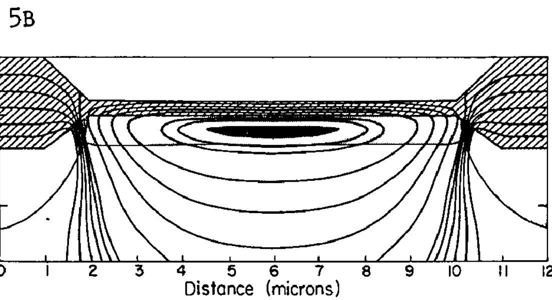


Fig. 5. (a) Electrostatic potential and electron distribution for different quantities of charge in the buried channel.

(b) Electrostatic potential and electron distribution in two dimensions for 10 μm wide buried channel.

(c) Potential barrier between buried channel and surface as a function of electron concentration for two buried-channel doses. Results of one- and two-dimensional models are shown.

5B



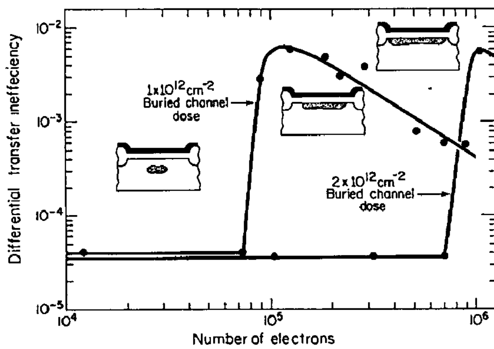


Fig. 6. Differential transfer inefficiency vs. number of electrons per pixel for vertical C.C.D. registers for two buried-channel doses.

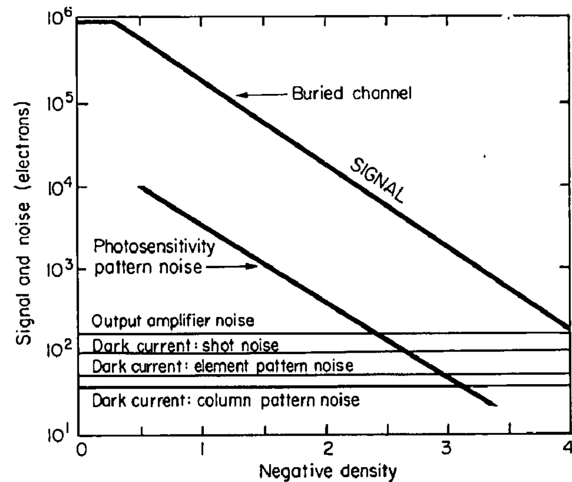


Fig. 7. Signal and noise as a function of the density of the photographic negative. Dynamic range of the sensor is 70 dB.

WEBSTER'S DESK DICTIONARY

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RHR PRESS
New York

Webster's Desk Dictionary

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Library of Congress Cataloging-in-Publication Data is available.

Visit the Random House Reference Web site at www.randomwords.com

Typeset and printed in the United States of America.

9 8 7 6 5 4 3 2 1

July 2001

ISBN: 0-375-42565-9

New York • Toronto • London • Sydney • Auckland

A

rooked. **2.** determined; talent.
nake numb. **2.** to make

n. a colorless, flamma-
om coal tar: used in
olvent.
), *v.t.* **1.** to dispose of
. to hand down.
: act of bequeathing. **2.**

-rat·ing. to scold; re-

mber of any of a group
the group of languages

d or **-reft, -reav·ing. 1.**
esp. by death. **2.** to de-
—be·reave/ment, *n.*

less cap.
disease caused by a de-
to paralysis and emacia-

, *n.* a part of the N Pa-
a.
nnecting the Bering Sea

in W California. 102,724.
a synthetic radioactive
97.
l of Germany. 3,121,000.
ern zone **(West Berlin)**
rlin).
. a group of British Is-
30. **—Ber·mu/dan, Ber·**

with a pl. v.) shorts ex-

n. the capital of Switzer-

rah, 1845–1923, French

., **-ried, -ry·ing.** *—n.* **1.**
y fruit, as the strawberry.
wheat. *—v.i.* **3.** to gather
like/, *adj.*
adj. violently or destruc-
r frenzied warrior = *ber-*

: sleeping space, as on a
ace allotted for a ship to
; position. *—v.t.* **4.** to al-
e into a berth. **—*Idiom.***
keep a careful distance

varieties of which are val-
beryllium.
a hard, light metallic el-
alloys to reduce fatigue.
t. no.: **4.**
., **-sought** or **-seeched,**
sk eagerly (for). **—be·**
·ly, *adv.*
t·ting. 1. to attack on all

or at the side of; near. **2.**
: *beside the point.* **4.** BE-
5. beside oneself, frantic;
e prepositional meanings
BESIDES is preferred, esp.

; furthermore. **2.** in addi-
rep. **4.** in addition to. **5.**
e besides me. **—Usage.**

ged, -sieg·ing. 1. to lay
. **3.** to importune, as with

smear.
to soil; sully.
om, esp. one of brush or

d, -sot·ting. 1. to stupefy

with drink. **2.** to make stupid or foolish, esp. with infatuation.

be·sought (bi sôt/), *v.* a pt. and pp. of BESEECH.

be·spat·ter (bi spat/ər), *v.t.* to spatter.

be·speak (bi spēk/), *v.t.,* **-spoke, -spo·ken** or **-spoke, -speak·ing. 1.** to reserve beforehand. **2.** to show; indicate.

best (best), *adj., superl. of* **good** *with* **better** *as compar.* **1.** of the highest quality or standing. **2.** most advantageous or suitable. **3.** largest: *the best part of a day.* *—adv., superl. of* **well** *with* **better** *as compar.* **4.** most excellently. **5.** in or to the highest degree. *—n.* **6.** someone or something that is best. **7.** salutations: *Give them my best.* *—v.t.* **8.** to get the better of; beat or surpass. **—*Idiom.*** **9. at best,** even under the most favorable circumstances. **10. get the best of, a.** to gain the advantage over. **b.** to defeat; subdue. **11. make the best of,** to cope with; accept.

bes·tial (bes/chəl, bēs/-), *adj.* **1.** of or having the form of a beast. **2.** brutal or inhuman. **—bes/ti·al/i·ty** (-chē al/i tē), *n.* **—bes/tial·ly,** *adv.*

bes/ti·ar/y (-chē er/ē), *n., pl.* **-ar·ies.** a collection of moralizing tales about real and mythical animals.

be·stir (bi stûr/), *v.t.,* **-stirred, -stir·ring.** to rouse to action.

best/ man/, *n.* the chief attendant of the bridegroom at a wedding.

be·stow (bi stō/), *v.t.* to present as a gift; confer. **—be·stow/al,** *n.*

be·stride (bi strīd/), *v.t.,* **-strode** or **-strid, -strid·den** or **-strid, -strid·ing. 1.** to get or be astride of. **2.** to step over with long strides.

best/sell/er, *n.* a product, as a book, that among those of its class sells very well at a given time. **—best/-sell/ing,** *adj.*

bet (bet), *v.,* **bet** or **bet·ted, bet·ting,** *n.* *—v.t.* **1.** to pledge (money, etc.) as a forfeit if one's forecast of a future event is wrong. **2.** to maintain as in a bet. *—v.i.* **3.** to make a bet. *—n.* **4.** a pledge made in betting. **5.** a thing pledged. **6.** something bet on. **7.** a person or thing considered a good choice.

be·ta (bā/tə; *esp. Brit.* bē/-), *n., pl.* **-tas.** the second letter of the Greek alphabet (Β, β).

be·take (bi tāk/), *v.t.,* **-took, -tak·en, -tak·ing.** to cause (oneself) to go.

be/ta par/ticle, *n.* an electron or positron emitted from an atomic nucleus during radioactive decay.

be/ta ray/, *n.* a stream of beta particles.

be·tel (bēt/l), *n.* an East Indian pepper plant.

be/tel nut/, *n.* the seed of a palm, chewed in many tropical regions together with slaked lime and betel leaves as a stimulant.

bête noire (bāt/ nwär/, bet/), *n., pl.* **bêtes noires** (bāt/ nwärz/, bet/). a person or thing intensely disliked or dreaded. [< F]

be·think (bi thingk/), *v.t.,* **-thought, -think·ing.** to cause (oneself) to consider or recollect.

Beth·le·hem (beth/li hem/, -lē əm), *n.* a town in the West Bank, near Jerusalem: birthplace of Jesus.

be·tide (bi tīd/), *v.t., v.i.,* **-tid·ed, -tid·ing.** to happen (to).

be·times (bi tīmz/), *adv.* early; in good time.

be·to·ken (bi tō/kən), *v.t.* **1.** to give evidence of; indicate. **2.** to portend.

be·tray (bi trā/), *v.t.* **1.** to deliver or expose to an enemy by treachery. **2.** to be unfaithful or disloyal to. **3.** to reveal (something meant to be hidden). **4.** to seduce and desert. **—be·tray/al,** *n.* **—be·tray/er,** *n.*

be·troth (bi trōth/, -trôth/), *v.t.* to promise to give in marriage. **—be·troth/al,** *n.*

be·trothed/, *adj.* **1.** engaged to be married. *—n.* **2.** the person to whom one is betrothed.

bet·ter (bet/ər), *adj., compar. of* **good** *with* **best** *as superl.* **1.** of superior quality or excellence. **2.** of superior suitability; preferable. **3.** larger; greater. **4.** improved in health. *—adv., compar. of* **well** *with* **best** *as superl.* **5.** in a more excellent manner. **6.** more completely. **7.** more: *lives better than a mile away.* *—v.t.* **8.** to make better; improve. **9.** to surpass or exceed. *—n.* **10.** something that is preferable. **11.** Usu., **-ters.** those superior to oneself. **—*Idiom.*** **12. get the better of,** to prevail against.

bet/ter·ment, *n.* the act of bettering; improvement.

bet/tor or **bet/ter,** *n.* a person who bets.

be·tween (bi twēn/), *prep.* **1.** in the space separating. **2.** intermediate to in time, quantity, or degree. **3.** linking; connecting. **4.** by the common participation of: *Between us, we can finish the job.* **5.** distinguishing one from the other in comparison. **6.** existing confidentially for: *We'll keep this between ourselves.* *—adv.* **7.** in the intervening space or time. **—Usage.** BETWEEN YOU AND I, though occasionally heard in the speech of educated persons, is not the commonly accepted form. Since the pronouns are objects of the preposition BETWEEN, the usual form is *between you and me.* See also AMONG.

be·twixt/ (-twikst/), *prep., adv.* **1.** between. **—*Idiom.*** **2. betwixt and between,** in a middle position.

bev·el (bev/əl), *n., v.,* **-eled, -el·ing** or (*esp. Brit.*) **-elled, -el·ling.** *—n.* **1.** the inclination or angle that one line or surface makes with another when not at right angles. **2.** an adjustable tool for laying out or measuring angles. *—v.t.* **3.** to cut at a bevel. *—v.i.* **4.** to slant; incline.

bev/el gear/, *n.* a gear meshing with a similar gear set at right angles.

bev·er·age (bev/ər ij), *n.* any drinkable liquid, esp. other than water. [< AF, = *bevre* to drink (< L *bibere*) + *-age*]

Bev/erly Hills/ (bev/ər lē), *n.* a city in SW California, surrounded by the city of Los Angeles. 32,367.

bev·y (bev/ē), *n., pl.* **-ies. 1.** a group of birds, esp. quail. **2.** a large group or collection.

be·wail (bi wāl/), *v.t.* to express deep sorrow for; lament.

be·ware (bi wâr/), *v.t., v.i.* to be wary, cautious, or careful (of).

be·wigged (bi wigd/), *adj.* wearing a wig.

be·wil·der (bi wil/dər), *v.t.* to confuse or puzzle completely. **—be·wil/der·ment,** *n.*

be·witch (bi wich/), *v.t.* **1.** to affect by witchcraft or magic. **2.** to charm; fascinate. **—be·witch/ing·ly,** *adv.* **—be·witch/ment,** *n.*

bey (bā), *n., pl.* **beys.** (formerly) a title of respect for Turkish dignitaries.

be·yond (bē ond/), *prep.* **1.** on, at, or to the farther side of. **2.** more distant than. **3.** outside the limits or reach of. *—adv.* **4.** farther on or away.

bez·el (bez/əl), *n.* **1.** the diagonal face at the end of the blade of a chisel or the like. **2.** the part of a cut gem above the setting. **3.** a grooved rim holding a gem or watch crystal in its setting.

bf or **b.f.,** boldface.

Bho·pal (bō päl/), *n.* a city in central India. 672,000.

Bhu·tan (bōō tän/), *n.* a kingdom in the Himalayas, NE of India. 1,400,000. **—Bhu·tan·ese** (bōōt/n ēz/, -ēs/), *n., pl.* **-ese,** *adj.*

Bi, *Chem. Symbol.* bismuth.

bi-, a combining form meaning: twice (*biannual*); two (*bilateral*). **—Usage.** Most words referring to periods of time and prefixed by BI- can be ambiguous. Since BI- can be taken to mean either "twice each" or "every two," a word like *biweekly* can be understood as "twice each week" or "every two weeks." Confusion is often avoided by using the prefix SEMI- meaning "twice each" or by using the appropriate phrases: *twice a week; every two months.*

bi·an·nu·al (bī an/yōō əl), *adj.* occurring twice a year; semiannual. **—bi·an/nu·al·ly,** *adv.*

bi·as (bī/əs), *n., adv., v.,* **bi·ased, bi·as·ing** or (*esp. Brit.*) **bi·assed, bi·as·sing.** *—n.* **1.** a diagonal line running across a woven fabric. **2.** a particular tendency or inclination; prejudice. *—adv.* **3.** in a diagonal manner. *—v.t.* **4.** to cause partiality in; prejudice.

bi·ath·lon (bī ath/lon), *n.* a sports contest combining cross-country skiing with rifle shooting.

bib (bib), *n.* **1.** a shield of cloth, paper, etc., tied under the chin to protect the clothing during a meal. **2.** the upper front part of an apron, overalls, or the like.

Bib., 1. Bible. **2.** biblical.

Bi·ble (bī/bəl), *n.* **1.** the sacred writings of the Christian religion, comprising the Old and New Testaments. **2.** the sacred writings of the Jewish religion; Old Testament. **3.** (*l.c.*) a reference work esteemed for its usefulness and authority. [< OF < ML < Gk *biblíon* book, papyrus roll, der. of *býblos* papyrus, after *Býblos,* Phoenician port known for export of papyrus] **—Bib·li·cal, bib·li·cal** (bib/li kəl), *adj.*

biblio-, a combining form meaning book (*bibliophile*).

bib·li·og·ra·phy (bib/lē og/rə fē), *n., pl.* **-phies.** a list of writings compiled upon some common principle, as

Oxford English Reference Dictionary

Second Edition, Revised

Edited by
Judy Pearsall and Bill Trumble

OXFORD
UNIVERSITY PRESS

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Great Clarendon Street, Oxford OX2 6DP

Oxford University Press is a department of the University of Oxford.
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Published in the United States
by Oxford University Press Inc., New York

© Oxford University Press 1995, 1996, 2002, 2003

First edition 1995
Second edition 1996
Reprinted with updates and corrections 2001
Revised second edition 2002
Reprinted with updates and corrections 2003

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British Library Cataloguing in Publication Data

Data available

Library of Congress Cataloging in Publication Data

Data available

ISBN 0-19-860652-4

10 9 8 7 6 5 4 3

Printed in Italy by
«La Tipografica Varese S.p.A.» Varese

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a

2 the body concerned in an action or process (*cavalcade*). **3** the product or result of a material or action (*arcade*; *lemonade*; *masquerade*). [from or after F *-ade* f. Prov., Sp., or Port. *-ada* or It. *-ata* f. L *-ata* fem. sing. past part. of verbs in *-are*]

-ade[2] /eɪd/ *suffix* forming nouns (*decade*) (cf. -AD[1]). [F *-ade* f. Gk *-as -ada*]

-ade[3] /eɪd/ *suffix* forming nouns: **1** = -ADE[1] (*brocade*). **2** a person concerned (*renegade*). [Sp. or Port. *-ado*, masc. form of *-ada*: see -ADE[1]]

Adelaide /ˈædəˌleɪd/ a city in Australia, the capital and chief port of the state of South Australia; pop. (1990) 1,049,870. Adelaide was named after the wife of William IV.

Adélie Land /æˈdeɪlɪ/ (also **Adélie Coast**) a section of the Antarctic continent south of the 60th parallel, between Wilkes Land and King George V Land. It was discovered in 1840 by the French naval explorer J.-S.-C. Dumont d'Urville, who named it after his wife.

Aden /ˈeɪd(ə)n/ a port in Yemen at the mouth of the Red Sea; pop. (1987) 417,370. Aden was formerly under British rule, first as part of British India (from 1839), then from 1935 as a Crown Colony. It was capital of the former South Yemen from 1967 until 1990.

Aden, Gulf of a part of the eastern Arabian Sea lying between the south coast of Yemen and the Horn of Africa.

Adenauer /ˈædɪˌnaʊə(r)/, Konrad (1876–1967), German statesman, first Chancellor of the Federal Republic of Germany 1949–63. He co-founded the Christian Democratic Union in 1945. As Chancellor, he is remembered for the political and economic transformation of his country. He secured the friendship of the US and was an advocate of strengthening political and economic ties with Western countries through NATO and the European Community.

adenine /ˈædɪˌniːn/ *n.* a purine found in all living tissue as a component base of DNA or RNA. [G *Adenin* formed as ADENOIDS: see -INE[4]]

adenoids /ˈædɪˌnɔɪdz/ *n.pl. Med.* a mass of enlarged lymphatic tissue between the back of the nose and the throat, often hindering speaking and breathing in the young. □ **adenoidal** /ˌædɪˈnɔɪd(ə)l/ *adj.* [Gk *adēn -enos* gland + -OID]

adenoma /ˌædɪˈnəʊmə/ *n.* (*pl.* **adenomas** or **adenomata** /-mətə/) *Med.* a glandlike benign tumour of epithelial tissue, which may in some cases become malignant. [f. Gk *adēn* gland]

adenosine /əˈdenəˌsiːn/ *n. Biochem.* a nucleoside of adenine and ribose present in all living tissue in combined form (see ADP, AMP). □ **adenosine triphosphate** (abbr. **ATP**) a nucleotide whose breakdown in living cells to the diphosphate provides energy for physiological processes. [ADENINE + RIBOSE]

adept /ˈædept, əˈdept/ *adj.* & *n.* ● *adj.* (foll. by *at, in*) thoroughly proficient. ● *n.* usu. /ˈædept/ a skilled performer; an expert. □ **adeptly** *adv.* **adeptness** *n.* [L *adeptus* past part. of *adipisci* attain]

adequate /ˈædɪkwət/ *adj.* **1** sufficient, satisfactory. **2** (foll. by *to*) proportionate. **3** barely sufficient. □ **adequacy** *n.* **adequately** *adv.* [L *adaequatus* past part. of *adaequare* make equal (as AD-, *aequus* equal)]

à deux /æ ˈdɜː/ *adv.* & *adj.* **1** for two. **2** between two. [F]

ad fin. /æd ˈfɪn/ *abbr.* at or near the end. [L *ad finem*]

adhere /ədˈhɪə(r)/ *v.intr.* **1** (usu. foll. by *to*) (of a substance) stick fast to a surface, another substance, etc. **2** (foll. by *to*) behave according to; follow in detail (*adhered to our plan*). **3** (foll. by *to*) give support or allegiance to. [F *adhérer* or L *adhaerere* (as AD-, *haerere haes-* stick)]

adherent /ədˈhɪərənt/ *n.* & *adj.* ● *n.* **1** a supporter of a party, person, etc. **2** a devotee of an activity. ● *adj.* **1** (foll. by *to*) faithfully observing a rule etc. **2** (often foll. by *to*) (of a substance) sticking fast. □ **adherence** *n.* [F *adhérent* (as ADHERE)]

adhesion /ədˈhiːʒ(ə)n/ *n.* **1** the act or process of adhering. **2** the capacity of a substance to stick fast. **3** *Med.* abnormal union of surfaces due to inflammation or injury. **4** the maintenance of contact between the wheels of a vehicle and the road. **5** the giving of support or allegiance. ¶ More common in physical senses (e.g. *the glue has good adhesion*), with *adherence* used in abstract senses (e.g. *adherence to principles*). [F *adhésion* or L *adhaesio* (as ADHERE)]

adhesive /ədˈhiːsɪv/ *adj.* & *n.* ● *adj.* sticky, enabling surfaces or substances to adhere to one another. ● *n.* an adhesive substance, esp. one used to stick other substances together. □ **adhesively** *adv.* **adhesiveness** *n.* [F *adhésif -ive* (as ADHERE)]

adhibit /ədˈhɪbɪt/ *v.tr.* (**adhibited, adhibiting**) **1** affix. **2** apply or administer (a remedy). □ **adhibition** /ˌædhɪˈbɪʃ(ə)n/ *n.* [L *adhibere adhibit-* (as AD-, *habere* have)]

ad hoc /æd ˈhɒk/ *adv.* & *adj.* for a particular (usu. exclusive) purpose (*an ad hoc appointment*). [L, = to this]

ad hominem /æd ˈhɒmɪˌnem/ *adv.* & *adj.* **1** relating to or associated with a particular person. **2** (of an argument) appealing to the emotions and not to reason. [L, = to the person]

adiabatic /ˌeɪdaɪəˈbætɪk/ *adj.* & *n. Physics* ● *adj.* **1** impassable to heat. **2** occurring without heat entering or leaving the system. ● *n.* a curve or formula for adiabatic phenomena. □ **adiabatically** *adv.* [Gk *adiabatos* impassable (as A-[1], *diabainō* pass)]

adiantum /ˌædɪˈæntəm/ *n.* **1** a fern of the genus *Adiantum*; maidenhair fern. **2** (in general use) a spleenwort. [L f. Gk *adianton* maidenhair (as A-[1], *diantos* wettable)]

adieu /əˈdjuː/ *int.* & *n.* ● *int.* goodbye. ● *n.* (*pl.* **adieus** or **adieux** /əˈdjuːz/) a goodbye. [ME f. OF f. *à* to + *Dieu* God]

Adi Granth /ˌɑːdɪ ˈgrʌnt/ the principal sacred scripture of Sikhism, also called the *Granth Sahib* or 'Revered Book'. The original compilation was made under the direction of Arjan Dev (1563–1606), the fifth Sikh guru; it contains hymns and religious poetry as well as the teachings of the first five gurus. Successive gurus added to the text: the tenth and last guru, Gobind Singh (1666–1708), declared that henceforward there would be no more gurus, the Adi Granth taking their place. [Hindi (= first book), f. Skr.]

ad infinitum /æd ˌɪnfɪˈnaɪtəm/ *adv.* without limit; for ever. [L]

ad interim /æd ˈɪntərɪm/ *adv.* & *adj.* for the meantime. [L]

adios /ˌædɪˈɒs/ *int.* goodbye. [Sp. *adiós* f. *a* to + *Dios* God]

adipocere /ˈædɪpəˌsɪə(r)/ *n.* a greyish fatty or soapy substance generated in dead bodies subjected to moisture. [F *adipocire* f. L *adeps adipis* fat + F *cire* wax f. L *cera*]

adipose /ˈædɪˌpəʊz, -ˌpəʊs/ *adj.* of or characterized by fat; fatty. □ **adipose tissue** fatty connective tissue in animals. □ **adiposity** /ˌædɪˈpɒsɪtɪ/ *n.* [mod.L *adiposus* f. *adeps adipis* fat]

Adirondack Mountains /ˌædɪˈrɒndæk/ (also **Adirondacks**) a range of mountains in New York State, source of the Hudson and Mohawk rivers.

Adis Abeba see ADDIS ABABA.

adit /ˈædɪt/ *n.* **1** a horizontal entrance or passage in a mine. **2** a means of approach. [L *aditus* (as AD-, *itus* f. *ire it-* go)]

Adivasi /ˌɑːdɪˈvɑːsɪ/ *n.* (*pl.* **Adivasis**) a member of the aboriginal tribal peoples of India. [Hindi *ādivāsī* original inhabitant]

Adj. *abbr.* (preceding a name) Adjutant.

adjacent /əˈdʒeɪs(ə)nt/ *adj.* (often foll. by *to*) lying near or adjoining. □ **adjacency** *n.* [ME f. L *adjacere* (as AD-, *jacere* lie)]

adjective /ˈædʒɪktɪv/ *n.* & *adj.* ● *n.* a word or phrase naming an attribute, added to or grammatically related to a noun to modify it or describe it. ● *adj.* additional; not standing by itself; dependent. □ **adjectival** /ˌædʒɪkˈtaɪv(ə)l/ *adj.* **adjectivally** *adv.* [ME f. OF *adjectif -ive* ult. f. L *adjicere adject-* (as AD-, *jacere* throw)]

adjoin /əˈdʒɔɪn/ *v.tr.* **1** (often as **adjoining** *adj.*) be next to and joined with. **2** *archaic* = ADD 1. [ME f. OF *ajoindre, ajoign-* f. L *adjungere adjunct-* (as AD-, *jungere* join)]

adjourn /əˈdʒɜːn/ *v.* **1** *tr.* **a** put off; postpone. **b** break off (a meeting, discussion, etc.) with the intention of resuming later. **2** *intr.* of persons at a meeting: **a** break off proceedings and disperse. **b** (foll. by *to*) transfer the meeting to another place. [ME f. OF *ajorner* (as AD-, *jorn* day ult. f. L *diurnus* DIURNAL): cf. JOURNAL, JOURNEY]

adjournment /əˈdʒɜːnmənt/ *n.* adjourning or being adjourned. □ **adjournment debate** *Brit.* a debate in the House of Commons on the motion that the House be adjourned, used as an opportunity for raising various matters.

adjudge /əˈdʒʌdʒ/ *v.tr.* **1** adjudicate (a matter). **2** (often foll. by *that* + clause, or *to* + infin.) pronounce judicially. **3** (foll. by *to*) award judicially. **4** *archaic* condemn. □ **adjudgement** *n.* (also **adjudgment**). [ME f. OF *ajuger* f. L *adjudicare*: see ADJUDICATE]

adjudicate /əˈdʒuːdɪˌkeɪt/ *v.* **1** *intr.* act as judge in a competition, court, tribunal, etc. **2** *tr.* **a** decide judicially regarding (a claim etc.). **b** (foll. by *to be* + complement) pronounce (*was adjudicated to be bankrupt*). □ **adjudicator** *n.* **adjudicative** /-kətɪv/ *adj.* **adjudication** /əˌdʒuːdɪˈkeɪʃ(ə)n/ *n.* [L *adjudicare* (as AD-, *judicare* f. *judex -icis* judge)]

adjunct /ˈædʒʌŋkt/ *n.* **1** (foll. by *to, of*) a subordinate or incidental thing. **2** an assistant; a subordinate person, esp. one with temporary appointment only. **3** *Gram.* a word or phrase used to amplify or modify the meaning of another word or words in a sentence. □ **adjunctive** /əˈdʒʌŋktɪv/ *adj.* [L *adjunctus*: see ADJOIN]

US005942774A

United States Patent [19]

Isogai et al.

[11] Patent Number: 5,942,774

[45] Date of Patent: Aug. 24, 1999

[54] **PHOTOELECTRIC CONVERSION ELEMENT AND PHOTOELECTRIC CONVERSION APPARATUS**

[75] Inventors: **Tadao Isogai**, Yokohama; **Atsushi Kamashita**, Kawasaki; **Satoshi Suzuki**, Yokohama, all of Japan

[73] Assignee: **Nikon Corporation**, Tokyo, Japan

[21] Appl. No.: **08/606,995**

[22] Filed: **Feb. 26, 1996**

[30] **Foreign Application Priority Data**

Feb. 24, 1995 [JP] Japan 7-060034
Feb. 21, 1996 [JP] Japan 8-033833

[51] **Int. Cl.**^{6} **H01L 27/146**

[52] **U.S. Cl.** **257/292**; 257/257; 257/258; 257/435; 257/445; 257/446; 257/448

[58] **Field of Search** 257/292, 256, 257/257, 258, 272, 435, 443, 446, 445, 448, 461; 358/482

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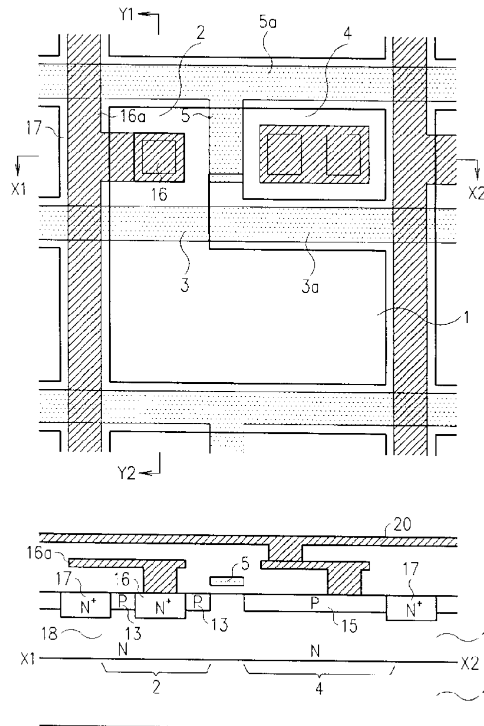
Primary Examiner—John Guay
Attorney, Agent, or Firm—Foley & Lardner

[57] **ABSTRACT**

A photoelectric conversion element includes a photoelectric conversion portion for generating and storing a charge according to incident light, an amplifying portion having a control region for generating a signal output according to the charge received in the control region from the photoelectric conversion portion, a transfer control portion for transferring the charge generated and stored in the photoelectric conversion portion to the control region of the amplifying portion, a reset-purpose charge draining region for draining the charge transferred to the control region of the amplifying portion, and a reset-purpose control region for controlling the reset-purpose charge draining region. A reset operation can be performed without operating the amplifying portion. Also, a photoelectric conversion apparatus having high sensitivity and low dissipation power can be obtained.

9 Claims, 14 Drawing Sheets



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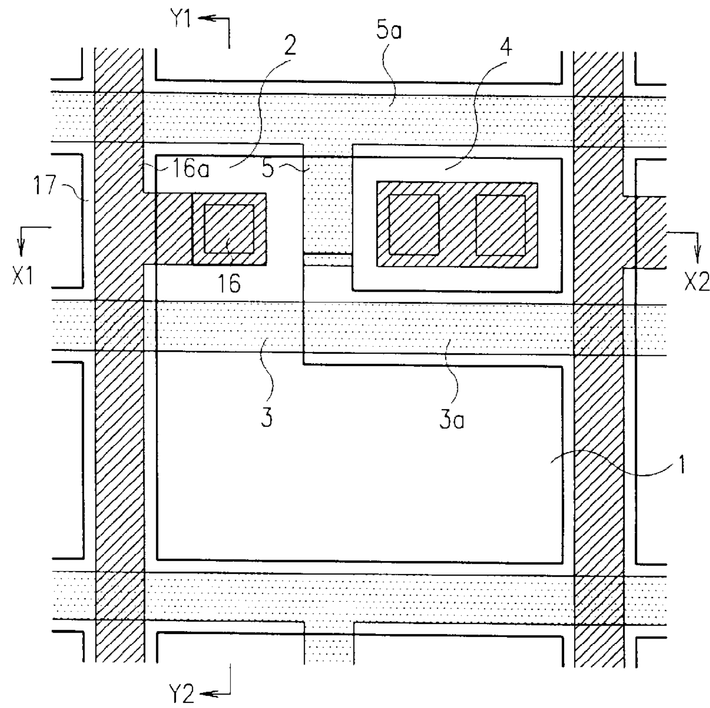

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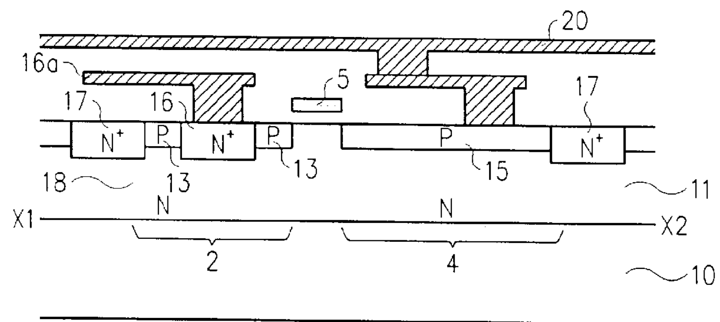
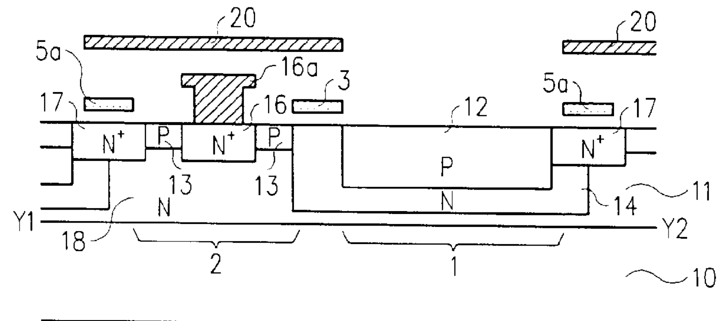


Fig. 1C



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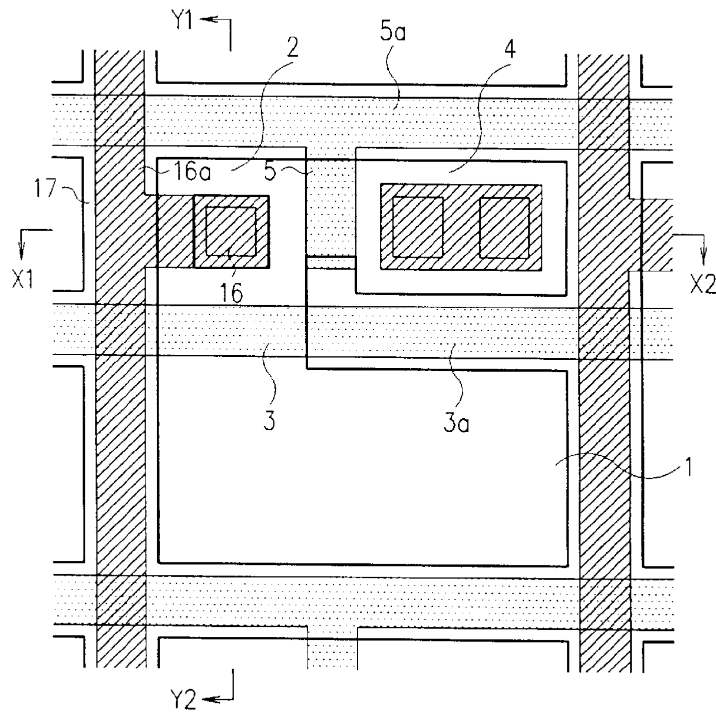

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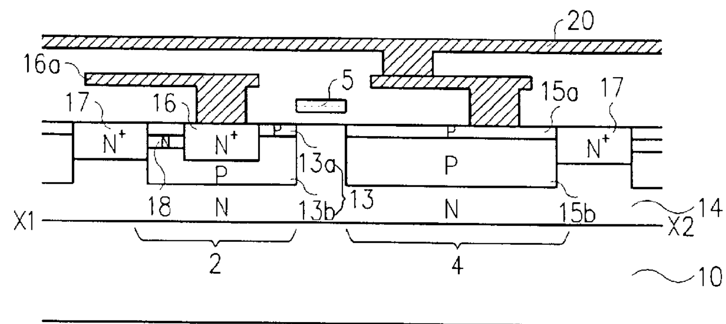

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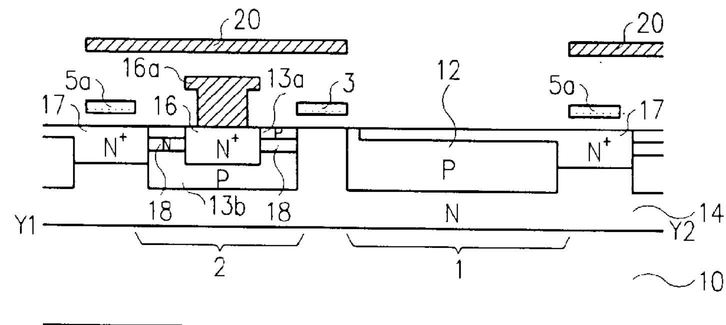
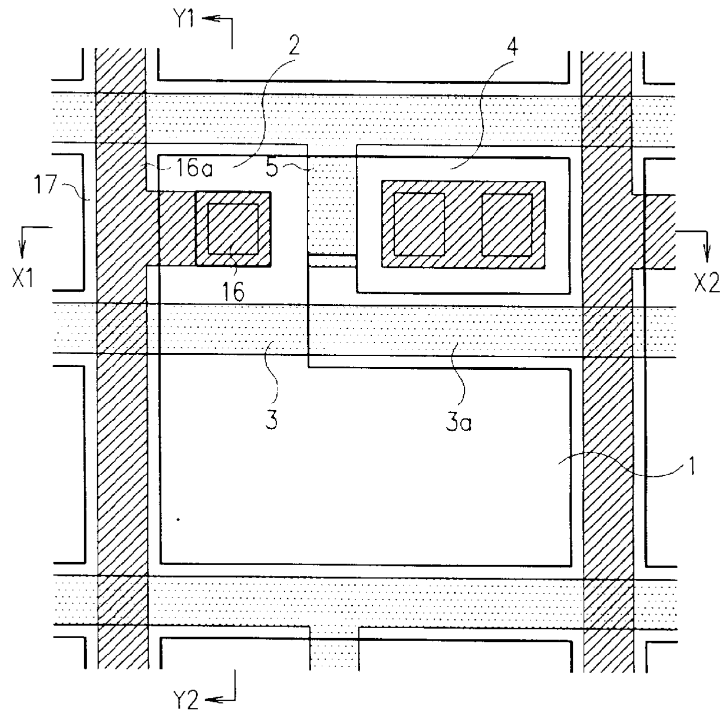


Fig. 3A



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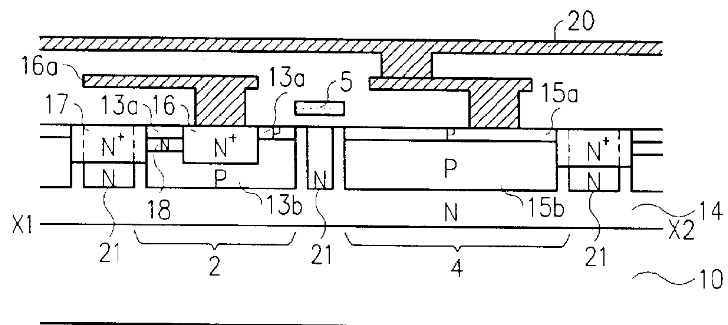

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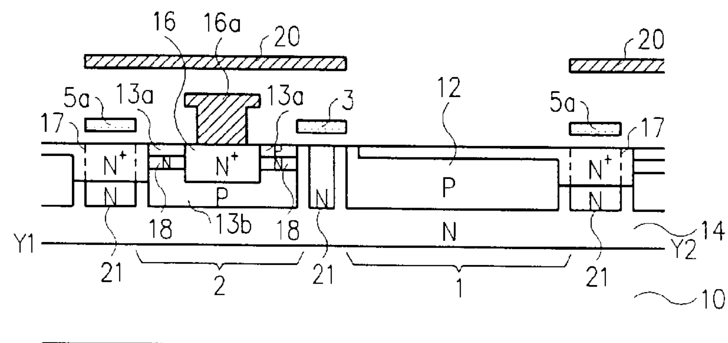

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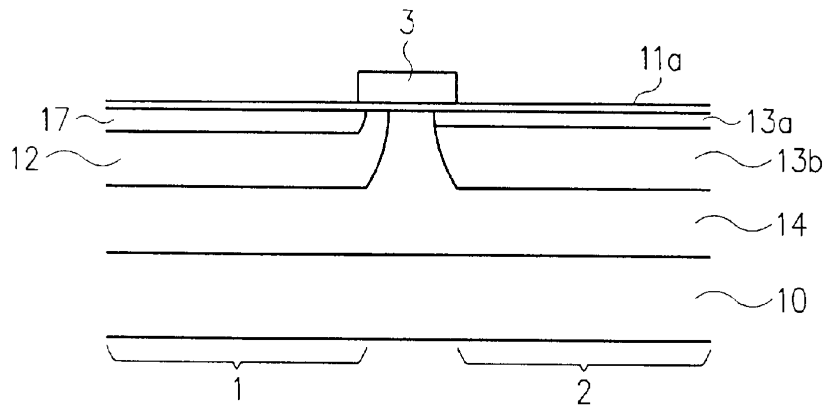

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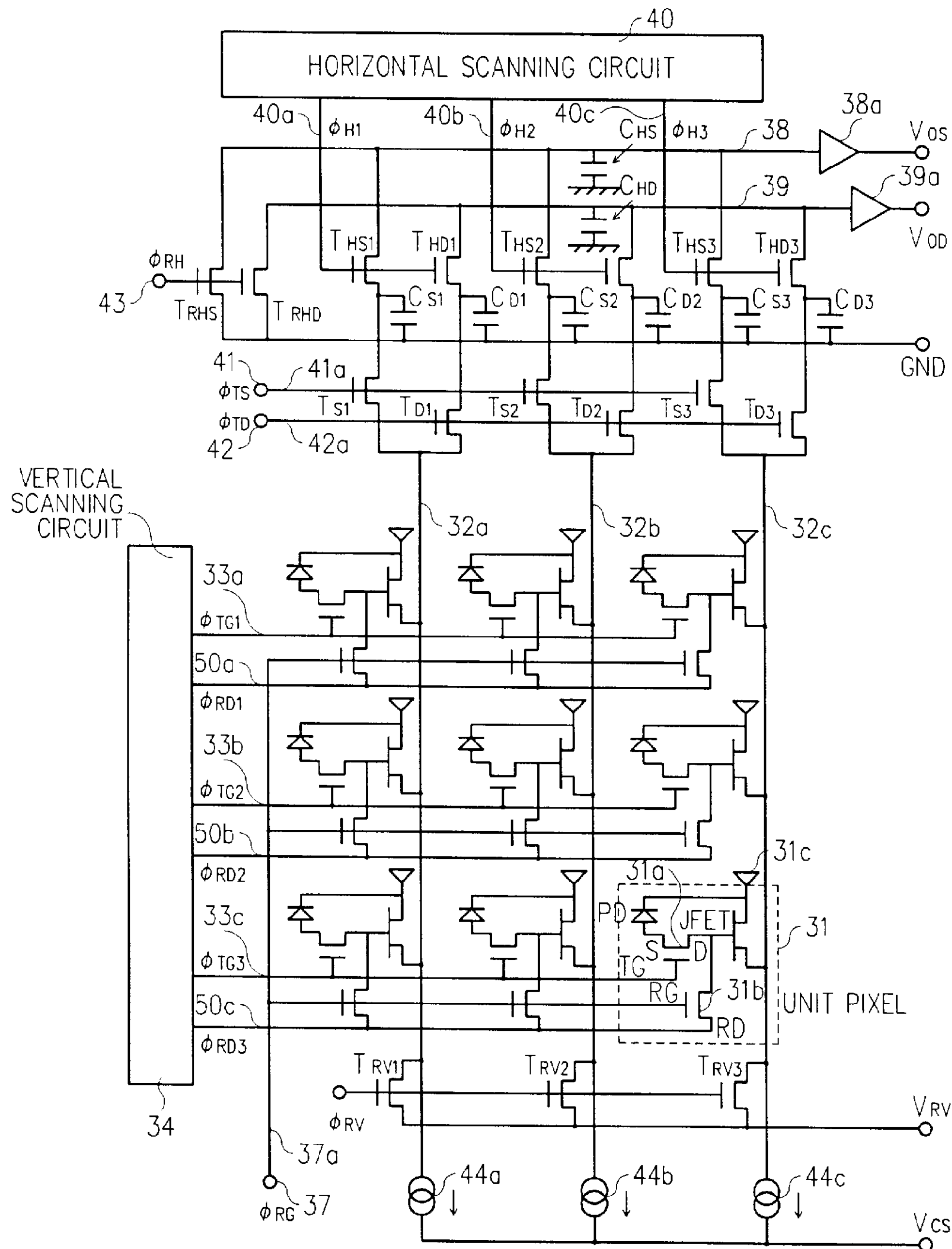

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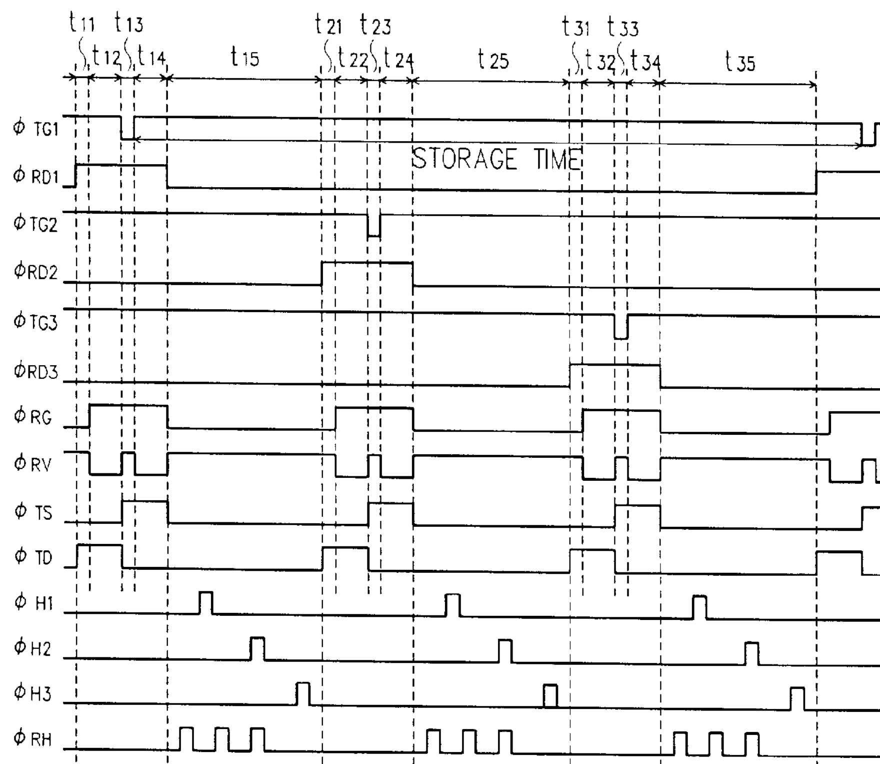

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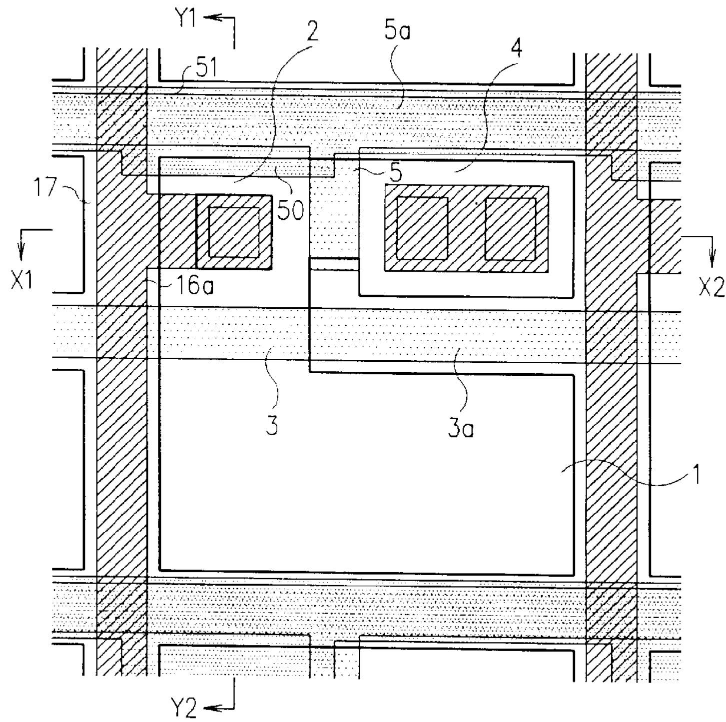

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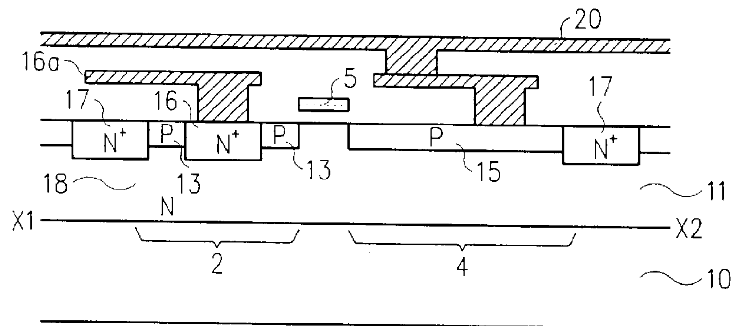

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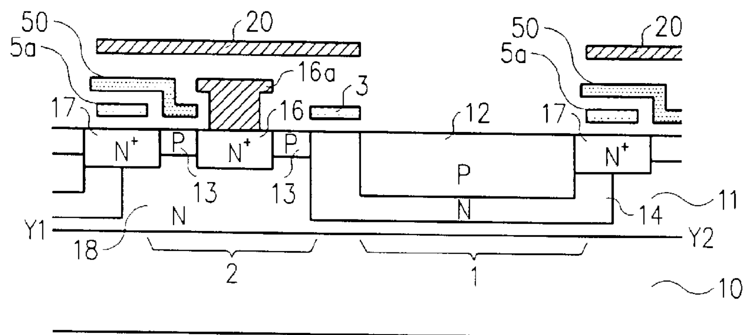
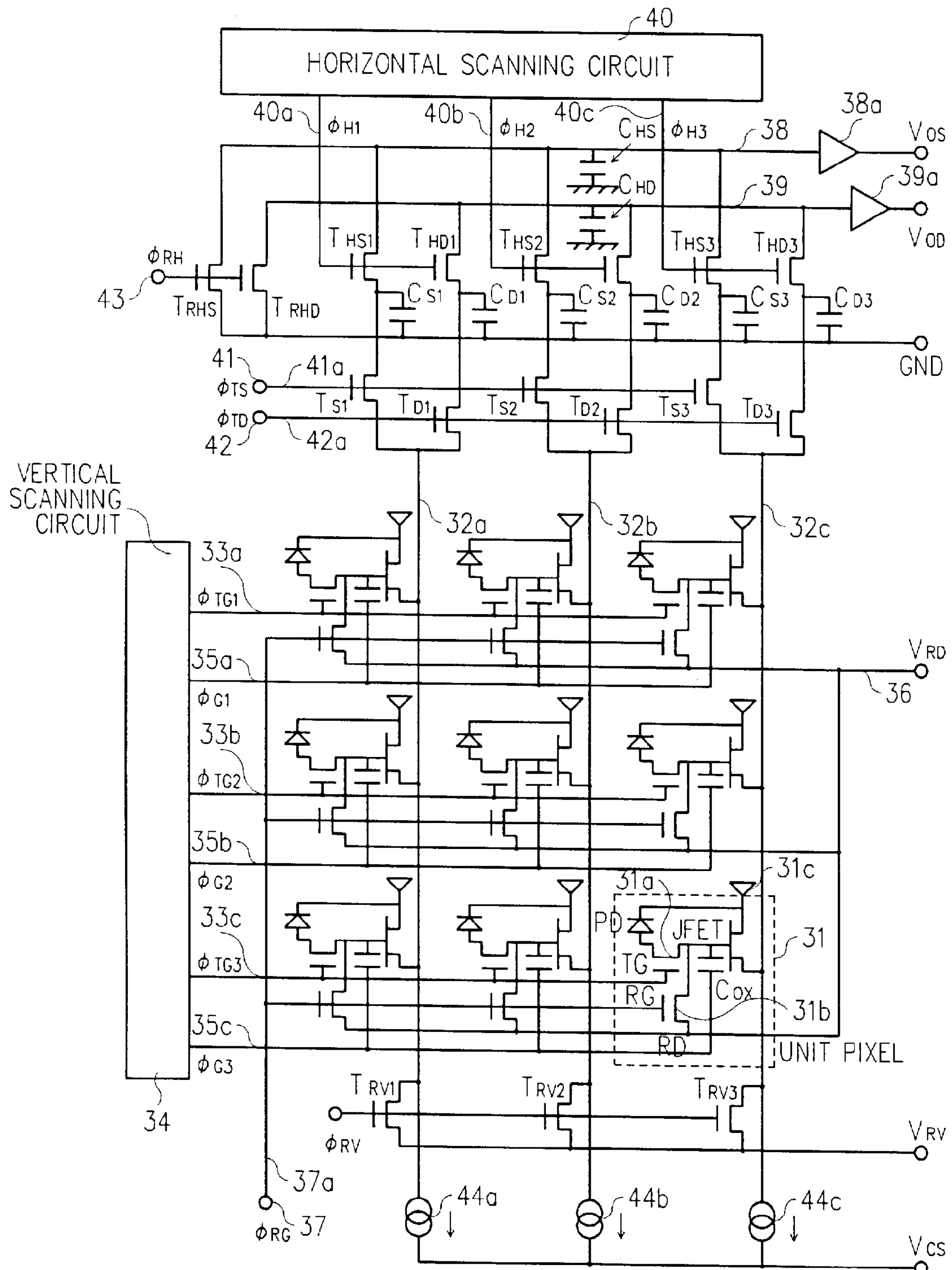


Fig. 8



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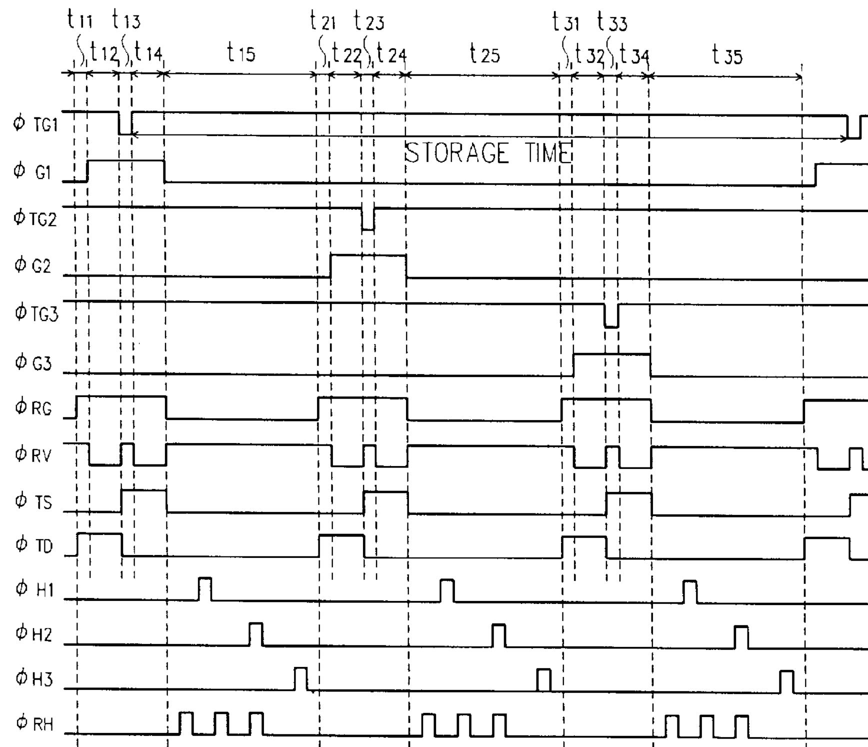

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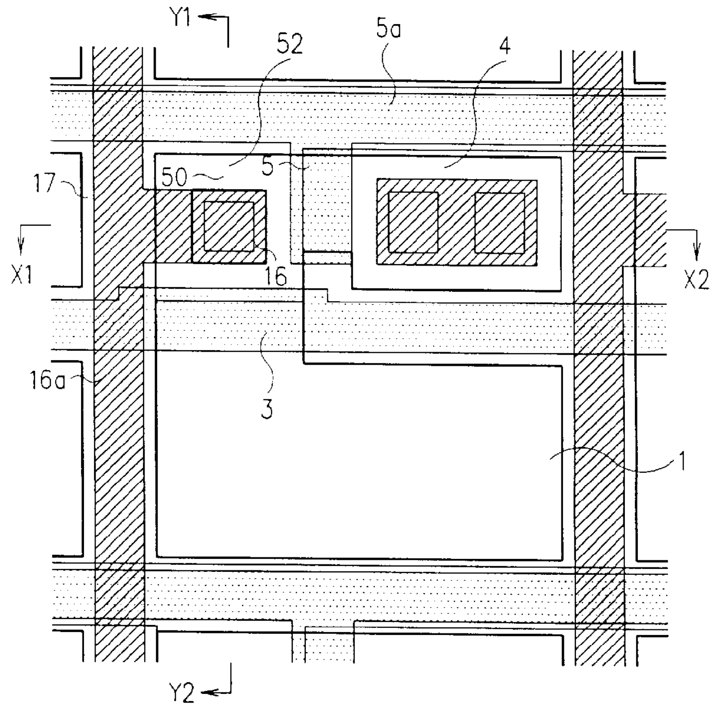

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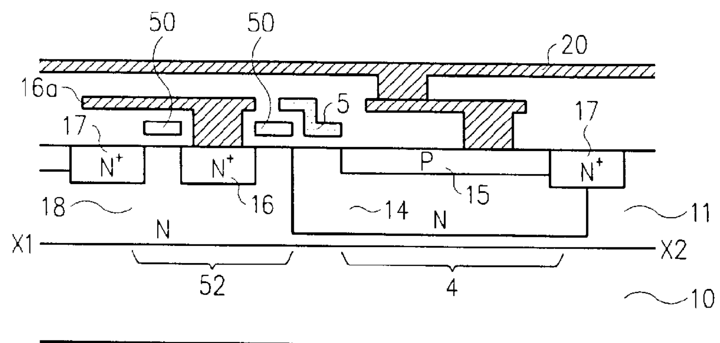

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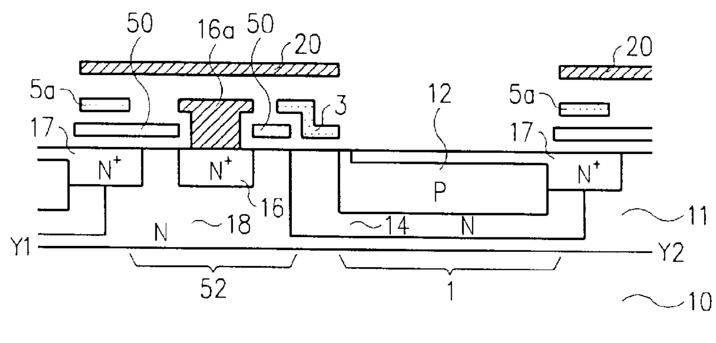

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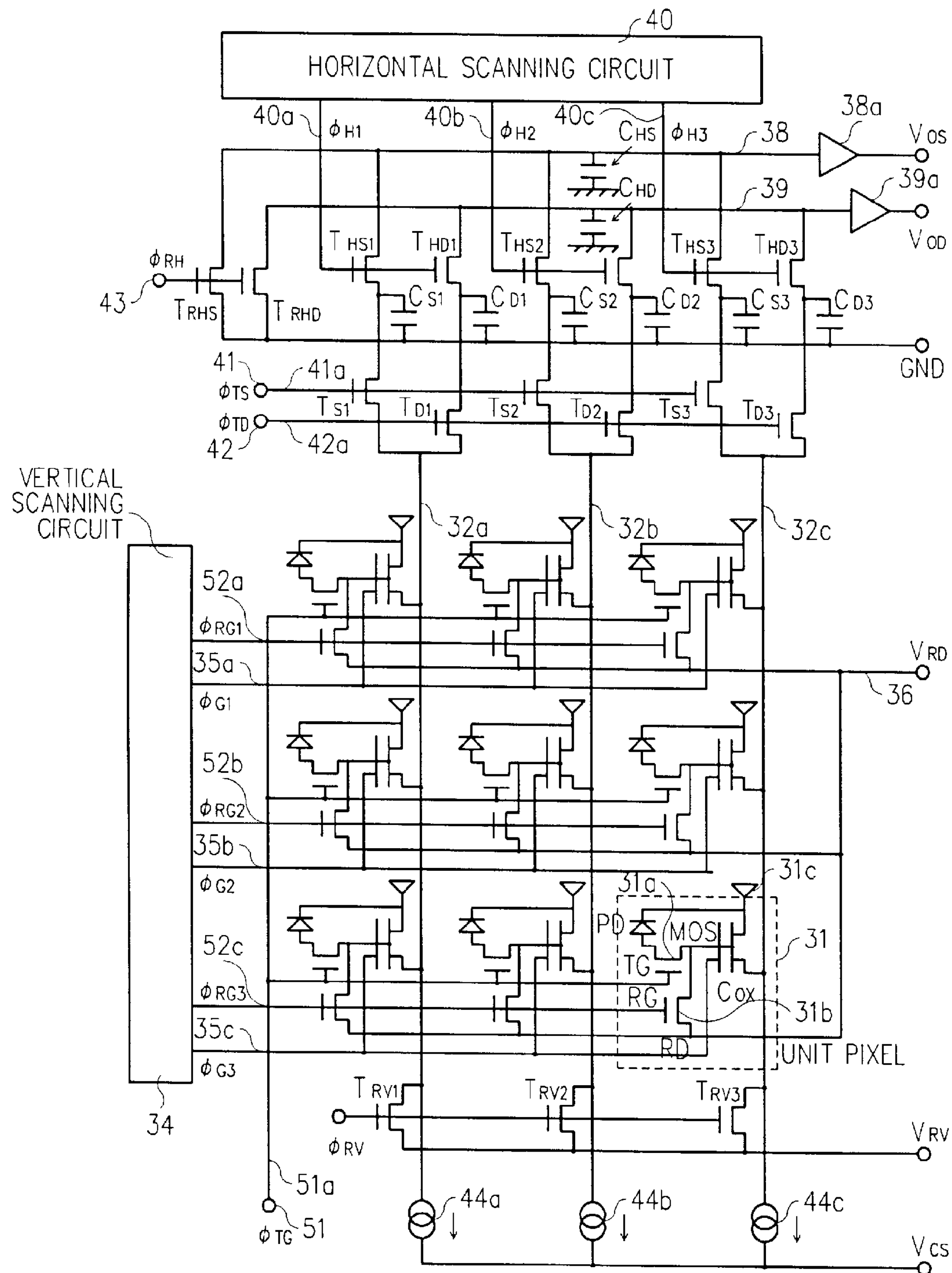


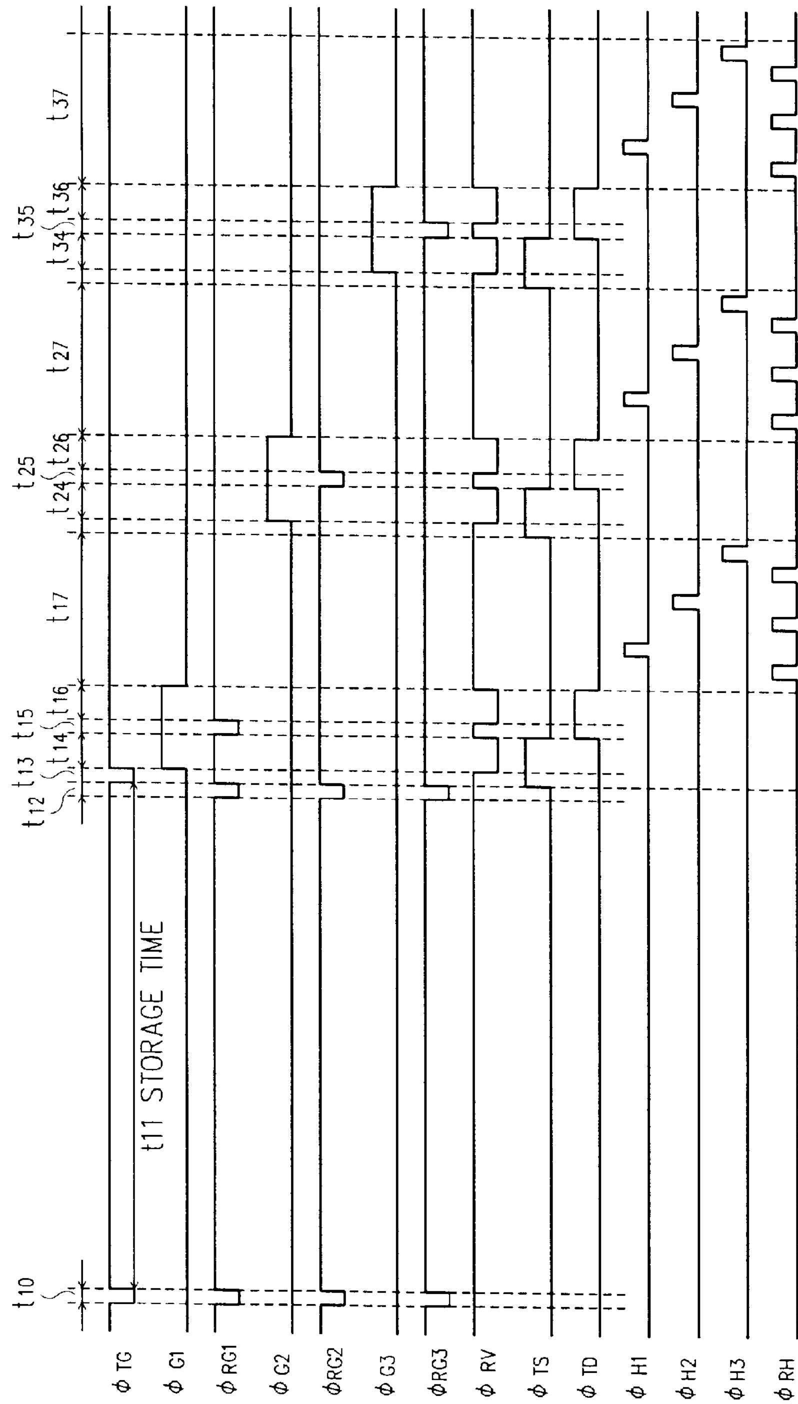


Fig. 12

Fig. 13A

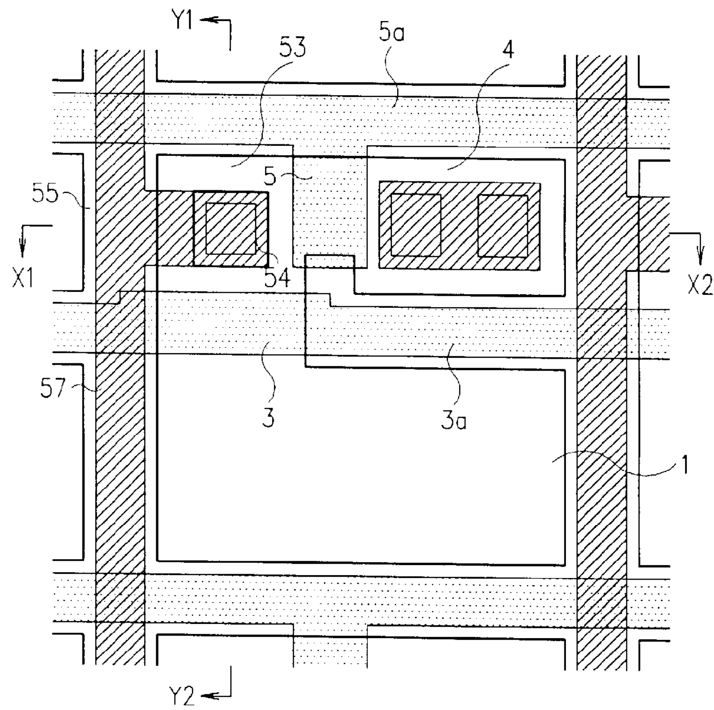


Fig. 13B

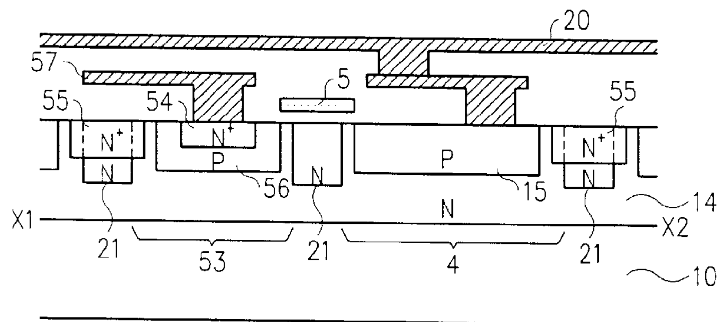


Fig. 13C

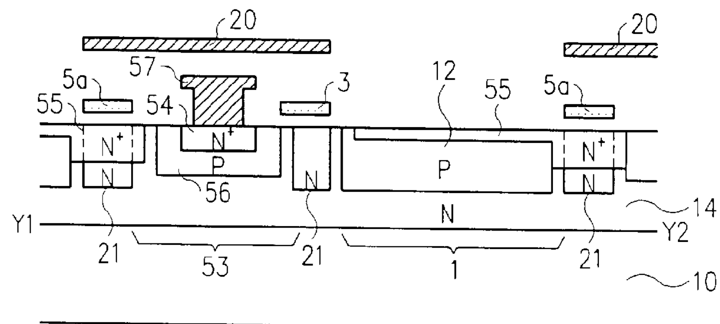


Fig. 14A

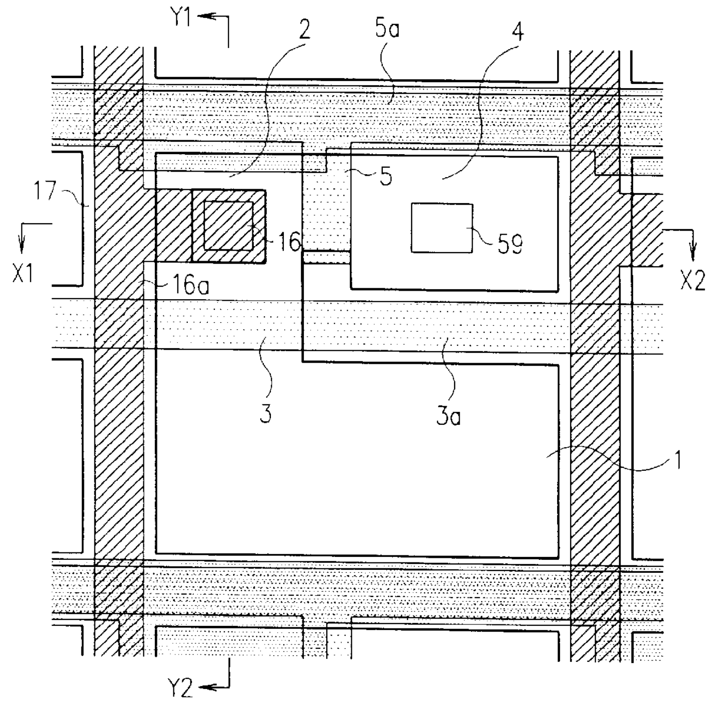


Fig. 14B

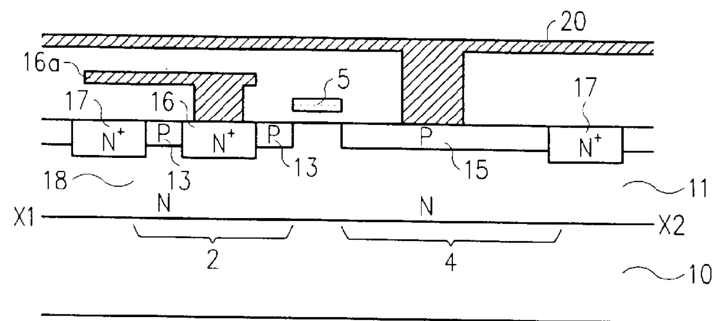
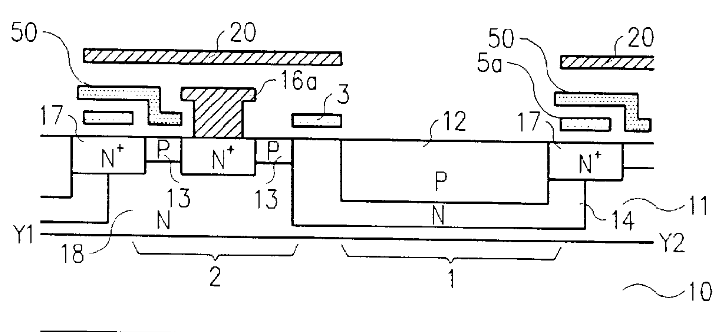


Fig. 14C



PHOTOELECTRIC CONVERSION ELEMENT AND PHOTOELECTRIC CONVERSION APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to photoelectric conversion elements and photoelectric conversion apparatus, and more particularly to photoelectric conversion elements that can perform a reset operation without operating an amplifying portion, and photoelectric conversion apparatus that can perform a high-speed reset operation.

2. Related Background Art

The conventional photoelectric conversion elements of an amplification type utilizing transistors, proposed in order to enhance the sensitivity of photoelectric conversion apparatus (including solid state image sensing devices etc.), include MOS type (normally, depletion MOS type) devices, bipolar type devices, and junction field effect transistor (JFET) type devices. In these photoelectric conversion elements, when light impinges on a MOS diode (of the MOS type) or on a pn junction diode (of the bipolar type or the JFET type), which is a part of constituent elements forming a photoelectric conversion element, the incident light is photoelectrically converted into a charge according thereto, the charge is stored, a signal according to the stored charge is amplified (in current amplification or in charge amplification), and then the amplified signal is output.

Among the above photoelectric conversion elements some photoelectric conversion elements are arranged to perform all operations including the photoelectric conversion operation, amplification operation, and initialization operation with a single transistor (which means that a photoelectric conversion element is composed of a single transistor). The photoelectric conversion elements of this type have two significant problems. Here, the initialization operation means an operation for setting the potential of a control region of the transistor to a certain reference value or an operation to completely deplete the control region. The control region of the transistor is a region for controlling the current, for example, which is a gate diffusion region in the JFET or a base diffusion region in the bipolar transistor.

The first problem is an increase of noise in the photoelectric conversion portion. For example, in the case of the MOS type device, photoelectric conversion is normally provided by a MOS diode with a gate electrode of polysilicon. In this case, since the silicon surface side is depleted at that point, it is directly affected by a great dark current appearing on the surface, resulting in increasing the noise. It also had the problem of a low utilization factor (quantum efficiency) of light because polysilicon has low transmittance of light.

The bipolar type and JFET type devices effecting photoelectric conversion by the pn junction diode are also affected by the dark current. This is because an ideal diode structure such as a buried photodiode suitably employed in a CCD image pickup element or the like cannot be realized because of the restriction that a part of the constituent elements of the transistor is utilized (which means that, in the case of the bipolar type and JFET type devices, a depletion layer occurring from the pn junction portion reaches the surface). Therefore, the noise becomes great because of the dark current.

Normally, these pn junction diodes perform such reset operation as to recombine the charge generated and stored,

by transient and considerably deep forward bias drive by capacitive coupling. However, this reset method will cause the problem of occurrence of reset noise and after-image (lag).

A further problem is that when the charge generated and stored was reset and when blooming (bleeding) suppressing operation was carried out, the transistor also operated (or became "on"), and a large current flowed in the transistor itself constituting the photoelectric conversion element, which greatly changed the bias point (operating point) of the transistor transiently to change the amplification factor. For example, when a photoelectric conversion apparatus is composed of a lot of such photoelectric conversion elements arrayed, there occur variations in outputs from the photoelectric conversion elements, causing problems of the lowering the performance of apparatus (for example, S/N ratios) and increasing dissipation power because of the many arrayed elements.

The second problem is that the sensitivity is limited. To begin with, the above various (MOS type, bipolar type, and JFET type) transistors (photoelectric conversion elements) utilize a potential change caused when the charge generated by photoelectric conversion is stored in the control region in a floating state, in order to effect current amplification or charge amplification. Namely, they obtain an amplified output by utilizing a change of the surface potential of silicon under the gate electrode, in the case of the depletion MOS type transistor, or a potential change of the base region in the case of the bipolar device or of the gate region, in the case of the JFET type device.

Accordingly, in order to achieve high sensitivity, it is necessary to increase an amount of this potential change (stored charge amount/capacitance). For that purpose, the capacitance of the control region is preferably as small as possible. However, the area of the photoelectric conversion portion (a light-receiving aperture ratio) needs to be increased in order to raise the utilization factor of incident light and thereby increase the charge amount. However, in the case of the photoelectric conversion element where only one transistor performs the all operations (including the photoelectric conversion operation, the amplification operation, and the initialization operation), the control region is nothing but the photoelectric conversion portion, and, therefore, the capacitance becomes greater with an increase of the aperture ratio. As a result, the sensitivity is limited.

Also proposed on the other hand are photoelectric conversion elements arranged in such a manner that the photoelectric conversion portion is separated from an amplifying transistor, the charge generated and stored in the photoelectric conversion portion is transferred through a transfer gate of a transfer control portion to the control region of the transistor, and an output is obtained by current amplification or charge amplification. For example, Japanese Patent Laid-open Nos. 5-235317 (corresponding to U.S. patent application Ser. No. 08/261,135) and 5-275670 disclose photoelectric conversion elements in which the amplifying portion of the depletion type MOS transistor or the JFET is combined with the photodiode and the transfer control portion (transfer gate).

In the photoelectric conversion elements arranged by separating the photoelectric conversion portion from the amplifying transistor and providing the transfer gate, as described above, if a buried photodiode is used for the photoelectric conversion portion, the photoelectric conversion elements can be achieved with high quantum efficiency and without occurrence of lag, dark current, or reset noise.

When a buried photodiode in a vertical overflow structure is used for the photoelectric conversion portion, the blooming suppressing operation by the amplifying transistor becomes unnecessary, because the photodiode has a blooming suppressing function. For example, when a photoelectric conversion apparatus is composed of such photoelectric conversion elements, the apparatus is free of the problem of increase of dissipation power and the problem that variations appear in outputs from the photoelectric conversion elements due to changes of bias points (operating points).

Further, because the photoelectric conversion portion is separated from the amplifying transistor, the structure and size of the transistor can be optimized by taking only the amplifying function into consideration. Therefore, high sensitivity can be secured by decreasing the capacitance of the control region.

In addition, the new problems including the dark current, lag, and reset noise, caused by the transistor itself, can effectively be removed by the configuration and drive method of the photoelectric conversion apparatus with these photoelectric conversion elements arranged in a matrix.

Thus, the photoelectric conversion element with the separate photoelectric conversion portion and amplifying transistor and with the transfer gate is considerably lowered in noise and enhanced in sensitivity, as compared with the photoelectric conversion element arranged to perform all operations (including the photoelectric conversion operation, the amplification operation, and the initialization operation) by a transistor.

However, the above conventional photoelectric conversion element (which is the photoelectric conversion element provided with the separate photoelectric conversion portion and amplifying transistor and the transfer gate) had the problem that there is no improvement in the reset operation compared to the other conventional photoelectric conversion element arranged to perform the all operations by a single transistor.

Namely, the conventional photoelectric conversion element (the photoelectric conversion element with the separate photoelectric conversion portion and amplifying transistor and the transfer gate) also had the problem that when the reset operation was started in order to initialize the control region of the transistor, the amplifying transistor itself also operated (or became "on") at the same time therewith.

As a result, a large current flows in the amplifying transistor, which greatly changes the bias point (operating point) of the amplifying transistor transiently, thereby changing the amplification factor. For example, when a photoelectric conversion apparatus was composed of a lot of photoelectric conversion elements of this type arrayed, there were problems that variations appeared in outputs from the photoelectric conversion elements, that the performance of the apparatus (for example, S/N ratios) was degraded, and that the dissipation power increased because of the array of many elements.

SUMMARY OF THE INVENTION

The present invention has been developed in view of the above circumstances, and an object thereof is to obtain a photoelectric conversion element capable of performing the reset operation without operating the amplifying portion.

Another object of the present invention is to obtain a photoelectric conversion element that can suppress occurrence of fixed pattern noise.

Still another object of the present invention is to obtain a photoelectric conversion element that can improve the aperture ratio and the degree of integration.

Still another object of the present invention is to obtain a photoelectric conversion element that can suppress the phenomenon of blur such as blooming due to obliquely incident light.

Still another object of the present invention is to obtain a photoelectric conversion element that can attain ideal characteristics such as suppressing the dark current, lag, and reset noise.

Still another object of the present invention is to obtain a photoelectric conversion element that can enhance the sensitivity.

A further object of the present invention is to obtain a photoelectric conversion apparatus that can suppress the degradation of performance (for example, S/N ratios) of the apparatus and the increase of dissipation power, as accomplished under the above circumstances.

Still another object of the present invention is to obtain a photoelectric conversion apparatus that can perform a high-speed reset operation.

Still another object of the present invention is to obtain a photoelectric conversion apparatus that can attain signal outputs according to only photogenerated charge components.

One aspect of the present invention is a photoelectric conversion element comprising: a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein; an amplifying portion having a control region for generating a signal output according to the charge received in the control region from said photoelectric conversion portion; a transfer control portion for transferring the charge generated and stored in the photoelectric conversion portion to the control region of the amplifying portion; reset-purpose charge draining means for draining the charge transferred to the control region of the amplifying portion; and reset-purpose control means for controlling the reset-purpose charge draining means.

Here, the photoelectric conversion portion generates the charge according to the incident light and stores it. The amplifying portion generates the signal output according to the charge received by the control region. The transfer control portion transfers the charge generated and stored in the above photoelectric conversion portion to the control region of the above amplifying portion. The reset-purpose charge draining means drains the charge transferred to the control region of the above amplifying portion. The reset-purpose control means controls the above reset-purpose charge draining means.

Namely, in the case of the conventional photoelectric conversion elements, when the reset operation is carried out in order to initialize the control region of the amplifying portion (or to eliminate the charge (signal charge) remaining in the control region), the amplifying portion itself is operated (or turned on) and thus, for example, a large current flows in the amplifying portion itself, which causes the problem that the amplifying factor changes because of large transient fluctuations of the bias point (operating point) of the amplifying portion.

Since in the present invention the reset-purpose charge draining means and the reset-purpose control means for initializing the control region of the amplifying portion are formed separately and independently, the amplifying portion does not operate upon the reset operation. This can solve the problem that the large current flows in the amplifying portion itself by the reset operation and it causes the amplification factor to change because of transient great fluctuations of the bias point (operating point) of the amplifying portion as in the conventional photoelectric conversion elements.

Generally, the above amplifying portion often comprises control means for controlling the control region of the amplifying portion by capacitive coupling. However, without provision of this control means, wiring to the control means is not necessary, fabrication is easy, the capacitance of the control region of the amplifying portion can be smaller by that degree of no provision of control means, and the sensitivity can be enhanced.

Another aspect of the present invention is the photoelectric conversion element further comprising the control means for controlling the control region of the amplifying portion by capacitive coupling.

Namely, the amplifying portion of the photoelectric conversion element often has the control means for controlling the control region of the amplifying portion by capacitive coupling. Also in the case of the photoelectric conversion element provided with the control means, the amplifying portion does not operate upon the reset operation by forming the reset-purpose charge draining means and reset-pnrpose control means for initializing the control region of the amplifying portion separately and independently from the amplifying portion. Thus, this arrangement can solve the problem that the large current flows in the amplifying portion itself by the reset operation and this causes the amplification factor to change because of large transient fluctuations of the bias point (operating point) of the amplifying portion.

Still another aspect of the present invention is the photoelectric conversion element wherein the amplifying portion is comprised of a field effect transistor (FET).

Namely, the above amplifying portion preferably can suppress generation of fixed pattern noise based on signal (charge) destruction. For that purpose, the amplifying portion is preferably constructed of a field effect transistor (FET) for amplifying the charge (signal charge) generated and stored in the photoelectric conversion portion on a non-destructive basis.

Still another aspect of the present invention is the photoelectric conversion element wherein an element isolation region of a predetermined conductivity type is formed between mutual regions of the photoelectric conversion portion, the amplifying portion, the transfer control portion, the reset-purpose charge draining means, and the reset-purpose control means.

The clearances of the mutual regions between the above photoelectric conversion portion, amplifying portion, transfer control portion, reset-purpose charge draining region, and reset-purpose control means are generally desired to be formed as small as possible in view of the aperture ratio and the degree of integration. However, it is difficult to make the clearances of the mutual regions small, because of the influence of so-called side diffusion of dopant (impurity) in the fabrication process of the photoelectric conversion element.

Accordingly, the aperture ratio and the degree of integration can be improved by forming the element isolation region of the predetermined conductivity type between the mutual regions of the photoelectric conversion portion, amplifying portion, transfer control portion, reset-purpose charge draining means, and reset-purpose control means whereby the above clearances of the mutual regions can be formed as small as possible.

Still another aspect of the present invention is the photoelectric conversion element wherein a metal interconnection connected to the reset-purpose charge draining means is formed of a light-shielding film for shielding incident light to the amplifying portion, the transfer control portion, the reset-purpose charge draining means, and the reset-purpose control means.

Namely, the metal interconnection also serves as a light-shielding film. It thus becomes unnecessary to form an extra light-shielding film for shielding the incident light, and it becomes possible to decrease the thickness of the entire photoelectric conversion element. Also, it becomes possible to improve the degree of integration, and to set the metal wiring and light-shielding film in the vicinity of the photoelectric conversion portion, thereby suppressing the phenomenon of bleeding such as blooming due to obliquely incident light.

Still another aspect of the present invention is the photoelectric conversion element wherein the photoelectric conversion portion is comprised of a pn junction photodiode of a vertical overflow structure.

Namely, also in the photoelectric conversion element in which the reset-pnrpose charge draining means and reset-purpose control means are provided separately and independently of the amplifying portion, the photoelectric conversion portion can be formed of the pn junction photodiode of the vertical overflow structure. Then the phenomenon of bleeding such as blooming and smear can be suppressed by constructing the photoelectric conversion portion of the pn junction photodiode of the vertical overflow structure.

Still another aspect of the present invention is the photoelectric conversion element wherein the photoelectric conversion portion is comprised of a buried photodiode of the vertical overflow structure.

Namely, also in the photoelectric conversion element provided with the reset-purpose charge draining means and reset-purpose control means separate and independent of the amplifying portion, the photoelectric conversion portion can be comprised of the buried photodiode of the vertical overflow structure. The ideal characteristics to suppress the bleeding phenomenon such as blooming and smear and to suppress the dark current, lag, and reset noise can be attained by forming the photoelectric conversion portion of the buried photodiode of the vertical overflow structure.

Still another aspect of the present invention is the photoelectric conversion element wherein the amplifying portion is comprised of a junction field effect transistor (JFET) and wherein a channel forming portion of the junction field effect transistor is formed of a first conductivity type gate region, a second conductivity type channel region, and a first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate.

Namely, the amplifying portion of the photoelectric conversion element may also be formed of the junction field effect transistor (JFET) and the channel forming portion of this junction field effect transistor (JFET) may be constructed of the first conductivity type gate region, the second conductivity type channel region, and the first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate. Accordingly, in amplifying the charge (signal charge), the charge (signal charge) is amplified through the first conductivity type gate region and the second conductivity type channel region.

Still another aspect of the present invention is the photoelectric conversion element wherein the amplifying portion is comprised of a junction field effect transistor (JFET) and wherein a channel forming portion of the junction field effect transistor (JFET) is formed of a first conductivity type

shallow gate region, a second conductivity type shallow channel region, a first condnctivity type gate region, a second conductivity type well region, and a first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate.

Namely, the amplifying portion of the photoelectric conversion element may be constructed of a junction field effect transistor (JFET), and the channel forming portion of this junction field effect transistor (JFET) is formed of the first conductivity type shallow gate region, the second conductivity type shallow channel region, the first conductivity type gate region, the second conductivity type well region, and the first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate.

Describing in more detail, the channel forming portion is shallowed (in shallow junction arrangement) by the first conductivity type shallow gate region and the second conductivity type shallow channel region so as to reduce the size of the entire junction field effect transistor. Also, the first conductivity type gate region and the first conductivity type semiconductor substrate are electrically separated by interposition of the second conductivity type well region between the first conductivity type gate region and the first conductivity type semiconductor substrate.

The shallowing improves transconductance, and the reduction of size increases the degree of integration and the aperture ratio and makes it possible to raise the sensitivity. The electric isolation between the gate (control region) and the semiconductor substrate of the junction field effect transistor (JFET) can make it possible to suppress the influence of substrate voltage (substrate bias effect) and to raise the amplification factor upon current amplification operation and the charge amplification factor upon source-follower operation.

Still another aspect of the present invention is the photoelectric conversion element wherein the amplifying portion is comprised of a junction field effect transistor (JFET), wherein a channel forming portion of the junction field effect transistor (JFET) is formed of a first conductivity type shallow gate region, a second conductivity type shallow channel region, a first conductivity type gate region, a second conductivity type well region, and a first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate, and wherein the first conductivity type shallow gate region and the first conductivity type gate region are electrically connected with each other in a portion other than the channel forming portion.

Namely, the amplifying portion of the photoelectric conversion element may be formed of the junction field effect transistor (JFET), wherein the channel forming portion of the junction field effect transistor (JFET) is constructed of the first conductivity type shallow gate region, the second conductivity type shallow channel region, the first conductivity type gate region, the second conductivity type well region, and the first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate. The first conductivity type shallow gate region and the first conductivity type gate region are electrically connected with each other in the portion other than the channel forming portion.

Accordingly, the shallowing improves the transconductance, and the reduction of size can increase the degree of integration and the aperture ratio and enhance the sensitivity by that degree. The arrangement in which the first conductivity type shallow gate region and first condnctivity type gate region are made electrically connected and in which the gate (control region) of the junction field effect transistor (JFET) and the semiconductor substrate are electrically separated can make it possible to greatly suppress the influence of substrate voltage (substrate bias effect) and to increase the amplification factor during the current amplification operation or the charge amplification factor during the source-follower operation.

Still another aspect of the present invention is the photoelectric conversion element wherein the photoelectric conversion portion is a buried photodiode of a vertical overflow structure, wherein the amplifying portion is comprised of a junction field effect transistor and a channel forming portion of the junction field effect transistor is formed of a first conductivity type shallow gate region, a second conductivity type shallow channel region, a first conductivity type gate region, a second conductivity type well region, and a first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate, wherein the first conductivity type shallow gate region and the first conductivity type gate region are electrically connected with each other in a portion other than the channel forming portion, and wherein an impurity concentration of the first conductivity type gate region is different from an impurity concentration of a charge storing portion of the buried photodiode. This enables operation of the buried photodiode and the junction field effect transistor under suitable conditions.

Still another aspect of the present invention is the photoelectric conversion element wherein the impurity concentration of the first conductivity type gate region is in the range of 6×10^{15} cm^{-3} to 3×10^{16} cm^{-3} and the impurity concentration of the charge storing portion of the buried photodiode is in the range of 5×10^{15} cm^{-3} to 3×10^{16} cm^{-3}. This enables operation of the buried photodiode and the junction field effect transistor under most suitable conditions.

Still another aspect of the present invention is the photoelectric conversion element wherein the amplifying portion is comprised of a MOS field effect transistor and this field effect transistor is of a depletion type.

This enables suppression of fixed pattern noise based on signal (charge) destruction. Since neither reset noise nor lag occurs upon the reset operation of the control region of the MOS field effect transistor, this arrangement is suitable for forming a photoelectric conversion element enabling electronic shutter operation with simultaneity in a frame.

Still another aspect of the present invention is the photoelectric conversion element wherein the amplifying portion is comprised of a bipolar transistor, the bipolar transistor having a collector of a high-concentration region of a predetermined conductivity type formed in a silicon surface layer portion surrounding the photoelectric conversion element, without forming a buried collector or a collector using a high-concentration substrate of a predetermined conductivity type.

This enables construction of a combination of the bipolar transistor with the photodiode of the vertical overflow structure, which can suppress pseudo signals such as blooming or smear.

Still another aspect of the present invention is a photoelectric conversion apparatus comprising: a plurality of photoelectric conversion elements arranged in a two-dimensional matrix, each photoelectric conversion element

comprising a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein, an amplifying portion having a control region for generating a signal output according to the charge received in the control region from the photoelectric conversion portion, a transfer control portion for transferring the charge generated and stored in the photoelectric conversion portion to the control region of the amplifying portion, reset-purpose charge draining means for draining the charge transferred to the control region of the amplifying portion, and reset-purpose control means for controlling the reset-purpose charge draining means.

Still another aspect of the present invention is the photoelectric conversion apparatus wherein the reset-purpose charge draining means of the respective photoelectric conversion elements arrayed at least in one scanning direction are arranged in parallel to each other.

By the arrangement in which the reset-purpose charge draining means of the respective photoelectric conversion elements arrayed in the horizontal scanning direction are arranged in parallel with each other, the amplifying portion always corresponds to the reset portion in each unit pixel of the photoelectric conversion element, whereby the control region of the amplifying portion can be initialized within a very short time to the potential of the reset portion. Namely, this arrangement makes high-speed reset operation possible.

Still another aspect of the present invention is the photoelectric conversion apparatus further comprising: a vertical scanning circuit; and a pulse drive source; wherein the transfer-purpose control means of the transfer control portion and the reset-purpose charge draining means in the photoelectric conversion elements are connected commonly along the horizontal scanning direction, thereby connecting to the vertical scanning circuit for pulse driving. The reset-purpose control means in all the photoelectric conversion elements are connected commonly to the pulse drive source.

In the photoelectric conversion apparatus constructed in the above arrangement, the voltage of the high level is first applied to the reset-purpose charge draining means in a certain specific horizontal line (selected row) by the vertical scanning circuit, and the voltage of the low level is applied to the reset-purpose charge draining means in the other horizontal lines (non-selected rows). Then the drive pulse from the pulse drive source is applied to the all reset-purpose control means.

As a result, the control regions of the amplifying portions in the photoelectric conversion elements in the selected row are initialized to the voltage of the high level, and the control regions of the amplifying portions in the photoelectric conversion elements in the non-selected rows to the voltage of the low level.

Employing the arrangement in which the initializing operation of the control regions of the amplifying portions is performed by the reset-purpose charge draining means and reset-purpose control means, the apparatus can obviate a need to perform the reset operation for recombining the charge (signal charge) by driving the control regions of the amplifying portions by a forward bias as in the conventional photoelectric conversion apparatus.

Thus, the invention can solve the problems that a large current flows in the amplifying portions and that in the case of the photoelectric conversion apparatus being constructed with a lot of photoelectric conversion elements arrayed, amplification factors vary because of large transient fluctuations of bias points (operating points) of the amplifying portions to cause variations of outputs from the respective photoelectric conversion elements, thereby degrading the performance of apparatus (for example, S/N ratios) and increasing the dissipation power.

After the control regions of the amplifying portions are initialized, the drive pulse sent from the vertical scanning circuit is applied to the transfer-purpose control means given in the above photoelectric conversion elements. As a result, the charges (signal charges) generated and stored in the photoelectric conversion portions in the above photoelectric conversion elements are transferred from the above photoelectric conversion portions to the control regions of the above amplifying portions, and the amplifying portions execute the amplifying operation of the charges (signal charges).

Still another aspect of the present invention is the photoelectric conversion apparatus further comprising: a vertical scanning circuit; a pulse drive source; and a power supply; wherein the transfer-purpose controlling means of the transfer control portions and the control means for controlling the control regions of the amplifying portions by capacitive coupling in the photoelectric conversion elements are connected commonly along the horizontal scanning direction, thereby connecting to the vertical scanning circuit for pulse driving, the reset-purpose control means and the reset-purpose charge draining means in all the photoelectric conversion elements are connected commonly, thereby the reset-purpose controlling means are connected to the pulse drive source and the reset-purpose charge draining means are connected to the power source.

Namely, the above arrangement is attained when the features of the present invention are applied to the most popular arrangement of a conventional photoelectric conversion apparatus. The feature of the present invention is to form the reset-purpose charge draining means and reset-purpose control means independently in order to initialize the control regions of the amplifying portions without operating the amplifying portions. Further, another feature of the present invention is to arrange the reset-purpose charge draining means of the respective photoelectric conversion elements in parallel with each other along the horizontal scanning direction in order to achieve high-speed reset operation. Then the above arrangement enables fabrication of the photoelectric conversion apparatus with little changing the arrangement of the conventional photoelectric conversion apparatus. The fabrication becomes easy accordingly.

In the photoelectric conversion apparatus constructed in the above arrangement, the voltage is fixedly supplied from the power supply to the reset-purpose charge draining means, and the reset-purpose charge draining means supplies the voltage thus supplied to the control regions of the amplifying portions. The reset-purpose control means operates (turns on or off) according to the drive pulse sent from the pulse drive source. Here, the operation (on or off) of the above reset-purpose control means controls the voltage supplied from the reset-purpose charge draining means to the control regions of the amplifying portions.

Namely, the voltage is supplied from the reset-purpose charge draining means to the control regions of the amplifying portions in accordance with the operation (on or off) of the reset-purpose control means. Then the potential of the control regions of the amplifying portions changes to the same potential as that of the reset-purpose charge draining means, thus initializing the control regions of the amplifying portions.

Since the amplifying portions do not operate (turn on) upon the initialization operation of the amplifying portions,

the invention can solve the problems that a large current flows in the amplifying portions, which causes large transient fluctuations of the bias points (operating points) of the amplifying portions, thereby changing the amplification factors and causing variations of outputs from the respective photoelectric conversion elements, that the performance (for example, S/N ratios) of the apparatus is degraded, and that the dissipation power increases because of the arrangement of many photoelectric conversion elements. Further, the present invention enables selecting or non-selecting operations of rows by using the control means for controlling the control regions of the amplifying portions by capacitive coupling.

Still another aspect of the present invention is the photoelectric conversion apparatus further comprising: a vertical scanning circuit; a pulse drive source; and a power supply; wherein the control means for controlling the control region of the amplifying portion by capacitive coupling and reset-purpose control means in the photoelectric conversion elements are connected commonly along the horizontal reading direction, thereby connecting to the vertical scanning circuit for pulse driving, the transfer-purpose controlling means of the transfer control portions and reset-purpose charge draining means in all the photoelectric conversion elements are connected commonly, thereby the transfer-purpose controlling means are connected to the pulse drive source and the reset-purpose charge draining means are connected to the power source.

When the drive pulse sent from the pulse drive source is applied to the transfer-purpose control means of the above transfer portions, the charges (signal charges) generated and stored in the photoelectric conversion portions in all the pixels are simultaneously transferred to the control regions of the amplifying portions. When the drive pulse sent from the vertical scanning circuit is applied to the control means for controlling the control regions of the above amplifying portions by capacitive coupling, the amplifying portions execute the amplification operation, and then the amplifying portions output signals amplified.

The reset-purpose control means operates (turns on or off) in accordance with the drive pulse sent from the vertical scanning circuit, and the voltage from the power supply connected to the reset-purpose charge draining means is supplied to the control regions of the above amplifying portions in accordance with this operation to turn the control regions of the amplifying portions into the same potential as that of the reset-purpose charge draining means, thus initializing the control regions of the amplifying portions.

This enables resetting of the control regions of the amplifying portions without operating (turning on) the amplifying portions, which enables suppression of the degradation of performance (for example, S/N ratios) of the apparatus and the increase of the dissipation power due to the arrangement of many photoelectric conversion elements. It is noted that the present invention enables an electronic shutter operation which is operated simultaneously in a frame.

Still another aspect of the present invention is the photoelectric conversion apparatus further comprising: a vertical scanning circuit for commonly driving the photoelectric conversion elements along the horizontal scanning direction; first memory means for storing signal outputs for one horizontal line immediately after the control regions of the amplifying portions are initialized according to vertical scanning; and second memory means for storing signal outputs for one horizontal line immediately after the charges are transferred to the control regions of the amplifying portions according to vertical scanning.

Namely, noise components are mixed in signal outputs immediately after the control regions of the amplifying portions are initialized, and charge components and noise components are mixed in signal outputs immediately after the charges (signal charges) generated and stored by the photoelectric conversion portions are transferred to the control regions of the amplifying portions.

Accordingly, a signal output immediately after the control region of each amplifying portion is initialized is separated from a signal output immediately after a charge (signal charge) generated and stored in each photoelectric conversion portion is transferred to the control region of the amplifying portion and a difference is taken between the two signal outputs, thereby obtaining a signal output according to only the photogenerated charge component.

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not to be considered as limiting the present invention.

Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A to **1**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 1 of the present invention;

FIGS. **2**A to **2**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 2 of the present invention;

FIGS. **3**A to **3**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 3 of the present invention;

FIG. **4** is a schematic sectional view to show the essential portion of the photoelectric conversion element according to Embodiment 4 of the present invention;

FIG. **5** is a circuit diagram to show a schematic layout of the photoelectric conversion apparatus according to Embodiment 5 of the present invention;

FIG. **6** is a pulse timing chart for explaining the operation of the circuit diagram shown in FIG. **5**;

FIGS. **7**A to **7**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 6 of the present invention;

FIG. **8** is a circuit diagram to show a schematic layout of the photoelectric conversion apparatus according to Embodiment 7 of the present invention;

FIG. **9** is a pulse timing chart for explaining the operation of the circuit diagram shown in FIG. **8**;

FIGS. **10**A to **10**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 8 of the present invention;

FIG. **11** is a circuit diagram to show a schematic layout of the photoelectric conversion apparatus according to Embodiment 9 of the present invention;

FIG. **12** is a pulse timing chart for explaining the operation of the circuit diagram shown in FIG. **11**;

FIGS. **13**A to **13**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 10 of the present invention; and

FIGS. **14**A to **14**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 11 of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiments of the present invention will be explained with reference to the drawings. In the drawings, same reference numerals denote same or equivalent portions, and redundant description will be omitted.

Embodiment 1

FIGS. **1**A to **1**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 1 of the present invention, wherein FIG. **1** is a plan view of the schematic structure to show the photoelectric conversion element, FIG. **1**B a cross section along X1–X2 line in FIG. **1**A, and FIG. **1**C a cross section along Y1–Y2 line in FIG. **1**A. In FIG. **1**A and the following FIGS. **2**A, **3**A, **7**A, **10**A, **13**A, **14**A, depiction of an aluminum film **20** is omitted.

In these drawings, the photoelectric conversion element according to Embodiment 1 is mainly composed of a photodiode (photoelectric conversion portion, PD) **1** for generating and storing a charge according to incident light, a junction field effect transistor ((amplifying portion): hereinafter referred to as JFET) **2** for outputting a signal according to the charge received by the control region, a transfer gate (transfer-purpose control means of the transfer control portion, TG) **3** for transferring the charge generated and stored by the photodiode **1** to the control region of JFET **2**, a reset drain (reset-purpose charge draining means, RD) **4** for draining the charge transferred to the control region of JFET **2**, and a reset gate (reset-purpose control means, RG) **5** for controlling the reset drain **4**. In addition, there are transfer gate line **3***a*, reset gate line **5***a*, and source line **16***a* formed as illustrated.

In more detail, an n-type silicon layer **11** to become a channel region is formed by epitaxial growth on a p-type silicon substrate **10**, and, for example, boron (B^+) or phosphorus (P^+) is introduced into the n-type silicon layer **11** by an ion implantation or thermal diffusion process or the like to form a p-type photodiode region **12**, a p-type gate region **13**, the reset drain **4**, etc. Further, the transfer gate **3** and reset gate **5** are formed through an insulating layer (not shown) by a lithography technique or the like, thus forming the photodiode **1** and JFET **2**.

An n-well region **14** of the photodiode **1** is formed in order to control the overflow potential of carriers generated in the pn junction to a predetermined value.

The transfer gate **3**, the p-type photodiode region **12** of photodiode **1**, and the p-type gate region **13** of JFET **2** compose a p-channel MOS transistor (MOSFET; see FIGS. **1**A and **1**C). Further, the reset gate **5**, a p-region **15** of reset drain **4** and the p-type gate region **13** of JFET **2** also compose a p-channel MOSFET (see FIGS. **1**A and **1**B).

The photodiode **1** includes, in order from the surface of the silicon layer to the p-type silicon substrate **10**, the p-type photodiode region **12**, the n-type silicon layer **11** (including the n-well region **14**), and the p-type silicon substrate **10**, thus forming a so-called pnp-type vertical overflow structure. This structure can suppress the phenomenon of blur such as blooming and smear due to carriers (holes in this Embodiment 1) generated accordingly.

JFET **2** is composed of an n^+-type source region **16**, an n^+-type drain region **17**, a p-type gate region **13**, and an n-type channel region **18** (n-channel). These are arranged to form a pnp-type structure of the p-type gate region **13**, the n-type channel region **18**, and the p-type silicon substrate **10** in order from the surface of the silicon layer to the p-type silicon substrate **10**. Consequently, the p-region (the p-type silicon substrate **10** in this Embodiment 1) below the n-type channel region **18**, originally having a function of back gate, is connected to a constant power supply. The thickness (height) from the surface of the silicon layer to the surface of the p-type silicon substrate **10** is about 6 μm.

Applying a pulse voltage to the reset gate **5**, the reset gate **5** and reset drain **4** initialize the control region of JFET **2** (the p-type gate region **13** in this Embodiment 1) to the potential of the reset drain **4**.

Thus, JFET **2** is kept from operating (or becoming on) upon the initialization operation, in contrast to the conventional photoelectric conversion element. For example, when a photoelectric conversion apparatus is constructed by arraying a lot of these elements, the apparatus is free of occurrence of variations in outputs from the photoelectric conversion elements, which were seen in the conventional apparatus due to flow of a large current to greatly change the bias points (operating points) of transistors and thereby result in different amplification factors of JFETs **2**. This results in preventing the dissipation power from becoming large and in decreasing dissipation power.

Although not shown in FIG. **1**A, wiring to the reset drain **4** (metal interconnection, which is an aluminum (Al) film **20** in this Embodiment 1) also serves as a light-shielding film for shielding portions other than the photodiode **1**, as seen from FIGS. **1**B and **1**C. This aluminum film **20** may be replaced by another metal film, which can be fabricated by depositing a metal film by the sputtering process.

Accordingly, the thickness (height) of the entire element can be kept smaller than that of an element with a further film dedicated to light shielding, which is formed on the top, the degree of integration and the aperture ratio for the photodiode **1** can be increased, and the phenomenon of blur such as blooming and smear due to obliquely incident light can be suppressed because of the structure wherein the metal wiring (aluminum film **20**) is disposed in the vicinity of the photodiode **1**.

Embodiment 2

FIGS. **2**A to **2**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 2 of the present invention, wherein FIG. **2**A is a plan view of the schematic structure to show the photoelectric conversion element, FIG. **2**B a cross section along X1–X2 line in FIG. **2**A, and FIG. **2**C a cross section along Y1–Y2 line in FIG. **2**A. This Embodiment 2 is different in the structure of the photodiode and the JFET **2** of the photoelectric conversion element from Embodiment 1.

Namely, the photodiode **1** of the photoelectric conversion element in Embodiment 2 is different from the photodiode **1** of the photoelectric conversion element in Embodiment 1 first in that a buried photodiode of an npnp type vertical overflow structure (wherein a buried photodiode is constructed by the npn structure and the overflow structure is constructed by the pnp structure) is formed from the surface of the silicon layer toward the p-type silicon substrate **10**.

Accordingly, the phenomenon of blur such as blooming and smear can be suppressed by the overflow structure for

absorbing overflowing carriers, while the buried photodiode prevents the depletion layer appearing in the pn junction portion from reaching the surface, thus suppressing the dark current. Since no charge remains in the photodiode (the photodiode becomes completely depleted) after transfer of charge, ideal characteristics can be achieved for suppressing the lag and reset noise.

Further, Embodiment 2 is also different from Embodiment 1 in that the n-well region **14**, which was formed only around the photodiode **1** in Embodiment 1, is formed over the entire surface of the p-type silicon substrate **10**. Generally, the photodiode of the vertical overflow structure is desirably constructed in such a manner that, in order to keep the quantum efficiency high, the pn junction is formed as deep as possible from the surface of the silicon layer toward the p-type silicon substrate **10**.

The n-well region **14** is formed deeper toward the p-type silicon layer **10** accordingly. Since the n-well region **14** diffuses (side-diffuses) in the lateral directions (in the directions perpendicular to the direction directed toward the p-type silicon substrate **10**) in this case, design taking account of this side diffusion is necessary. Embodiment 2 employs the structure in which the n-well region **14** is formed over the entire surface of the p-type silicon substrate **10** and JFET **2** is formed in this n-well region **14**, thereby avoiding influence of the side diffusion of the n-well region **14** and raising the degree of integration and the aperture ratio.

The JFET **2** of the photoelectric conversion element in this Embodiment **2** is first different from the structure of JFET **2** in Embodiment 1 in that the whole (particularly, the channel portion) is shallowed (in shallow junction arrangement). Shallowing the JFET **2** for performing only the amplification operation decreases the dimensions (size) of the entire JFET **2** by that shallowing degree, which can raise the degree of integration of the entire photoelectric conversion element and the aperture ratio of the photodiode **1**.

In addition, the above arrangement can enhance a characteristic as an amplifying portion, that is, transconductance (gm), and can improve a saturation characteristic (or reduce a drain voltage dependence of a saturation region). An increase of transconductance (gm) is of course important, for example when the JFET **2** is used for current amplification, and it can lower the time constant (or increase the speed) or can enhance the sensitivity in the case of source-follower operation (namely, in the case of charge amplification by capacitive load).

Second, the JFET **2** of the photoelectric conversion element in Embodiment 2 is so arranged that p-type gate regions **13** (see FIG. **2**B, a first conductivity type shallow gate region **13***a* and a first conductivity type gate region **13***b*) are formed above and below the channel (n-channel) and these first conductivity type shallow gate region **13***a* and first conductivity type gate region **13***b* are electrically connected in a portion where the channel is not formed.

Further, it is different from JFET **2** in Embodiment **1** in that the p-type gate regions **13** are electrically separated from the p-type silicon substrate **10** by the n-well region **14**. This can greatly reduce influence of the substrate voltage (substrate bias effect) on the characteristics of the photoelectric conversion element itself.

In addition, for example when a photoelectric conversion apparatus is composed of such photoelectric conversion elements and when JFETs **2** are in the source-follower operation, the reduction of the drain voltage dependence as discussed previously and the reduction of the substrate bias effect will present a great effect on enhancement of the sensitivity of pixels arrayed in the photoelectric conversion apparatus and on suppression of variations of sensitivity (for example, on suppression of the fixed pattern noise).

As explained above, the JFET **2** of the photoelectric conversion element according to Embodiment 2 can have an improved degree of integration and an improved aperture ratio and also have higher sensitivity than the photoelectric conversion element according to Embodiment 1, and can suppress the variations of sensitivity.

Embodiment 3

FIGS. **3**A to **3**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 3 of the present invention, wherein FIG. **3**A is a plan view of the schematic structure to show the photoelectric conversion element, FIG. **3**B a cross section along **X1–X2** line in FIG. **3**A, and FIG. **3**C a cross section along **Y1–Y2** line in FIG. **3**A. The photoelectric conversion element according to Embodiment 3 is different from the above two embodiments in that an element isolation region **21** of a predetermined conductivity type (the n-type in this Embodiment 3) is formed in the peripheral regions of the photodiode **1**, JFET **2**, and reset drain **4** (including the regions where the transfer gate **3** and reset gate **5** are formed).

Since p-type regions of the photodiode **1**, JFET **2**, and reset drain **4** each are normally formed in the n-well region **14**, they are electrically isolated from each other by this n-well region **14**. Generally, the desired isolation of the n-well region **14** is to define the isolation width as small as possible from the viewpoint of increasing the degree of integration and the aperture ratio.

However, the p-type regions of the photodiode **1**, JFET **2**, and reset drain **4** cannot be formed to shallow (shallow in the direction of from the silicon surface toward the substrate) because of performance of the photoelectric conversion element. Particularly, as to the photodiode **1**, it is instead desired to form it to be deep from the silicon surface toward the substrate in view of the quantum efficiency. It is thus the case that the spread (side diffusion) becomes great in the lateral directions (in the directions perpendicular to the direction directed toward the substrate) and a reduction of the isolation width cannot easily be done.

Thus, this Embodiment 3 is arranged to suppress the above side diffusion of the p-type regions by forming the n-type element isolation region **21**, thereby decreasing the isolation width, increasing the degree of integration of the entire photoelectric conversion element and the aperture ratio of photodiode **1**, and facilitating control of the threshold voltage of the transfer gate **3** and reset gate **5**.

Embodiment 4

FIG. **4** is a schematic sectional view to show an essential portion of the photoelectric conversion element according to Embodiment 4 of the present invention. FIG. **4** depicts a portion of FIG. **2**C or **3**C, therefore, the present embodiment can be explained by using the figures for embodiment of 2 or 3.

The photodiode according to this embodiment is a buried photodiode (BPD) **1** having a vertical overflow structure, as shown in FIG. **4**. Thus, the p-type diffusion layer **12** used herein needs to satisfy the following conditions. An SiO_2 film **11***a* is formed on the silicon surface.

(1) An excessive photogenerated charge should overflow into the substrate.

(2) The photogenerated charge should be completely transferred to the JFET 2 upon signal reading, so that the p-type diffusion of BPD 1 may be completely depleted.

On the other hand, p-type diffusion used in JFET 2 needs to satisfy the following conditions.

(1) The charge transferred from BPD 1 should not overflow into the substrate.

(2) Punch-through should not occur between the source n^+-diffusion of JFET 2 and the n-well region 14.

(3) The p-type diffusion region should not be depleted under the bias conditions in operation as JFET 2.

In order to simultaneously satisfy these conditions, optimization is rather easy by setting the concentrations of the p-type diffusion regions in BPD 1 and JFET 2 separately to different values.

Thus, in the photoelectric conversion element in the present embodiment, these impurity concentrations are separately set so that the impurity concentration of the charge storing portion 12, which is the p-type diffusion region of BPD 1, may be in the range of 5×10^{15} cm^{-3} to 3×10^{16} cm^{-3} and so that the impurity concentration of the first conductivity type gate region 13*b*, which is the p-type diffusion region of JFET 2, may be in the range of 6×10^{15} cm^{-3} to 3×10^{16} cm^{-3}. Here, these impurity concentrations can be controlled by changing the implantation conditions in boron ion implantation, for example by changing a dose.

Embodiment 5

FIG. 5 is a circuit diagram to show the schematic structure of the photoelectric conversion apparatus according to Embodiment 5 in which photoelectric conversion elements, as described in above each Embodiment 1–4 (FIG. 1 to FIG. 4) are arranged in a two-dimensional matrix. FIG. 6 is a pulse timing chart for explaining the operation of the circuit diagram shown in FIG. 5. The photoelectric conversion apparatus in the following description will be explained as an example where the photoelectric conversion elements are those shown in FIG. 1, but the same can be applied to the cases using the photoelectric conversion elements shown in FIG. 2 to FIG. 4.

As shown in FIG. 5, each pixel 31 is composed of a photodiode PD for generating and storing a charge according to incident light, a JFET for generating a signal output according to the charge received by its control region, a transfer control element (p-channel MOSFET) 31*a* having a transfer gate TG for transferring the charge generated and stored in the photodiode 1 to the control region of JFET, a reset drain RD which is a reset-purpose charge draining means for draining the charge transferred to the control region of JFET, and a reset element (p-channel MOSFET) 31*b* having a reset gate RG, which is a reset-purpose control means for controlling the reset drain RD.

The source of each JFET is connected in common to a vertical source line 32*a*, 32*b*, 32*c* in each column of the matrix arrangement. All pixels 31 are connected in common to a drain power-supply 31*c* through a wiring (not shown) or diffusion layer formed on the drain side of each JFET and on the cathode side of the photodiode PD. Further, the anode side of each photodiode 1 and the control region of JFET 2 are connected to the source or the drain of the transfer control element 31*a*, respectively.

The transfer gates (transfer gate electrodes) 3 of the transfer control elements 31*a* in each row are connected in common to a clock line 33*a*, 33*b*, 33*c* to be scanned by a vertical scanning circuit 34. When a drive pulse Φ_{TG1}–Φ_{TG3} sent from the vertical scanning circuit 34 is applied, the apparatus is arranged to sequentially operate the transfer control elements 31*a* in each row.

A reset element 31*b* is given for each pixel 31, and reset drains RD of the reset elements 31*b* are arranged in parallel in each row as being connected in common to a clock line 50*a*, 50*b*, 50*c* to be scanned in each row of the matrix arrangement by the vertical scanning circuit 34. The reset gates (reset gate electrodes) 5 of all the pixels are connected in common through a row line 37*a* to a drive pulse generating circuit 37. The source of each reset element 31*b* is formed in common with the drain of transfer control element 31*a*. When a drive pulse Φ_{RG} sent from the drive pulse generating circuit 37 is applied to the reset gate (reset gate electrode) 5, this reset element 31*b* is arranged to operate.

The vertical source line 32*a*, 32*b*, 32*c*, on one hand, is connected in each column through a MOS transistor for transferring a light signal output T_{S1}, T_{S2}, T_{S3} and through a MOS transistor for transferring a dark output T_{D1}, T_{D2}, T_{D3} to one electrode of a capacitor for storing the light signal output (second memory element) C_{S1}, C_{S2}, C_{S3} and to one electrode of a capacitor for storing the dark output (first memory element) C_{D1}, C_{D2}, C_{D3} and then is connected through MOS transistors for selection of horizontal reading T_{HS1}, T_{HS2}, T_{HS3}, T_{HD1}, T_{HD2}, T_{HD3} to a signal output line 38 and a dark output line 39. Generally, parasitic capacitances C_{HS}, C_{HD} exist in the signal output line 38 and dark output line 39. A buffer amplifier 38*a*, 39*a* is connected to one end of each of the signal output line 38 and dark output line 39.

The signal output line 38 and dark output line 39, on the other hand, are connected to the drains of MOS transistors for resetting the signal output lines T_{RHS}, T_{RHD}, respectively, and the sources of MOS transistors T_{RHS}, T_{RHD} are grounded (GND) as being connected to the other electrodes of the above capacitors for storing the light signal output C_{S1}, C_{S2}, C_{S3} and capacitors for storing the dark output C_{D1}, C_{D2}, C_{D3}. When a drive pulse Φ_{RH} sent from the drive pulse generating circuit 43 is applied to the gate electrodes of the MOS transistors for resetting the signal output lines T_{RHS}, T_{RHD}, the MOS transistors T_{RHS}, T_{RHD} are arranged to start operating.

A horizontal selection line 40*a*, 40*b*, 40*c* connected to a horizontal scanning circuit 40 in each column is connected in common to the gate electrodes of the MOS transistors for selection of horizontal reading T_{HS1}, T_{HS2}, T_{HS3} and T_{HD1}, T_{HD2}, T_{HD3}, so that horizontal reading may be controlled by a drive pulse Φ_{H1} to Φ_{H3} sent from the horizontal scanning circuit 40.

The gate electrodes of the above MOS transistors for transferring the light signal outputs T_{S1}, T_{S2}, T_{S3} are connected through a clock line for light signal 41*a* and the gate electrodes of the above MOS transistors for transferring the dark outputs T_{D1}, T_{D2}, T_{D3} are connected through a clock line for dark output 42*a*, each to a drive pulse generating circuit 41 or 42. When a drive pulse Φ_{TS} or Φ_{TD} sent from the drive pulse generating circuit 41 or 42 is applied to the gate electrodes through either line, these MOS transistors for transmission of light signal output T_{S1}, T_{S2}, T_{S3} and MOS transistors for transmission of dark output T_{D1}, T_{D2}, T_{D3} are arranged alternately to operate in a predetermined order.

The above vertical source line 32*a*, 32*b*, 32*c* in each column, on the other hand, is connected to the drain of a transistor for reset T_{RV1}, T_{RV2}, T_{RV3} and to a constant current source for source-follower reading 44*a*, 44*b*, 44*c*. A power-supply voltage V_{RV} is supplied to the source of each reset

transistor T_{RV1}, T_{RV2}, T_{RV3}, and a power-supply voltage V_{CS} is supplied to the constant current sources for source-follower reading **44**a, **44**b, **44**c.

A reset pulse Φ_{RV} is supplied to the gate electrodes of the reset transistors T_{RV1}, T_{RV2}, T_{RV3}, and with a change of this reset pulse Φ_{RV} to high level the reset transistors T_{RV1}, T_{RV2}, T_{RV3} become on so as to ground the vertical source lines **32**a, **32**b, **32**c (when V_{RV}=GND).

The constant current sources for source-follower reading **44**a, **44**b, **44**c control the time constant of source-follower operation, and also suppress variations of the time constant due to fluctuations of the bias point for every pixel **31** to equalize the gains, thus suppressing the fixed pattern noise (hereinafter referred to as FPN).

The operation of the photoelectric conversion apparatus according to Embodiment 5 of the present invention is next explained referring to the pulse timing chart shown in FIG. **6**. In FIG. **6**, the period between t_{11} and t_{15} represents the reading operation of pixels **31** in the first row, and thereafter the periods between t_{21} and t_{25} and between t_{31} and t_{35} correspond to the second row and the third row, respectively. Further, t_{11} to t_{14} each are so defined that t_{11} is the period for the initialization operation of JFETs **2**, t_{12} the period for the source-follower operation of JFETs **2** in the first row after initialization, t_{13} the period for the transfer operation of signal charges from the photodiodes **1** to the JFETs **2** in the first row, and t_{14} the period for the source-follower operation of JFETs **2** after transfer, and these four operations are carried out in the horizontal blanking period. Further, t_{15} is the image signal output period.

First, as shown in FIG. **6**, the drive pulse Φ_{RD1} is set to the high level while keeping the drive pulses Φ_{RD2} and Φ_{RD3} at the low level) at the start of period t_{11} whereby the voltage drive pulse is applied to the reset drains **4** of pixels **31** in the first row. Then the high level voltage is applied to the control regions of JFETs **2** of the pixels **31** in the first row and the low level voltage is applied to the control regions of JFETs **2** of the pixels **31** in the other rows through the reset gates **5** of all the pixels **31** already set in a conductive (on) state at the low level. By this operation, the control regions of these JFETs **2** are initialized (the charges therein are drained) and the JFETs **2** in the first row are selected (on) while the JFETs **2** in the other rows are not selected (off).

Namely, selection (on) or non-selection (off) of JFETs **2** is effected depending upon whether the voltage drive pulse (Φ_{RD1}, Φ_{RD2}, Φ_{RD3}) is sent to a row of the reset drains **4** or not. Then, the control regions of JFETs **2** in the selected row are initialized to the high level voltage and the control regions of JFETs **2** in the non-selected row are initialized to the low level voltage.

At the end of period t_{11} (or at the start of period t_{12}) the drive pulse Φ_{RG} is changed to the high level so as to change the reset gates **5** into a non-conductive (off) state whereby the control regions of the respective JFETs **2** are kept in a floating state as maintaining the selected (on) or the non-selected (off) state.

At the same time (at the start of period t_{12}), the drive pulse Φ_{RV} is changed to the low level to bring the reset transistors T_{RV1} to T_{RV3} into an interrupted (off) state, and the JFETs **2** in the first row perform the source-follower operation in this period t_{12}. During this period t_{12} the drive pulse Φ_{TD} is at the high level to keep the MOS transistors for transfer of dark output T_{D1}, T_{D2}, T_{D3} in a conductive state (on) and output (output at dark) voltages corresponding to the potentials immediately after the initialization of the control regions of the JFETs **2** are stored in the capacitors for storage of dark output C_{D1}, C_{D2}, C_{D3}.

In the period t_{13}, the drive pulse Φ_{TG1} is turned to the low level to bring the transfer gates **3** from the non-conductive (off) state to the conductive (on) state, and the drive pulse Φ_{TS} is changed to the high level and the drive pulse Φ_{TD} to the low level, thereby changing the MOS transistors for transfer of light signal output T_{S1}, T_{S2}, T_{S3} into the conductive (on) state and the MOS transistors for transfer of dark output T_{D1}, T_{D2}, T_{D3} into the non-conductive (off) state.

As a result, charges generated and stored in the photodiodes **1** in the first row are transferred to the control regions of JFETs **2**. After transfer of charge the potential of each control region of JFET **2** changes (increases in this case) by a degree of charge amount/gate capacitance. The reason why the transfer gates **3** change into the conductive (on) state when the drive pulse Φ_{TG1} is kept at the low level in FIG. **6** is that the transfer control elements **31**a are of the p-channel type and thus the polarity of the drive pulse Φ_{TG1} is opposite to that of the other drive pulses.

In the period t_{14}, similarly as in the period t_{12}, the drive pulse Φ_{TG1} is changed to the high level to bring the transfer gates **3** in the first row into the non-conductive (off) state whereby the charges photoelectrically converted in the photodiodes **1** are stored, and the drive pulse Φ_{RV} is changed to the low level to bring the reset transistors T_{RV1} to T_{RV3} into the interrupted (off) state whereby the JFETs **2** in the first row perform the source-follower operation.

Since during this period t_{14} the drive pulse Φ_{TS} is at the high level, the MOS transistors for transfer of light signal output T_{S1}, T_{S2}, T_{S3} are kept in the conductive state (on), and output (signal output) voltages corresponding to potentials after the charges are transferred to the control regions of the respective JFETs **2** are stored in the capacitors for storage of light signal output C_{S1}, C_{S2}, C_{S3}. In the period t_{15}, the drive pulses Φ_{RD1}, Φ_{RG}, Φ_{TS} are each changed to the low level and the drive pulse Φ_{RV} to the high level, so that the output voltages (image signals) stored in the capacitors for storage of light signal output C_{S1} to C_{S3} and capacitors for storage of dark output C_{D1} to C_{D3} are ready to be output to the output terminals V_{OS}, V_{OD}.

Then sequentially outputting the drive pulses Φ_{H1} to Φ_{H3} from the horizontal scanning circuit **40** and the drive pulse Φ_{RH} from the drive pulse generating circuit **43**, the image signals stored in the capacitors for storage of light signal output C_{S1} to C_{S3} and the capacitors for storage of dark output C_{D1} to C_{D3} are read out into the horizontal reading lines of signal output line **38** and dark output line **39**, respectively, then, the image signals are output from the terminals V_{OS}, V_{OD}, while horizontal reading lines of signal output line **38** and dark output line **39** are reset.

The image signals obtained from the output terminals V_{OS}, V_{OD} are subjected to arithmetic processing by an external arithmetic circuit not shown. This is effected as follows. Since an image signal obtained from the output terminal V_{OS} contains a charge component (S) and a dark component (D) and an image signal obtained from the output terminal V_{OD} contains only the dark component (D), only the image signal according to the charge component (S) is extracted by the arithmetic processing of the image signals obtained from the output terminals V_{OS}, V_{OD} (by subtraction processing ($V_{OS}-V_{OD}$)).

The above reading operation for the first row in the periods t_{11} to t_{15} is repeated similarly for the second row and the third row in the periods t_{21} to t_{25} and in the periods t_{31} to t_{35}, respectively. Since the photoelectric conversion apparatus in the first embodiment is arranged in such a manner that the reset element **31**b is provided for each pixel **31** and

the reset drains **4** are arranged in parallel with each other in each row, the reset operation becomes very fast and the total time of the periods t_{11} to t_{15}, t_{21} to t_{25}, t_{31} to t_{35} becomes shorter than those of the conventional photoelectric conversion apparatus.

Embodiment 6

FIGS. **7**A to **7**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 6 of the present invention, wherein FIG. **7**A is a plan view of the schematic structure to show the photoelectric conversion element, FIG. **7**B a cross section along **X1**–X2 line in FIG. **7**A, and FIG. **7**C a cross section along Y1–Y2 line in FIG. **7**A. The photoelectric conversion element shown in FIGS. **7**A to **7**C is most different from the photoelectric conversion elements shown in FIG. **1** to FIG. **4** in that a gate electrode **50** is formed for controlling the control region of JFET **2** by capacitive coupling in JFET **2** (the amplifying portion). The other structure of this photoelectric conversion element is the same as the photoelectric conversion element shown in FIG. **1**. A gate line **51** is formed as shown in FIG. **7**A.

In ordinary JFET **2**, the gate electrode **50** for controlling the control region by capacitive coupling is formed. However, the photoelectric conversion elements shown in FIG. **1** to FIG. **4** exclude the gate electrode **50**. The differences due to the formation of gate electrode **50** will be explained in the next description of a photoelectric conversion apparatus having photoelectric conversion elements (FIGS. **7**A to **7**C) arranged in a two-dimensional matrix where the gate electrode **50** is formed.

The photoelectric conversion element shown in FIGS. **7**A to **7**C is the same as the photoelectric conversion element shown in FIGS. **1**A to **1**C except that the gate electrode **50** is formed. If the structures of photodiode **1** and JFET **2** of the photoelectric conversion element shown in FIGS. **7**A to **7**C are replaced by the structures of photodiode **1** and JFET **2** of the photoelectric conversion element shown in FIGS. **2**A to **2**C, the photoelectric conversion element thus obtained becomes the same as the photoelectric conversion element shown in FIGS. **2**A to **2**C except that the gate electrode **50** is formed. Further, if the element isolation region **21** of the predetermined conductivity type is formed between the mutual regions of the photodiode **1**, JFET **2**, and reset drain **4** of the photoelectric conversion element shown in FIGS. **7**A to **7**C, it becomes the same as the photoelectric conversion element shown in FIGS. **3**A to **3**C except that the gate electrode **50** is formed. The description of the same portions is thus omitted herein.

Embodiment 7

FIG. **8** is a circuit diagram to show the schematic structure of the photoelectric conversion apparatus according to Embodiment 7 of the present invention, in which the photoelectric conversion elements shown in FIGS. **7**A to **7**C are arranged in a two-dimensional matrix. Comparing FIG. **8** with FIG. **5** (Embodiment 5), the photoelectric conversion apparatus shown in FIG. **8** is arranged in such a manner that the gate electrodes **50** of JFETs **2** forming the respective pixels (photoelectric conversion elements) **31** in each row are connected in common to the vertical scanning circuit **34**. The gate electrodes **50** are pulse-driven.

In the photoelectric conversion apparatus as explained in FIG. **5** the reset drains **4** were pulse-driven instead of the above gate electrodes **50**, because no gate electrodes **50** were formed in the JFETs **2**. It is, however, noted that the photoelectric conversion apparatus explained in FIG. **5** can obviate a need to form wiring to the gate electrodes **50** because no gate electrodes **50** are formed in the JFETs **2**. Accordingly, the capacitance of each control region of JFET **2** can be decreased because of the absence of the gate electrode **50**, thus presenting an advantage that the sensitivity can be enhanced.

In contrast, the photoelectric conversion apparatus shown in FIG. **8** has an advantage that the reset drains **4** do not have to be pulse-driven because the gate electrodes **50** are formed in the JFETs **2**.

In the photoelectric conversion apparatus shown in FIG. **8**, each pixel **31** is composed of a photodiode **1** for generating and storing a charge according to incident light, a gate electrode **50** for controlling the control region by capacitive coupling, a JFET **2** for producing a signal output according to the charge received by the control region, a transfer control element (p-channel MOSFET) **31***a* having a transfer gate **3** for transferring the charge generated and stored in the photodiode **1** to the control region of JFET **2**, a reset drain **4** for draining the charge transferred to the control region of JFET **2**, and a reset element (p-channel MOSFET) **31***b* having a reset gate **5** for controlling the reset drain **4**.

The sources of JFETs **2** in each column of the matrix arrangement are connected in common to the vertical source line **32***a*, **32***b*, **32***c*. All the pixels are connected in common to the drain power-supply **31***c* through a wiring (not shown) or diffusion layer on the drain side of each JFET **2** and on the cathode side of photodiode **1**. Further, the anode side of each photodiode **1** and the control region of JFET **2** each are connected to the source or the drain of the transfer control element **31***a*.

The transfer gates (transfer gate electrodes) **3** of the transfer control elements **31***a* are connected in common in each row of the matrix arrangement to the clock line **33***a*, **33***b*, **33***c* to be scanned by the vertical scanning circuit **34**, and with application of the drive pulse Φ_{TG1} to Φ_{TG3} sent from the above vertical scanning circuit **34** the transfer control elements **31***a* are sequentially operated in each row.

The gate electrodes **50** in JFETs **2** are connected in common in each row of the matrix arrangement to the clock line **35***a*, **35***b*, **35***c* to be scanned by the vertical scanning circuit **34**, and the JFETs **2** are sequentially operated in each row when the drive pulse Φ_{G1}–Φ_{G3} sent from the above vertical scanning circuit **34** is applied thereto.

A reset element **31***b* is given for each pixel **31**, and reset drains **4** of all the pixels are connected in common to the power-supply voltage V_{RD} through a row line **36**. The reset gates (reset gate electrodes) **5** of the all pixels are also connected in common through the row line **37***a* to the drive pulse generating circuit **37**. The source of each reset element **31***b* is formed in common with the drain of transfer control element **31***a*. When a drive pulse Φ_{RG} sent from the drive pulse generating circuit **37** is applied to the reset gate **5**, this reset element **31***b* is arranged to operate, thus initializing the control region of JFET **2**.

The above vertical source line **32***a*, **32***b*, **32***c*, on one hand, is connected in each column through a MOS transistor for transferring the light signal output T_{S1}, T_{S2}, T_{S3} and through MOS transistor for transferring a dark output T_{D1}, T_{D2}, T_{D3} to one electrode of the capacitor for storing the light signal output (second memory element) C_{S1}, C_{S2}, C_{S3} and to one electrode of the capacitor for storing the dark output (first memory element) C_{D1}, C_{D2}, C_{D3} and then is connected through the MOS transistors for selection of horizontal reading T_{HS1}, T_{HS2}, T_{HS3}, T_{HD1}, T_{HD2}, T_{HD3} to the signal

output line **38** and the dark output line **39**. Generally, parasitic capacitances C_{HS}, C_{HD} exist in the signal output line **38** and dark output line **39**. A buffer amplifier **38***a*, **39***a* is connected to one end of each of the signal output line **38** and dark output line **39**.

The above signal output line **38** and dark output line **39** are connected to the drains of MOS transistors for resetting the signal output lines T_{RHS}, T_{RHD}, respectively, and the sources of MOS transistors T_{RHS}, T_{RHD} are grounded (GND) as being connected to the other electrodes of the above capacitors for storing the light signal output C_{S1}, C_{S2}, C_{S3} and capacitors for storing the dark output C_{D1}, C_{D2}, C_{D3}. When a drive pulse Φ_{RH} sent from the drive pulse generating circuit **43** is applied to the gate electrodes of the MOS transistors for resetting the signal output lines T_{RHS}, T_{RHD}, the MOS transistors T_{RHS}, T_{RHD} are arranged to start operating.

A horizontal selection line **40***a*, **40***b*, **40***c* connected to a horizontal scanning circuit **40** in each column is connected in common to the gate electrodes of the MOS transistors for selection of horizontal reading T_{HS1}, T_{HS2}, T_{HS3} and T_{HD1}, T_{HD2}, T_{HD3}, so that horizontal reading may be controlled by a drive pulse Φ_{H1} to Φ_{H3} sent from the horizontal scanning circuit **40**.

The gate electrodes of the above MOS transistors for transferring the light signal outpnts T_{S1}, T_{S2}, T_{S3} are connected through a clock line for light signal **41***a* and the gate electrodes of the above MOS transistors for transferring the dark outputs T_{D1}, T_{D2}, T_{D3} are connected through a clock line for dark output **42***a*, each to a drive pulse generating circuit **41** or **42**. When a drive pulse Φ_{TS} or Φ_{TD} sent from the drive pulse generating circuit **41** or **42** is applied to the gate electrodes through either line, these MOS transistors for transmission of light signal output T_{S1}, T_{S2}, T_{S3} and MOS transistors for transmission of dark output T_{D1}, T_{D2}, T_{D3} are arranged alternately to operate in a predetermined order.

The above vertical source line **32***a*, **32***b*, **32***c* in each column, on the other hand, is connected to the drain of a transistor for reset T_{RV1}, T_{RV2}, T_{RV3} and to a constant current source for source-follower reading **44***a*, **44***b*, **44***c*. A power-supply voltage V_{RV} is supplied to the source of each reset transistor T_{RV1}, T_{RV2}, T_{RV3}, and a power-supply voltage V_{CS} is supplied to the constant current sources for source-follower reading **44***a*, **44***b*, **44***c*.

A reset pulse Φ_{RV} is supplied to the gate electrodes of the reset transistors T_{RV1}, T_{RV2}, T_{RV3}, and with a change of this reset pulse Φ_{RV} to the high level the reset transistors T_{RV1}, T_{RV2}, T_{RV3} become on so as to ground the vertical source lines **32***a*, **32***b*, **32***c* (when V_{RV}=GND).

The constant current sources for source-follower reading **44***a*, **44***b*, **44***c* control the time constant of source-follower operation, and also suppress variations of the time constant due to fluctuations of bias point for every pixel **31** to equalize the gains, thus suppressing FPN.

The operation of the photoelectric conversion apparatus according to Embodiment 7 of the present invention shown in FIG. **8** is next explained referring to the pulse timing chart shown in FIG. **9**. In FIG. **9**, the period between t_{11} and t_{15} represents the reading operation of pixels **31** in the first row, and thereafter the periods between t_{21} and t_{25} and between t_{31} and t_{35} correspond to the second row and the third row, respectively. Further, t_{11} to t_{14} each are so defined that t_{11} is the period for the initialization operation of JFET **2**, t_{12} the period for the source-follower operation of JFET **2** in the first row after initialization, t_{13} the period for the transfer operation of signal charge from the photodiode **1** to the JFET **2** in the first row, and t_{14} the period for the source-follower operation of JFET **2** after transfer, and these four operations are carried out in the horizontal blanking period. Further, t_{15} is the image signal output period.

First, as shown in FIG. **9**, in the period t_{11} the drive pulses Φ_{RG} and Φ_{TD} are changed to the high level whereby the reset gates **5** of the respective pixels **31** are changed from the conductive (on) state into the non-conductive (off) state and the MOS transistors for transfer of dark output T_{D1}, T_{D2}, T_{D3} are changed into the conductive (on) state.

As a result, the control regions of all JFETs **2** come to have the potential of the power-supply voltage V_{RD} connected through the reset drains **4** and the row line **36** so as to be initialized (the charges are drained), thus turning to a floating state. The reason why the drive pulse Φ_{RG} to the reset gates **5** is at the high level to keep the reset gates **5** in the non-conductive state (off) is that the polarity is opposite to that of the other drive pulses because the reset elements **31***b* are of the p-channel type.

Next at the start of the period t_{12}, the drive pulse Φ_{G1} is changed to the high level to raise the potential of the gate electrodes of JFETs **2** in the first row, whereby the JFETs **2** in the first row are selected (on) and the JFETs in the second and the other rows are not selected (off). Namely, when the reset gates **5** are in the non-conductive state (off), selection (on) or non-selection (off) of JFETs **2** is effected depending upon whether the drive pulse (Φ_{G1}, Φ_{G2}, Φ_{G3}) is sent to a row of the gate electrodes of JFETs or not.

At the same time (at the start of period t_{12}), the drive pulse Φ_{RV} is changed to the low level to bring the reset transistors T_{RV1} to T_{RV3} into an interrupted (off) state, and the JFETs **2** in the first row perform the source-follower operation in this period t_{12}. During this period t_{12} the drive pulse Φ_{TD} is at the high level to keep the MOS transistors for transfer of dark output T_{D1}, T_{D2}, T_{D3} in a conductive state (on) and output (output at dark) voltages corresponding to the potentials immediately after the initialization of the control regions of the JFETs **2** are stored in the capacitors for storage of dark output C_{D1}, C_{D2}, C_{D3}.

In the period t_{13}, the drive pulse Φ_{TG1} is turned to the low level to bring the transfer gates **3** from the non-conductive (off) state into the conductive (on) state, and the drive pulse Φ_{TS} is changed to the high level and the drive pulse Φ_{TD} to the low level, thereby changing the MOS transistors for transfer of light signal output T_{S1}, T_{S2}, T_{S3} into the conductive (on) state and the MOS transistors for transfer of dark output T_{D1}, T_{D2}, T_{D3} into the non-conductive (off) state.

As a result, charges generated and stored in the photodiodes **1** in the first row are transferred to the control regions of JFETs **2**. After transfer of charge the potential of each control region of JFET **2** changes (increases in this case) by a degree of charge amount/gate capacitance. The reason why the transfer gates **3** are in the conductive state (on) when the drive pulse Φ_{TG1} is kept at the low level in FIG. **9** is that the transfer control elements **31***a* are of the p-channel type and thus the polarity is opposite to that of the other drive pulses.

In the period t_{14}, similarly as in the period t_{12}, the drive pulse Φ_{TG1} is changed to the high level to bring the transfer gates **3** in the first row into the non-conductive (off) state whereby the charges photoelectrically converted in the photodiodes **1** are kept as stored, and the drive pulse Φ_{RV} is changed to the low level to bring the reset transistors T_{RV1} to T_{RV3} to the interrupted (off) state whereby the JFETs **2** in the first row perform the source-follower operation.

Since during this period t_{14} the drive pulse Φ_{TS} is at the high level, the MOS transistors for transfer of light signal

output T_{S1}, T_{S2}, T_{S3} are kept in the conductive state (on), and output (signal output) voltages corresponding to potentials after the charges are transferred to the control regions of the respective JFETs **2** are stored in the capacitors for storage of light signal output C_{S1}, C_{S2}, C_{S3}.

In the period t_{15}, the drive pulses Φ_{RD1}, Φ_{RG}, Φ_{TS} are each changed to the low level and the drive pulse Φ_{RV} to the high level, so that the output voltages (image signals) stored in the capacitors for storage of light signal output C_{S1} to C_{S3} and capacitors for storage of dark output C_{D1} to C_{D3} are ready to be output to the output terminals V_{OS}, V_{OD}.

Then sequentially outputting the drive pulses Φ_{H1} to Φ_{H3} from the horizontal scanning circuit **40** and the drive pulse Φ_{RH} from the drive pulse generating circuit **43**, the image signals stored in the capacitors for storage of light signal output C_{S1} to C_{S3} and the capacitors for storage of dark output C_{D1} to C_{D3} are read out into the horizontal reading lines of signal output line **38** and dark output line **39**, respectively, then, the image signals are output from the terminals V_{OS}, V_{OD}, while horizontal reading lines of signal output line **38** and dark output line **39** are reset.

The image signals obtained from the output terminals V_{OS}, V_{OD} are subjected to arithmetic processing by an external arithmetic circuit not shown. This is effected as follows. Since an image signal obtained from the output terminal V_{OS} contains a charge component (S) and a dark component (D) and an image signal obtained from the output terminal V_{OD} contains only the dark component (D), only the image signal according to the charge component (S) is extracted by the arithmetic processing of the image signals obtained from the output terminals V_{OS}, V_{OD} (by subtraction processing ($V_{OS}-V_{OD}$)).

The above reading operation for the first row in the periods t_{11} to t_{15} is repeated similarly for the second row and the third row in the periods t_{21} to t_{25} and in the periods t_{31}, to t_{35}, respectively. Since the photoelectric conversion apparatus shown in FIG. **8** is arranged in such a manner that the reset element **31b** is provided for each pixel **31** and the reset drains **4** of all the pixels are arranged in parallel with each other, the reset operation becomes very fast and the total time of the periods t_{11} to t_{15}, t_{21} to t_{25}, t_{31} to t_{35} becomes shorter than those of the conventional photoelectric conversion apparatus.

Embodiment 8

FIGS. **10A–10C** are schematic structural drawings to show the photoelectric conversion element according to Embodiment 8 of the present invention, wherein FIG. **10A** is a plan view of the schematic structure to show the photoelectric conversion element, FIG. **10B** a cross section along **X1–X2** line in FIG. **10A**, and FIG. **10C** a cross section along **Y1–Y2** line in FIG. **10A**. The photoelectric conversion element according to this Embodiment 8 is different from the above embodiments in that a depletion type MOS transistor **52** is used for the amplifying portion.

The MOS transistor performs so-called non-destructive amplification operation without destroying the charge (signal charge) during amplification operation, similarly as JFET **2**, and thus has a property of rarely causing FPN. Further, the MOS transistor has no residual charge in the control region (the surface of silicon (n-type silicon layer) under the gate electrode) upon reset of signal charge, thus having a property of rarely causing lag and reset noise. Accordingly, it is suitable for example for forming a solid state image sensing device capable of performing electronic shutter operation by keeping simultaneity in a frame.

Embodiment 9

FIG. **11** is a circuit diagram to show the schematic structure of the photoelectric conversion apparatus according to Embodiment 9 of the present invention, in which the photoelectric conversion elements shown in FIGS. **10A–10C** are arranged in a two-dimensional matrix. FIG. **12** is a pulse timing chart for explaining the operation of the circuit diagram shown in FIG. **11**.

The photoelectric conversion apparatus shown in FIG. **11** is different from the photoelectric conversion apparatus as explained in FIG. **5** (Embodiment 5) and in FIG. **8** (Embodiment 7) in that the amplifying portions of pixels **31** are MOS transistors (MOS), the transfer gates **3** of transfer control elements **31a** of all the pixels are connected in common through a row line **51a** to the drive pulse generating circuit **51**, and the reset gates **5** of the reset elements **31b** in each row are arranged to be operated by the drive pulse (Φ_{RG1}–Φ_{RG3}) sent from the vertical scanning circuit **34** through the clock line **52a**, **52b**, **52c**. Employing the arrangement of the photoelectric conversion apparatus shown in FIG. **11**, the photoelectric conversion apparatus can realize the electronic shutter operation with simultaneity in a frame.

Now, the operation of the photoelectric conversion apparatus shown in FIG. **11** is explained referring to the pulse timing chart shown in FIG. **12**. First, as shown in FIG. **12**, in the period t_{10} the drive pulses Φ_{TG} and Φ_{RG1}–Φ_{RG3} are changed to the low level, whereby the transfer gates **3** and reset gates **5** of the respective pixels **31** are changed from the non-conductive (off) state into the conductive (on) state.

As a result, not only the control regions of the MOS transistors (MOS) but also the photodiodes **1** are electrically connected to the reset drains **4**, whereby the photodiodes **1** are depleted to be initialized and the control regions of the MOS transistors (MOS) are initialized to the potential of the reset drains **4**.

Then, in the period t_{11} the drive pulses Φ_{TG} and Φ_{RG1}–Φ_{RG3} are changed to the high level to change the transfer gates **3** and reset gates **5** of the respective pixels **31** into the non-conductive (off) state and to bring the photodiodes **1** into a charge storing state. The period t_{11} becomes a shutter time.

Next, in the period t_{12}, the drive pulses Φ_{RG1}–Φ_{RG3} are again set to the low level to change the reset gates **5** of the respective pixels **31** from the non-conductive (off) state to the conductive (on) state. As a result, the potential of the control regions of the MOS transistors (MOS) turn to the potential of the reset drains **4** connected through the row line **36** to the power-supply voltage V_{RD}, and dark currents occurring in the MOS transistors (MOS) during the period t_{11} are eliminated, thus again initializing the MOS transistors (MOS). This initialization operation of the MOS transistors (MOS) is a necessary operation for long-term storage in the photodiodes **1** in the case of image pickup in a still picture mode.

In the period t_{13} the drive pulse Φ_{TS} is set to the high level to change the MOS transistors for transfer of light signal output T_{S1}, T_{S2}, T_{S3} into the conductive (on) state, the drive pulses Φ_{RG1}–Φ_{RG3} are set to the high level to turn the reset gates **5** of the respective pixels **31** into the non-conductive (off) state, and the drive pulse Φ_{TG} is set to the low level to turn the transfer gates **3** of the respective pixels **31** into the conductive (on) state. As a result, the charges generated and stored in the period t_{11} are transferred from the photodiodes **1** to the control regions of MOS transistors.

In the periods t_{14} to t_{17} the reading operation of the pixels **31** in the first row is carried out substantially in the same

manner as in the photoelectric conversion apparatus shown in FIG. **5** and FIG. **8**. Namely, the operation in the periods t_{14}–t_{17} in the photoelectric conversion apparatus shown in FIG. **11** corresponds to the operation in the periods t_{12}–t_{15} in the photoelectric conversion apparatus shown in FIG. **5** and FIG. **8**.

Namely, in the period t_{14} of the photoelectric conversion apparatus shown in FIG. **10**, the drive pulse Φ_{G1} is set to the high level to raise the potential of the gate electrodes operated by capacitive coupling, and the drive pulse Φ_{RV} is set to the low level to turn the reset transistors T_{RV1}–T_{RV3} into the interrupted state (off), whereby the MOS transistors (MOS) in the first row perform the source-follower operation (charge amplification operation by capacitive load). Here, selection (on) or non-selection (off) of MOS transistors (MOS) in each row is determined by the drive pulses (Φ_{G1}–Φ_{G3}) to the gate electrodes.

During this period t_{14} the drive pulse Φ_{TS} is already set at the high level so as to keep the MOS transistors for transfer of light signal output T_{S1}, T_{S2}, T_{S3} in the conductive state (on), and output (signal output) voltages corresponding to potentials after the charges are transferred to the control regions of MOS transistors are stored in the capacitors for storage of light signal output C_{S1}, C_{S2}, C_{S3}.

Next, in the period t_{15}, the drive pulse Φ_{TD} is set to the high level to turn the MOS transistors for transfer of dark output T_{D1}, T_{D2}, T_{D3} into the conductive state (on), and the drive pulse Φ_{RG} to the low level to turn the reset gates **5** in the first row into the conductive state (on), whereby the control regions of the MOS transistors (MOS) in the first row are reset (the charges are drained).

Further, in the period t_{16}, the drive pulse Φ_{RV} is again set to the low level to turn the reset transistors T_{RV1}–T_{RV3} into the interrupted state (off), and the MOS transistors (MOS) in the first row perform the source-follower operation after reset.

During this period t_{16} the drive pulse Φ_{TD} is already set at the high level to keep the MOS transistors for transfer of dark output T_{D1}, T_{D2}, T_{D3} in the conductive state (on), and output (output at dark) voltages corresponding to the potentials after reset of the control regions of MOS transistors (MOS) are stored in the capacitors for storage of dark output C_{D1}, C_{D2}, C_{D3}.

Then in the period t_{17} the drive pulses Φ_{G1}, Φ_{TD} are set each to the low level and the drive pulse Φ_{RV} to the high level so as to get ready to output the output voltages (image signals) stored in the capacitors for storage of light signal output C_{S1}–C_{S3} and the capacitors for storage of dark output C_{D1}–C_{D3} to the output terminals V_{OS}, V_{OD}. Then sequentially outputting the drive pulses Φ_{H1}–Φ_{H3} from the horizontal scanning circuit **40** and the drive pulse Φ_{RH} from the drive pulse generating circuit **43**, the image signals stored in the capacitors for storage of light signal output C_{S1}–C_{S3} and the capacitors for storage of dark output C_{D1}–C_{D3} are transferred to the horizontal reading lines of signal output line **38** and dark output line **39**, respectively, then the image signals are output from the terminals V_{OS}, V_{OD}, while horizontal reading lines of signal output line **38** and dark output line **39** are reset.

The above completes the reading operation of the first row, and the reading operation is then carried out for the second row in the periods t_{24}–t_{27} and for the third line in the periods t_{34}–t_{37}.

The photoelectric conversion apparatus shown in FIG. **11** was explained as to the case of image pickup mainly of still pictures, but the apparatus can be applied to the cases for picking up a moving picture. Namely, the electronic shutter operation can be applied to the cases for picking up the moving picture. However, in the cases for picking up the moving picture, the operation in the periods t_{10}–t_{13} shown in FIG. **12** (among which the period t_{12} is not necessary in the case of the moving picture) needs to be performed within the vertical blanking period. Thus, there is a certain limitation on the variable range of shutter speed.

The photoelectric conversion apparatus shown in FIG. **11** (capable of performing the electronic shutter operation with simultaneity in a frame) can employ not only the MOS type photoelectric conversion elements, but also the JFET type or the bipolar type photoelectric conversion elements, as long as they are constructed in the structure operable by capacitive coupling. However, the most preferred elements are the MOS type photoelectric conversion elements causing no reset noise, because the reset operation is interposed between two source-follower operations.

Embodiment 10

FIGS. **13**A to **13**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 10 of the present invention, wherein FIG. **13**A is a plan view of the schematic structure to show the photoelectric conversion element, FIG. **13**B a cross section along X1–X2 line in FIG. **13**A, and FIG. **13**C a cross section along Y1–Y2 line in FIG. **13**A. The photoelectric conversion element shown in FIGS. **13**A to **13**C is different from the above embodiments in that a bipolar transistor **53** is used for the amplifying portion. The emitter **54**, collector **55**, and base **56** are constructed as shown in the drawings, and the emitter electrode **57** and emitter line **58** are formed as shown.

In the bipolar transistor **53** shown in FIGS. **13**A to **13**C, the collector region is formed in the silicon (n-well region **14**) surface layer part without forming the n^+-type buried collector or the collector using the high-concentration n-type substrate usually used. This arrangement thus enables the combination of the bipolar transistor **53** with the photodiode **1** in the vertical overflow structure, which can suppress the variations in the output signals due to blooming, smear or the like.

Since Embodiment 10 excludes the electrode for driving the base region by capacitive coupling, the capacitance of the control region becomes small and high sensitivity can be secured.

Embodiment 11

FIGS. **14**A to **14**C are schematic structural drawings to show the photoelectric conversion element according to Embodiment 11 of the present invention, wherein FIG. **14**A is a plan view of the schematic structure to show the photoelectric conversion element, FIG. **14**B a cross section along X1–X2 line in FIG. **14**A, and FIG. **14**C a cross section along Y1–Y2 line in FIG. **14**A. In the photoelectric conversion element shown in FIGS. **14**A–**14**C, a metal line connected to the reset-purpose charge draining means (reset drain **4**) also serving as a light-shielding film (aluminum film **20**) may be connected directly to the p-type reset drain region **15** through a contact hole **59**, which is different from FIGS. **1**A to **1**C in Embodiment 1.

In each of the above embodiments the transfer control element **31***a* and reset element **31***b* were explained as MOS type field effect transistors (MOSFETs), but the same effects can be attained when they are formed as bipolar transistors.

As explained above, the photoelectric conversion elements according to the present invention are provided with

the reset-purpose charge draining means for draining the charge transferred to the control region of the amplifying portion and the above reset-purpose control means, which presents the effect that the reset operation can be performed without operating the amplifying portion.

This achieves the effect to suppress the variations of the amplification factor due to large transient fluctuations of bias point (operating point) of the amplifying portion with flow of a large current in the amplifying portion itself.

Since the photoelectric conversion elements according to the present invention have the amplifying portion formed of the field effect transistor (FET), they have the effects that the charge (signal charge) is not destroyed in the amplifying operation and occurrence of fixed pattern noise (FPN) can be suppressed.

Further, the photoelectric conversion elements according to the present invention have the effects of increases of the aperture ratio and the degree of integration, because the element isolation region of the predetermined conductivity type is formed between the mutual regions of the photoelectric conversion portion, the amplifying portion, the transfer control portion, the reset-purpose charge draining means, and the reset-purpose control means.

Since in the photoelectric conversion elements according to the present invention the metal interconnection connected to the reset-purpose charge draining means is formed as a light-shielding film for shielding incident light to the amplifying portion, the transfer control portion, the reset-purpose charge draining means, and reset-purpose control means, they also have the effect of suppressing the phenomenon of blur such as blooming due to obliquely incident light.

Since in the photoelectric conversion elements according to the present invention the photoelectric conversion portion is the buried photodiode in the vertical overflow structure, they have the effects of suppressing the phenomenon of blur such as blooming and smear and achieving ideal characteristics by suppressing the dark current, lag, and reset noise.

Since the photoelectric conversion elements according to the present invention are constructed in such a structure that the channel forming portion of the amplifying portion of the photoelectric conversion element is formed of the first conductivity type shallow gate region, the second conductivity type shallow channel region, the first conductivity type gate region, the second conductivity type well region, and the first conductivity type semiconductor substrate in order from the semiconductor surface toward the inside of substrate. Therefore, the elements have the effects that the degree of integration and the aperture ratio can be improved and the sensitivity can be enhanced.

The photoelectric conversion elements according to the present invention are constructed in such a structure that the channel forming portion of the amplifying portion of the photoelectric conversion element is formed of the first conductivity type shallow gate region, the second conductivity type shallow channel region, the first conductivity type gate region, the second conductivity type well region, and the first conductivity type semiconductor substrate in order from the semiconductor surface toward the inside of substrate and that the first conductivity type shallow gate region is electrically connected with the first conductivity type gate region. Therefore, the elements have the effects that the degree of integration and the aperture ratio can be improved and the sensitivity can be enhanced.

As explained above, the photoelectric conversion apparatus according to the present invention is constructed in such an arrangement that the photoelectric conversion elements with the reset-purpose charge draining means for draining the charges transferred to the control regions of the amplifying portions and the above reset-purpose control means are arranged in a two-dimensional matrix, and thus have the effects of suppressing degradation of performance (for example, S/N ratios) of the apparatus and of increasing dissipation power.

The photoelectric conversion apparatus according to the present invention has the effect of performing a high-speed reset operation, because the photoelectric conversion apparatus is constructed in such a manner that the reset-purpose charge draining means of the photoelectric conversion elements arrayed in the horizontal scanning direction are arranged in parallel to each other.

The photoelectric conversion apparatus according to the present invention is constructed in such an arrangement that the apparatus has the first memory means for storing signal outputs for one horizontal line immediately after the control regions of the above amplifying portions are initialized according to vertical scanning and the second memory means for storing signal outputs for one horizontal line immediately after the above charges are transferred to the control regions of the above amplifying portions according to vertical scanning and that the apparatus obtains differences between the signal outputs stored in these memory means. Therefore, the apparatus has the effect that the signal outputs according to only the photogenerated charge components can be obtained.

From the invention thus described, it will be obvious that the invention may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

The basic Japanese Application No. 60034/1995 filed on Feb. 24, 1995 is hereby incorporated by reference.

What is claimed is:

1. A photoelectric conversion element comprising:

a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein;

an amplifying portion having a control region for generating a signal output according to the charge received in the gate region from said photoelectric conversion portion;

a transfer control portion for transferring the charge generated and stored in said photoelectric conversion portion to the control region of said amplifying portion;

a reset control region for draining the charge transferred to the control region of said amplifying portion; and

a reset control electrode for controlling the electrical connection between said reset control region and the control region of said amplifying portion,

wherein said amplifying portion is comprised of a junction field effect transistor having a vertical semiconductor structure composed of a first conductivity type gate region, a second conductivity type channel region, and a first conductivity type semiconductot substrate, in order from the semiconductor surface toward the inside of the semiconductor substrate.

2. A photoelectric conversion element, comprising:

a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein;

an amplifying portion having a control region for generating a signal output according to the charge received in the control region from said photoelectric conversion portion;

a transfer control portion for transferring the charge generated and stored in said photoelectric conversion portion to the control region of said amplifying portion;

a reset control region for draining the charge transferred to the control region of said amplifying portion; and

a reset control electrode for controlling the electrical connection between said reset control region and the control region of said amplifying portion,

wherein said amplifying portion is a junction field effect transistor having a vertical semiconductor structure composed of a first conductivity type shallow gate region, a second conductivity type shallow channel region, a first conductivity type gate region, a second conductivity type well region, and a first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate.

3. A photoelectric conversion element, comprising:

a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein;

an amplifying portion having a control region for generating a signal output according to the charge received in the control region from said photoelectric conversion portion;

a transfer control portion for transferring the charge generated and stored in said photoelectric conversion portion to the control region of said amplifying portion;

a reset control region for draining the charge transferred to the control region of said amplifying portion; and

a reset control electrode for controlling the electrical connection between said reset control region and the control region of said amplifying portion,

wherein said amplifying portion is a junction field effect transistor having a vertical semiconductor structure composed of a first conductivity type shallow gate region, a second conductivity type shallow channel region, a first conductivity type gate region, a second conductivity type well region, and a first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate, and wherein said first conductivity type shallow gate region and said first conductivity type gate region are electrically connected with each other in a portion other than the channel forming portion.

4. A photoelectric conversion element, comprising:

a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein;

an amplifying portion having a control region for generating a signal output according to the charge received in the control region from said photoelectric conversion portion;

a transfer control portion for transferring the charge generated and stored in said photoelectric conversion portion to the control region of said amplifying portion;

a reset control region for draining the charge transferred to the control region of said amplifying portion; and

a reset control electrode for controlling the electrical connection between said reset control region and the control region of said amplifying portion,

wherein said photoelectric conversion portion is a buried photodiode having a vertical overflow structure, wherein said amplifying portion is a junction field effect transistor having a vertical semiconductor structure composed of a first conductivity type shallow gate region, a second conductivity type shallow channel region, a first conductivity type gate region, a second conductivity type well region, and a first conductivity type semiconductor substrate in the order from the semiconductor surface toward the inside of the semiconductor substrate, wherein said first conductivity type shallow gate region and said first conductivity type gate region are electrically connected with each other in a portion other than the channel forming portion, and wherein an impurity concentration of said first conductivity type gate region is different from an impurity concentration of a charge storing portion of said buried photodiode.

5. The photoelectric conversion element according to claim **4**, wherein the impurity concentration of said first conductivity type gate region is in the range of 6×10^{15} cm^{-3} to 3×10^{16} cm^{-3} and the impurity concentration of said charge storing portion of the buried photodiode is in the range of 5×10^{15} cm^{-3} to 3×10^{16} cm^{-3}.

6. A photoelectric conversion apparatus comprising:

a plurality of photoelectric conversion elements arranged in a two-dimensional matrix, each said photoelectric conversion element comprising a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein, an amplifying portion having a control region for generating a signal output according to the charge received in the control region from said photoelectric conversion portion, a transfer control portion for transferring the charge generated and stored in said photoelectric conversion portion to the control region of said amplifying portion, a reset control region for draining the charge transferred to the control region of said amplifying portion, and a reset control electrode for controlling the electrical connection between said reset control region and the control region of said amplifying portion;

a vertical scanning circuit; and

a pulse drive source;

wherein each of transfer control portions and reset control regions of said photoelectric conversion elements is respectively connected commonly along a horizontal scanning direction, thereby connecting to said vertical scanning circuit for pulse driving, and

wherein a reset control electrode of each of said photoelectric conversion elements is connected commonly to said pulse drive source.

7. A photoelectric conversion apparatus comprising:

a plurality of photoelectric conversion elements arranged in a two-dimensional matrix, each said photoelectric conversion element comprising a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein, an amplifying portion having a control region for generating a signal output according to the charge received in the control region from said photoelectric conversion portion, a transfer control portion for transferring the charge generated and stored in said photoelectric conversion portion to the control region of said amplifying portion reset control region for draining the charge transferred to the control region of said amplifying portion, and a reset control electrode for controlling the electrical connection between said reset control region and the control region of said amplifying portion, and a control means for controlling the control region of said amplifying portion by capacitive coupling;

a vertical scanning circuit;

a pulse drive source; and

a power supply;

wherein each of transfer control portions and control means for controlling the control regions of said amplifying portions by capacitive coupling of said photoelectric conversion elements is respectively connected commonly along a horizontal scanning direction, thereby connecting to said vertical scanning circuit for pulse driving, and wherein a reset control electrode and a reset control region of each of said photoelectric conversion elements is respectively connected commonly, such that each of said reset control electrodes is connected to said pulse drive source and each of said reset control regions is connected to said power supply.

8. A photoelectric conversion apparatus comprising:

a plurality of photoelectric conversion elements arranged in a two-dimensional matrix, each said photoelectric conversion element comprising a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein, an amplifying portion having a control region for generating a signal output according to the charge received in the control region from said photoelectric conversion portion, a transfer control portion for transferring the charge generated and stored in said photoelectric conversion portion to the control region of said amplifying portion, a reset control region for draining the charge transferred to the control region of said amplifying portion, a reset control electrode for controlling the electrical connection between said reset control region and the control region of said amplifying portion, and a control means for controlling the control region of said amplifying portion by capacitive coupling;

a vertical scanning circuit;

a pulse drive source; and

a power supply;

wherein a control means for controlling the control region of said amplifying portion by capacitive coupling and a reset control electrode of each of said photoelectric conversion elements is respectively connected commonly along a horizontal scanning direction, thereby connecting to said vertical scanning circuit for pulse driving, and

wherein each of transfer control portions and reset control regions of each of said photoelectric conversion elements is respectively connected commonly, such that each of said transfer control portions is connected to said pulse drive source and each of said reset control regions is connected to said power supply.

9. A photoelectric conversion apparatus comprising:

a plurality of photoelectric conversion elements arranged in a two-dimensional matrix, each said photoelectric conversion element comprising a photoelectric conversion portion for generating a charge according to incident light and storing the charge therein, an amplifying portion having a control region for generating a signal output according to the charge received in the control region from said photoelectric conversion portion, a transfer control portion for transferring the charge generated and stored in said photoelectric conversion portion to the control region of said amplifying portion, a reset control region for draining the charge transferred to the control region of said amplifying portion, and a reset control electrode for controlling the electrical connection between said reset control region and the control region of said amplifying portion;

a vertical scanning circuit for commonly driving said photoelectric conversion elements along a horizontal scanning direction;

first memory means for storing signal outputs for one horizontal line immediately after control regions of said amplifying portions are initialized according to vertical scanning; and

second memory means for storing signal outputs for one horizontal line immediately after said charges are transferred to the control regions of said amplifying portions according to vertical scanning.

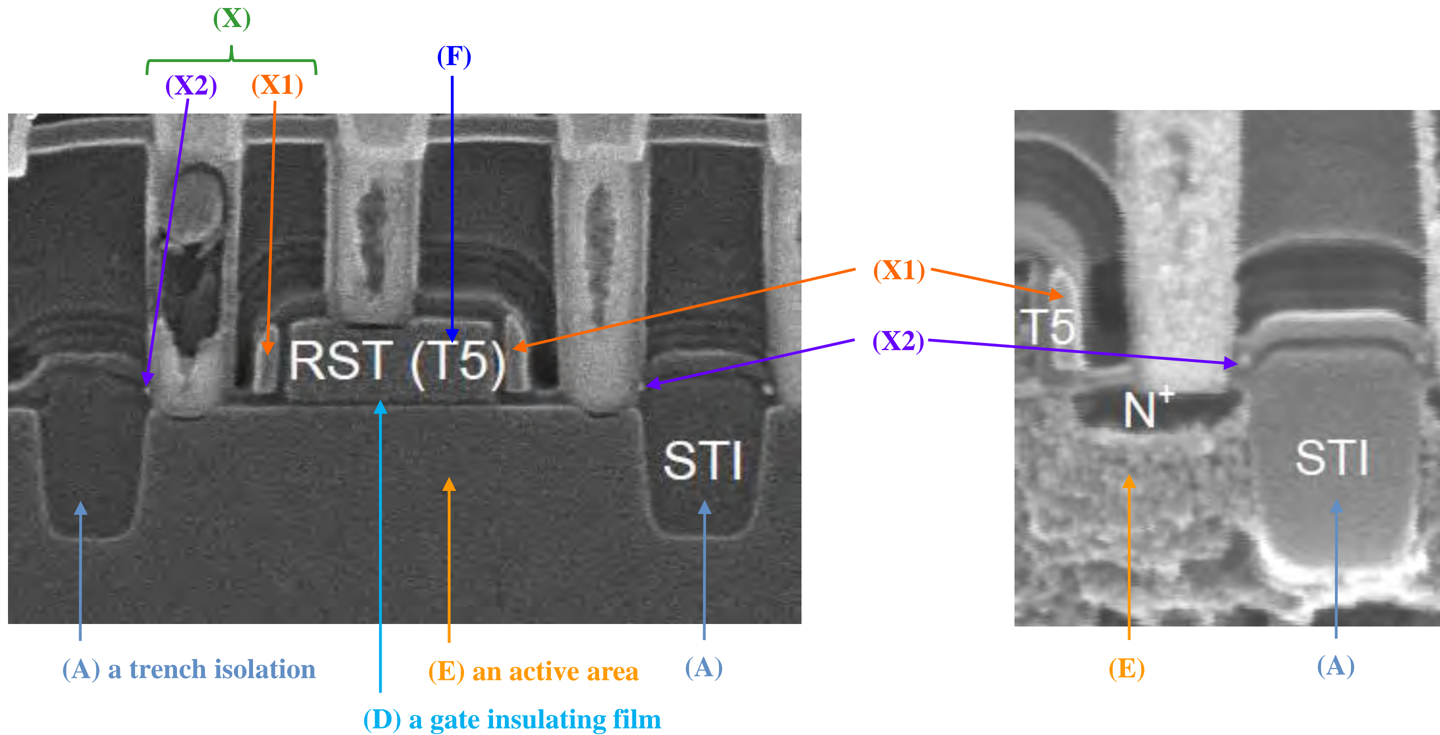
* * * * *

USP 6,709,950 - OmniVision Technologies, Inc. OV8858 (PureCel)

Claim 12

a third step of forming **(F) a gate electrode** on the gate insulating film; after the third step, a fourth step of forming **(X) an insulating film** on the substrate; a fifth step of anisotropically etching the insulating film so as to form **(X1) first sidewalls** on both side surfaces of the gate electrode and form **(X2) second sidewalls** on a side surface of a step portion in the boundary between the trench isolation and the active area; and

The gate electrode (F) is formed on the gate insulating film (D).
An insulating film (X) is etched to form first sidewalls (X1) on the gate electrode (F) and second sidewalls (X2) on the step between the STI and active areas.



USP 6,794,677 - OmniVision Technologies, Inc. OV5650 (OmniBSI)

Claim 1
such that a sum perimeter of **(B) the first linear pattern**, **(E) the second linear pattern**, and **(G) the dummy pattern** per unit area is equal to or less than a perimeter of **(B) the first linear pattern** per unit area.

The first linear pattern (B) density is greater than the average pattern density of (B) the first linear pattern, (E) the second linear pattern, and (G) the dummy pattern.

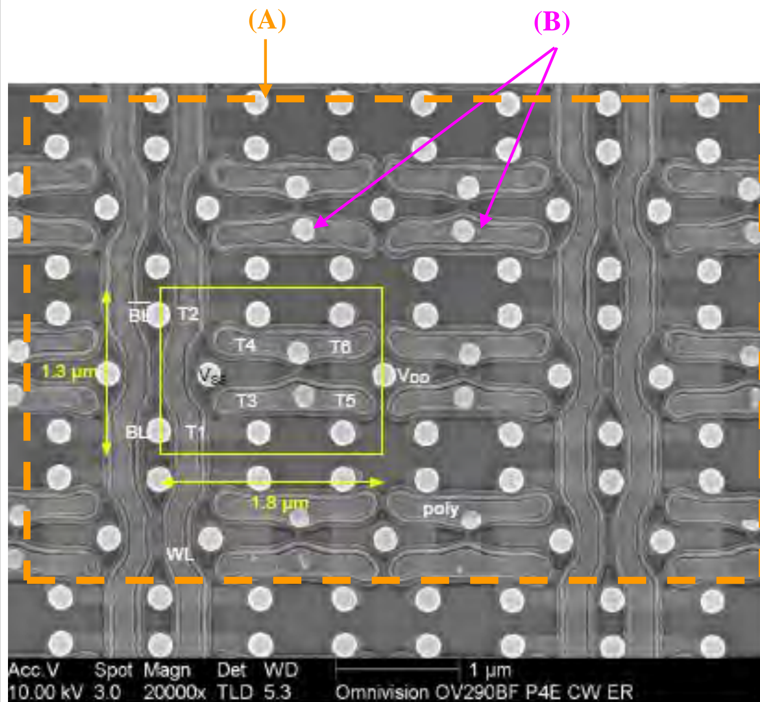


Figure 5.2.3 6T SRAM at Poly

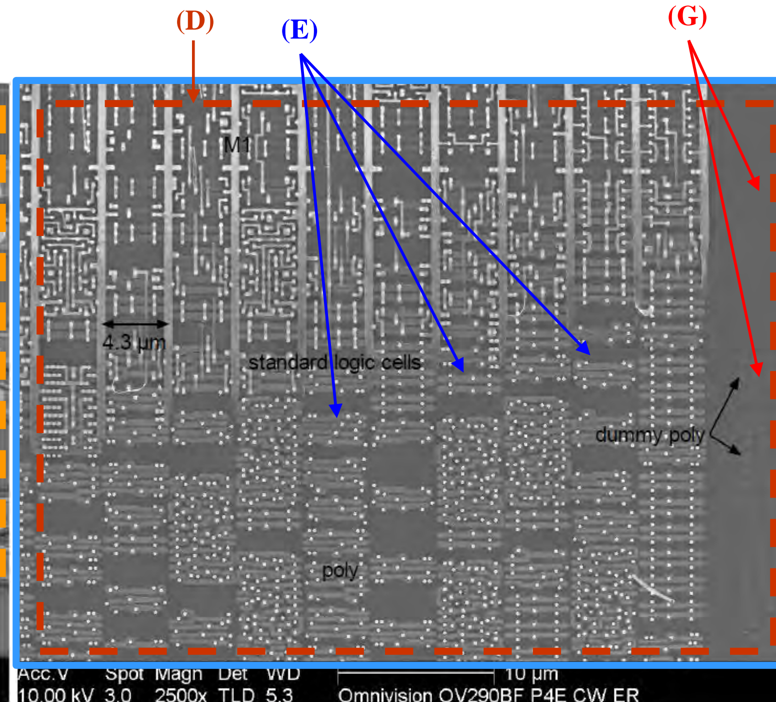


Figure 2.4.2 Standard Logic – Bevel Sample

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

GODO KAISHA IP BRIDGE 1, **Plaintiff,** **v.** **OMNIVISION TECHNOLOGIES, INC.,** **Defendant.**	**Case No. 1:16-cv-00290-MN** **DECLARATION OF DR. JACK C. LEE, PH.D., IN SUPPORT OF DEFENDANT OMNIVISION TECHNOLOGIES, INC.'S ANSWERING CLAIM CONSTRUCTION BRIEF**

I, Dr. Jack C. Lee, declare as follows:

I. Personal Background

1. I am a professor in the Electrical and Computer Engineering Department at The University of Texas at Austin. I have over 35 years of experience as a researcher, educator, and consultant in the field of semiconductor process technology and semiconductor design. I have attached a current copy of my *curriculum vitae* ("CV"), a true and correct copy of which is attached as Exhibit A. The relevant highlights are summarized below.

2. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from the University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from the University of California, Berkeley ("UC Berkeley").

3. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

4. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin ("UT Austin"). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised 40 students who received a doctoral degree under my guidance. I am currently the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at UT Austin.

5. My current research interests include: semiconductor fabrication processes including device isolation and contact formation; semiconductor device characterization and modeling; dielectric processes, characterization and reliability; high-K gate dielectrics and metal gate electrodes in semiconductor devices ("CMOS/MOSFETs"); and alternative transistor channel materials. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation ("SRC"), SEMATECH, Texas Emerging Technology Funds, and others. My research is conducted in our nanofabrication facility with approximately 12,000 sq. ft. of Class 1000/100 clean room space, which is located in the Microelectronics Research Center ("MRC") at The University of Texas at Austin. The MRC is equipped with state-of-the-art equipment for nanofabrication including a CMP machine, capability for nanoscale lithography, etching, deposition of various materials such as polysilicon, insulator, and metal, silicide layer formation, etc. Characterization tools such as optical microscopes, probe stations, an HP 4155A semiconductor parameter analyzer, curve tracers, stylus profilometer, etc. are available in the laboratory. Device packaging facilities include wire bonding and dicing.

6. I am a named inventor on at least seven U.S. patents pertaining to semiconductor and dielectric technology, which are listed in my CV (Exhibit A).

7. To date, I have authored over 500 journal publications and conference proceeding papers, and have coauthored seven books and book chapters on semiconductor processes and devices. Much of my research and publications since about 1998 focus on the topic of semiconductor devices, semiconductor memory and fabrication processes. I have also been recognized with numerous research awards including the prestigious SRC Inventor Recognition Award from Semiconductor Research Corporation for my work on dielectric technology and characterization.

8. In 2002, I became an IEEE fellow for my contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices. I was awarded the IEEE Electron Devices Society Distinguished Lecturer from 2004-2016.

9. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor devices, memory devices and technologies (e.g., Flash memory devices and CMP processes), at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at some of the most prestigious conferences and symposia in the field, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting.

10. Plaintiff Godo Kaisha IP Bridge 1 ("IP Bridge") has asserted U.S. Patent Nos. 6,538,324 ("the'324 patent"), 6,709,950 ("the '950 patent"), 6,794,677 ("the '677 patent"), 8,084,796 ("the '796 patent"), 8,106,431 ("the '431 patent"), 8,378,401 ("the '401 patent") (collectively, the "Asserted Patents"). I have been asked by counsel for Defendant OmniVision Technologies, Inc. ("OmniVision") to review the '324 patent and the '950 patent and to opine on how certain terms in those patents would be understood by a person of ordinary skill in the field

of the asserted patents. I have also been asked to opine on the plain and ordinary meaning of certain terms in the ’324 and ’950 patents as they would have been understood by a person of ordinary skill in the art at the time of the alleged invention for those patents in light of the specification and patent file history for the respective patents.

11. I am being compensated for the work I have performed on this matter at my standard rate of $575 per hour. My compensation is not in any way dependent on the outcome of this litigation.

12. In preparing this declaration, I have considered the asserted patents, their prosecution histories, and the attached exhibits.

13. I reserve the right to supplement this declaration to address any further information that I become aware of in the future.

II. Person of Ordinary Skill in the Art

14. I understand that “a person of ordinary skill in the art” is a hypothetical person who is presumed to have known the relevant art at the time of the invention.

15. In my opinion, a person of ordinary skill in the art for the ’324 and ’950 patents would have a Master’s Degree in electrical engineering, applied physics, material science or equivalent and at least two years of industrial or commercial experience in the design, development, and fabrication of semiconductor devices.

III. Background of the Technology

16. The ’324 and ’950 patents are directed to two types of technology relating to semiconductor devices: (1) barrier structures for semiconductor devices (the ’324 patent); and (2) semiconductor devices and processes for manufacturing semiconductor devices for integrated circuits (the ’950 patent).

17. The '324 patent discloses "a barrier film preventing diffusion of copper from a copper wiring layer formed on a semiconductor substrate." '324 patent at Abstract; *see also id.* at 1:22-33, 2:2-6. The diffusion barrier film is "a multi-layered structure of first and second films wherein the first film is composed of crystalline metal containing nitrogen therein, and the second film is composed of amorphous metal nitride." *Id.* The crystalline film serves to adhere the barrier film to the copper wiring layer and the amorphous metal nitride film serves to prevent diffusion of copper through the barrier film. *See id.* at 6:32-52 ("In the diffusion-barrier film in accordance with the present invention, a copper film makes direct contact with a crystalline metal film containing nitrogen therein, ensuring high adhesion therebetween ….In the diffusion-barrier film in accordance with the present invention, an amorphous metal film containing nitrogen therein lies under a crystalline metal film containing nitrogen therein…That is, by forming a copper wiring layer on the diffusion-barrier film in accordance with the present invention, it is possible to not only ensure high crystallinity and high adhesion of a copper wiring layer, but also to prevent copper diffusion."). The diffusion barrier film lines the surfaces of recesses or holes formed in an interlayer insulating film, which are then filled with a copper wiring layer. *See id.* at 2:2-6 ("Then, a thin diffusion-barrier film is formed on surfaces of the recess and the through-hole therewith such that the recess and the through-hole ***is completely covered at surfaces thereof with the diffusion-barrier film*** in order to prevent copper diffusion from uncovered region") (emphasis added), 14:45-49 ("The first insulating film 12a is formed with via-holes which is filled with a copper wiring layer 44 with ***a diffusion-barrier film 17 being sandwiched between an inner surface of each of the via-holes and the copper wiring layer 44***") (emphasis added); *see also id.* at 2:6-15, 9:26-33, 10:60-64, 11:8-12, 11:26-34, 13:46-50, 14:50-59, 15:9-16. The '324 patent describes how incomplete coverage was a problem with

conventional barrier films at that time. *See id.* at 4:1-31 ("The third problem relates to coverage of a film formed by sputtering…***it would almost impossible to deposit a metal film such that such a recess or hole is completely covered with the metal film***…In accordance with the collimate sputtering, it is possible to deposit a metal film on a bottom of a recess formed at a surface of a substrate, but ***it is not possible to deposit a metal film onto an inner sidewall of the recess***.") (emphasis added). The '324 patent describes methods for forming the barrier film along the entire bottom and sidewalls of the insulating film and the copper wiring layer that is formed in the barrier-film-lined hole or recess. *See id.* at 7:13-22 ("The method of fabricating a diffusion-barrier film employs...sputtering where a nitrogen-containing gas has a pressure equal to or greater than 5 Pa,…thus, there can be obtained coverage for ***entirely covering a recess or hole formed at a surface of a substrate, with the diffusion-barrier film***.") (emphasis added); *see also id.*. at 9:26-42, 10:52-11:53, 12:33-49, 13:66-14:11, 16:29-53. The diffusion barrier film is needed along the entire bottom and sidewalls of the copper wiring layer to prevent the copper from diffusing into the insulating film, which can lead to short circuiting with other copper wiring layers in the insulating film, and from diffusing into the semiconductor substrate, which can "induce reduction in carrier lifetime" leading to degraded transistor performance and increased power consumption. *See id.* 1:22-25.

18. The '950 patent discloses semiconductor devices and processes for manufacturing semiconductor devices for integrated circuits, such as those for preventing the problems resulting from over-etching of isolation regions due to alignment mask shift. *See id.* '950 Patent 3:4-23 ("…a part of the isolation 2b is included in the connection hole 14 when the exposing area of the resist film 25a is shifted toward the isolation 2b due to the mask alignment shift in the photolithography"), 5:50-54 ("The object of the present invention is improving the

structure of an isolation, so as to prevent the problems caused because the edge of the isolation is trenched in etching for the formation of a connection hole or sidewalls.”). Transistors in a semiconductor device are created through a series of deposition, etching, and doping steps. *See id.* at 12:12-13:40. Transistors in a semiconductor substrate are separated by isolation regions to prevent them from electrically interfering with each other. *See id.* at 7:63-65 (“ In this manner, the function of the trench isolation to isolate each semiconductor element can be prevented from degrading.”). In order to provide an electrical connection to a transistor, a mask must be applied to allow an etching process to remove insulating material over the source or drain region of the transistor. *See id.* at 1:40-47, 2:62-65. If this mask shifts from its intended alignment, the isolation region can be over-etched, which can cause the source or drain contact to extend below the top surface of the semiconductor substrate. *See id.* at 3:4-23. This incorrect source/drain contact placement can result in increased junction leakage current, which increases power consumption, and short circuiting the source or drain contact with the semiconductor substrate, which can cause the circuit to malfunction. *See id.* at 3:4-23, 7:60-65. The ’950 patent implements a raised isolation region, a laminated film composed of two different films with different etching properties, and insulating sidewalls to address the issues related to over-etching due to mask alignment shift. *See id.* at 5:59-64, 7:15-20, 7:55-60, 20:38-61, 23:17-22, 23:56-63.

IV. Analysis of the Barrier Film Patent

a. “multi-layered structure of first and second films”

19. I have examined the ’324 patent and its file history, and in particular the claim term “multi-layered structure of first and second films” in claims 1 and 5. In my opinion, a person of ordinary skill in the art would understand this term to mean “multi-layered structure of first and second films covering the entire bottom and sidewalls of the copper wiring layer”

because a diffusion barrier film cannot prevent the diffusion of copper from a copper wiring layer if it does not completely cover the entire bottom and sidewalls of the copper wiring layer.

20. Copper (Cu) has low resistivity. This means that for wiring having the same dimensions, copper has lower resistance than gold, aluminum, and tungsten. With lower resistance, semiconductor devices using copper interconnects exhibit higher speed than aluminum (Al) interconnects. Copper also has better reliability (*i.e.*, less electro-migration) than aluminum.

Metal	Bulk Resistivity [μΩ•cm]
Ag	1.63
Cu	1.67
Au	2.35
Al	2.67
W	5.65

21. One problem with copper interconnects is that copper has a high diffusion rate into interlayer insulating films ("dielectrics"), such as those composed of silicon oxide (SiO_2) and semiconductor substrates, such as those composed of silicon. Transistors are generally formed in a semiconductor substrate and additional levels of circuitry, which are separated by interlayer insulating films, are layered over the semiconductor substrate. Copper diffusion into the interlayer insulating films can lead to unintended electrical shorting between neighboring interconnect wires, causing circuit malfunction. Copper diffusion into the semiconductor substrate at the transistor level can "induce reduction in carrier lifetime," which can degrade transistor performance and increase leakage current and power consumption of the semiconductor device. '324 patent at 1:22-25.

22. Thus, it is my opinion that the claimed diffusion barrier film in the '324 patent must be present on the entire bottom and sidewalls of the copper wiring layer (*i.e.*, the interface between the interlayer insulating films and the copper wiring layer) to prevent the diffusion of copper into the interlayer insulating films or further down into the semiconductor substrate. If the diffusion barrier film is not present on the entire bottom and sidewalls of the copper wiring layer, *i.e.*, there is a place between the interlayer insulating film and the copper wiring layer where the diffusion barrier film is ***not*** present, the copper can diffuse through the space not covered by the diffusion barrier film and cause the problems discussed above, such as the degradation of transistor performance and the increase of leakage current and power consumption of the semiconductor device.

23. Incomplete coverage is a problem with the conventional barrier films at the time that the '324 patent was meant to specifically address. *See e.g.* '324 patent at 4:1-31. In view of this problem regarding incomplete coverage, the '324 specification discloses barrier films that cover the entire bottoms and sidewalls of the holes in which the copper wiring layer is deposited (*i.e.* barrier films that cover the bottoms and sidewalls of the copper wiring layer). *See* '324 patent at 2:2-15, 11:11-12, 14:62-65, 14:45-49, 15:9-14. The '324 patent also explains that "[i]n the diffusion-barrier film in accordance with ***the present invention***, ***a copper film makes direct contact with a crystalline metal film*** containing nitrogen therein, ensuring high adhesion therebetween and high crystallinity of a copper film." '324 patent at 6:32-36 (emphasis added). The '324 patent discloses a number of techniques, such as increasing the sputtering pressure, controlling the concentration of nitrogen gas, or switching the RF power, for covering the entire bottom and sidewalls of the recesses and holes, which the copper wiring layers occupy, with the claimed diffusion barrier film. *See* '324 patent at 7:13-22 ("The method of fabricating a

diffusion-barrier film employs...sputtering where a nitrogen-containing gas has a pressure equal to or greater than 5 Pa,…thus, there can be obtained coverage for ***entirely covering a recess or hole formed at a surface of a substrate, with the diffusion-barrier film***.”) (emphasis added), 12:33-42 (“As mentioned above, when the tantalum target is selected, a crystalline structure, composition and resistivity of a film to be formed by sputtering vary in dependence on both a concentration of nitrogen gas in sputtering gas and RF power. Conversely speaking, this means that it is possible to control characteristics of a film to be formed by sputtering, by controlling both a concentration of nitrogen gas in sputtering gas and RF power. The present invention is based on this discovery”); *see also id.* at 9:26-42, 11:1-34, 12:42-49. In addition, every embodiment illustrated in the patent shows the barrier film covering the entire sidewalls and bottom of the copper wiring layer. *See* ’324 patent at Figs. 4B-4D, 7-8, 23, 25-26, 30-31.

24. It is my opinion that the ’324 patent seeks to provide a solution to the problem of incomplete coverage for diffusion barrier films and that this solution requires the diffusion barrier film to cover the entire bottoms and sidewalls of the holes in which the copper wiring layer is deposited. This diffusion barrier film is comprised of a crystalline metal film, which serves to adhere the barrier film to the copper wiring layer, and an amorphous metal nitride film, which serves to prevent the diffusion of copper beyond the barrier film. *See* ’324 patent at 6:32-52.

25. In the “Summary of the Invention” section of the ’324 patent, the ’324 patent explains that the copper wiring layer must be formed on the diffusion barrier film and that the diffusion barrier film must cover a recess or hole that is subsequently filled with a copper wiring layer. *See* ’324 patent at 6:42-52 (explaining that “by ***forming a copper wiring layer on the diffusion-barrier film in accordance with the present invention***, it is possible to not only ensure

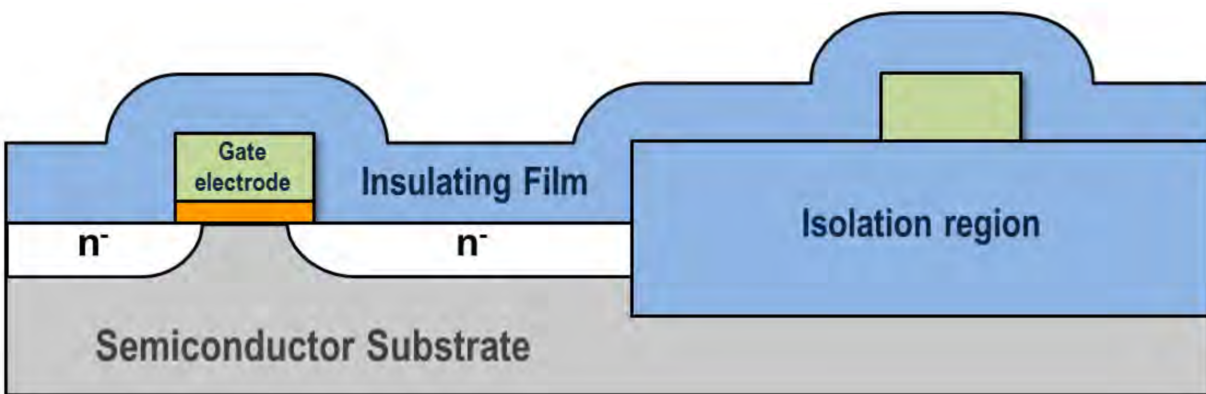
high crystallinity and high adhesion of a copper wiring layer, but also to prevent copper diffusion.") (emphasis added); *see also id.* at 7:39-44 ("Summary of Invention" section explaining that "***a thin copper film is formed on the diffusion-barrier film*** in vacuum. As a result, there is obtained a multi-layered structure comprised of the diffusion-barrier film and the copper wiring film without a metal oxide layer being sandwiched therebetween.") (emphasis added), 6:13-18 ("forming ***a diffusion-barrier film to cover the recess or hole*** therewith without exposing to atmosphere, the diffusion-barrier film having a multi-layered structure of first and second films, the first film being composed of crystalline metal containing nitrogen therein, the second film being composed of amorphous metal nitride…***forming a copper film on the diffusion-barrier film***") (emphasis added); *see also id.* at 7:19-22 ("thus, there can be obtained coverage for ***entirely covering a recess or hole*** formed at a surface of a substrate, ***with the diffusion-barrier film***.") (emphasis added). It is my opinion that such disclosures indicate that the invention claimed in the '324 patent requires the barrier film to cover the entire bottom and sidewalls of the copper wiring layer and that such coverage is not limited to a preferred embodiment of the '324 patent, though all of the preferred embodiments in the '324 patent illustrate a barrier film that covers the entire bottom and sidewalls of the copper wiring layer.

V. Analysis of the Isolation Region Patent ('950 patent)

a. "second sidewalls on a side surface of a step portion"

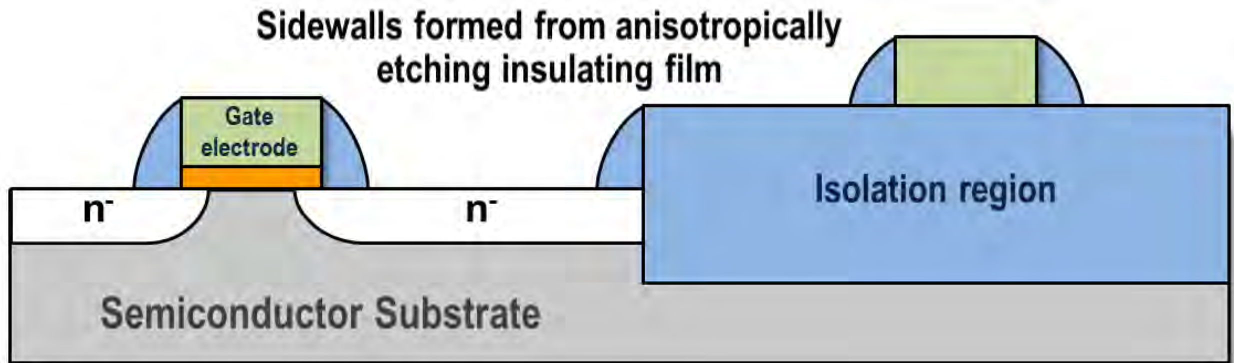
26. I have examined the '950 patent's term "second sidewalls on a side surface of a step portion" in claim 12. In my opinion, a person of ordinary skill in the art would understand this term to mean "second sidewalls substantially covering a side surface of a step portion" in view of the context of the claims, specification, and prosecution history.

27. A purpose of the step sidewall is to provide a gradual decrease in height from the raised isolation region to the top of the semiconductor substrate such that a metal layer (*e.g.*, an "interconnection" for electrically connecting transistors to make an electronic circuit) will not be disconnected when going from the raised isolation region down to the substrate. *See* '950 patent at 7:15-20 ("…the abrupt level difference between the surfaces of the isolation and the active area can be released by the step sidewall…[t]herefore…an upper interconnection is prevented from being disconnected and increasing in its resistance."). The step sidewall in the '950 patent provides a gradual decrease in height from the isolation region to the top of the semiconductor substrate because it is made from an insulating film, which has been deposited conformally over the entire semiconductor substrate, that is anisotropically etched. As shown in the image below, the insulating film follows the contour of the surface it is being deposited over; thus, the height (*i.e.* vertical dimension) of the insulating film adjacent to the step of the isolation region is larger than the height of the insulating film on the planar region (*i.e.*, on the substrate surface and on top of the isolation region).

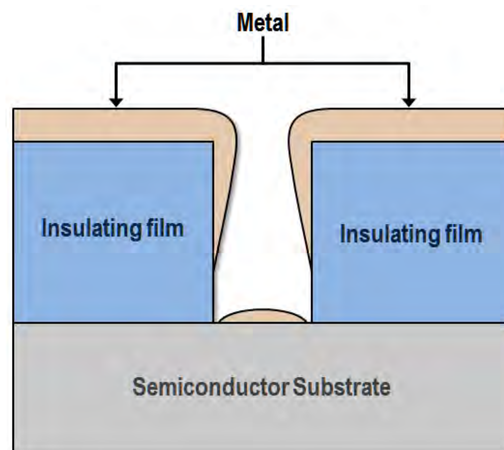


28. Next, the insulating film is anisotropically etched. "Anisotropically etched" means that the insulating film is etched directionally, *e.g.* it etches in the downward direction. Because the height of the insulating film adjacent to the step of the isolation region is larger than

the height of the insulating film on the planar region, when the insulating film on the planar region is etched away, a "rounded" sidewall remains adjacent to the step that gradually decreases in height from the raised isolation region to the top of the semiconductor substrate, for example, as shown in the image below.



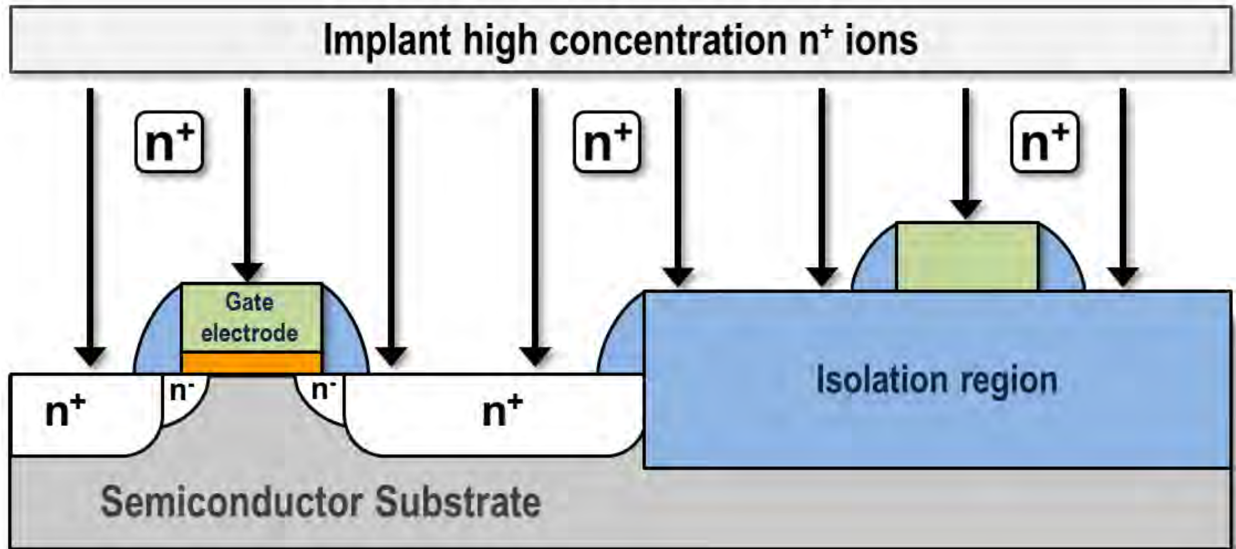
29. A sharp drop (as opposed to a gradual decline) from the top of the isolation region to the top of the semiconductor substrate can cause a disconnect in a metal layer formed over this drop because the thickness of the metal layer during deposition decreases as it crosses an abrupt step, for example, as shown in the image below.



30. This decrease in thickness can lead to high electrical resistance in metal lines and mechanical cracking and failure, *i.e.* a disconnect. On the other hand, if the decrease in height from the top of the isolation region to the top of the semiconductor substrate is more gradual, the

thickness of an overlying metal layer is more uniform during deposition. Thus, the step sidewall needs to substantially cover the step side surface of the isolation region to prevent a sharp drop from the top of the isolation region to the top of the semiconductor substrate, which would increase the resistance of or completely disconnect an overlying metal layer thereby degrading the performance or even causing a malfunction of the semiconductor device.

31. Another purpose of the step sidewalls, as evidenced by the claim language, is to insulate, as they are formed from an "insulating film." The '950 patent explains that "the step sidewall disposed at the edge of the trench isolation can prevent the impurity ions from being implanted below the edge of the isolation." '950 patent at 7:55-57; *see also id.* at 26:43-49, 27:49-54. In other words, the step sidewall acts as a buffer during the doping of the source and drain ("S/D") regions of a transistor that prevents the doping ions from being implanted below the isolation region, which could result in increased junction leakage current and power consumption. Ion implantation is a process by which ions of an impurity, such as phosphorus or boron, are accelerated into a semiconductor substrate, thereby changing the properties of the implanted regions (*e.g.*, doping concentration and electrical resistance). It is important to note that the ions are implanted over the entire semiconductor substrate. Thus, to dope a specific localized region, a mask is needed to block the ions from being implanted into certain portions the semiconductor substrate. The mask can be a photoresist, polysilicon, or an insulator, such as a sidewall. For example, as shown in the image below, the sidewalls are used to block the heavily doped n^+ ion implantation from encroaching underneath the gate electrode or isolation region.



32. As discussed above, the isolation region is used to prevent the transistors in a semiconductor device from electrically interfering with each other. In other words, the isolation region serves to minimize any leakage current between transistors through the semiconductor substrate. Lower leakage current means lower power consumption for the semiconductor device. The effectiveness of the isolation region depends on the impurity concentration below the isolation region such that any unintended implantation of doping ions below the isolation region can result in increased junction leakage and power consumption. If the sidewall does not substantially cover the side surface of the isolation region step, impurity ions can be implanted below the isolation region. Thus, the sidewalls need to substantially cover the side surface of a step portion of the isolation region in order to prevent doping ions from being implanted below the isolation region.

33. The '950 patent further explains that "the step sidewall can prevent the silicide layer from being formed at a deep portion" of the isolation region. '950 patent at 7:59-60; *see also id.* at 23:56-63. In other words, when forming silicide over the source/drain ("S/D") region of the transistor, the step sidewall can prevent the silicide from being formed in the boundary

between the silicon substrate and the isolation region, which can effectively prevent a short circuit from occurring between the S/D electrode and the channel stop region. Silicide is a highly conductive layer of compound material composed of silicon and metal. For example, $TiSi_2$ is a titanium-silicon compound called titanium silicide; and likewise, WSi_2 (tungsten silicide) is another common silicide used in semiconductor devices. Silicides are used in semiconductor technology to reduce the resistance of polysilicon lines and dopant regions. They are also used to form a better contact (*i.e.*, lower resistance) between a semiconductor region and a metal layer. A common method of forming a silicide layer in semiconductor devices is by chemical reaction. First, a metal, such as titanium, is deposited over the entire semiconductor substrate. The semiconductor substrate is then annealed at a high temperature, which causes silicide to form wherever the semiconductor and metal are in contact, for example, on the source/drain regions of the transistors. The unreacted metal, such as the titanium on the top of the isolation region, is then selectively etched away. If the sidewall does not substantially cover the side surface of the isolation region, silicide can be formed at the boundary between the isolation region and the semiconductor substrate, which can cause a short circuit from between the source/drain electrode and the semiconductor region under the isolation region, commonly referred to as the “channel stop region.” This short-circuit can cause the semiconductor device to malfunction. Thus, the sidewalls need to substantially cover the side surface of a step portion of the isolation region in order to prevent silicide from forming at the boundary between the isolation region and the semiconductor substrate.

34. Every embodiment in the ’950 patent illustrates that etching the insulating film to form sidewalls results in sidewalls covering the entire side surface of either the gate electrode or

step portion of the isolation. *See* '950 patent at Figs. 3(c), 4(a), 5(a), 6(c), 7(a), 9(a), 10(a), 11(a), 12, 13(e), 14(d), 15(c), 16(b), 17, 18(a), 19, 20(e), 21(a)).

35. It is my opinion that a person of ordinary skill in the art would reasonable understand the scope of sidewalls that substantially cover the side surface of a step portion of a boundary between a trench isolation and an active area in light of the specification and prosecution history of the '950 patent.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed at Austin, TX on September 26, 2018.

Jack C. Lee, Ph.D.

Jack C. Lee is a Professor of the Electrical and Computer Engineering Department and holds the Cullen Trust for Higher Education Endowed Professorship in Engineering # 4 at The University of Texas at Austin. He received the B.S. and M.S. degrees in electrical engineering from University of California, Los Angeles, in 1980 and 1981, respectively; and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1988. From 1979 to 1984, he was a Member of Technical Staff at the TRW Microelectronics Center, CA, in the High-Speed Bipolar Device Program. He worked on bipolar device and circuit design, fabrication and testing. In 1988, he joined the faculty of The University of Texas at Austin. His current research and teaching interests include semiconductor device (i.e. MOSFETs) fabrication processes and packaging, characterization and modeling, dielectric process, characterization and reliability, high-K gate dielectrics and electrode, semiconductor memory applications, and alternative channel materials. Dr. Lee has over 30 years of experience in semiconductor technology and dielectric processing and over 2 years of industrial and commercial experience (1981-1984). Furthermore, he has been consulting with several semiconductor companies. He has published over 550 journal publications and conference proceedings and several patents; and co-authored 6 book and book chapters on semiconductor devices. He has also been recognized with many teaching and research awards including the prestigious SRC Inventor Recognition Award from Semiconductor Research Corporation for his work on dielectric technology and characterization. Dr. Lee is a Fellow of IEEE and has been a Distinguished Lecturer for the IEEE Electron Devices Society.

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Professor, Department of Electrical and Computer Engineering
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Associate Professor, Department of Electrical and Computer Engineering
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Ph.D. in Electrical Engineering, University of California at Berkeley,
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Selected Awards

IEEE Electron Devices Society Distinguished Lecturer, 2004 - 2016.

Fellow, The Institute of Electrical and Electronic Engineers (IEEE), 2002 “For contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices”

Gordon Lepley IV Endowed Memorial Teaching Award, ECE Department, The University of Texas at Austin, 2004
Cullen Trust For Higher Education Endowed Professorship in Engineering, 2000-
Dean's Fellow, College of Engineering, The University of Texas at Austin, 1999, 2003
Lockheed Fort-Worth Division Award for Excellence in Engineering Teaching, College of Engineering, The University of Texas at Austin, 1996
Award of Excellence, Halliburton Foundation, 1993
Departmental Teaching Award, College of Engineering, The University of Texas at Austin, 1993
SRC Inventor Recognition Award, Semiconductor Research Corporation, 1991
Hughes Aircraft Company Endowed Faculty Fellowship in Engineering, The University of Texas at Austin, 1991- 2000
Outstanding Engineering Teaching by an Assistant Professor, College of Engineering, The University of Texas at Austin, 1991
Best Paper Award, SEMATECH Centers of Excellence Coordination Meeting, 1990.
Dow Outstanding Young Faculty Award, American Society for Engineering Education, 1990
Engineering Research Initiation Award, Engineering Foundation of the United Engineering Trustees, 1989
Best Paper Award, IEEE International Reliability Physics Symposium, 1988

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