IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

GODO KAISHA IP BRIDGE 1,	)	
	)	
Plaintiff,	)	
	)	
v.	)	C.A. No. 16-290 (MN)
	)	
OMNIVISION TECHNOLOGIES, INC.	)	
	)	
Defendant.	)	

APPENDIX IN SUPPORT OF THE JOINT CLAIM CONSTRUCTION BRIEF

Plaintiff Godo Kaisha IP Bridge 1 and Defendant OmniVision Technologies, Inc. submit this appendix in support of the Joint Claim Construction Brief as follows:

Description	App.
US Patent No. 8,084,796 B2 to Mori, et al.	App. 0001-0021
April 6, 2011 Amendment in '796 patent file history	App. 0022-0029
September 11, 2011 Notice of Allowability in '796 patent file history	App. 0030-0032
US Patent No. 8,106,431 B2 to Mori, et al.	App. 0033-0053
December 15, 2010 Amendment in '431 patent file history	App. 0054-0063
May 12, 2010 Amendment in '431 patent file history	App. 0064-0073
September 30, 2011 Notice of Allowability in '431 patent file history	App. 0074-0076
US Patent No. 8,378,401 B2 to Mori, et al.	App. 0077-0099
August 27, 2012 Amendment in '401 patent file history	App. 0100-0112
November 14, 2012 Notice of Allowability in '401 patent file history	App. 0113-0115
US Patent No. 7,436,010 B2 to Mori, et al.	App. 0116-0137
May 8, 2006 Amendment in '010 patent file history	App. 0138-0156

October 24, 2006 Amendment in ’010 patent file history	App. 0157-0174
March 29, 2007 Amendment in ’010 patent file history	App. 0175-0187
September 24, 2007 Amendment in ’010 patent file history	App. 0188-0201
March 21, 2008 Amendment in ’010 patent file history	App. 0202-0212
US Patent No. 6,160,281 to Guidash	App. 0213-0227
US Patent No. 6,310,366 B1 to Rhodes, et al.	App. 0228-0243
US Patent No. 6,794,677 to Tamaki, et al.	App. 0244-0264
January 22, 2004 Amendment in ’677 patent file history	App. 0265-0269
US Patent No. 6,709,950 B2 to Segawa, et al.	App. 0270-0308
January 15, 2003 Amendment in ’950 patent file history	App. 0309-0326
October 24, 2003 Amendment in ’950 patent file history	App. 0327-0338
November 6, 2003 Notice of Allowability in ’950 patent file history	App. 0339-0340
US Patent No. 6,538,324 B1 to Tagami, et al.	App. 0341-0371
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June 11, 2002 Response/Remarks in ’324 patent file history	App. 0379-0382
August 9, 2002 Amendment in ’324 patent file history	App. 0383-0390
September 10, 2002 Notice of Allowability in ’324 patent file history	App. 0391-0393
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US Patent No. 5,942,774 to Isogai, et al.	App. 0442-0473

Respectfully Submitted,

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US008084796B2

(12) **United States Patent**
Mori et al.

(10) **Patent No.: US 8,084,796 B2**
(45) **Date of Patent: Dec. 27, 2011**

(54) **SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME**

(75) Inventors: **Mitsuyoshi Mori**, Kyoto (JP); **Takumi Yamaguchi**, Kyoto (JP); **Takahiko Murata**, Osaka (JP)

(73) Assignee: **Panasonic Corporation**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 465 days.

(21) Appl. No.: **12/202,804**

(22) Filed: **Sep. 2, 2008**

(65) **Prior Publication Data**

US 2009/0002538 A1 Jan. 1, 2009

Related U.S. Application Data

(63) Continuation of application No. 10/706,918, filed on Nov. 14, 2003, now Pat. No. 7,436,010.

(30) **Foreign Application Priority Data**

Feb. 13, 2003 (JP) 2003-034692

(51) **Int. Cl.**
H01L 31/062 (2006.01)

(52) **U.S. Cl.** .. **257/292**; 257/223; 257/445; 257/E27.139

(58) **Field of Classification Search** 257/223, 257/258, 291, 292, 443–445
See application file for complete search history.

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Primary Examiner — Wael Fahmy
Assistant Examiner — John C Ingham
(74) *Attorney, Agent, or Firm* — McDermott Will & Emery LLP

(57) **ABSTRACT**

A solid state imaging apparatus includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. Charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

4 Claims, 10 Drawing Sheets

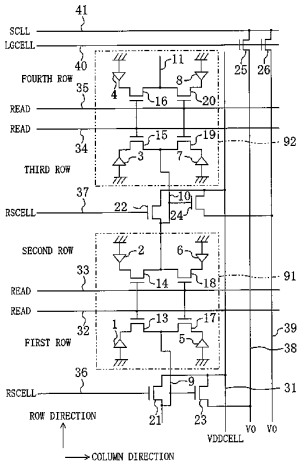

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FIG. 1

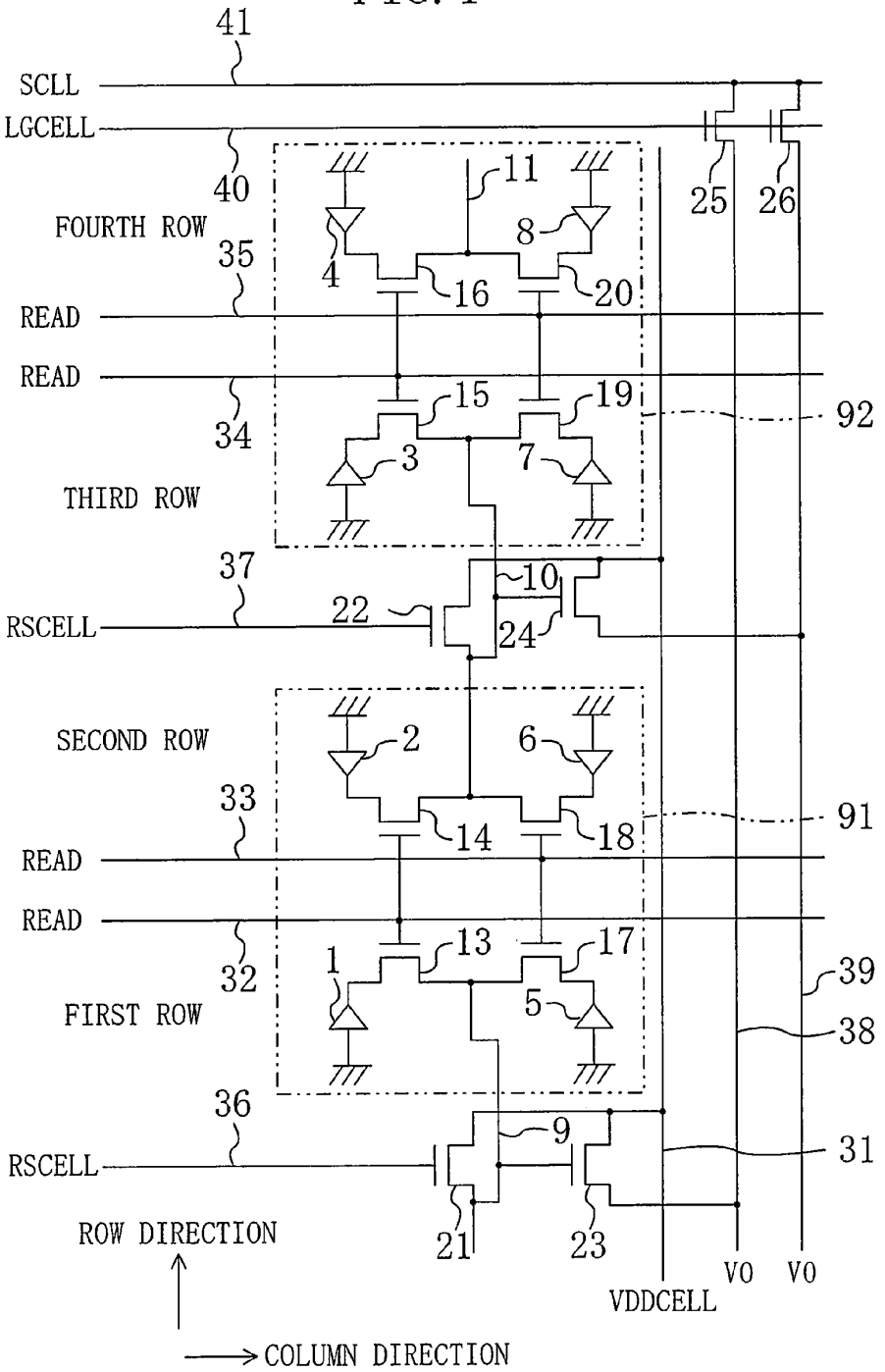

41
SCLL
LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
33
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
2
6
14
18
91
13
17
1
5
39
38
9
31
21
23
VO
VO
VDDCELL

FIG. 2

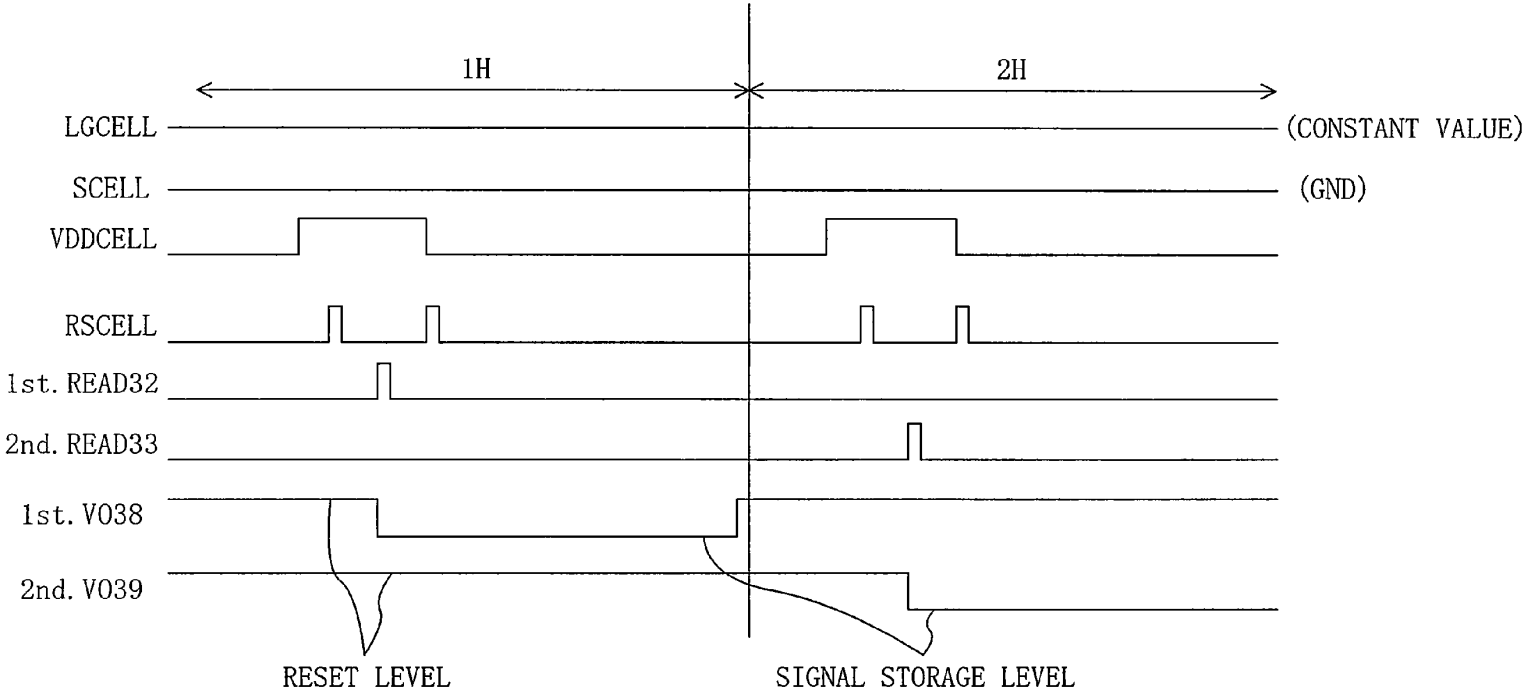

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
RSCELL
1st. READ32
2nd. READ33
1st. V038
2nd. V039
RESET LEVEL
SIGNAL STORAGE LEVEL

FIG. 3

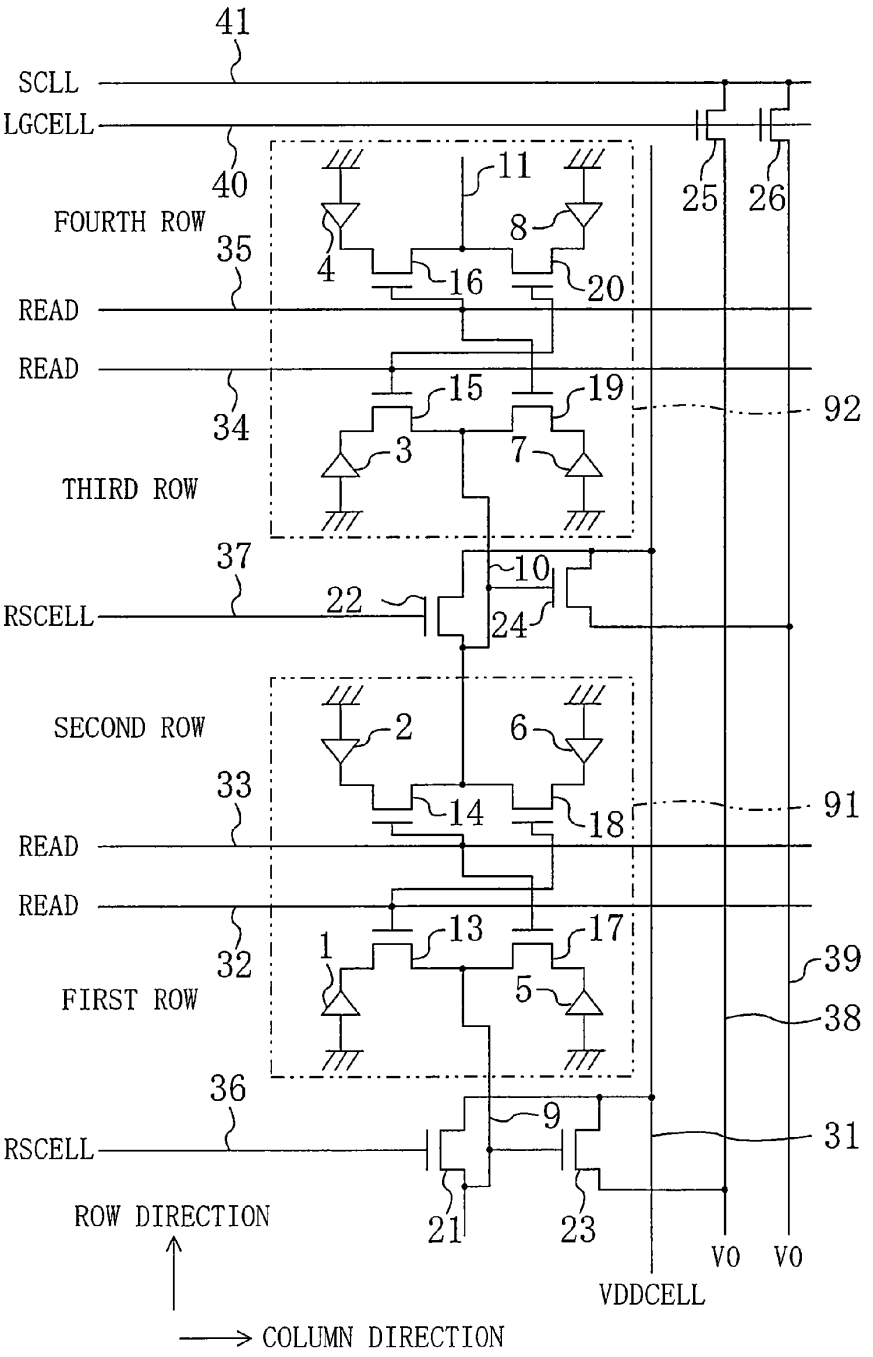

41
SCLL
LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
33
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
2
6
14
18
91
1
13
17
39
5
38
9
31
21
23
VO
VO
VDDCELL

FIG. 4

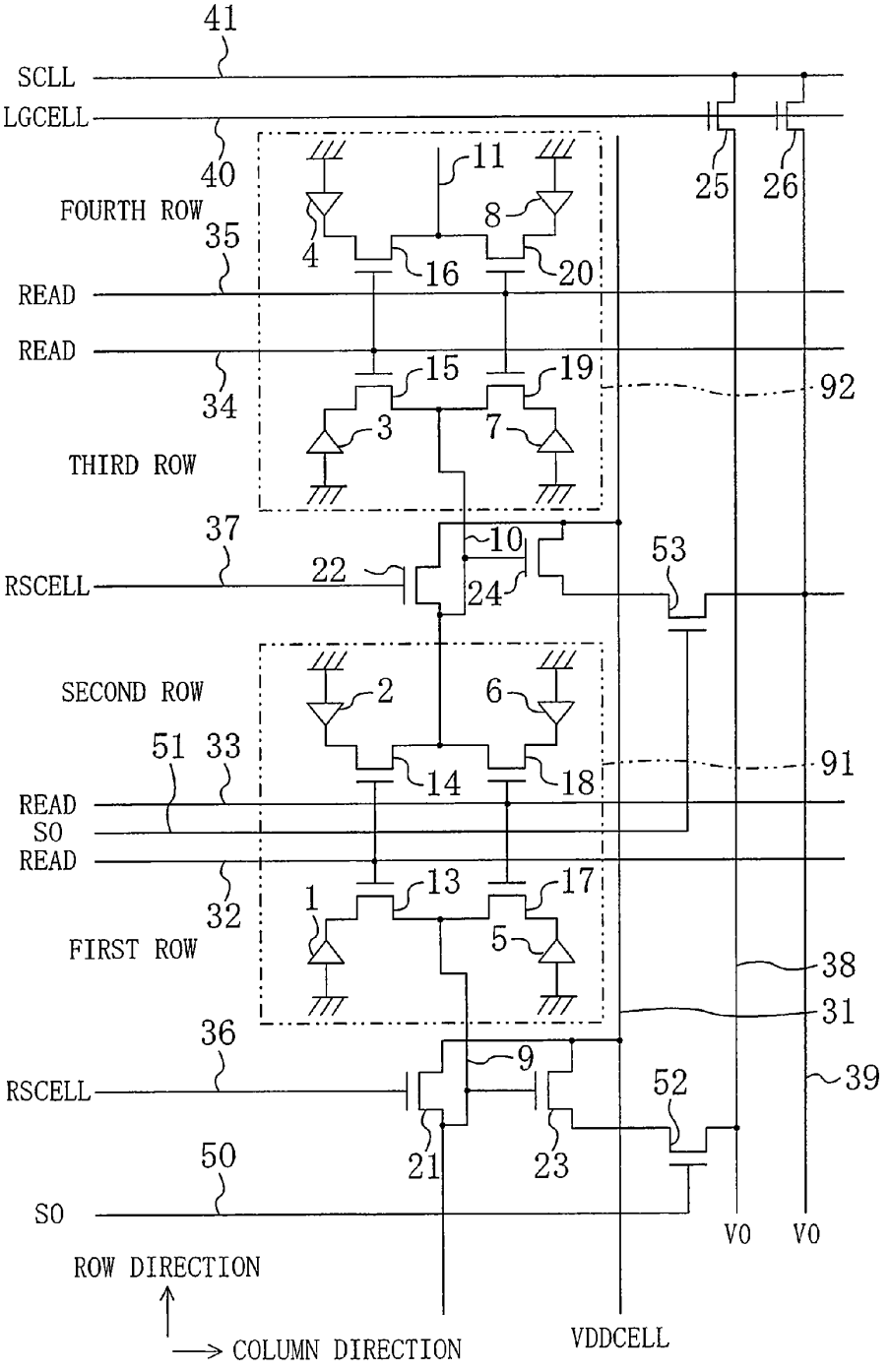

41
SCLL
LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
51
33
READ
SO
READ
32
FIRST ROW
36
RSCELL
50
SO
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
15
19
3
7
10
22
24
53
2
6
14
18
1
13
17
5
9
21
23
52
25
26
92
91
38
31
39
VO
VO
VDDCELL

FIG. 5

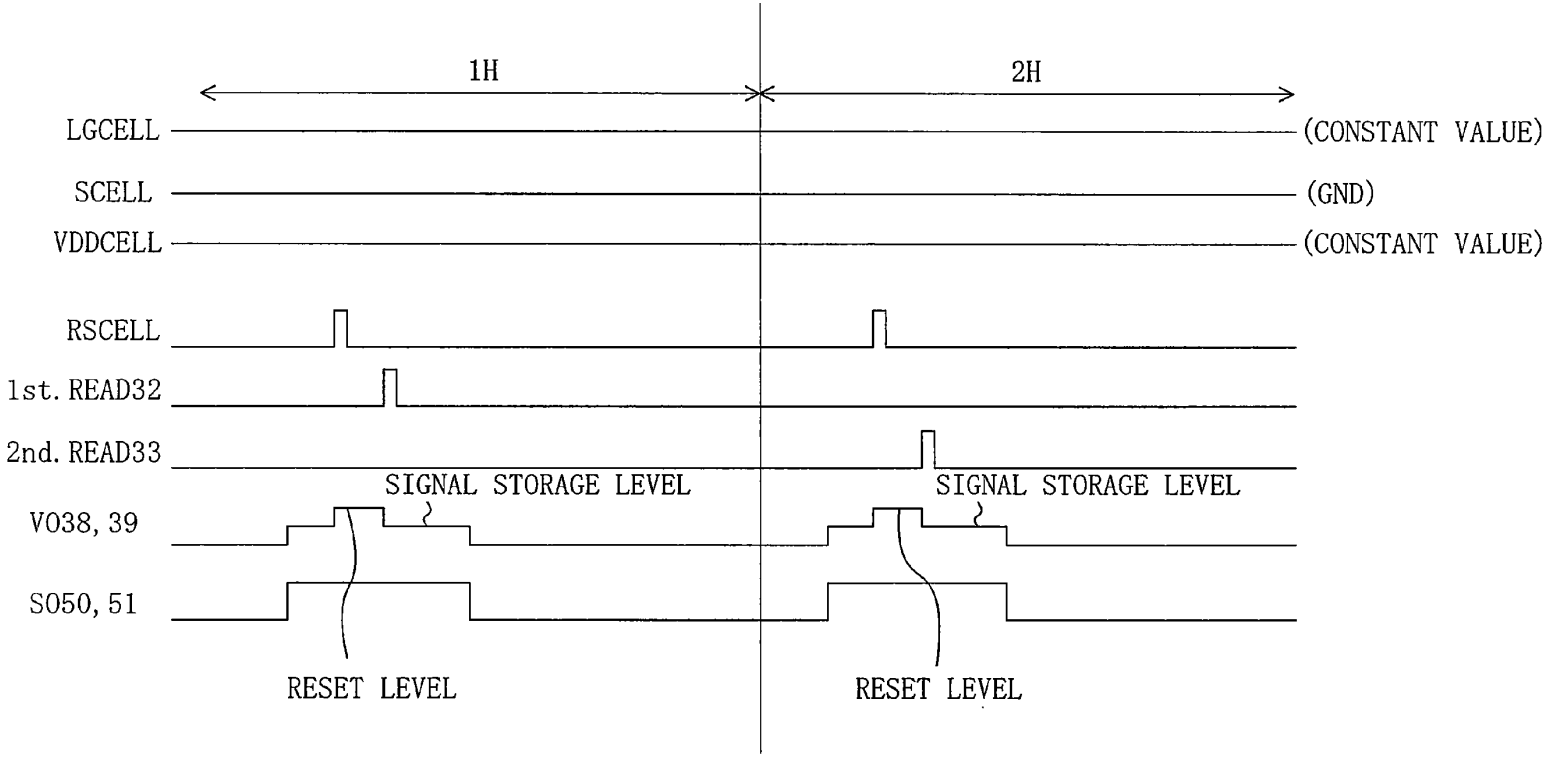

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
(CONSTANT VALUE)
RSCELL
1st. READ32
2nd. READ33
SIGNAL STORAGE LEVEL
SIGNAL STORAGE LEVEL
VO38, 39
SO50, 51
RESET LEVEL
RESET LEVEL

FIG. 6

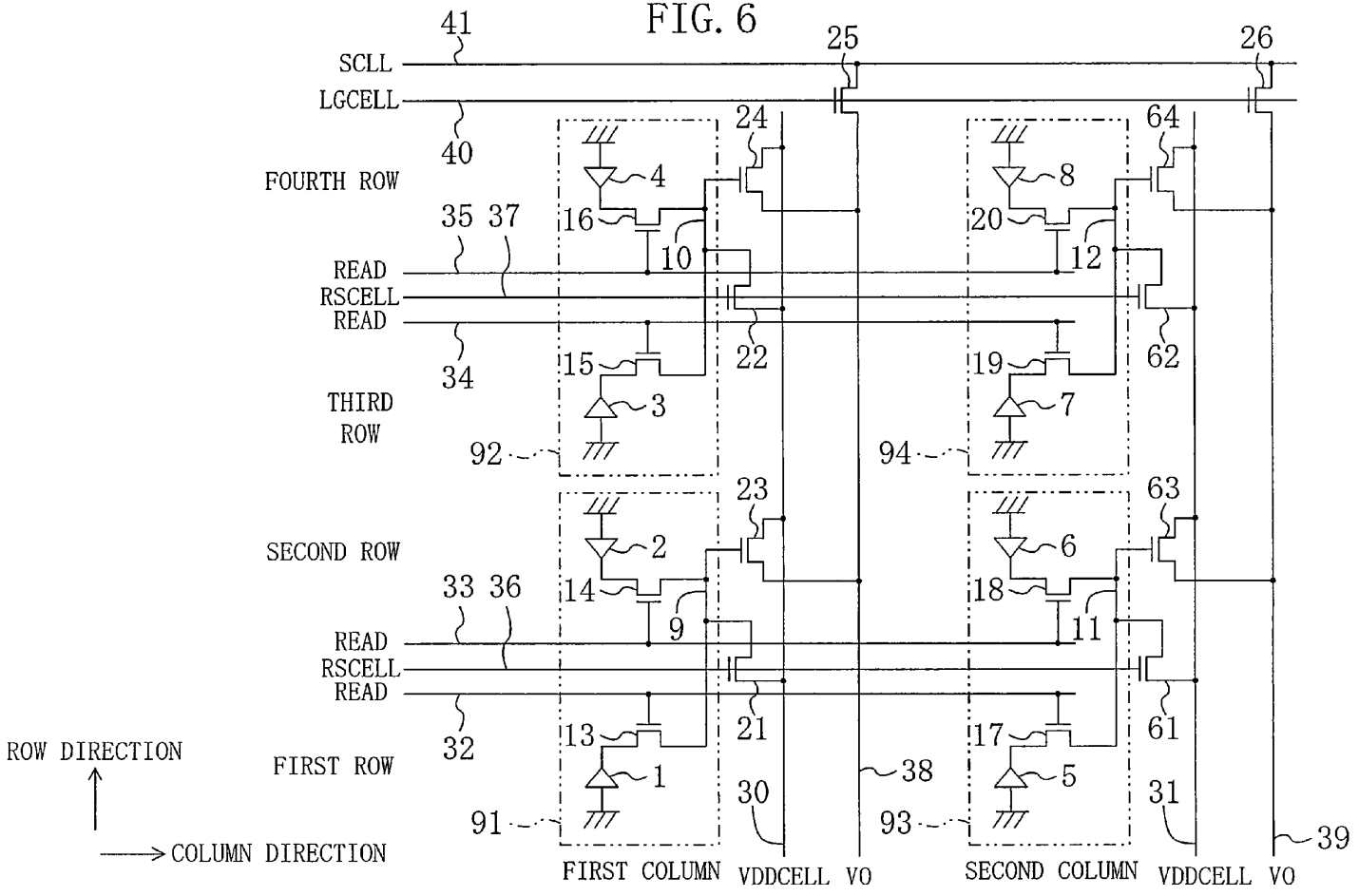
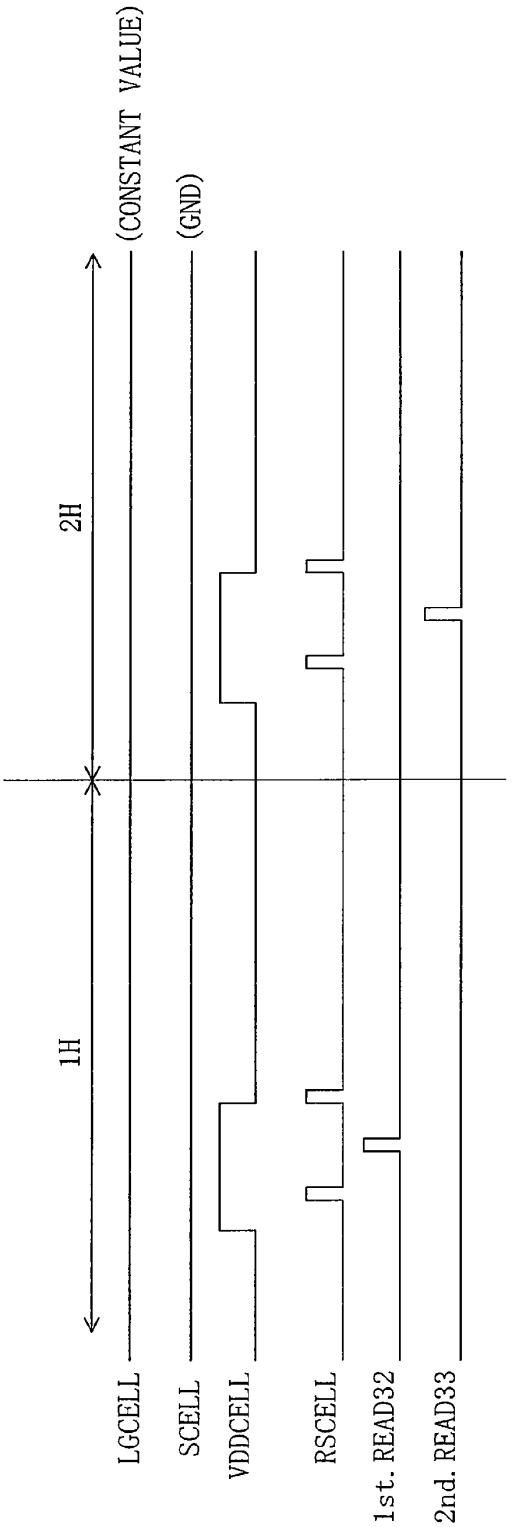

41
SCLL
LGCELL
40
FOURTH ROW
35 37
READ
RSCELL
READ
34
THIRD ROW
92
SECOND ROW
33 36
READ
RSCELL
READ
32
FIRST ROW
91
ROW DIRECTION
COLUMN DIRECTION
25
26
24
64
4
8
16
20
10
12
22
62
15
19
3
7
94
23
63
2
6
14
18
9
11
21
61
13
17
1
5
30
38
93
31
39
FIRST COLUMN
VDDCELL VO
SECOND COLUMN
VDDCELL VO

FIG. 7


(CONSTANT VALUE)
(GND)
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1H
LGCELL
SCELL
VDDCELL
RSCELL
1st. READ32
2nd. READ33

FIG. 8

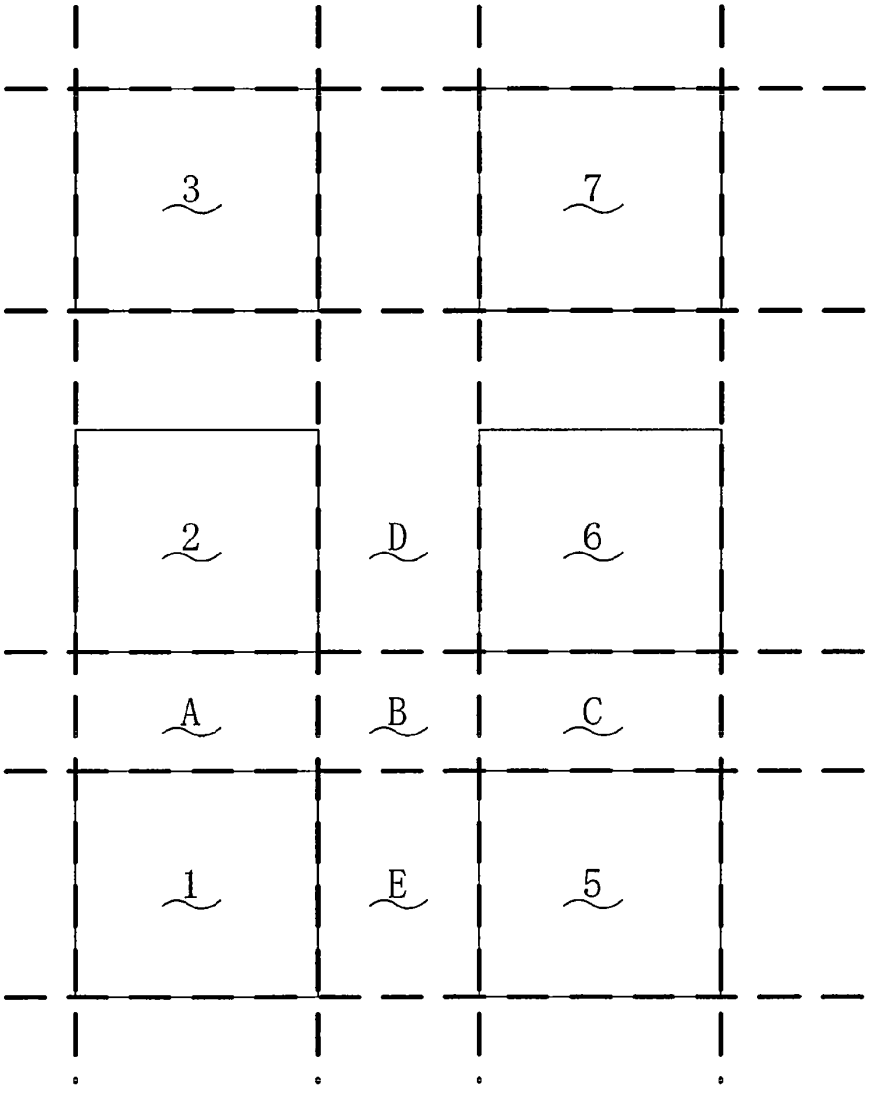
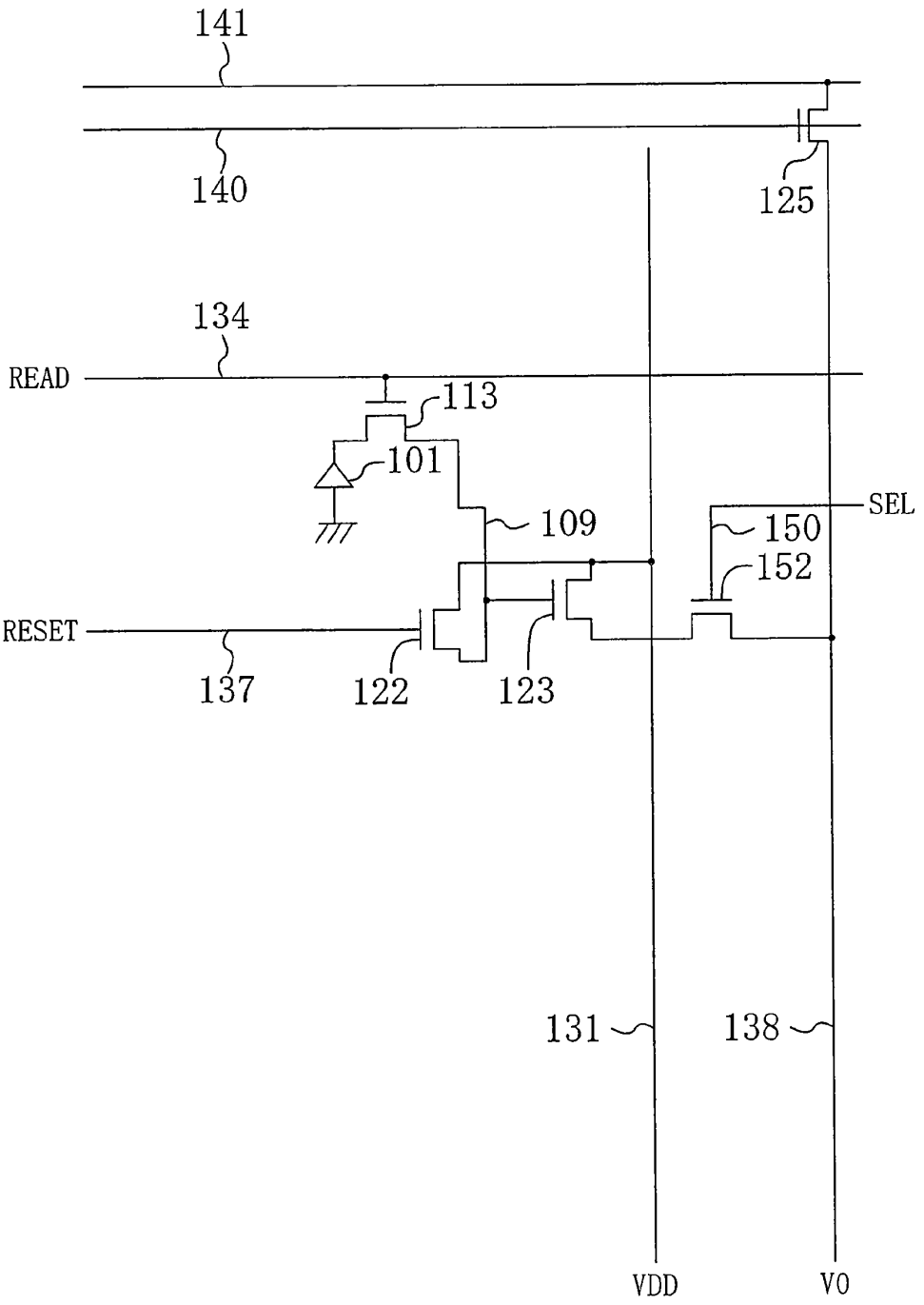


FIG. 9

FD SECTION	PIXEL AMPLIFIER	RESET GATE	APERTURE RATIO
A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	10%
		D REGION、B REGION、E REGION	25%
	D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	35%
D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	20%
	D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	20%

FIG. 10

PRIOR ART



SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

RELATED APPLICATIONS

This application is a Continuation of U.S. application Ser. No. 10/706,918, filed Nov. 14, 2003 now U.S. Pat. No. 7,436,010, claiming priority of Japanese Application No. 2003-034692, filed Feb. 13, 2003, the entire contents of each of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a solid state imaging apparatus in which a plurality of photoelectric conversion sections are arranged in an array, a method for driving the solid state imaging apparatus and a camera using the solid state imaging apparatus.

FIG. **10** is a diagram illustrating a general circuit configuration for a MOS type image sensor, i.e., a known solid imaging apparatus (e.g., see M. H. White, D. R. Lange, F. C. Blaha and I. A. Mach, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels", IEEE J. Solid-State Circuits, SC-9, pp. 1-13 (1974)).

As shown in FIG. **10**, a photoelectric conversion cell includes a photodiode (PD) section **101**, a transfer transistor **113**, a reset transistor **122**, a pixel amplifier transistor **123**, a select transistor **152**, a floating diffusion (FD) section **109**, a power supply line **131** and an output signal line **138**.

The PD section **101** of which the anode is grounded is connected to the drain of the transfer transistor **113** at the cathode. The source of the transfer transistor **113** is connected to the respective sources of the FD section **109**, the gate of the pixel amplifier transistor **123** and the source of the reset transistor **122**. The gate of the transfer transistor **113** is connected to a read-out line **134**. The reset transistor **122** which receives a reset signal **137** at the gate includes a drain connected to the drain of the pixel amplifier transistor **123** and the power supply line **131**. The source of the pixel amplifier transistor **123** is connected to the drain of the select transistor **152**. The select transistor **152** receives a selection signal SEL at the gate and includes a source connected to the output signal line **138**.

The output signal line **138** is connected to the source of a load gate **125**. The gate of the load gate **125** is connected to a load gate line **140** thereof and the drain is connected to a source power supply line **141**.

In this configuration, a predetermined voltage is applied to the load gate line **140** so that the load gate **125** becomes a constant current source, and then the transfer transistor **113** is temporarily turned ON to transfer charge photoelectric-converted in the PD section **101** to the FD section **109**. Then, the potential of the PD section **101** is detected by the pixel amplifier transistor **123**. In this case, by turning the select transistor **152** ON, signal charge can be detected through the output signal line **138**.

However, in the known solid state apparatus, four transistors **113**, **122**, **123** and **152** and five lines **131**, **134**, **137**, **138** and **150** are required for total in each photoelectric conversion cell. Accordingly, the areas of transistor and line sections in a cell are increased. For example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD section **101** to the photoelectric conversion cell is only about 5%. Therefore, it is difficult to ensure a sufficiently large area of opening of the PD section **101** and also to reduce the size of the photoelectric conversion cell.

SUMMARY OF THE INVENTION

It is an object of the present invention to solve the above-described problems and, to reduce, in a FDA (floating diffusion amplifier) system, the size of a photoelectric conversion cell while increasing an aperture area of a photoelectric conversion section.

To achieve the above-described object, the present invention has been deviced, so that a configuration in which a transistor and an interconnect can be shared by a plurality of photoelectric conversion (PD) sections is used in a solid state imaging apparatus.

Specifically, a first solid sate imaging apparatus includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections which are included in the same row; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. In the apparatus, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

In the first solid imaging apparatus, each said floating diffusion section is shared by ones of the photoelectric conversion sections included in the same row, and furthermore, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections. Thus, the number of read-out lines per photoelectric conversion cell becomes 0.5. As a result, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in the same column. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in the same column can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

Moreover, in the first solid state imaging apparatus, it is preferable that wherein each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in two adjacent columns, respectively. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in two adjacent columns, respectively, can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by a row which is read out by a transfer transistor connected to one of the read-out line and another row which is adjacent to the read-out row.

It is preferable that the first solid state imaging apparatus further includes: a signal line for outputting a signal from each said pixel amplifier transistor to the outside; and a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line. Thus, charges from one of the photoelectric conversion sections which are included in adjacent rows, respectively, can be detected through a shared signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by photoelectric conversion sections which are adjacent to each other in the row direction or in the column direction. Thus, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that in each said floating diffusion section, a reset section for resetting charge stored in the floating diffusion section is provided. Thus, it is possible to stop, after charge read out from a photoelectric conversion section has been detected by an amplifier, detection of charge by the pixel amplifier transistor.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction. Thus, a high quality image can be obtained from signals read out from the photoelectric conversion sections.

It is preferable that the first solid state imaging apparatus further includes a signal processing circuit for processing an output signal from each said pixel amplifier transistor. Thus, a high quality image can be obtained.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film. Thus, a power supply line can be formed in a different interconnect layer from an interconnect layer in which an output signal line connected to a pixel amplifier transistor is formed. Therefore, the size of a photoelectric conversion cell can be further reduced and also the aperture area can be increased.

A method for driving a solid state imaging apparatus according to the present invention is directed to a method for driving the first solid state imaging apparatus of the present invention and includes: a first step of transferring, in each said photoelectric conversion cell, by a first read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which are not included in the same row but included in two columns adjacent to each other, respectively, to one of the floating diffusion sections connected to said ones of the photoelectric conversion sections; and a second step of transferring, by a second read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which have not been read out in the first step to the same floating diffusion section connected to said ones of the photoelectric conversion sections as that in the first step.

A second solid state imaging apparatus according to the present invention includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows; a plurality of floating diffusion sections each being connected, via each of a plurality of transfer transistors, to each of ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same column in each said photoelectric conversion cell, and each being shared by said ones of the photoelectric conversion sections; a plurality of read-out lines each being connected to one of the transfer transistors and independently reading out charge from each of said ones of the photoelectric conversion sections to each said floating diffusion section shared by said ones of the photoelectric conversion sections; and a plurality of pixel amplifier transistors each detecting and outputting the potential of the floating diffusion section.

In the second solid state apparatus, each said floating diffusion section is connected to some of the plurality of transfer transistors, is shared by ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same. Furthermore, some of the plurality of read-out lines each independently reading out charge from each of said ones of the photoelectric conversion sections are connected to each said transfer transistor. Thus, a row-select transistor which is usually provided is not needed. As a result, the number of interconnects per photoelectric conversion section is reduced from 5 to 3.5. Therefore, the area of the photoelectric conversion cell itself can be reduced while increasing the area of the photoelectric sections.

It is preferable that the second solid state imaging apparatus further includes a reset transistor for resetting charge stored in each said floating diffusion section and the drain of the reset transistor is connected to the drain of the pixel amplifier transistor so that a drain is shared by the reset transistor and the pixel amplifier transistor. Thus, an interconnect connecting between the drain of the reset transistor and the drain of the pixel amplifier transistor can be shared. Accordingly, the number of interconnects per the photoelectric conversion cell can be further reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion sections which are adjacent to each other in the row direction in each said photoelectric conversion cell. Thus, the area of floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and a gate of the MIS transistor is arranged in the column direction. Thus, each said the read-out line can be also function as an interconnect of a transfer transistor, so that the area of the read-out lines occupying the photoelectric conversion cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the area of the pixel amplifier transistor per photoelectric conversion cell can be reduced whereas the area of the photoelectric conversion sections can be increased. Therefore, light sensitivity is increased.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor and each said floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect connecting between the pixel amplifier transistor and the floating diffusion section can be shortened, so that the areas of the pixel amplifier transistor and the floating diffusion section per photoelectric conversion cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between ones of the photoelectric cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so as to

have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

Moreover, in the second solid state imaging apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and each said pixel amplifier transistor is arranged between respective gates of the MIS transistor and another MIS transistor. Thus, an empty region located in an area of the cell in which a row and a column intersect to each other can be utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the area of the reset transistors per photoelectric conversion section can be reduced. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said pixel amplifier transistor and the floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect between the floating diffusion section can be omitted and the source of the reset transistor and the floating diffusion section can be connected to each other to be shared. Therefore, the areas of the reset transistors and the floating diffusion sections per photoelectric conversion cell can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is connected to a line arranged between ones of the photoelectric cells which are adjacent to each other in the row direction. Thus, pitches of the photoelectric sections in row directions can be matched in a simple manner, so that resolution is improved.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so as to have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

In this case, it is preferable that each said transfer transistor is made of an MIS transistor, and each said reset transistor is arranged between respective gate of the MIS transistor and another MIS transistor. Thus, an empty region located in an area of the cell in which a row and a column intersect to each other can be utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, the area of the floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in at least one of the row direction and the column direction. Thus, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that the line connecting respective drains of the reset transistor and the pixel amplifier transistor also functions as a light-shielding film. Thus, the number of interconnects per photoelectric conversion cell can be reduced. Therefore, the area of the photoelectric sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

It is preferable that each of the first and second solid state imaging apparatus further includes a signal processing circuit for processing an output signal output from each said pixel amplifier transistor. Thus, a high resolution image can be obtained.

A camera according to the present invention includes the first or second solid state imaging apparatus of the present invention. Thus, the camera of the present invention can achieve a high resolution image.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a first embodiment of the present invention.

FIG. **2** is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment.

FIG. **3** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment.

FIG. **4** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a second embodiment of the present invention.

FIG. **5** is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment.

FIG. **6** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention.

FIG. **7** is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment.

FIG. **8** is a plane view schematically illustrating a layout of the photoelectric conversion cell in the solid state imaging apparatus of the third embodiment.

FIG. **9** is a table showing the aperture ratio of PD sections to a photoelectric conversion cell in each of regions A through E of FIG. **8** where a transistor and the like are arranged.

FIG. **10** is a circuit diagram illustrating a photoelectric conversion cell in a known solid imaging apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

A first embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **1** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to the first embodiment of the present invention.

As shown in FIG. **1**, for example, photoelectric conversion (PD) sections **1**, **2**, **3** and **4** each of which is made of a photodiode and converts incident light to electric energy are arranged in this order in the row direction. Furthermore, PD sections **5**, **6**, **7** and **8** are arranged in this order in the row direction so that the PD sections **5**, **6**, **7** and **8** are adjacent to the PD sections **1**, **2**, **3** and **4**, respectively, in the column direction.

Here, in this application, the row direction means to be the direction in which a row number increases and the column direction means to be the direction in which a column number increases.

Between the first and 0^{th} rows (not shown), a first floating diffusion (FD) section **9** for storing photoelectric-converted charges from the PD sections **1** and **5** included in the first row and PD sections included in the 0^{th} row is provided. Between the second and third rows, a second floating diffusion section **10** for storing photoelectric-converted charges from the PD sections **2** and **6** included in the second row and the PD sections **3** and **7** included in the third row is provided so as to be surrounded by the PD sections **2**, **3**, **6** and **7**. Between the fourth and fifth rows (not shown), a third floating diffusion section **11** for storing photoelectric-converted charges from the PD sections **4** and **8** included in the fourth row and PD sections included in the fifth row is provided. In this manner, each of the FD sections **9**, **10** and **11** is shared by four PD sections.

In this case, a cell including the PD sections **1**, **2**, **5** and **6** is a first photoelectric conversion cell **91** and a cell including the PD sections **3**, **4**, **7** and **8** is a second photoelectric conversion cell **92**.

In the first photoelectric conversion cell **91**, a transfer transistor **13** made of an N channel FET for transferring charge from the PD section **1** to the first FD section **9** is connected between the PD section **1** included in the first row and the first FD section **9**, and a transfer transistor **17** made of an N channel FET for transferring charge from the PD section **5** to the first FD section **9** is connected between the PD section **5** and the first FD section **9**.

Moreover, in the first photoelectric conversion cell **91**, a transfer transistor **14** made of an N channel FET for transferring charges from the PD section **2** to the second FD section **10** is connected between the PD section **2** included in the second row and the second FD section **10**, and a transfer transistor **18** made of an N channel FET for transferring charges from the PD section **6** to the second FD section **10** is connected between the PD section **6** and the second FD section **10**.

As a characteristic of the first embodiment, the transfer transistor **13** included in the first row and the transfer transistor **14** included in the second row are connected to a first read-out (READ) line **32** while the transfer transistor **17** included in the first row and the transfer transistor **18** included in the second row are connected to a second READ line **33**.

In the second photoelectric conversion cell **92**, a transfer transistor **15** made of an N channel FET for transferring charge from the PD section **3** to the second FD section **10** is connected between the PD section **3** included in the third row and the second FD section **10**, and a transfer transistor **19** made of an N channel FET for transferring charge from the PD section **7** to the second FD section **10** is connected between the PD section **7** and the second FD section **10**.

Moreover, in the second photoelectric conversion cell **92**, a transfer transistor **16** made of an N channel FET for transferring charges from the PD section **4** to the third FD section **11** is connected between the PD section **4** included in the fourth row and the third FD section **11**, and a transfer transistor **20** made of an N channel FET for transferring charges from the PD section **8** to the third FD section **11** is connected between the PD section **8** and the third FD section **11**.

Also, in this cell, the transfer transistor **15** included in the third row and the transfer transistor **16** included in the fourth row are connected to the third READ line **34** while the transfer transistor **19** included in the third row and the transfer transistor **20** are connected to the fourth READ line **35**.

To the first FD section **9**, a first reset transistor **21** made of an N channel FET is connected. The first reset transistor **21** includes a source connected to the first FD section **9**, a drain connected to a photoelectric conversion cell power supply (VDDCELL) line **31** and a gate connected to a first reset pulse (RSCELL) line **36**. Thus, charge stored in the first FD section **9** is made to flow through the VDDCELL line **31** by a RSCELL signal.

In the same manner, a second reset transistor **22** made of an N channel FET is connected to the second FD section **10**. The second reset transistor **22** includes a source connected to the second FD section **10**, a drain connected to the VDDCELL line **31** and a gate connected to a second RSCELL line **37**. Note that although not shown in FIG. **1**, a reset transistor of the same configuration as that of the first reset transistor **21** or the like is provided in the third FD section **11**.

To the first FD section **9** and the first reset transistor **21**, a first pixel amplifier transistor **23** made of an N channel FET is connected. The first pixel amplifier transistor **23** includes a gate connected to the first FD section **9**, a drain connected to the VDDCELL line **31** and a source connected to a first output signal (VO) line **38**.

In the same manner, a second pixel amplifier transistor **24** made of an N channel FET is connected to the second FD section **10** and the second reset transistor **22**. The second pixel amplifier transistor **24** includes a gate connected to the second FD section **10**, a drain connected to the VDDCELL line **31** and a source connected to a second VO line **39**.

The first VO line **38** and the second VO line **39** are connected to not only the pixel amplifier transistors **23** and **24**, respectively, but also first and second load transistors **25** and **26**, respectively. Each of the first and second load transistor **25** and **26** is made of an N channel for constituting a source follower amplifier. A load gate (LGCELL) line **40** is connected to each of the gates of the first and second load transistors **25** and **26**. A source power supply (SCLL) line **41** is connected to each of the respective drains of first and second load transistors **25** and **26**.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **2** is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment. In this case, a series of operations is completed in a horizontal blanking period (=1 H).

Moreover, as for the detection order of signal charges from the PD sections **1** through **8** arranged in an array, detection is simultaneously carried out in the first and second rows and then detection is simultaneously carried out in the third and fourth rows.

As shown in FIG. **2**, first, high level voltage is applied to the LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source, and then during a period in which the potential of the VDDCELL line **31** is high level, each of the RSCELL lines **36** and **37** is set to be a high level in a pulse state to temporarily turn each of the reset transistors **21** and **22** ON. Thus, each of charges stored in the first FD section **9** in the first photoelectric conversion cell **91** and in the second FD section **10** in the second photoelectric conversion cell **92** is made to flow through the VDDCELL line **31**. In this case, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to

the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **2** is transferred to the second FD section **10**. For charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

Subsequently, when the VDDCELL line **31** is turned to be in a low level OFF state and each of the RSCELL lines **36** and **37** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **10** becomes in the same OFF level state as that of the VDDCELL line **31**. Thus, each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **24** is not operated and thus the vertical line scanning circuit is in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at a reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **17** and **18** ON. Thus, charge stored in the PD section **5** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the second FD section **10**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

In this manner, charges detected during the first horizontal blanking period **1**H and charges detected during the second horizontal blanking period **2**H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges.

Subsequently, by driving the PD sections in the third and fourth rows in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

Note that in the first embodiment, the circuit configuration and driving method in which after every second column, i.e., every odd-numbered column including the PD sections **1** and **2** have been read out, charges in every even-numbered column including the PD sections **5** and **6** are detected have been described. However, this embodiment is not limited thereto but READ lines can be increased to detect charge in every third column at the same timing as described above.

In the solid state imaging apparatus of the first embodiment, as shown in the circuit configuration of FIG. **1**, for example, four PD sections share a FD section, a pixel amplifier transistor and a reset transistor. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 1.5. The number of interconnects can be reduced from 5 (required in the known solid state imaging apparatus) to 2.5. For example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections to the photoelectric conversion cell is about 35%. Therefore, it is possible to reduce the cell sizes of the photoelectric conversion cells **91** and **92** and to largely increase the aperture ratio of the PD section at the same time.

In this connection, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are detected by a READ line at the same timing is applied to the known circuit configuration. If a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 10%.

Moreover, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are read out by a READ line, and a FD section and a pixel amplifier transistor included in a row which adjacent to an unread row in a photoelectric conversion cell are shared by two photoelectric sections to detect signal charge is applied to the known circuit configuration. With a driving method in which signal charges are simultaneously detected in the two photoelectric conversion sections, for example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 15%.

Modified Example of First Embodiment

FIG. **3** is a diagram illustrating a circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment of the present invention. Also, in this modified example, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. **3**, for example, in the first photoelectric conversion cell **91**, the first READ line **32** is connected to the transfer transistor **13** and the transfer transistor **18** included in adjacent columns, respectively, while the second READ line **33** is connected to the transfer transistor **14** and the transfer transistor **17** included in adjacent columns, respectively. Thus, even if connections are made with respect to the PD sections **1**, **2**, **5** and **6** included in two adjacent rows with the first and second READ lines **32** and **33** interposed between the PD sections **1** and **5** and the PD sections **2** and **6** so that signal charges from the PD sections which are not included in

the same columns are transferred, charge can be detected at the same timing as that shown in FIG. **2**.

For example, when the first READ line **32** is temporarily turned ON, signal charge is transferred from the PD section **1** to the first FD section **9** via the transfer transistor **13** and, at the same time, signal charge is transferred from the PD section **6** to the second FD section **10** via the transfer transistor **18**.

Note that in the modified example of the first embodiment, signal charges from two of the four PD sections included in a photoelectric conversion cell **91** are read out during the horizontal blanking period **1**H. However, instead of this, signal charges from all of the four PD sections may be read out.

Moreover, by performing signal processing to signal charges from all of the photoelectric conversion cells which have been read out during different horizontal blanking periods, a high quality image with a large number of pixels can be obtained.

Second Embodiment

Hereinafter, a second embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **4** is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a second embodiment of the present invention. In FIG. **4**, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

First, differences of the solid state imaging apparatus of FIG. **4** from that of the first embodiment shown in FIG. **1** will be described.

In the second embodiment, an configuration in which the first and second pixel amplifier transistors **23** and **24** are connected to the first and second output signal (VO) lines **38** and **39**, respectively, via the first and second select transistors **52** and **53** each of which made of an N channel FET, respectively, is used.

To the respective gates of the first and second select transistors **52** and **53**, first and second select (SO) lines **50** and **51** to which a switching pulse is applied are connected, respectively.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **5** is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment. In this case, a series of operations is completed in a horizontal blanking period (=1 H).

As shown in FIG. **5**, first, a predetermined voltage is applied to the LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source and the potential of the VDDCELL line **31** is set to be a high level. Subsequently, each of the RSCELL lines **36** and **37** is set to be a high level in a pulse state to temporarily turn each of the reset transistors **21** and **22** ON. Thus, each of charges stored in the first FD section **9** and in the second FD section **10** is made to flow through the VDDCELL line **31**. In this case, in each of the pixel amplifier transistors **23** and **24**, each of the select transistors **52** and **53** has been turned ON in advance, so that a signal level at a reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **2** is transferred to the second FD section **10**. Thereafter, for charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively.

Subsequently, by changing each of the first and second SO lines **50** and **51** to a high level to keep the first and second transistors **52** and **53** ON, stored charge signals of the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24** are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit.

Thereafter, each of the first and second SO lines **50** and **51** is set back to be a low level to turn the first and second select transistors **52** and **53** OFF, so that each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** is selected, each of the pixel amplifier transistors **23** and **24** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of the FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **17** and **18** ON. Thus, charge stored in the PD section **5** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the second FD section **10**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the stored signals whose voltage level have been detected selectively conducts the first and second VO lines **38** and **39** and are introduced to the noise cancellation circuit. Then, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

Thus, with the first and second select transistors **52** and **53** between the FD section **9** and the first VO line **38** and between the FD section **10** and the second VO line **39**, respectively. Thus, the number of transistors per photoelectric conversion cell is 1.75. Moreover, the number of interconnects is 2.75. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells **91** and **92** and also to largely improve the aperture ratio of PD sections.

Note that also in the second embodiment, as in the modified example of the first embodiment, for example, a configuration in which the transfer transistor **13** and the transfer transistor **18** located diagonally to the transfer transistor **13** are connected to the first READ line **32**, and the transfer transistor **14**

and the transfer transistor **17** located diagonally to the transfer transistor **14** are connected to the second READ line **33** may be used.

Moreover, in the photoelectric conversion cell **91**, the PD sections are arranged in two rows and two columns. However, the present invention is not limited thereto, but the PD sections may be arranged in two rows and three columns and, furthermore, may be arranged in three or more rows and three or more columns.

Third Embodiment

Hereinafter, a third embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **6** is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention. In FIG. **6**, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. **6**, in the solid state imaging apparatus of the third embodiment, first through fourth photoelectric conversion cells **91**, **92**, **93** and **94** are arranged in a matrix.

For example, the first photoelectric conversion cell **91** includes photoelectric conversion (PD) sections **1** and **2** arranged in regions which is located in the first column of an array and the first row and which is located in the first column of and the second rows of the array, respectively. The PD sections **1** and **2** share a first FD section **9** via transfer transistors **13** and **14** each of which is made of an N channel FET, respectively.

To the first FD section **9**, the first reset transistor **21** made of an N channel FET is connected. The first reset transistor **21** includes a source connected to the first FD section **9**, a drain connected to the first FD section **9** and a gate connected to a first RSCELL line **36**. Thus, charge stored in the first FD section **9** is made to flow through a first VDDCELL line **30** by a RSCELL signal.

To the first FD section **9** and the first reset transistor **21**, a first pixel amplifier transistor **23** of an N channel FET is connected. The first pixel amplifier transistor made of an N channel FET includes a gate connected to the first FD section **9**, a drain connected to the first VDDCELL line **30** and a source connected to a first VO line **38**.

In the same manner, PD sections **3** and **4** arranged in regions of an array forming a second photoelectric conversion cell **92** which is located in the first column and the third row and which is located in the first column and the fourth row, respectively, share a second FD section **10** via transfer transistors **15** and **16**, respectively. A second reset transistor **22** selectively conducts the second FD section **10** and the first VDDCELL line **30**. Moreover, a second pixel amplifier transistor **24** which receives the signal potential of the second FD section **10** at the gate and receives the power supply potential of the first VDDCELL line **30** at the drain outputs a detected signal corresponding to a received signal potential to the first VO line **38**.

PD sections **5** and **6** arranged in regions of an array forming a third photoelectric conversion cell **93** which is located in the second column and the first row and which is located in the second column and the second row, respectively, share a third FD section **11** via transfer transistors **17** and **18**, respectively. A third reset transistor **61** selectively conducts the third FD section **11** and a second VDDCELL line **31**. Moreover, a third pixel amplifier transistor **63** which receives the signal potential of the third FD section **11** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs a detected signal corresponding to a received signal potential to a second VO line **39**.

PD sections **7** and **8** arranged in regions of an array forming a fourth photoelectric conversion cell **94** which is located in the second column and the third row and which is located in the second column and the fourth row, respectively, share a fourth FD section **12** via transfer transistors **19** and **20**, respectively. A fourth reset transistor **62** selectively conducts the fourth FD section **12** and a second VDDCELL line **31**. Moreover, a fourth pixel amplifier transistor **64** which receives the signal potential of the fourth FD section **12** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs a detected signal corresponding to a received signal potential to a second VO line **39**.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **7** is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment. In this case, a series of operations is completed in a horizontal blanking period (=1 H).

Moreover, as for the detection order of signal charges from the PD sections **1** through **8** arranged in an array, detection is carried out sequentially from the first row to the second row and so on.

As shown in FIG. **7**, first, high level voltage is applied to a LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source, and then during a period in which the potentials of the first VDDCELL line **30** and the VDDCELL line **31** are set to be high level, the first RSCELL lines **36** is set to be high level in a pulse state to temporarily turn each of the reset transistors **21** and **61** ON. Thus, charges stored in the first FD section **9** in the first photoelectric conversion cell **91** and in the third FD section **11** in the third photoelectric conversion cell **93** are made to flow through the first VDDCELL line **30** and the VDDCELL line **31**, respectively. In this case, in each of the pixel amplifier transistors **23** and **63**, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **61** has been turned OFF, high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **5** in the second row is transferred to the third FD section **11**. For charges transferred to the first FD section **9** and the third FD section **11**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the third pixel amplifier transistor **63**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **63** can be detected.

Subsequently, when each of the VDDCELL lines **30** and **31** is turned to be in a low level OFF state and the first RSCELL line **36** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **11** becomes in the same

OFF level state as that of each of the VDDCELL lines **30** and **31**. Then, each of the pixel amplifier transistors **23** and **63** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL line **36** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **63** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **61** is temporarily turned ON to reset charges of the FD sections **9** and **11**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **63**, a signal level at the reset time is detected, detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **61** has bee turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **14** and **18** ON. Thus, charge stored in the PD section **2** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the third FD section **11**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the third FD section **11**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the third pixel amplifier transistor **63**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **63** can be detected

In this manner, charges detected during the first horizontal blanking period **1**H and charges detected during the second horizontal blanking period **2**H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges. Thus, in the third embodiment, for example, the power supply potentials which are to be applied to the respective drains of the first reset transistor **21** and the first pixel amplifier transistor **23** vary in the same manner. Therefore, the known row selection transistor **152** is not necessarily provided.

Subsequently, if the PD sections in the third and fourth rows are driven in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

As has been described, the solid state imaging apparatus of the third embodiment has, for example, a configuration in which the two PD sections **1** and **2** share the first FD section **9**, the first pixel amplifier transistor **23** and the first reset transistor **21**. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 2. Moreover, the number of interconnects can be reduced from 5 (required in the known apparatus) to 3.5. Accordingly, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD sections **1** and **2** is about 30%. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells and also to largely improve the aperture ratio of the PD section.

Note that each of the reset transistors **21**, **22**, **61** and **62** is made of an N channel type MOS transistor. However, in each of the reset transistors **21**, **22**, **61** and **62** made of, instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second RSCELL lines **36** and **37**, each of the reset transistors **21**, **22**, **61** and **62** is turned ON.

In the same manner, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is made of an N channel type MOS transistor. However, in each of the pixel amplifier transistors **23**, **24**, **63** and **64** made of, instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second VDDVELL lines **30** and **31**, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is turned ON to be in a potential detection period in which signal potentials from the corresponding FD sections **9**, **10**, **11** and **12** are detected.

Hereinafter, in the layout in which each of the PD sections **1**, **2**, **3**, **5**, **6** and **7** arranged as shown in FIG. **8**, a region of the cell located between the PD sections **1** and **2** is referred to as an "A region"; a region of the cell surrounded by the PD sections **1**, **2**, **5** and **6** is referred to as a "B region"; a region of the cell located between the PD sections **5** and **6** is referred to as a "C region"; a region of the cell located between the PD sections **2** and **6** is referred to as a "D region"; and a region of the cell located between the PD sections **1** and **5** is referred to as an "E region". Then, by arranging the FD sections **9** and **11**, the pixel amplifier transistors **23** and **63**, and the reset transistors **21** and **61** in regions in the cell indicated in the FIG. **9**, respectively, the aperture ratio of the PD sections to the photoelectric conversion cell can be improved in any case, compared to the known solid state imaging apparatus. Moreover, the size of the cell can be reduced.

Furthermore, as also shown in FIG. **9**, if the FD sections **9** and **11** are arranged in the A and C regions, respectively, the aperture of the PD sections can be improved to be about 30% by arranging in parallel the READ lines **32** and **33** for driving the transfer transistors **13** and **14**, respectively.

Moreover, as shown in FIG. **9**, for example, the aperture of the PD sections can be improved to be about 30% by arranging the first RSCELL line **36** between the PD sections **2** and **3**.

Moreover, as shown in FIG. **8**, by arranging the PD sections so as to be spaced apart from one another by a certain distance at least in one of the row direction and the column direction, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

Moreover, although not shown in the drawings, by using the first VDDCELL line **30** and the second VDDCELL line **31** as light-shielding films for separating the photoelectric conversion cells from one another, the first VO line **38** and the second VO line **39** can be formed in different interconnect layers. Thus, the sizes of the photoelectric conversion cells **91** and **92** can be reduced and also the aperture area of the PD sections can be increased.

Moreover, with the solid state imaging apparatus of any one of the first through third embodiments, a camera which is small-sized and provides a high resolution image can be obtained.

What is claimed is:

1. A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the plurality of photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors;

a plurality of pixel amplifier transistors each detecting and outputting the potential of each of the plurality of floating diffusion sections; and

a plurality of power supply lines applying voltage to drain sections of the pixel amplifier transistors, wherein

the plurality of photodiodes includes a first photodiode and a second photodiode,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the plurality of transfer transistors includes a first transfer transistor and a second transfer transistor,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the first and the second photodiodes are in the same column,

one of the plurality of floating diffusion sections is connected to the first photodiode via the first transfer transistor and is connected to the second photodiode via the second transfer transistor,

the plurality of read-out lines are disposed between the first and the second photodiodes,

the first read-out line is connected to a gate of the first transfer transistor,

the second read-out line is connected to a gate of the second transfer transistor, and

the plurality of read-out lines and one of the plurality of power supply lines intersect with each other.

2. The solid state imaging apparatus of claim **1**, wherein each said read-out line is connected to two of the transfer transistors which are not included in the same column.

3. A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section; and

a plurality of signal lines each transferring an output from each said pixel amplifier transistor, wherein

the plurality of photodiodes includes a first photodiode and a second photodiode,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the plurality of transfer transistors includes a first transfer transistor and a second transfer transistor,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the first and the second photodiodes are in the same column,

one of the plurality of floating diffusion sections is connected to the first photodiode via the first transfer transistor and is connected to the second photodiode via the second transfer transistor,

the plurality of read-out lines are disposed between the first and the second photodiodes,

the first read-out line is connected to a gate of the first transfer transistor,

the second read-out line is connected to a gate of the second transfer transistor, and

the plurality of read-out lines and one of the plurality of signal lines intersect with each other.

4. The solid state imaging apparatus of claim **3**, wherein each said read-out line is connected to two of the transfer transistors which are not included in the same column.

* * * * *

Docket No.: 079195-0552 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Mitsuyoshi MORI, et al.	:	Confirmation Number: 2044
Application No.: 12/202,804	:	Group Art Unit: 2814
Filed: September 02, 2008	:	Examiner: INGHAM, JOHN C

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated December 6, 2010, having a three-month shortened statutory period for response set to expire on March 6, 2011, and the petition for a one-month extension of time up to and including April 6, 2011 being filed concurrently herewith, reconsideration of the above-identified application is respectfully requested in view of the following amendment and remarks.

AMENDMENT TO THE CLAIMS

1-30. (Cancelled)

31. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes ~~photoelectric conversion cells each including a plurality of photoelectric conversion sections~~ arranged in an array ~~of at least two rows and one column~~;

a plurality of floating diffusion sections each being connected to ~~each of~~ ones of the plurality of photodiodes ~~photoelectric conversion sections which are included in each said photoelectric conversion cell~~ via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors;

a plurality of pixel amplifier transistors each detecting and outputting the potential of each of the plurality of ~~said the~~ floating diffusion sections ~~section~~; and

a plurality of power supply lines applying voltage to drain sections of the pixel amplifier transistors, wherein

the plurality of photodiodes includes a first photodiode and a second photodiode,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the plurality of transfer transistors includes a first transfer transistor and a second transfer transistor,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the first and the second photodiodes are in the same column,

one of the plurality of floating diffusion sections is connected to the first photodiode via the first transfer transistor and is connected to the second photodiode via the second transfer transistor,

the plurality of read-out lines are disposed between the first and the second photodiodes,

the first read-out line is connected to a gate of the first transfer transistor,

the second read-out line is connected to a gate of the second transfer transistor, and

the plurality of read-out lines and one of the plurality of power supply lines intersect with each other.

32. (Canceled)

33. (Previously presented) The solid state imaging apparatus of claim 31, wherein each said read-out line is connected to two of the transfer transistors which are included in the same column.

34. (Previously presented) The solid state imaging apparatus of claim 31, wherein each said read-out line is connected to two of the transfer transistors which are not included in the same column.

35. (Currently amended) The solid state imaging apparatus of claim 31, wherein each of said floating diffusion sections is shared by said ones of the plurality of photodiodes ~~photoelectric conversion sections~~ which are adjacent to each other in the column direction.

36. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes ~~photoelectric conversion cells each including a plurality of photoelectric conversion sections~~ arranged in an array ~~of at least two rows and one column~~;

a plurality of floating diffusion sections each being connected to ~~each of~~ ones of the photodiodes ~~photoelectric conversion sections which are included in each said photoelectric conversion cell~~ via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section; and

a plurality of signal lines each transferring an output from each said pixel amplifier transistor, wherein

the plurality of photodiodes includes a first photodiode and a second photodiode,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the plurality of transfer transistors includes a first transfer transistor and a second transfer transistor,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the first and the second photodiodes are in the same column,

one of the plurality of floating diffusion sections is connected to the first photodiode via the first transfer transistor and is connected to the second photodiode via the second transfer transistor,

the plurality of read-out lines are disposed between the first and the second photodiodes,

the first read-out line is connected to a gate of the first transfer transistor,

the second read-out line is connected to a gate of the second transfer transistor, and

the plurality of read-out lines and one of the plurality of signal lines intersect with each other

~~each said signal line is disposed between ones of the photoelectric conversion cells which are adjacent to each other in the column direction~~.

37. (Canceled)

38. (Previously presented) The solid state imaging apparatus of claim 36, wherein each said read-out line is connected to two of the transfer transistors which are included in the same column.

39. (Previously presented) The solid state imaging apparatus of claim 36, wherein each said read-out line is connected to two of the transfer transistors which are not included in the same column.

40. (Currently amended) The solid state imaging apparatus of claim 36, wherein each of said floating diffusion sections is shared by said ones of the plurality of photodiodes ~~photoelectric conversion sections~~ which are adjacent to each other in the column direction.

41-44. (Canceled)

REMARKS

As a preliminary matter, it is noted that the Examiner has not provided a complete initialed copy of the Information Disclosure Statement filed on October 8, 2010. While USP No. 6,310,366 to Rhodes et al. was initialed, the United States Office Action listed in the "Other Art" section of the PTO-1449 was not initialed. It is respectfully requested that the Examiner provide Applicants another initialed copy of the October 8, 2010 IDS indicating that ***each*** of the prior art references cited therein have been considered and made of record.

Claim 43 stands rejected under 35 U.S.C. § 112, first paragraph (enablement) and claims 41-44 stand rejected under 35 U.S.C. § 102 as being anticipated by Takahashi '753. Solely in order to expedite prosecution, claims 41-44 have been canceled without prejudice/disclaimer to the subject matter embodied thereby, rendering these rejections moot.

Claims 31 and 36 are independent and stand rejected under 35 U.S.C. § 102 as being anticipated by Guidash '281 ("Guidash") and Rhodes et al. '366 ("Rhodes"). These rejections are respectfully traversed for the following reasons.

It is respectfully submitted that none of the cited prior art, alone or in combination, disclose or suggest the particular arrangement and configuration of elements comprising the solid state imaging apparatus embodied by claims 31 and 36. For example, each of claims 31 and 36 embody an arrangement in which a plurality of read-out lines are disposed between the first and the second photodiodes. One exemplary embodiment of such a configuration is illustrated in Figure 6 of Applicants' drawings, in which read-out lines 32 and 33 are disposed between photodiodes 1 and 2 in the same column (*see* page 24+ of Applicants' specification).

Turning to the cited prior art, Guidash discloses an alleged read-out line TGC for each photodiode. However, as shown in Figure 2 thereof, it appears the PD elements 11 in each of the two illustrated rows are connected to the same TGC line, and that only one alleged read-out line TGC is arranged between photodiodes in the same column but different rows. That is, between the two rows of PD elements, there is only one alleged read-out line as in conventional arrangements. Rhodes similarly discloses only one alleged read-out line between photodiodes in the same column but different rows (*see* Figure 4), and therefore does not suggest a plurality of read-out lines are disposed between the first and the second photodiodes for reasons similar to those discussed above regarding Guidash. Moreover, Hashimoto '684 used in the rejection of claims 35 and 40 fails to disclose or suggest an arrangement and configuration in which "the first and the second photodiodes are in the same column, … the first read-out line is connected to a gate of the first transfer transistor, [and] the second read-out line is connected to a gate of the second transfer transistor" as further embodied in claims 31 and 36.

Accordingly, none of the cited prior art, alone or in combination, disclose or suggest ***the particular arrangement and configuration of elements*** comprising the solid state imaging apparatus embodied by claims 31 and 36. As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that the cited prior art does not anticipate claims 31 and 36, nor any claim dependent thereon.

"All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 165 USPQ 494, 496 (CCPA 1970).

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. §§ 102 and 103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
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Date: April 6, 2011

Notice of Allowability	Application No. 12/202,804	Applicant(s) MORI ET AL.	
	Examiner JOHN C. INGHAM	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendments filed 17 Aug. 2011*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *31,34,36 and 39*.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 9/2/2008
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/JOHN C INGHAM/ Examiner, Art Unit 2814	/Wael M Fahmy/ Supervisory Patent Examiner, Art Unit 2814

DETAILED ACTION

Allowable Subject Matter

1. Claims **31, 34, 36 and 39** are allowed.

2. The following is an examiner's statement of reasons for allowance: the prior art does not disclose or make obvious the solid state imaging apparatus of claims 31 or 36, including wherein the first and second photodiodes are in the same column, one of the plurality of floating diffusion sections is connected to the first photodiode via the first transfer transistor and is connected to the second photodiode via the second transfer transistor, the plurality of read out lines are disposed between the first and second photodiodes, the first read out line is connected to a gate of the first transfer transistor, the second read out line is connected to a gate of the second transfer transistor, and the plurality of read out lines and one of the plurality of power and supply lines intersect with each other.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on Monday to Friday, 9AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Examiner, Art Unit 2814

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814

(12) **United States Patent**
Mori et al.

(10) **Patent No.: US 8,106,431 B2**
(45) **Date of Patent: Jan. 31, 2012**

(54) **SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME**

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(73) Assignee: **Panasonic Corporation**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 326 days.

(21) Appl. No.: **12/178,250**

(22) Filed: **Jul. 23, 2008**

(65) **Prior Publication Data**

US 2008/0284882 A1 Nov. 20, 2008

Related U.S. Application Data

(63) Continuation of application No. 10/706,918, filed on Nov. 14, 2003, now Pat. No. 7,436,010.

(30) **Foreign Application Priority Data**

Feb. 13, 2003 (JP) 2003-034692

(51) **Int. Cl.**
H01L 31/062 (2006.01)

(52) **U.S. Cl.** **257/292**; 257/223; 257/291; 257/444; 257/445; 257/E27.132; 257/E27.139

(58) **Field of Classification Search** 257/291–293, 257/443–445, 223, E27.132, E27.139
See application file for complete search history.

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Primary Examiner — Wael Fahmy
Assistant Examiner — John C Ingham
(74) *Attorney, Agent, or Firm* — McDermott Will & Emery LLP

(57) **ABSTRACT**

A solid state imaging apparatus includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. Charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

12 Claims, 10 Drawing Sheets

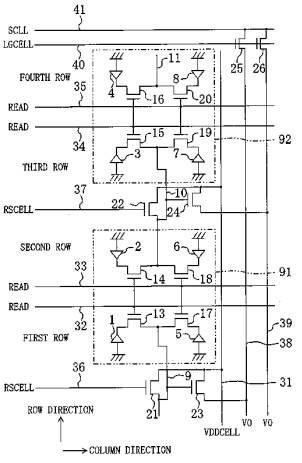

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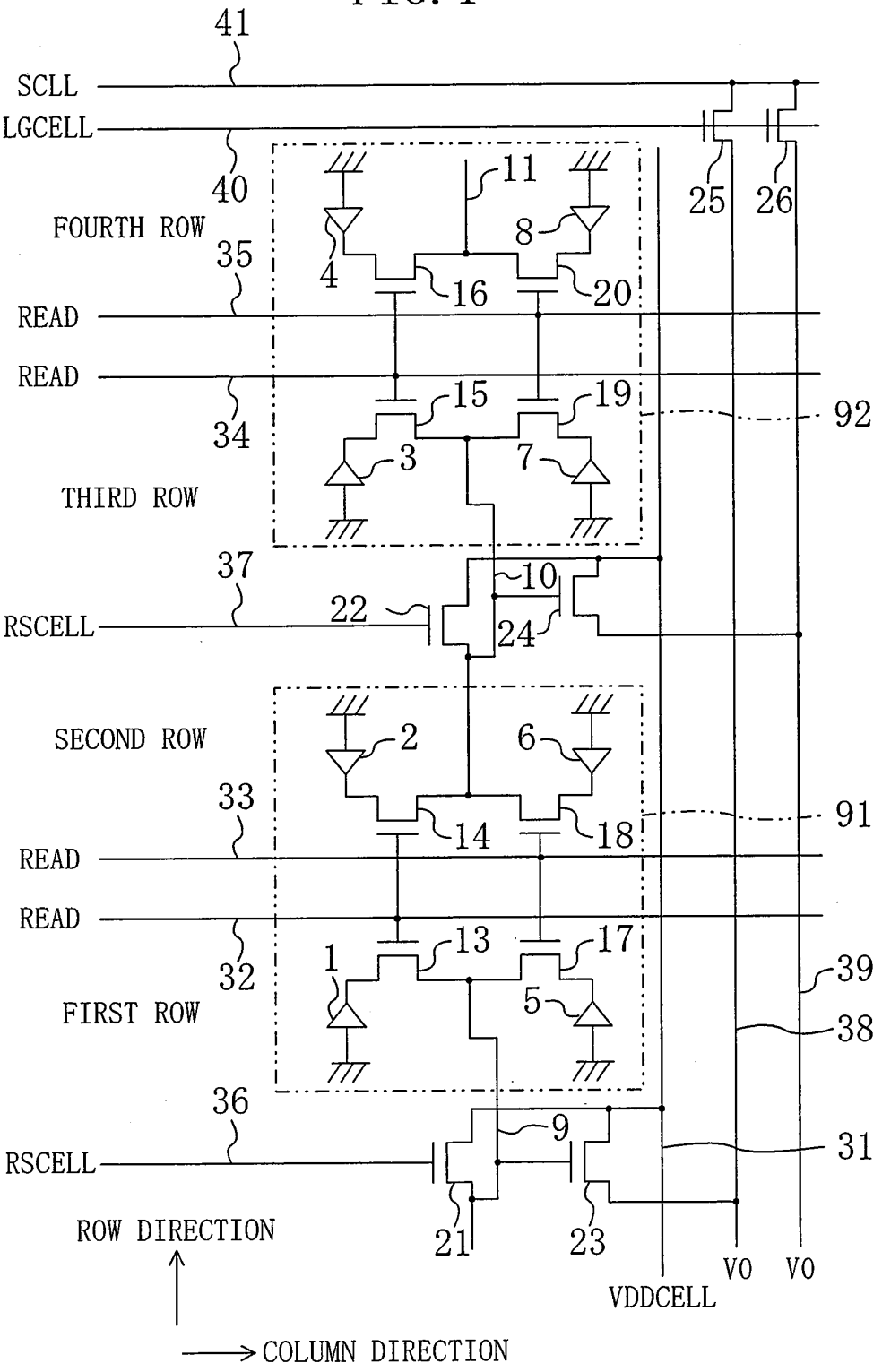
FIG. 1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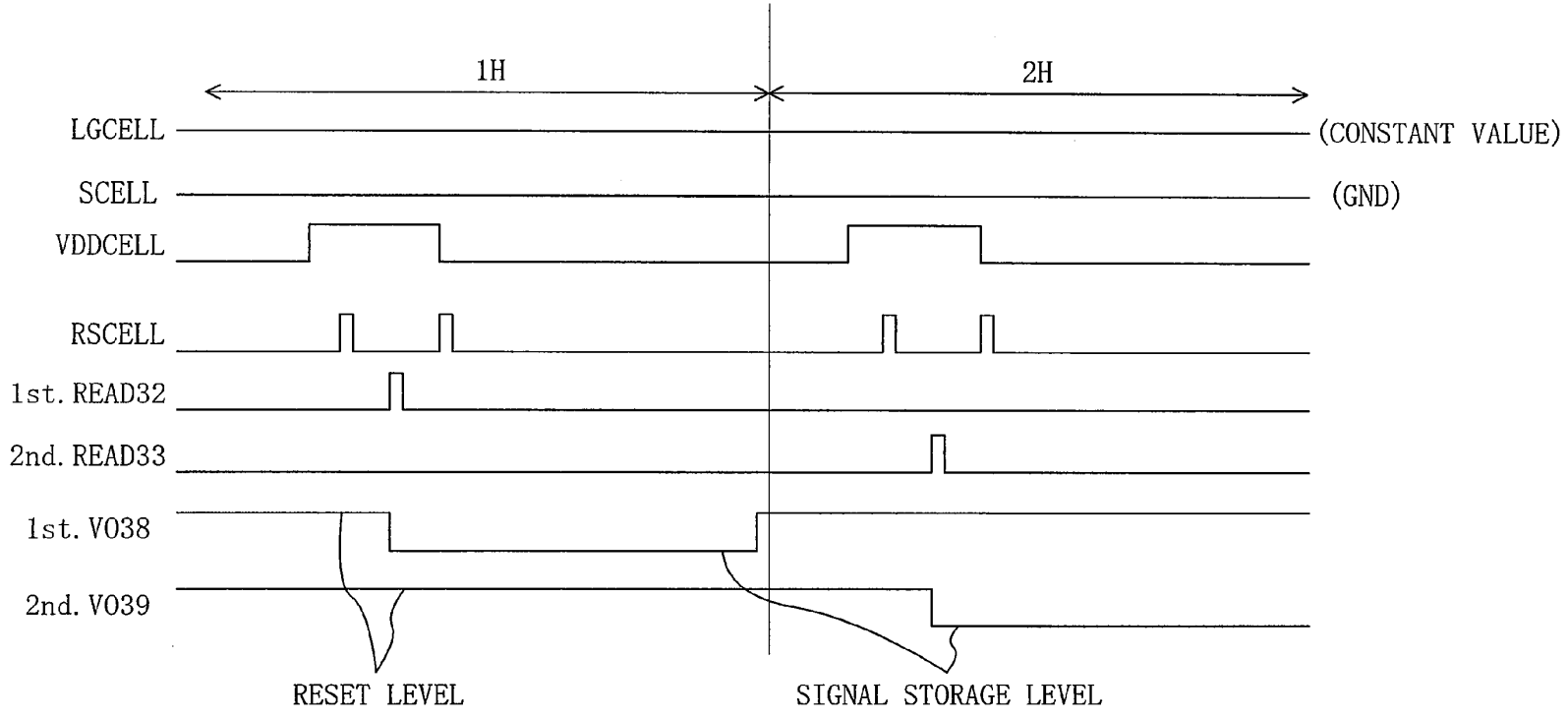
LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
33
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
2
6
14
18
91
13
17
1
5
39
38
9
31
21
23
VDDCELL
VO
VO

FIG. 2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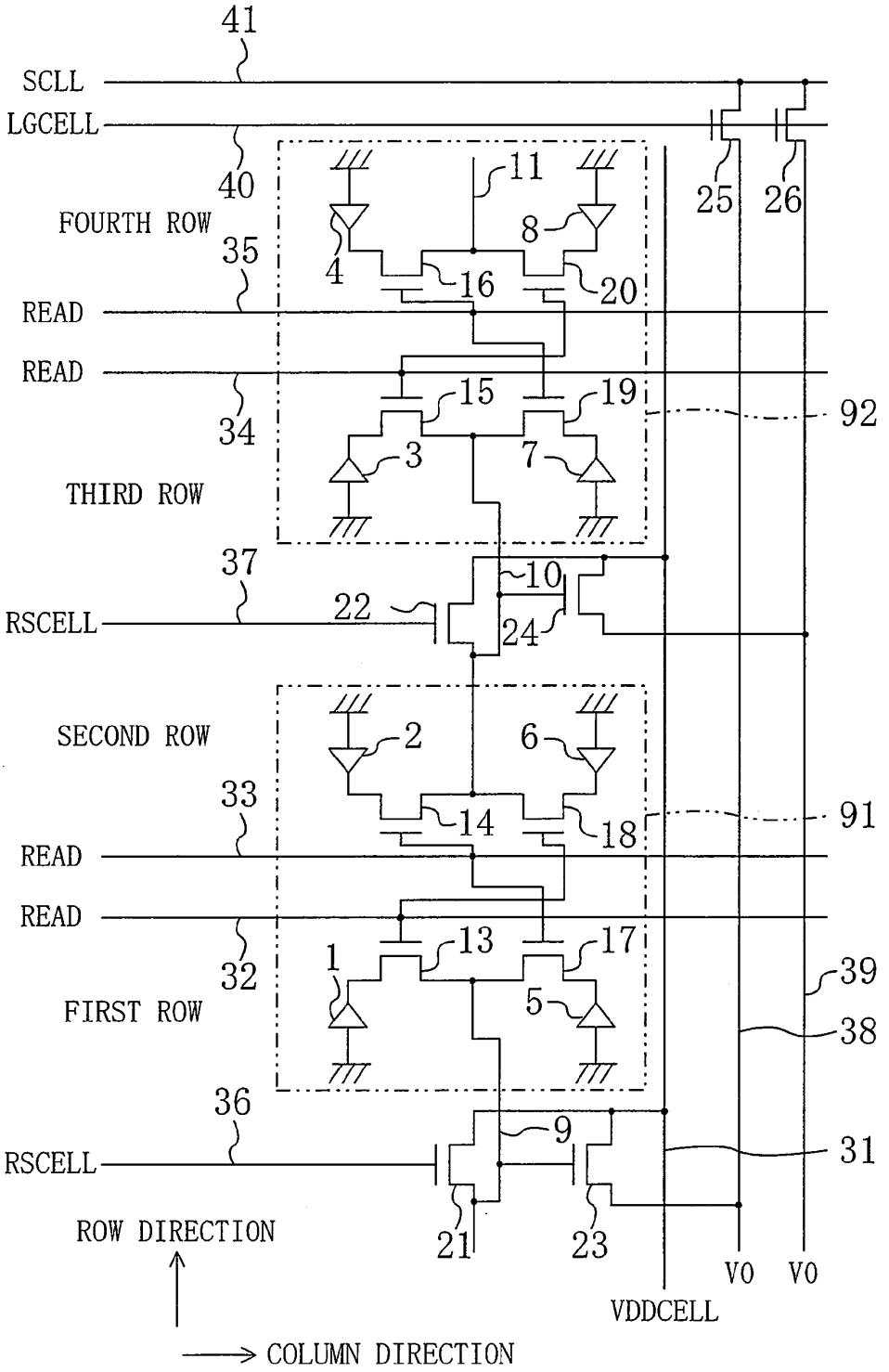
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
RSCELL
1st. READ32
2nd. READ33
1st. VO38
2nd. VO39
RESET LEVEL
SIGNAL STORAGE LEVEL

FIG. 3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40
FOURTH ROW
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READ
READ
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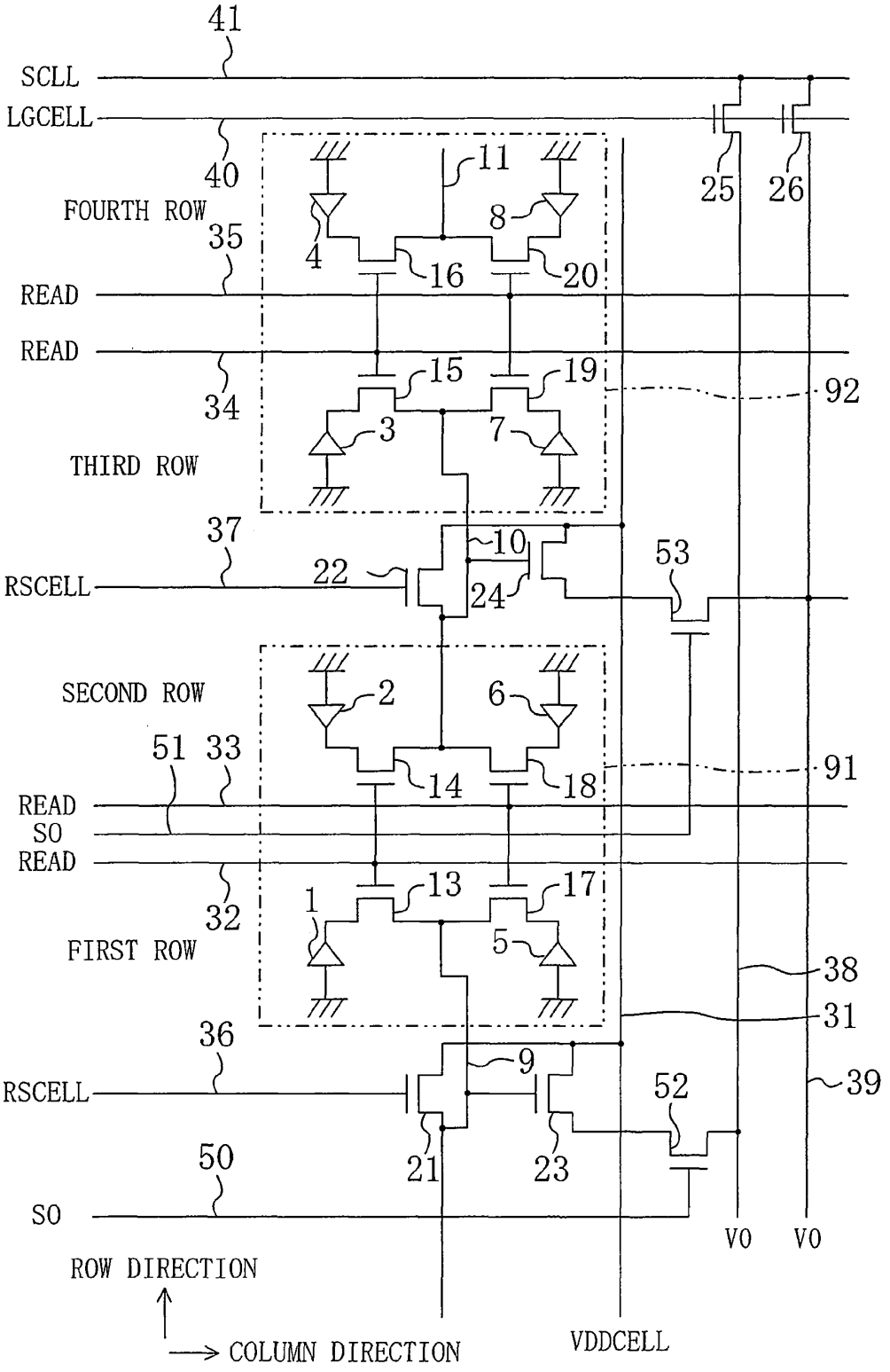
THIRD ROW
37
RSCELL
SECOND ROW
33
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
2
6
14
18
91
1
13
17
39
5
38
9
31
21
23
VO
VO
VDDCELL

FIG. 4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FOURTH ROW
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READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
51
33
READ
SO
READ
32
FIRST ROW
36
RSCELL
50
SO
ROW DIRECTION
COLUMN DIRECTION
VDDCELL
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
53
2
6
14
18
91
1
13
17
5
38
31
9
52
39
21
23
VO
VO

FIG. 5

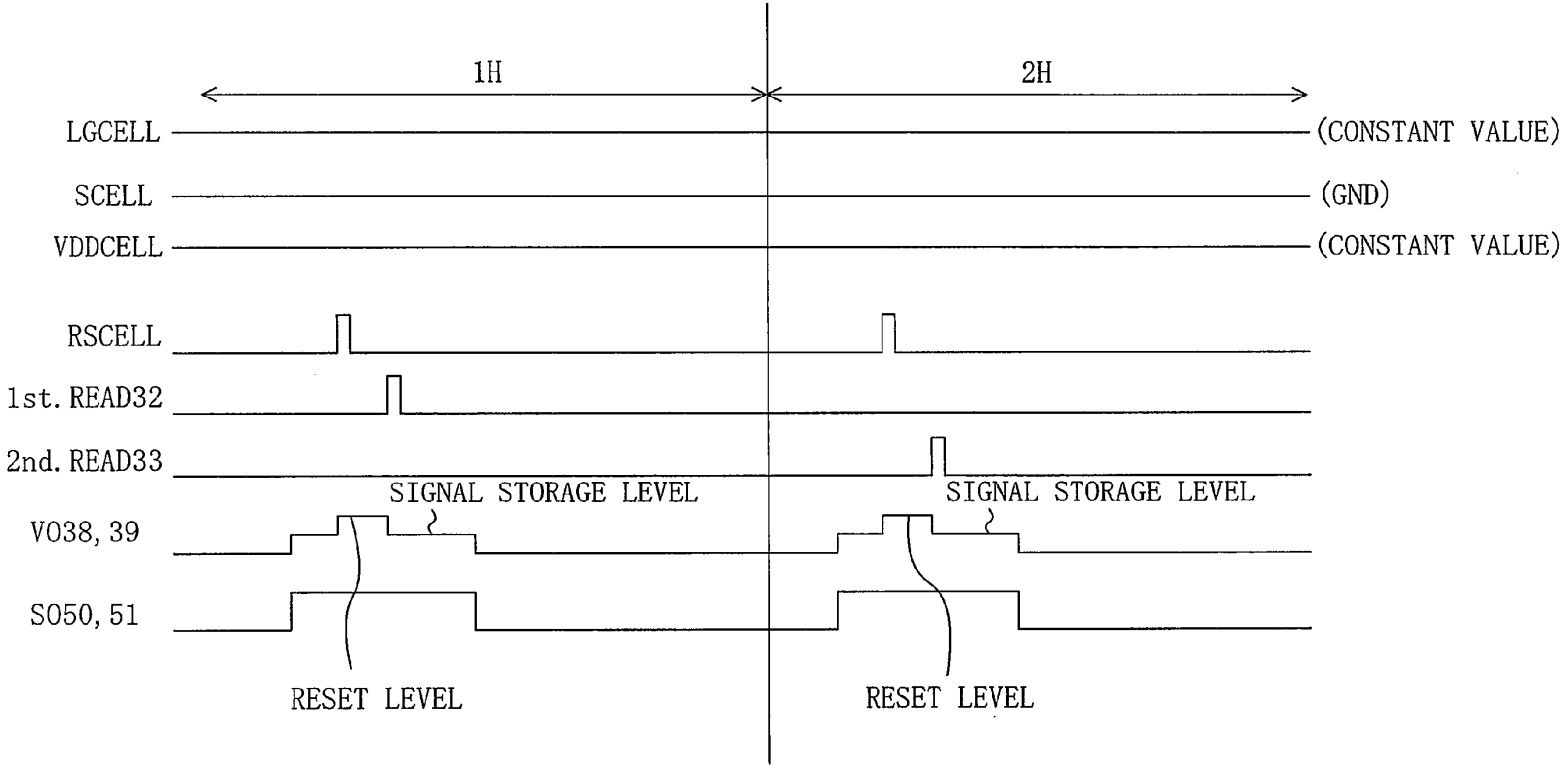

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
(CONSTANT VALUE)
RSCELL
1st. READ32
2nd. READ33
SIGNAL STORAGE LEVEL
SIGNAL STORAGE LEVEL
VO38, 39
SO50, 51
RESET LEVEL
RESET LEVEL

FIG. 6

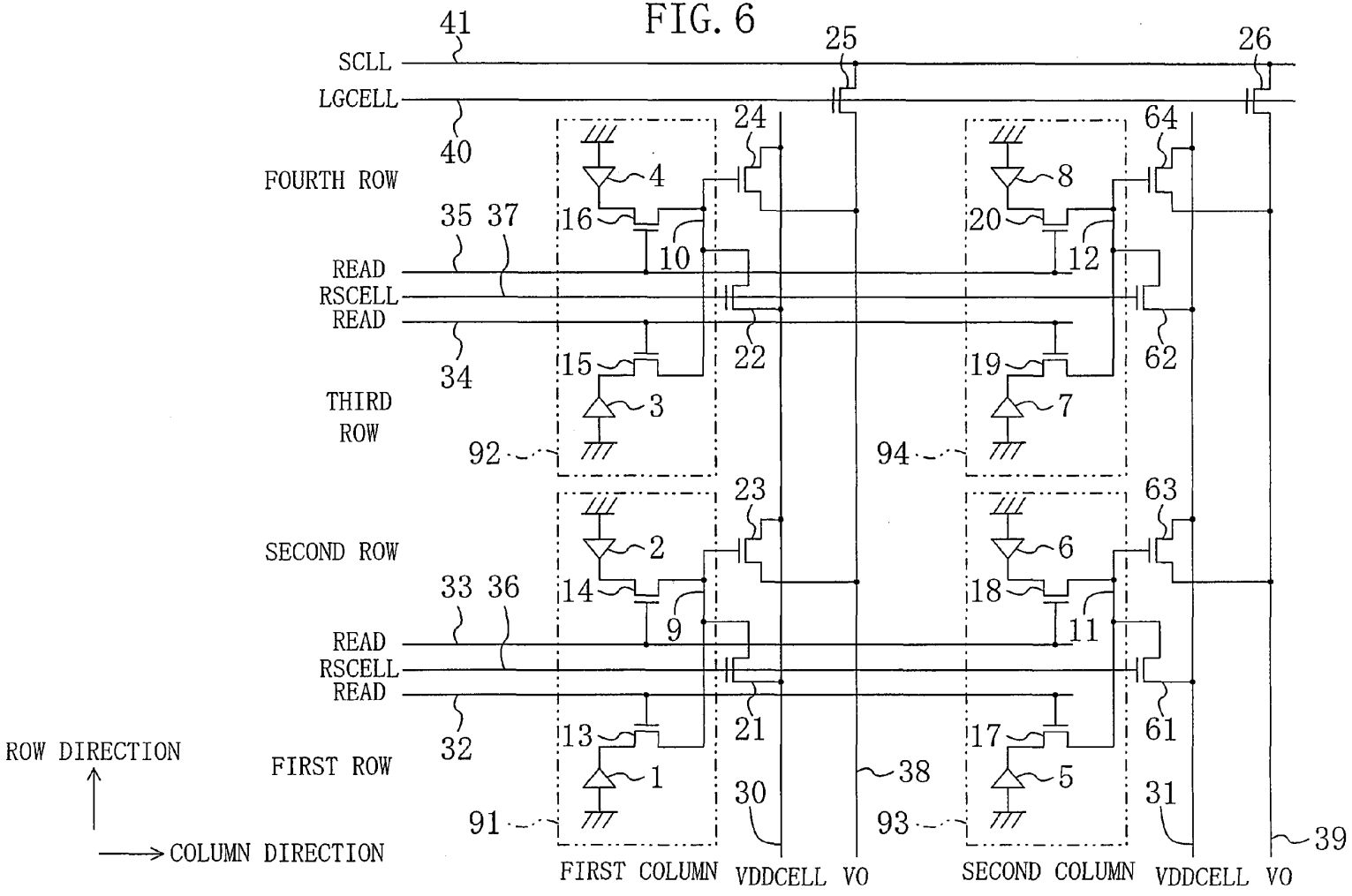

41
SCLL
LGCELL
40
FOURTH ROW
35 37
READ
RSCELL
READ
34
THIRD ROW
SECOND ROW
33 36
READ
RSCELL
READ
32
FIRST ROW
ROW DIRECTION
COLUMN DIRECTION
25
26
24
64
4
8
16
20
10
12
22
62
15
19
3
7
92
94
23
63
2
6
14
18
9
11
21
61
13
17
1
5
38
30
31
39
91
93
FIRST COLUMN
VDDCELL
VO
SECOND COLUMN
VDDCELL
VO

FIG. 7

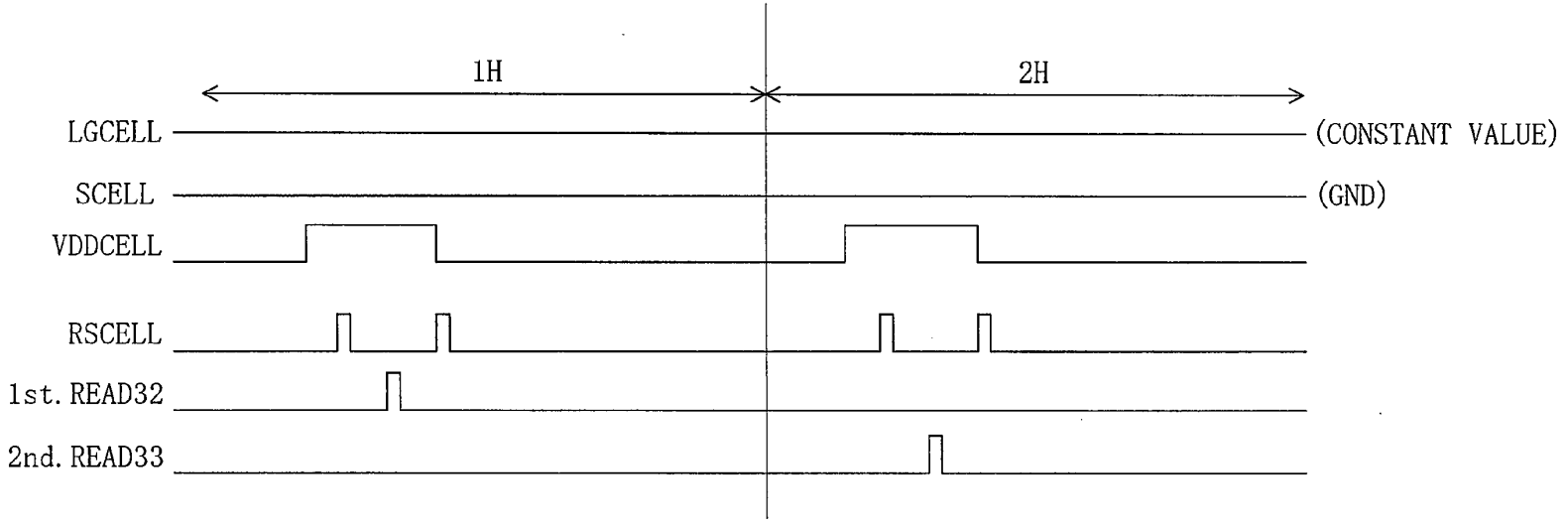

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
RSCELL
1st. READ32
2nd. READ33

FIG. 8

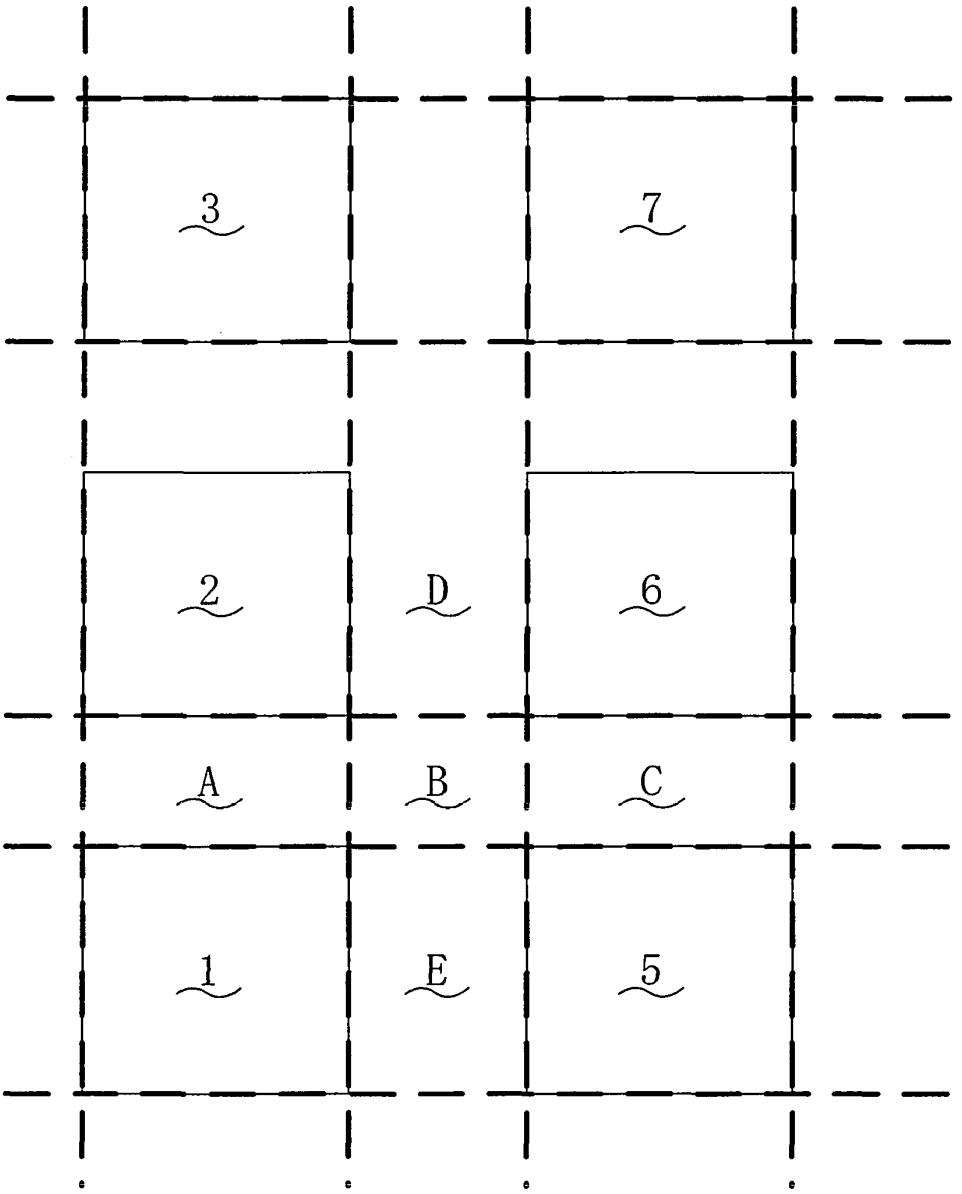
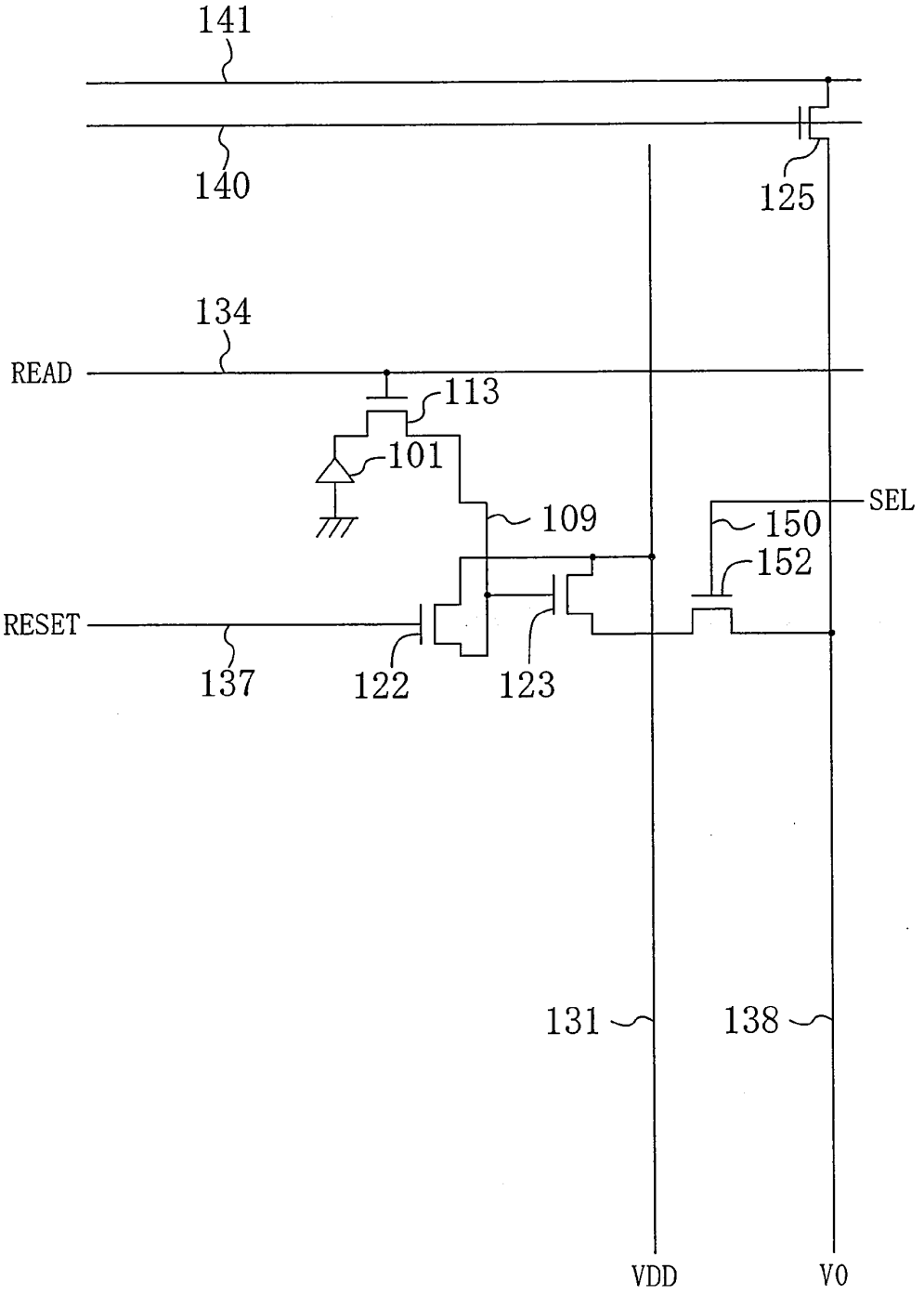


FIG. 9

FD SECTION	PIXEL AMPLIFIER	RESET GATE	APERTURE RATIO
A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	10%
		D REGION、B REGION、E REGION	25%
	D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	35%
D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	20%
	D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	20%

FIG. 10

PRIOR ART



SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

RELATED APPLICATIONS

This application is a Continuation of U.S. application Ser. No. 10/706,918, filed Nov. 14, 2003 now U.S. Pat. No. 7,436,010, claiming priority of Japanese Application No. 2003-034692, filed Feb. 13, 2003, the entire contents of each of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a solid state imaging apparatus in which a plurality of photoelectric conversion sections are arranged in an array, a method for driving the solid state imaging apparatus and a camera using the solid state imaging apparatus.

FIG. **10** is a diagram illustrating a general circuit configuration for a MOS type image sensor, i.e., a known solid imaging apparatus (e.g., see M. H. White, D. R. Lange, F. C. Blaha and I. A. Mach, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels", IEEE J. Solid-State Circuits, SC-9, pp. 1-13 (1974)).

As shown in FIG. **10**, a photoelectric conversion cell includes a photodiode (PD) section **101**, a transfer transistor **113**, a reset transistor **122**, a pixel amplifier transistor **123**, a select transistor **152**, a floating diffusion (FD) section **109**, a power supply line **131** and an output signal line **138**.

The PD section **101** of which the anode is grounded is connected to the drain of the transfer transistor **113** at the cathode. The source of the transfer transistor **113** is connected to the respective sources of the FD section **109**, the gate of the pixel amplifier transistor **123** and the source of the reset transistor **122**. The gate of the transfer transistor **113** is connected to a read-out line **134**. The reset transistor **122** which receives a reset signal **137** at the gate includes a drain connected to the drain of the pixel amplifier transistor **123** and the power supply line **131**. The source of the pixel amplifier transistor **123** is connected to the drain of the select transistor **152**. The select transistor **152** receives a selection signal SEL at the gate and includes a source connected to the output signal line **138**.

The output signal line **138** is connected to the source of a load gate **125**. The gate of the load gate **125** is connected to a load gate line **140** thereof and the drain is connected to a source power supply line **141**.

In this configuration, a predetermined voltage is applied to the load gate line **140** so that the load gate **125** becomes a constant current source, and then the transfer transistor **113** is temporarily turned ON to transfer charge photoelectric-converted in the PD section **101** to the FD section **109**. Then, the potential of the PD section **101** is detected by the pixel amplifier transistor **123**. In this case, by turning the select transistor **152** ON, signal charge can be detected through the output signal line **138**.

However, in the known solid state apparatus, four transistors **113**, **122**, **123** and **152** and five lines **131**, **134**, **137**, **138** and **150** are required for total in each photoelectric conversion cell. Accordingly, the areas of transistor and line sections in a cell are increased. For example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD section **101** to the photoelectric conversion cell is only about 5%. Therefore, it is difficult to ensure a sufficiently large area of opening of the PD section **101** and also to reduce the size of the photoelectric conversion cell.

SUMMARY OF THE INVENTION

It is an object of the present invention to solve the above-described problems and, to reduce, in a FDA (floating diffusion amplifier) system, the size of a photoelectric conversion cell while increasing an aperture area of a photoelectric conversion section.

To achieve the above-described object, the present invention has been devised, so that a configuration in which a transistor and an interconnect can be shared by a plurality of photoelectric conversion (PD) sections is used in a solid state imaging apparatus.

Specifically, a first solid sate imaging apparatus includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections which are included in the same row; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. In the apparatus, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

In the first solid imaging apparatus, each said floating diffusion section is shared by ones of the photoelectric conversion sections included in the same row, and furthermore, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections. Thus, the number of read-out lines per photoelectric conversion cell becomes 0.5. As a result, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in the same column. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in the same column can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

Moreover, in the first solid state imaging apparatus, it is preferable that wherein each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in two adjacent columns, respectively. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in two adjacent columns, respectively, can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by a row which is read out by a transfer transistor connected to one of the read-out line and another row which is adjacent to the read-out row.

It is preferable that the first solid state imaging apparatus further includes: a signal line for outputting a signal from each said pixel amplifier transistor to the outside; and a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line. Thus, charges from one of the photoelectric conversion sections which are included in adjacent rows, respectively, can be detected through a shared signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by photoelectric conversion sections which are adjacent to each other in the row direction or in the column direction. Thus, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that in each said floating diffusion section, a reset section for resetting charge stored in the floating diffusion section is provided. Thus, it is possible to stop, after charge read out from a photoelectric conversion section has been detected by an amplifier, detection of charge by the pixel amplifier transistor.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction. Thus, a high quality image can be obtained from signals read out from the photoelectric conversion sections.

It is preferable that the first solid state imaging apparatus further includes a signal processing circuit for processing an output signal from each said pixel amplifier transistor. Thus, a high quality image can be obtained.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film. Thus, a power supply line can be formed in a different interconnect layer from an interconnect layer in which an output signal line connected to a pixel amplifier transistor is formed. Therefore, the size of a photoelectric conversion cell can be further reduced and also the aperture area can be increased.

A method for driving a solid state imaging apparatus according to the present invention is directed to a method for driving the first solid state imaging apparatus of the present invention and includes: a first step of transferring, in each said photoelectric conversion cell, by a first read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which are not included in the same row but included in two columns adjacent to each other, respectively, to one of the floating diffusion sections connected to said ones of the photoelectric conversion sections; and a second step of transferring, by a second read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which have not been read out in the first step to the same floating diffusion section connected to said ones of the photoelectric conversion sections as that in the first step.

A second solid state imaging apparatus according to the present invention includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows; a plurality of floating diffusion sections each being connected, via each of a plurality of transfer transistors, to each of ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same column in each said photoelectric conversion cell, and each being shared by said ones of the photoelectric conversion sections; a plurality of read-out lines each being connected to one of the transfer transistors and independently reading out charge from each of said ones of the photoelectric conversion sections to each said floating diffusion section shared by said ones of the photoelectric conversion sections; and a plurality of pixel amplifier transistors each detecting and outputting the potential of the floating diffusion section.

In the second solid state apparatus, each said floating diffusion section is connected to some of the plurality of transfer transistors, is shared by ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same. Furthermore, some of the plurality of read-out lines each independently reading out charge from each of said ones of the photoelectric conversion sections are connected to each said transfer transistor. Thus, a row-select transistor which is usually provided is not needed. As a result, the number of interconnects per photoelectric conversion section is reduced from 5 to 3.5. Therefore, the area of the photoelectric conversion cell itself can be reduced while increasing the area of the photoelectric sections.

It is preferable that the second solid state imaging apparatus further includes a reset transistor for resetting charge stored in each said floating diffusion section and the drain of the reset transistor is connected to the drain of the pixel amplifier transistor so that a drain is shared by the reset transistor and the pixel amplifier transistor. Thus, an interconnect connecting between the drain of the reset transistor and the drain of the pixel amplifier transistor can be shared. Accordingly, the number of interconnects per the photoelectric conversion cell can be further reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion sections which are adjacent to each other in the row direction in each said photoelectric conversion cell. Thus, the area of floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and a gate of the MIS transistor is arranged in the column direction. Thus, each said the read-out line can be also function as an interconnect of a transfer transistor, so that the area of the read-out lines occupying the photoelectric conversion cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the area of the pixel amplifier transistor per photoelectric conversion cell can be reduced whereas the area of the photoelectric conversion sections can be increased. Therefore, light sensitivity is increased.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor and each said floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect connecting between the pixel amplifier transistor and the floating diffusion section can be shortened, so that the areas of the pixel amplifier transistor and the floating diffusion section per photoelectric conversion cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between ones of the photoelectric cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so as to

have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

Moreover, in the second solid state imaging apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and each said pixel amplifier transistor is arranged between respective gates of the MIS transistor and another MIS transistor. Thus, an empty region located in an area of the cell in which a row and a column intersect to each other can be utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the area of the reset transistors per photoelectric conversion section can be reduced. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said pixel amplifier transistor and the floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect between the floating diffusion section can be omitted and the source of the reset transistor and the floating diffusion section can be connected to each other to be shared. Therefore, the areas of the reset transistors and the floating diffusion sections per photoelectric conversion cell can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is connected to a line arranged between ones of the photoelectric cells which are adjacent to each other in the row direction. Thus, pitches of the photoelectric sections in row directions can be matched in a simple manner, so that resolution is improved.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so as to have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

In this case, it is preferable that each said transfer transistor is made of an MIS transistor, and each said reset transistor is arranged between respective gate of the MIS transistor and another MIS transistor. Thus, an empty region located in an area of the cell in which a row and a column intersect to each other can be utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, the area of the floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in at least one of the row direction and the column direction. Thus, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that the line connecting respective drains of the reset transistor and the pixel amplifier transistor also functions as a light-shielding film. Thus, the number of interconnects per photoelectric conversion cell can be reduced. Therefore, the area of the photoelectric sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

It is preferable that each of the first and second solid state imaging apparatus further includes a signal processing circuit for processing an output signal output from each said pixel amplifier transistor. Thus, a high resolution image can be obtained.

A camera according to the present invention includes the first or second solid state imaging apparatus of the present invention. Thus, the camera of the present invention can achieve a high resolution image.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a first embodiment of the present invention.

FIG. **2** is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment.

FIG. **3** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment.

FIG. **4** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a second embodiment of the present invention.

FIG. **5** is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment.

FIG. **6** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention.

FIG. **7** is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment.

FIG. **8** is a plane view schematically illustrating a layout of the photoelectric conversion cell in the solid state imaging apparatus of the third embodiment.

FIG. **9** is a table showing the aperture ratio of PD sections to a photoelectric conversion cell in each of regions A through E of FIG. **8** where a transistor and the like are arranged.

FIG. **10** is a circuit diagram illustrating a photoelectric conversion cell in a known solid imaging apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

A first embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **1** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to the first embodiment of the present invention.

As shown in FIG. **1**, for example, photoelectric conversion (PD) sections **1**, **2**, **3** and **4** each of which is made of a photodiode and converts incident light to electric energy are arranged in this order in the row direction. Furthermore, PD sections **5**, **6**, **7** and **8** are arranged in this order in the row direction so that the PD sections **5**, **6**, **7** and **8** are adjacent to the PD sections **1**, **2**, **3** and **4**, respectively, in the column direction.

Here, in this application, the row direction means to be the direction in which a row number increases and the column direction means to be the direction in which a column number increases.

Between the first and 0^{th} rows (not shown), a first floating diffusion (FD) section **9** for storing photoelectric-converted charges from the PD sections **1** and **5** included in the first row and PD sections included in the 0^{th} row is provided. Between the second and third rows, a second floating diffusion section **10** for storing photoelectric-converted charges from the PD sections **2** and **6** included in the second row and the PD sections **3** and **7** included in the third row is provided so as to be surrounded by the PD sections **2**, **3**, **6** and **7**. Between the fourth and fifth rows (not shown), a third floating diffusion section **11** for storing photoelectric-converted charges from the PD sections **4** and **8** included in the fourth row and PD sections included in the fifth row is provided. In this manner, each of the FD sections **9**, **10** and **11** is shared by four PD sections.

In this case, a cell including the PD sections **1**, **2**, **5** and **6** is a first photoelectric conversion cell **91** and a cell including the PD sections **3**, **4**, **7** and **8** is a second photoelectric conversion cell **92**.

In the first photoelectric conversion cell **91**, a transfer transistor **13** made of an N channel FET for transferring charge from the PD section **1** to the first FD section **9** is connected between the PD section **1** included in the first row and the first FD section **9**, and a transfer transistor **17** made of an N channel FET for transferring charge from the PD section **5** to the first FD section **9** is connected between the PD section **5** and the first FD section **9**.

Moreover, in the first photoelectric conversion cell **91**, a transfer transistor **14** made of an N channel FET for transferring charges from the PD section **2** to the second FD section **10** is connected between the PD section **2** included in the second row and the second FD section **10**, and a transfer transistor **18** made of an N channel FET for transferring charges from the PD section **6** to the second FD section **10** is connected between the PD section **6** and the second FD section **10**.

As a characteristic of the first embodiment, the transfer transistor **13** included in the first row and the transfer transistor **14** included in the second row are connected to a first read-out (READ) line **32** while the transfer transistor **17** included in the first row and the transfer transistor **18** included in the second row are connected to a second READ line **33**.

In the second photoelectric conversion cell **92**, a transfer transistor **15** made of an N channel FET for transferring charge from the PD section **3** to the second FD section **10** is connected between the PD section **3** included in the third row and the second FD section **10**, and a transfer transistor **19** made of an N channel FET for transferring charge from the PD section **7** to the second FD section **10** is connected between the PD section **7** and the second FD section **10**.

Moreover, in the second photoelectric conversion cell **92**, a transfer transistor **16** made of an N channel FET for transferring charges from the PD section **4** to the third FD section **11** is connected between the PD section **4** included in the fourth row and the third FD section **11**, and a transfer transistor **20** made of an N channel FET for transferring charges from the PD section **8** to the third FD section **11** is connected between the PD section **8** and the third FD section **11**.

Also, in this cell, the transfer transistor **15** included in the third row and the transfer transistor **16** included in the fourth row are connected to the third READ line **34** while the transfer transistor **19** included in the third row and the transfer transistor **20** are connected to the fourth READ line **35**.

To the first FD section **9**, a first reset transistor **21** made of an N channel FET is connected. The first reset transistor **21** includes a source connected to the first FD section **9**, a drain connected to a photoelectric conversion cell power supply (VDDCELL) line **31** and a gate connected to a first reset pulse (RSCELL) line **36**. Thus, charge stored in the first FD section **9** is made to flow through the VDDCELL line **31** by a RSCELL signal.

In the same manner, a second reset transistor **22** made of an N channel FET is connected to the second FD section **10**. The second reset transistor **22** includes a source connected to the second FD section **10**, a drain connected to the VDDCELL line **31** and a gate connected to a second RSCELL line **37**. Note that although not shown in FIG. **1**, a reset transistor of the same configuration as that of the first reset transistor **21** or the like is provided in the third FD section **11**.

To the first FD section **9** and the first reset transistor **21**, a first pixel amplifier transistor **23** made of an N channel FET is connected. The first pixel amplifier transistor **23** includes a gate connected to the first FD section **9**, a drain connected to the VDDCELL line **31** and a source connected to a first output signal (VO) line **38**.

In the same manner, a second pixel amplifier transistor **24** made of an N channel FET is connected to the second FD section **10** and the second reset transistor **22**. The second pixel amplifier transistor **24** includes a gate connected to the second FD section **10**, a drain connected to the VDDCELL line **31** and a source connected to a second VO line **39**.

The first VO line **38** and the second VO line **39** are connected to not only the pixel amplifier transistors **23** and **24**, respectively, but also first and second load transistors **25** and **26**, respectively. Each of the first and second load transistor **25** and **26** is made of an N channel for constituting a source follower amplifier. A load gate (LGCELL) line **40** is connected to each of the gates of the first and second load transistors **25** and **26**. A source power supply (SCLL) line **41** is connected to each of the respective drains of first and second load transistors **25** and **26**.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **2** is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment. In this case, a series of operations is completed in a horizontal blanking period (=1 H).

Moreover, as for the detection order of signal charges from the PD sections **1** through **8** arranged in an array, detection is simultaneously carried out in the first and second rows and then detection is simultaneously carried out in the third and fourth rows.

As shown in FIG. **2**, first, high level voltage is applied to the LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source, and then during a period in which the potential of the VDDCELL line **31** is high level, each of the RSCELL lines **36** and **37** is set to be a high level in a pulse state to temporarily turn each of the reset transistors **21** and **220**N. Thus, each of charges stored in the first FD section **9** in the first photoelectric conversion cell **91** and in the second FD section **10** in the second photoelectric conversion cell **92** is made to flow through the VDDCELL line **31**. In this case, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to

the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **2** is transferred to the second FD section **10**. For charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

Subsequently, when the VDDCELL line **31** is turned to be in a low level OFF state and each of the RSCELL lines **36** and **37** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **10** becomes in the same OFF level state as that of the VDDCELL line **31**. Thus, each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **24** is not operated and thus the vertical line scanning circuit is in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at a reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **17** and **18** ON. Thus, charge stored in the PD section **5** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the second FD section **10**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

In this manner, charges detected during the first horizontal blanking period **1**H and charges detected during the second horizontal blanking period **2**H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges.

Subsequently, by driving the PD sections in the third and fourth rows in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

Note that in the first embodiment, the circuit configuration and driving method in which after every second column, i.e., every odd-numbered column including the PD sections **1** and **2** have been read out, charges in every even-numbered column including the PD sections **5** and **6** are detected have been described. However, this embodiment is not limited thereto but READ lines can be increased to detect charge in every third column at the same timing as described above:

In the solid state imaging apparatus of the first embodiment, as shown in the circuit configuration of FIG. **1**, for example, four PD sections share a FD section, a pixel amplifier transistor and a reset transistor. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 1.5. The number of interconnects can be reduced from 5 (required in the known solid state imaging apparatus) to 2.5. For example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections to the photoelectric conversion cell is about 35%. Therefore, it is possible to reduce the cell sizes of the photoelectric conversion cells **91** and **92** and to largely increase the aperture ratio of the PD section at the same time.

In this connection, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are detected by a READ line at the same timing is applied to the known circuit configuration. If a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 10%.

Moreover, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are read out by a READ line, and a FD section and a pixel amplifier transistor included in a row which adjacent to an unread row in a photoelectric conversion cell are shared by two photoelectric sections to detect signal charge is applied to the known circuit configuration. With a driving method in which signal charges are simultaneously detected in the two photoelectric conversion sections, for example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 15%.

Modified Example of First Embodiment

FIG. **3** is a diagram illustrating a circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment of the present invention. Also, in this modified example, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. **3**, for example, in the first photoelectric conversion cell **91**, the first READ line **32** is connected to the transfer transistor **13** and the transfer transistor **18** included in adjacent columns, respectively, while the second READ line **33** is connected to the transfer transistor **14** and the transfer transistor **17** included in adjacent columns, respectively. Thus, even if connections are made with respect to the PD sections **1**, **2**, **5** and **6** included in two adjacent rows with the first and second READ lines **32** and **33** interposed between the PD sections **1** and **5** and the PD sections **2** and **6** so that signal charges from the PD sections which are not included in

the same columns are transferred, charge can be detected at the same timing as that shown in FIG. **2**.

For example, when the first READ line **32** is temporarily turned ON, signal charge is transferred from the PD section **1** to the first FD section **9** via the transfer transistor **13** and, at the same time, signal charge is transferred from the PD section **6** to the second FD section **10** via the transfer transistor **18**.

Note that in the modified example of the first embodiment, signal charges from two of the four PD sections included in a photoelectric conversion cell **91** are read out during the horizontal blanking period **1**H. However, instead of this, signal charges from all of the four PD sections may be read out.

Moreover, by performing signal processing to signal charges from all of the photoelectric conversion cells which have been read out during different horizontal blanking periods, a high quality image with a large number of pixels can be obtained.

Second Embodiment

Hereinafter, a second embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **4** is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a second embodiment of the present invention. In FIG. **4**, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

First, differences of the solid state imaging apparatus of FIG. **4** from that of the first embodiment shown in FIG. **1** will be described.

In the second embodiment, an configuration in which the first and second pixel amplifier transistors **23** and **24** are connected to the first and second output signal (VO) lines **38** and **39**, respectively, via the first and second select transistors **52** and **53** each of which made of an N channel FET, respectively, is used.

To the respective gates of the first and second select transistors **52** and **53**, first and second select (SO) lines **50** and **51** to which a switching pulse is applied are connected, respectively.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **5** is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment. In this case, a series of operations is completed in a horizontal blanking period (=1 H).

As shown in FIG. **5**, first, a predetermined voltage is applied to the LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source and the potential of the VDDCELL line **31** is set to be a high level. Subsequently, each of the RSCELL lines **36** and **37** is set to be a high level in a pulse state to temporarily turn each of the reset transistors **21** and **22** ON. Thus, each of charges stored in the first FD section **9** and in the second FD section **10** is made to flow through the VDDCELL line **31**. In this case, in each of the pixel amplifier transistors **23** and **24**, each of the select transistors **52** and **53** has been turned ON in advance, so that a signal level at a reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **2** is transferred to the second FD section **10**. Thereafter, for charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively.

Subsequently, by changing each of the first and second SO lines **50** and **51** to a high level to keep the first and second transistors **52** and **53** ON, stored charge signals of the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24** are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit.

Thereafter, each of the first and second SO lines **50** and **51** is set back to be a low level to turn the first and second select transistors **52** and **53** OFF, so that each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** is selected, each of the pixel amplifier transistors **23** and **24** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of the FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **17** and **18** ON. Thus, charge stored in the PD section **5** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the second FD section **10**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the stored signals whose voltage level have been detected selectively conducts the first and second VO lines **38** and **39** and are introduced to the noise cancellation circuit. Then, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

Thus, with the first and second select transistors **52** and **53** between the FD section **9** and the first VO line **38** and between the FD section **10** and the second VO line **39**, respectively. Thus, the number of transistors per photoelectric conversion cell is 1.75. Moreover, the number of interconnects is 2.75. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells **91** and **92** and also to largely improve the aperture ratio of PD sections.

Note that also in the second embodiment, as in the modified example of the first embodiment, for example, a configuration in which the transfer transistor **13** and the transfer transistor **18** located diagonally to the transfer transistor **13** are connected to the first READ line **32**, and the transfer transistor **14**

and the transfer transistor **17** located diagonally to the transfer transistor **14** are connected to the second READ line **33** may be used.

Moreover, in the photoelectric conversion cell **91**, the PD sections are arranged in two rows and two columns. However, the present invention is not limited thereto, but the PD sections may be arranged in two rows and three columns and, furthermore, may be arranged in three or more rows and three or more columns.

Third Embodiment

Hereinafter, a third embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **6** is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention. In FIG. **6**, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. **6**, in the solid state imaging apparatus of the third embodiment, first through fourth photoelectric conversion cells **91**, **92**, **93** and **94** are arranged in a matrix.

For example, the first photoelectric conversion cell **91** includes photoelectric conversion (PD) sections **1** and **2** arranged in regions which is located in the first column of an array and the first row and which is located in the first column of and the second rows of the array, respectively. The PD sections **1** and **2** share a first FD section **9** via transfer transistors **13** and **14** each of which is made of an N channel FET, respectively.

To the first FD section **9**, the first reset transistor **21** made of an N channel FET is connected. The first reset transistor **21** includes a source connected to the first FD section **9**, a drain connected to the first FD section **9** and a gate connected to a first RSCELL line **36**. Thus, charge stored in the first FD section **9** is made to flow through a first VDDCELL line **30** by a RSCELL signal.

To the first FD section **9** and the first reset transistor **21**, a first pixel amplifier transistor **23** of an N channel FET is connected. The first pixel amplifier transistor made of an N channel FET includes a gate connected to the first FD section **9**, a drain connected to the first VDDCELL line **30** and a source connected to a first VO line **38**.

In the same manner, PD sections **3** and **4** arranged in regions of an array forming a second photoelectric conversion cell **92** which is located in the first column and the third row and which is located in the first column and the fourth row, respectively, share a second FD section **10** via transfer transistors **15** and **16**, respectively. A second reset transistor **22** selectively conducts the second FD section **10** and the first VDDCELL line **30**. Moreover, a second pixel amplifier transistor **24** which receives the signal potential of the second FD section **10** at the gate and receives the power supply potential of the first VDDCELL line **30** at the drain outputs a detected signal corresponding to a received signal potential to the first VO line **38**.

PD sections **5** and **6** arranged in regions of an array forming a third photoelectric conversion cell **93** which is located in the second column and the first row and which is located in the second column and the second row, respectively, share a third FD section **11** via transfer transistors **17** and **18**, respectively. A third reset transistor **61** selectively conducts the third FD section **11** and a second VDDCELL line **31**. Moreover, a third pixel amplifier transistor **63** which receives the signal potential of the third FD section **11** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs a detected signal corresponding to a received signal potential to a second VO line **39**.

PD sections **7** and **8** arranged in regions of an array forming a fourth photoelectric conversion cell **94** which is located in the second column and the third row and which is located in the second column and the fourth row, respectively, share a fourth FD section **12** via transfer transistors **19** and **20**, respectively. A fourth reset transistor **62** selectively conducts the fourth FD section **12** and a second VDDCELL line **31**. Moreover, a fourth pixel amplifier transistor **64** which receives the signal potential of the fourth FD section **12** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs a detected signal corresponding to a received signal potential to a second VO line **39**.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **7** is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment. In this case, a series of operations is completed in a horizontal blanking period (=1 H).

Moreover, as for the detection order of signal charges from the PD sections **1** through **8** arranged in an array, detection is carried out sequentially from the first row to the second row and so on.

As shown in FIG. **7**, first, high level voltage is applied to a LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source, and then during a period in which the potentials of the first VDDCELL line **30** and the VDDCELL line **31** are set to be high level, the first RSCELL lines **36** is set to be high level in a pulse state to temporarily turn each of the reset transistors **21** and **61** ON. Thus, charges stored in the first FD section **9** in the first photoelectric conversion cell **91** and in the third FD section **11** in the third photoelectric conversion cell **93** are made to flow through the first VDDCELL line **30** and the VDDCELL line **31**, respectively. In this case, in each of the pixel amplifier transistors **23** and **63**, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **61** has been turned OFF, high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **5** in the second row is transferred to the third FD section **11**. For charges transferred to the first FD section **9** and the third FD section **11**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the third pixel amplifier transistor **63**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **63** can be detected.

Subsequently, when each of the VDDCELL lines **30** and **31** is turned to be in a low level OFF state and the first RSCELL line **36** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **11** becomes in the same

OFF level state as that of each of the VDDCELL lines **30** and **31**. Then, each of the pixel amplifier transistors **23** and **63** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL line **36** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **63** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **61** is temporarily turned ON to reset charges of the FD sections **9** and **11**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **63**, a signal level at the reset time is detected, detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **61** has bee turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **14** and **18** ON. Thus, charge stored in the PD section **2** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the third FD section **11**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the third FD section **11**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the third pixel amplifier transistor **63**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **63** can be detected.

In this manner, charges detected during the first horizontal blanking period **1**H and charges detected during the second horizontal blanking period **2**H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges. Thus, in the third embodiment, for example, the power supply potentials which are to be applied to the respective drains of the first reset transistor **21** and the first pixel amplifier transistor **23** vary in the same manner. Therefore, the known row selection transistor **152** is not necessarily provided.

Subsequently, if the PD sections in the third and fourth rows are driven in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

As has been described, the solid state imaging apparatus of the third embodiment has, for example, a configuration in which the two PD sections **1** and **2** share the first FD section **9**, the first pixel amplifier transistor **23** and the first reset transistor **21**. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 2. Moreover, the number of interconnects can be reduced from 5 (required in the known apparatus) to 3.5. Accordingly, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD sections **1** and **2** is about 30%. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells and also to largely improve the aperture ratio of the PD section.

Note that each of the reset transistors **21**, **22**, **61** and **62** is made of an N channel type MOS transistor. However, in each of the reset transistors **21**, **22**, **61** and **62** made of, instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second RSCELL lines **36** and **37**, each of the reset transistors **21**, **22**, **61** and **62** is turned ON.

In the same manner, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is made of an N channel type MOS transistor. However, in each of the pixel amplifier transistors **23**, **24**, **63** and **64** made of, instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second VDDVELL lines **30** and **31**, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is turned ON to be in a potential detection period in which signal potentials from the corresponding FD sections **9**, **10**, **11** and **12** are detected.

Hereinafter, in the layout in which each of the PD sections **1**, **2**, **3**, **5**, **6** and **7** arranged as shown in FIG. **8**, a region of the cell located between the PD sections **1** and **2** is referred to as an "A region"; a region of the cell surrounded by the PD sections **1**, **2**, **5** and **6** is referred to as a "B region"; a region of the cell located between the PD sections **5** and **6** is referred to as a "C region"; a region of the cell located between the PD sections **2** and **6** is referred to as a "D region"; and a region of the cell located between the PD sections **1** and **5** is referred to as an "E region". Then, by arranging the FD sections **9** and **11**, the pixel amplifier transistors **23** and **63**, and the reset transistors **21** and **61** in regions in the cell indicated in the FIG. **9**, respectively, the aperture ratio of the PD sections to the photoelectric conversion cell can be improved in any case, compared to the known solid state imaging apparatus. Moreover, the size of the cell can be reduced.

Furthermore, as also shown in FIG. **9**, if the FD sections **9** and **11** are arranged in the A and C regions, respectively, the aperture of the PD sections can be improved to be about 30% by arranging in parallel the READ lines **32** and **33** for driving the transfer transistors **13** and **14**, respectively.

Moreover, as shown in FIG. **9**, for example, the aperture of the PD sections can be improved to be about 30% by arranging the first RSCELL line **36** between the PD sections **2** and **3**.

Moreover, as shown in FIG. **8**, by arranging the PD sections so as to be spaced apart from one another by a certain distance at least in one of the row direction and the column direction, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

Moreover, although not shown in the drawings, by using the first VDDCELL line **30** and the second VDDCELL line **31** as light-shielding films for separating the photoelectric conversion cells from one another, the first VO line **38** and the second VO line **39** can be formed in different interconnect layers. Thus, the sizes of the photoelectric conversion cells **91** and **92** can be reduced and also the aperture area of the PD sections can be increased.

Moreover, with the solid state imaging apparatus of any one of the first through third embodiments, a camera which is small-sized and provides a high resolution image can be obtained.

What is claimed is:

1. A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of reset pulse lines each being connected to at least one of the plurality of reset transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion section,

wherein the plurality of photodiodes includes a first photodiode, a second photodiode and a third photodiode,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the third photodiode is in row n+2,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the first read-out line and the second read-out line are disposed between the row n and the row n+1,

one of the plurality of reset pulse lines is disposed between the row n+1 and the row n+2,

one of the plurality of pixel amplifier transistors is disposed between the row n+1 and the row n+2.

2. The solid state imaging apparatus of claim **1**, wherein each of said plurality of read-out lines is connected to two of the plurality of transfer transistors which are included in the same column.

3. The solid state imaging apparatus of claim **1**, wherein each of said plurality of read-out lines is connected to two of the plurality of transfer transistors which are not included in the same column.

4. The solid state imaging apparatus of claim **1**, wherein each of said plurality of floating diffusion sections is shared by said ones of the plurality of photodiodes which are adjacent to each other in the column direction.

5. A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of reset pulse lines each being connected to at least one of the plurality of reset transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion section,

wherein the plurality of photodiodes includes a first photodiode, a second photodiode and a third photodiode,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the third photodiode is in row n+2,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the first read-out line and the second read-out line are disposed between the row n and the row n+1,

one of the plurality of reset pulse lines is disposed between the row n+1 and the row n+2, and

the first and second photodiodes do not share each said floating diffusion section.

6. The solid state imaging apparatus of claim **5**, wherein each of said plurality of read-out lines is connected to two of the plurality of transfer transistors which are included in the same column.

7. The solid state imaging apparatus of claim **5**, wherein each of said plurality of read-out lines is connected to two of the plurality of transfer transistors which are not included in the same column.

8. The solid state imaging apparatus of claim **5**, wherein each of said plurality of floating diffusion sections is shared by said ones of the plurality of photodiodes which are adjacent to each other in the column direction.

9. A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of reset pulse lines each being connected to at least one of the plurality of reset transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion section,

wherein the plurality of photodiodes includes a first photodiode, a second photodiode and a third photodiode,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the third photodiode is in row n+2,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the first read-out line and the second read-out line are disposed between the row n and the row n+1,

one of the plurality of reset pulse lines is disposed between the row n+1 and the row n+2, and

each said pixel amplifier transistor is disposed between adjacent rows.

10. The solid state imaging apparatus of claim **9**, wherein each of said plurality of read-out lines is connected to two of the plurality of transfer transistors which are included in the same column.

11. The solid state imaging apparatus of claim **9**, wherein each of said plurality of read-out lines is connected to two of the plurality of transfer transistors which are not included in the same column.

12. The solid state imaging apparatus of claim **9**, wherein each of said plurality of floating diffusion sections is shared by said ones of the plurality of photodiodes which are adjacent to each other in the column direction.

* * * * *

Docket No.: 079195-0551 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Mitsuyoshi MORI, et al.	:	Confirmation Number: 5957
Application No.: 12/178,250	:	Group Art Unit: 2814
Filed: July 23, 2008	:	Examiner: INGHAM, JOHN C.

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated September 17, 2010, having a three-month shortened statutory period for response set to expire on December 17, 2010, reconsideration of the above-identified application is respectfully requested in view of the following amendment and remarks.

AMENDMENT TO THE SPECIFICATION

Please amend the paragraph beginning on page 2, line 22 as follows:

To achieve the above-described object, the present invention has been devised ~~deviced~~, so that a configuration in which a transistor and an interconnect can be shared by a plurality of photoelectric conversion (PD) sections is used in a solid state imaging apparatus.

AMENDMENT TO THE CLAIMS

1-30. (Cancelled)

31. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes ~~photoelectric conversion cells each including a plurality of photoelectric conversion sections~~ arranged in an array ~~of at least two rows and one column~~;

a plurality of floating diffusion sections each being connected to ~~each of~~ ones of the photodiodes ~~photoelectric conversion sections which are included in each said photoelectric conversion cell~~ via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion section,

wherein the plurality of photodiodes includes a first photodiode, a second photodiode and a third photodiode,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the third photodiode is in row n+2,

the first, second and third photodiodes are in the same column,

the plurality of read-out lines are disposed between the first and second photodiodes ~~within the photoelectric conversion cells~~, and

one of the plurality of ~~each said~~ pixel amplifier ~~transistor~~ transistors is disposed between the second and third photodiodes ~~arranged between ones of the photoelectric conversion cells which are adjacent to each other in the row direction~~.

32. (Canceled)

33. (Previously presented) The solid state imaging apparatus of claim 31, wherein each said read-out line is connected to two of the transfer transistors which are included in the same column.

34. (Previously presented) The solid state imaging apparatus of claim 31, wherein each said read-out line is connected to two of the transfer transistors which are not included in the same column.

35. (Currently amended) The solid state imaging apparatus of claim 31, wherein each said floating diffusion ~~sections~~ section is shared by said ones of the photodiodes ~~photoelectric conversion sections~~ which are adjacent to each other in the column direction.

36. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes ~~photoelectric conversion cells each including a plurality of photoelectric conversion sections~~ arranged in an array ~~of at least two rows and one column~~;

a plurality of floating diffusion sections each being connected to ~~each of~~ ones of the photodiodes ~~photoelectric conversion sections which are included in each said photoelectric conversion cell~~ via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion section,

wherein the plurality of photodiodes includes a first photodiode, a second photodiode and a third photodiode,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the third photodiode is in row n+2,

the first, second and third photodiodes are in the same column, and

the plurality of read-out lines are disposed between the first and second photodiodes ~~ones of photoelectric conversion sections~~ which are adjacent to each other in the row direction ~~in the same column~~ and do not share each said floating diffusion section.

37. (Canceled)

38. (Previously presented) The solid state imaging apparatus of claim 36, wherein each said read-out line is connected to two of the transfer transistors which are included in the same column.

39. (Previously presented) The solid state imaging apparatus of claim 36, wherein each said read-out line is connected to two of the transfer transistors which are not included in the same column.

40. (Currently amended) The solid state imaging apparatus of claim 36, wherein each said floating diffusion section ~~sections~~ is shared by said ones of the photodiodes ~~photoelectric conversion sections~~ which are adjacent to each other in the column direction.

41. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes ~~photoelectric conversion cells each including a plurality of photoelectric conversion sections~~ arranged in an array ~~of at least two rows and one column~~;

a plurality of floating diffusion sections each being connected to ~~each of~~ ones of the photodiodes ~~photoelectric conversion sections which are included in each said photoelectric conversion cell~~ via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion section,

wherein the plurality of photodiodes includes a first photodiode, a second photodiode and a third photodiode,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the third photodiode is in row n+2,

the first, second and third photodiodes are in the same column,

the plurality of read-out lines are disposed between the first and second photodiodes, and

each said pixel amplifier transistor is disposed between ones of photodiodes ~~photoelectric conversion sections~~ which are adjacent to each other in the row direction in the same column and share each said floating diffusion section.

42. (Canceled)

43. (Previously presented) The solid state imaging apparatus of claim 41, wherein each said read-out line is connected to two of the transfer transistors which are included in the same column.

44. (Previously presented) The solid state imaging apparatus of claim 41, wherein each said read-out line is connected to two of the transfer transistors which are not included in the same column.

45. (Currently amended) The solid state imaging apparatus of claim 41, wherein each said floating diffusion section ~~sections~~ is shared by said ones of the photodiodes ~~photoelectric conversion sections~~ which are adjacent to each other in the column direction.

REMARKS

Claims 31, 36 and 41 are independent and stand rejected under 35 U.S.C. § 102 as being anticipated by Kochi '131 ("Kochi"). This rejection is respectfully traversed for the following reasons.

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Ingham. As a result of the interview, it was tentatively agreed that the enclosed amendment overcomes the pending rejections. Examiner Ingham indicated that he would conduct an updated prior art search and reconsideration, after which a final decision would be made. Applicants and Applicants' representative would like to thank Examiner Ingham for his courtesy in conducting the interview and for his assistance in resolving issues. A summary of the interview discussion follows.

Each of claims 31, 36 and 41 recites in pertinent part, "a first photodiode, a second photodiode and a third photodiode, the first photodiode is in row n, the second photodiode is in row n+1, the third photodiode is in row n+2, the first, second and third photodiodes are in the same column, [and] the ***plurality*** of read-out lines are disposed between the first and second photodiodes" (emphasis added). According to one aspect of the present invention, such a configuration can make it possible to reduce the size of a photoelectric conversion cell while nonetheless increasing an aperture area of a photoelectric conversion section.

In contrast, as shown in Figure 1 thereof, Kochi discloses a conventional read-out line arrangement in which the alleged plurality of read-out lines tx12, tx22 are not disposed between the alleged first and second photodiodes 1-1, 1-2. In the conventional arrangement of Kochi, each read-out line is connected to the alleged transfer transistors only in the column direction so that a *single* read-out line is disposed between respective photodiodes. Accordingly, there is no

disclosed need or desire to arrange at least two read-out lines between two photodiodes in the same column and adjacent in the row direction. Indeed, Kochi is at best cumulative to Applicants' admitted prior art illustrated in Figure 10 of Applicants' drawings. Only Applicants have recognized and considered the aforementioned dual effects, and conceived of the novel and non-obvious configuration which can make it possible to realize said effects.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Kochi does not anticipate claims 31, 36 and 41, nor any claim dependent thereon.

"All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 165 USPQ 494, 496 (CCPA 1970).

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 31, 36 and 41 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102/103 be withdrawn.

Application No.: 12/178,250

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Docket No.: 079195-0551 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Mitsuyoshi MORI, et al.	:	Confirmation Number: 5957
Application No.: 12/178,250	:	Group Art Unit: 2814
Filed: July 23, 2008	:	Examiner: INGHAM, JOHN C.

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

AMENDMENT

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated February 14, 2011, having a three-month shortened statutory period for response set to expire on May 14, 2011 (Saturday), reconsideration of the above-identified application is respectfully requested in view of the following amendment and remarks.

AMENDMENT TO THE CLAIMS

1-30. (Cancelled)

31. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; [[and]]

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of reset pulse lines each being connected to at least one of the plurality of reset transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion section,

wherein the plurality of photodiodes includes a first photodiode, a second photodiode and a third photodiode,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the third photodiode is in row n+2,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the first read-out line and the second read-out line are disposed between the row n and the row n+1,

one of the plurality of reset pulse lines is disposed between the row n+1 and the row n+2,

~~the first, second and third photodiodes are in the same column,~~

~~the plurality of read-out lines are disposed between the first and second photodiodes,~~ and

one of the plurality of pixel amplifier transistors is disposed between the row n+1 ~~second~~ and the row n+2 ~~third photodiodes~~.

32. (Canceled)

33. (Currently amended) The solid state imaging apparatus of claim 31, wherein each of said plurality of read-out [[line]] lines is connected to two of the plurality of transfer transistors which are included in the same column.

34. (Currently amended) The solid state imaging apparatus of claim 31, wherein each of said plurality of read-out [[line]] lines is connected to two of the plurality of transfer transistors which are not included in the same column.

35. (Currently amended) The solid state imaging apparatus of claim 31, wherein each of said plurality of floating diffusion ~~section~~ sections is shared by said ones of the plurality of photodiodes which are adjacent to each other in the column direction.

36. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; [[and]]

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of reset pulse lines each being connected to at least one of the plurality of reset transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion section,

wherein the plurality of photodiodes includes a first photodiode, a second photodiode and a third photodiode,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the third photodiode is in row n+2,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the first read-out line and the second read-out line are disposed between the row n and the row n+1,

one of the plurality of reset pulse lines is disposed between the row n+1 and the row n+2, and

~~the first, second and third photodiodes are in the same column, and~~

~~the plurality of read-out lines are disposed between~~ the first and second photodiodes ~~which are adjacent to each other in the row direction and~~ do not share each said floating diffusion section.

37. (Canceled)

38. (Currently amended) The solid state imaging apparatus of claim 36, wherein each of said plurality of read-out [[line]] lines is connected to two of the plurality of transfer transistors which are included in the same column.

39. (Currently amended) The solid state imaging apparatus of claim 36, wherein each of said plurality of read-out [[line]] lines is connected to two of the plurality of transfer transistors which are not included in the same column.

40. (Currently amended) The solid state imaging apparatus of claim 36, wherein each of said plurality of floating diffusion ~~section~~ sections is shared by said ones of the plurality of photodiodes which are adjacent to each other in the column direction.

41. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; [[and]]

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of reset pulse lines each being connected to at least one of the plurality of reset transistors; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion section,

wherein the plurality of photodiodes includes a first photodiode, a second photodiode and a third photodiode,

the first photodiode is in row n, where n is a positive integer,

the second photodiode is in row n+1,

the third photodiode is in row n+2,

the plurality of read-out lines includes a first read-out line and a second read-out line,

the first read-out line and the second read-out line are disposed between the row n and the row n+1,

one of the plurality of reset pulse lines is disposed between the row n+1 and the row n+2,

~~the first, second and third photodiodes are in the same column,~~

~~the plurality of read-out lines are disposed between the first and second photodiodes,~~ and

each said pixel amplifier transistor is disposed between ~~ones of photodiodes which are~~ adjacent rows ~~to each other in the row direction in the same column and share each said floating diffusion section~~.

42. (Canceled)

43. (Currently amended) The solid state imaging apparatus of claim 41, wherein each of said plurality of read-out [[line]] lines is connected to two of the plurality of transfer transistors which are included in the same column.

44. (Currently amended) The solid state imaging apparatus of claim 41, wherein each of said plurality of read-out [[line]] lines is connected to two of the plurality of transfer transistors which are not included in the same column.

45. (Currently amended) The solid state imaging apparatus of claim 41, wherein each of said plurality of floating diffusion ~~section~~ sections is shared by said ones of the plurality of photodiodes which are adjacent to each other in the column direction.

REMARKS

Claims 31 and 41 stand objected to for informalities. It is respectfully submitted that the enclosed amendment obviates the alleged informalities. Accordingly, it is respectfully requested that this objection be withdrawn.

Claims 31, 36 and 41 are independent and stand rejected under 35 U.S.C. § 103 as being unpatentable over Guidash '869 ("Guidash") in view of Hashimoto et al. '684 ("Hashimoto"). This rejection is respectfully traversed for the following reasons.

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Ingham. As a result of the interview, the Examiner agreed that the enclosed amendment overcomes the pending rejections and objection. Applicants and Applicants' representative would like to thank Examiner Ingham for his courtesy in conducting the interview and for his assistance in resolving issues. A summary of the interview discussion follows.

Each of claims 31, 36 and 41 recites in pertinent part, "the first read-out line and the second read-out line are disposed between the row n and the row n+1, one of the plurality of reset pulse lines is disposed between the row n+1 and the row n+2… ." In contrast, Guidash discloses a reset line (through reset transistor 36) arranged in the same row as the read-out line. In fact, Guidash expressly discloses that the reset line is shared (col. 3, lines 59-62), thereby teaching away from moving the reset line to a row that is different than the row in which the read-out line is arranged. Similarly, as shown in Figure 5 of Hashimoto, the alleged read lines 58,59 and reset pulse line 62 are all arranged within the same row. Accordingly, neither Guidash

nor Hashimoto, alone or in combination, discloses or suggests arranging at least one reset pulse line and read-out line in different rows in the manner embodied in claims 31, 36 and 41.

According to one aspect of the present invention, such a configuration can make it possible to reduce the size of a photoelectric conversion cell while nonetheless increasing an aperture area of a photoelectric conversion section. Only Applicants have recognized and considered the aforementioned dual effects, and conceived of the novel and non-obvious configuration which can make it possible to realize said effects.

"All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 165 USPQ 494, 496 (CCPA 1970).

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 31, 36 and 41 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If

there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Ramyar Farid
Registration No. 46,692

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:MWE
Facsimile: 202.756.8087
Date: May 12, 2011

Notice of Allowability	Application No. 12/178,250	Applicant(s) MORI ET AL.	
	Examiner JOHN C. INGHAM	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amenments filed 12 May 2011*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *31,33-36,38-41 and 43-45*.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/20/11
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/JOHN C INGHAM/ Examiner, Art Unit 2814	/Wael M Fahmy/ Supervisory Patent Examiner, Art Unit 2814

DETAILED ACTION

Allowable Subject Matter

1. Claims 31, 33-36, 38-41 and 43-45 are allowed.

2. The following is an examiner's statement of reasons for allowance: the prior art does not disclose or make obvious the solid state imaging apparatus of claims 31, 36 or 41, firstly including a plurality of read-out lines each being selectively connected to at least two of the transfer transistors, a plurality of reset pulse lines, the first read-out line and the second read-out line disposed between the row n and the row n+1, one of the plurality of reset pulse lines disposed between the row n+1 and the row n+2, and secondly including one of the plurality of pixel amplifier transistors disposed between adjacent rows (as claimed in claims 31 and 41), or including the first and second photodiodes which do not share each of the floating diffusion sections (as claimed in claim 36).

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on Monday to Friday, 9AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOHN C INGHAM/
Examiner, Art Unit 2814

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814

US008378401B2

(12) **United States Patent**
Mori et al.

(10) **Patent No.: US 8,378,401 B2**
(45) **Date of Patent: Feb. 19, 2013**

(54) **SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME**

(75) Inventors: **Mitsuyoshi Mori**, Kyoto (JP); **Takumi Yamaguchi**, Kyoto (JP); **Takahiko Murata**, Osaka (JP)

(73) Assignee: **Panasonic Corporation**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/335,537**

(22) Filed: **Dec. 22, 2011**

(65) **Prior Publication Data**

US 2012/0098040 A1 Apr. 26, 2012

Related U.S. Application Data

(60) Division of application No. 12/178,250, filed on Jul. 23, 2008, now Pat. No. 8,106,431, which is a continuation of application No. 10/706,918, filed on Nov. 14, 2003, now Pat. No. 7,436,010.

(30) **Foreign Application Priority Data**

Feb. 13, 2003 (JP) 2003-034692

(51) **Int. Cl.**
H01L 31/062 (2012.01)

(52) **U.S. Cl.** . **257/292**; 257/223; 257/444; 257/E27.132; 257/E27.139

(58) **Field of Classification Search** 257/223, 257/291–293, 443–445, E27.132, E27.139
See application file for complete search history.

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(Continued)

Primary Examiner — John C Ingham
(74) *Attorney, Agent, or Firm* — McDermott Will & Emery LLP

(57) **ABSTRACT**

A solid state imaging apparatus includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. Charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

42 Claims, 10 Drawing Sheets

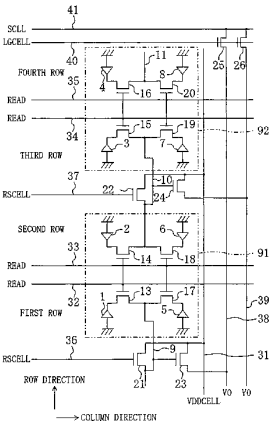

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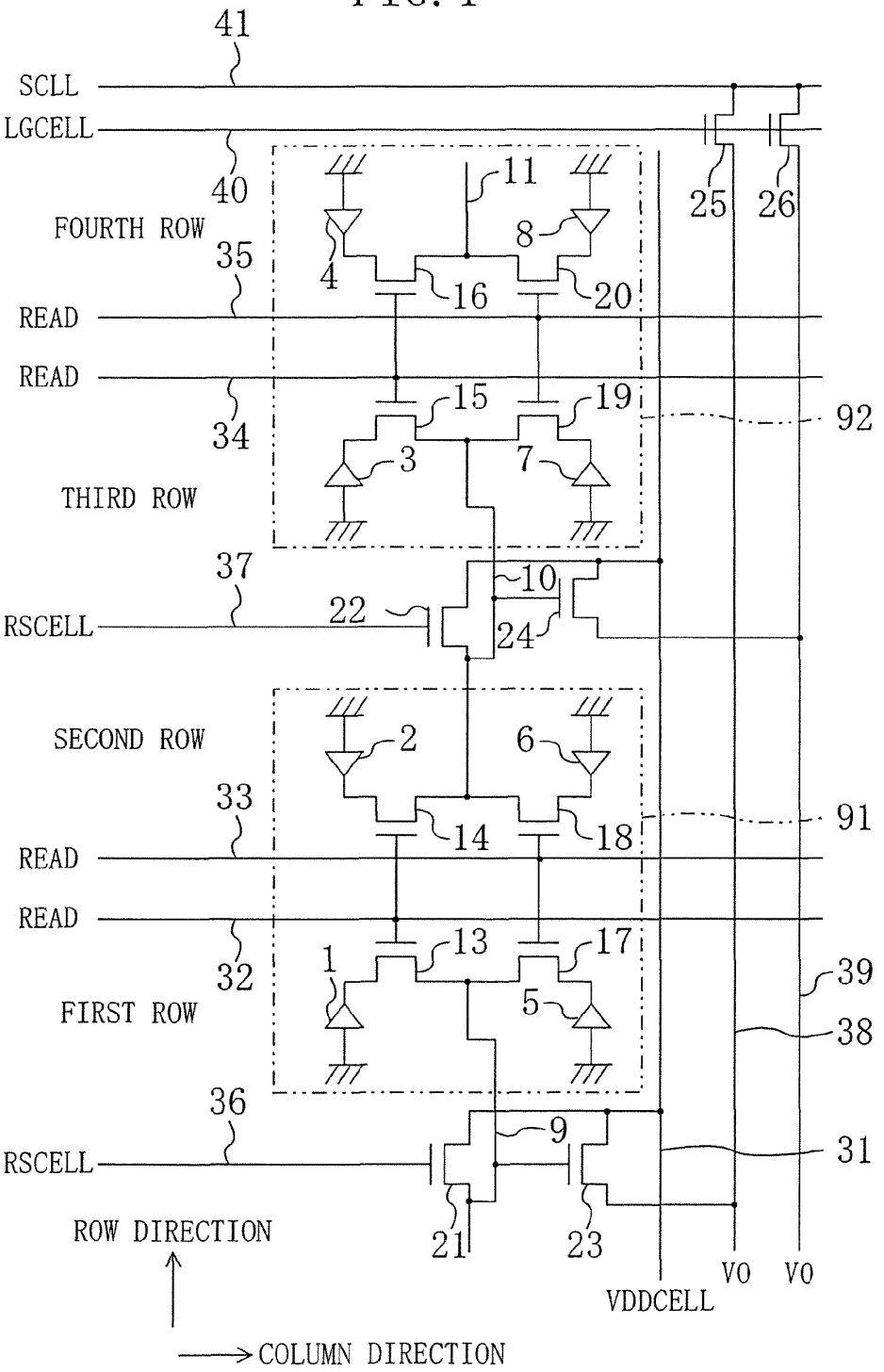
FIG. 1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LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
33
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
2
6
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17
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1
5
38
9
31
21
23
VO
VO
VDDCELL

FIG. 2

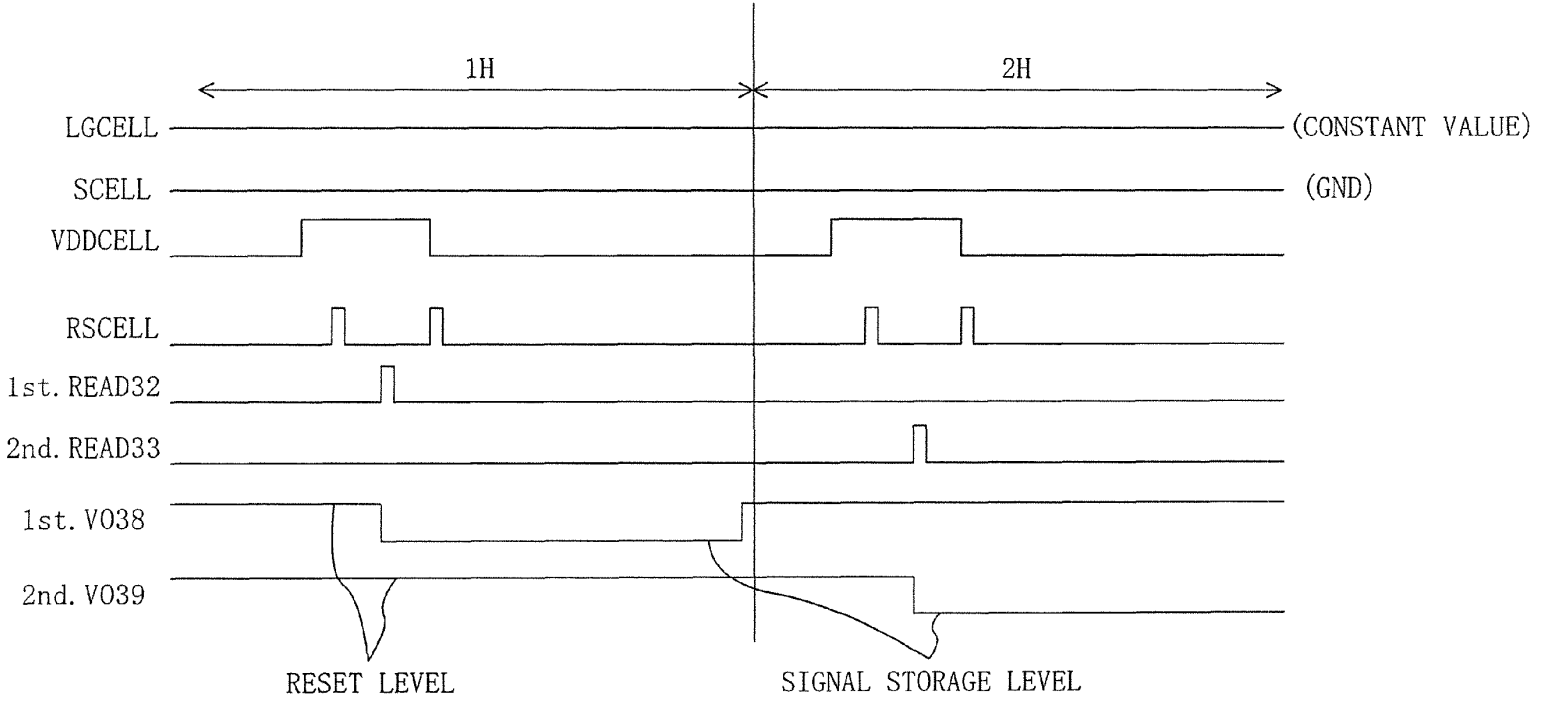
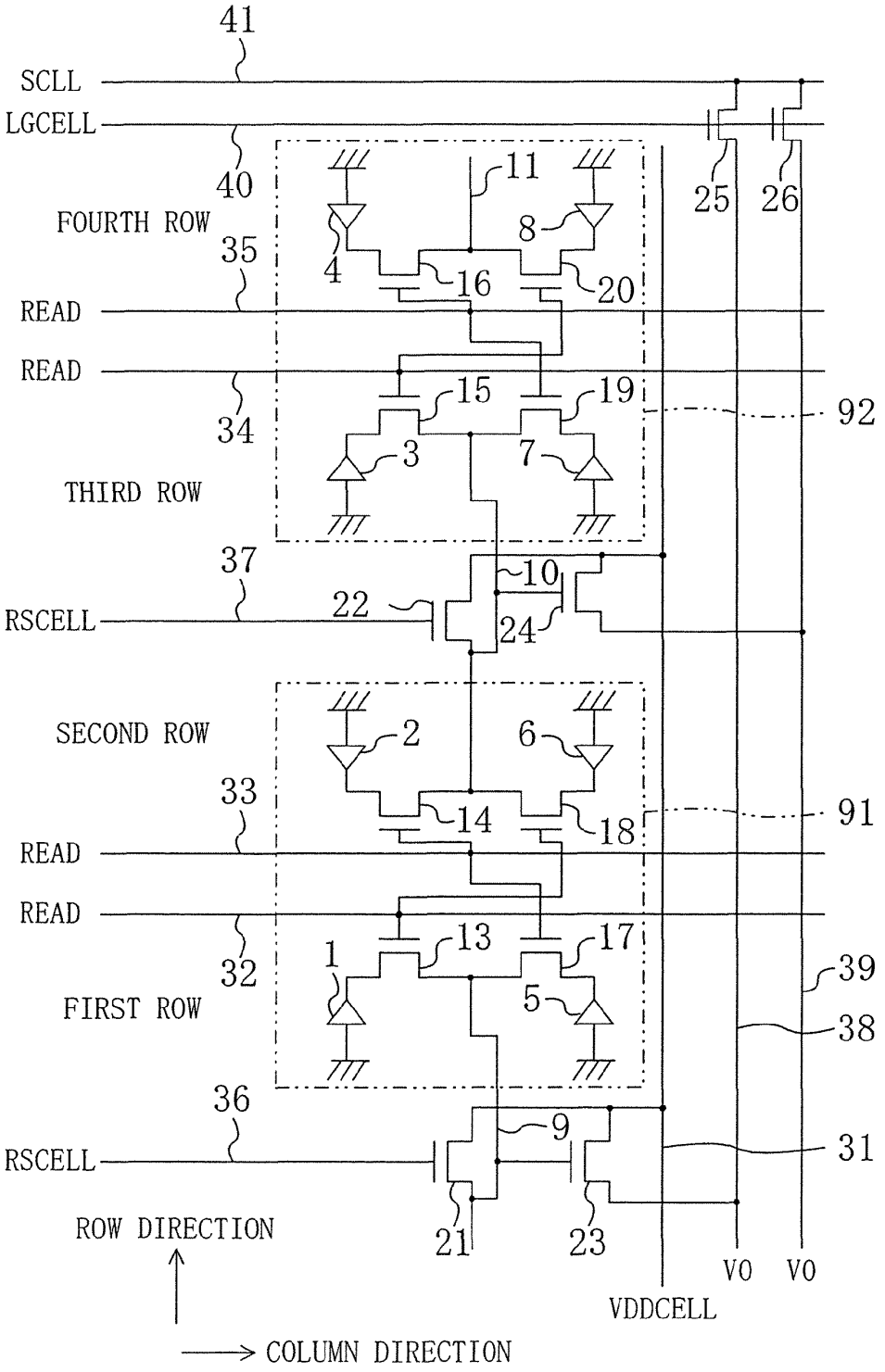

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
RSCELL
1st. READ32
2nd. READ33
1st. VO38
2nd. VO39
RESET LEVEL
SIGNAL STORAGE LEVEL

FIG. 3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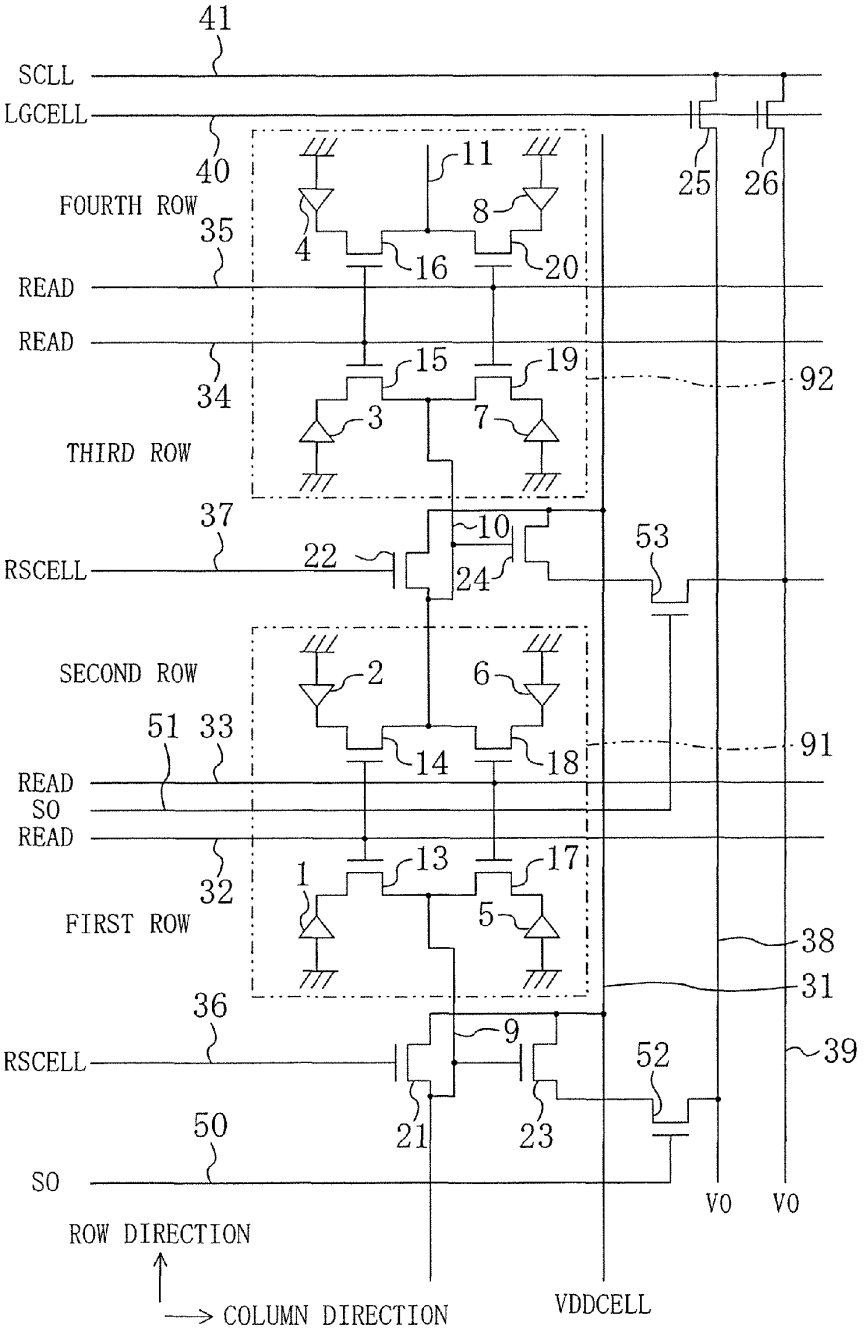
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
15
19
3
7
10
22
24
2
6
14
18
1
13
17
5
9
21
23
25
26
92
91
39
38
31
VO
VO
VDDCELL

FIG. 4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LGCELL
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35
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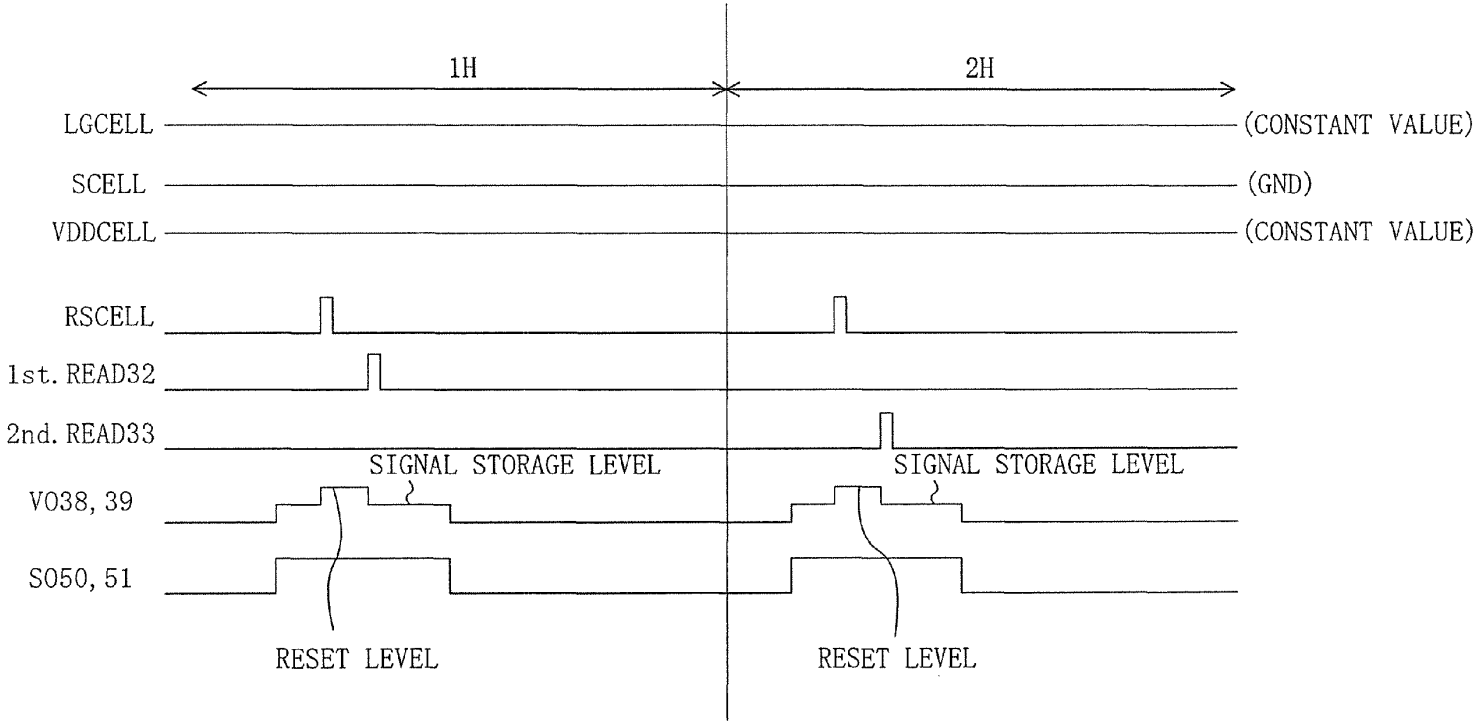
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
51
33
READ
SO
READ
32
FIRST ROW
36
RSCELL
50
SO
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
53
2
6
14
18
91
1
13
17
5
38
31
9
52
39
21
23
VO
VO
VDDCELL

FIG. 5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2H
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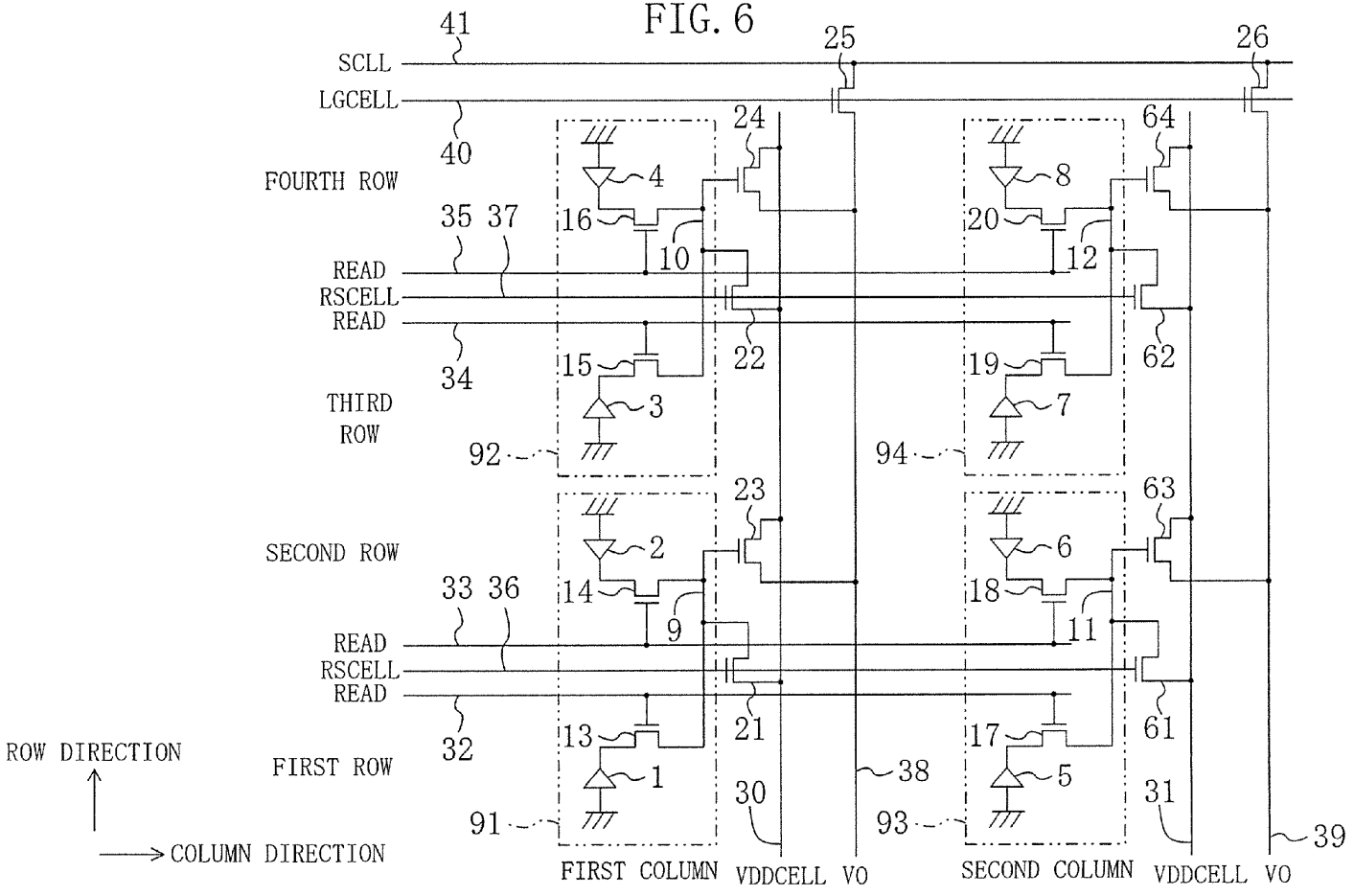
SCELL
(GND)
VDDCELL
(CONSTANT VALUE)
RSCELL
1st. READ32
2nd. READ33
SIGNAL STORAGE LEVEL
SIGNAL STORAGE LEVEL
VO38, 39
SO50, 51
RESET LEVEL
RESET LEVEL

FIG. 6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SCLL
LGCELL
40
FOURTH ROW
35 37
READ
RSCELL
READ
34
THIRD ROW
SECOND ROW
33 36
READ
RSCELL
READ
32
FIRST ROW
ROW DIRECTION
COLUMN DIRECTION
25
26
24
64
4
8
16
20
10
12
22
62
15
19
3
7
92
94
23
63
2
6
14
18
9
11
21
61
13
17
1
5
38
30
31
39
91
93
FIRST COLUMN
VDDCELL
VO
SECOND COLUMN
VDDCELL
VO

FIG. 7

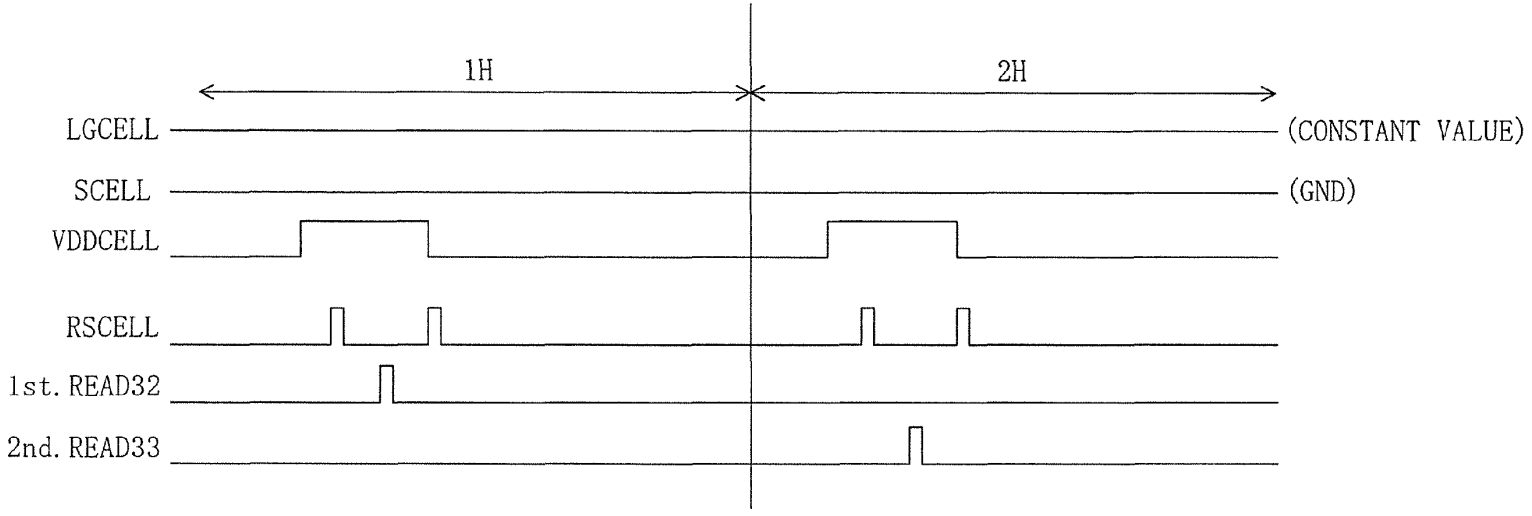

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
RSCELL
1st. READ32
2nd. READ33

FIG. 8

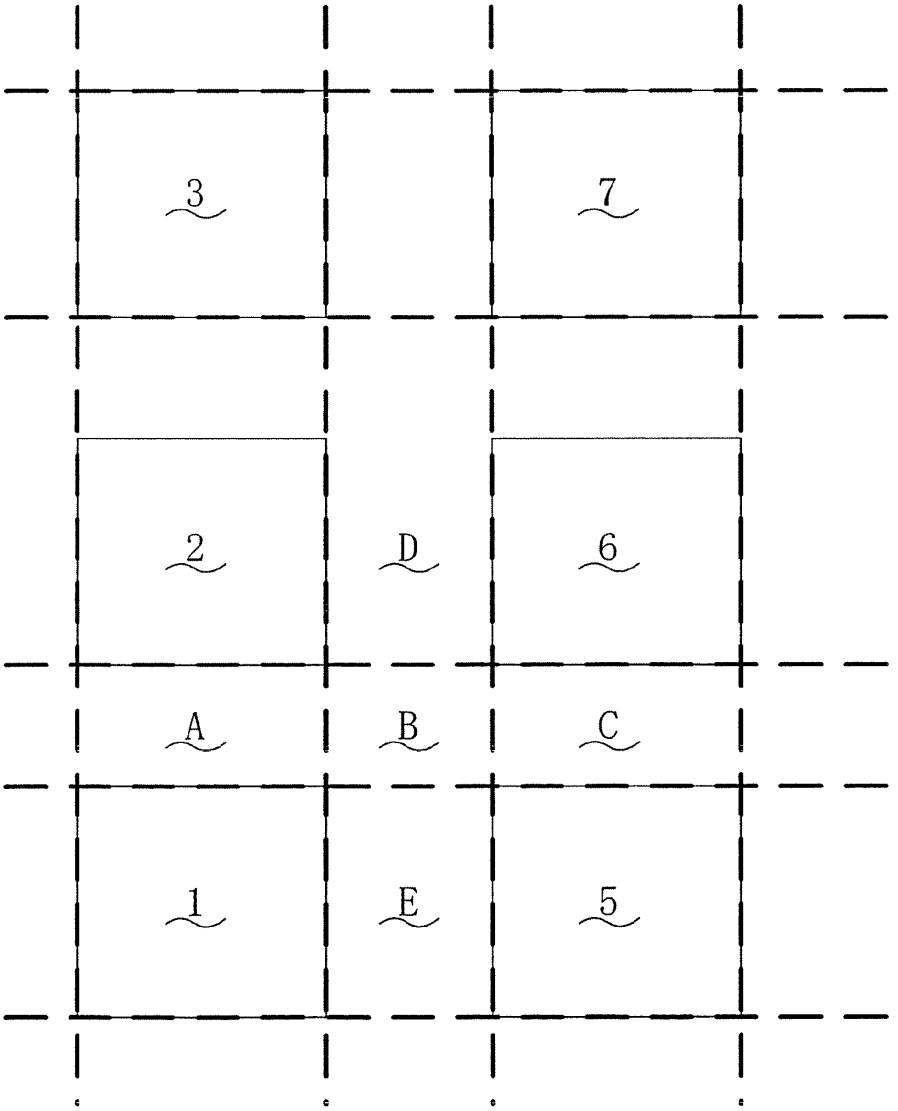
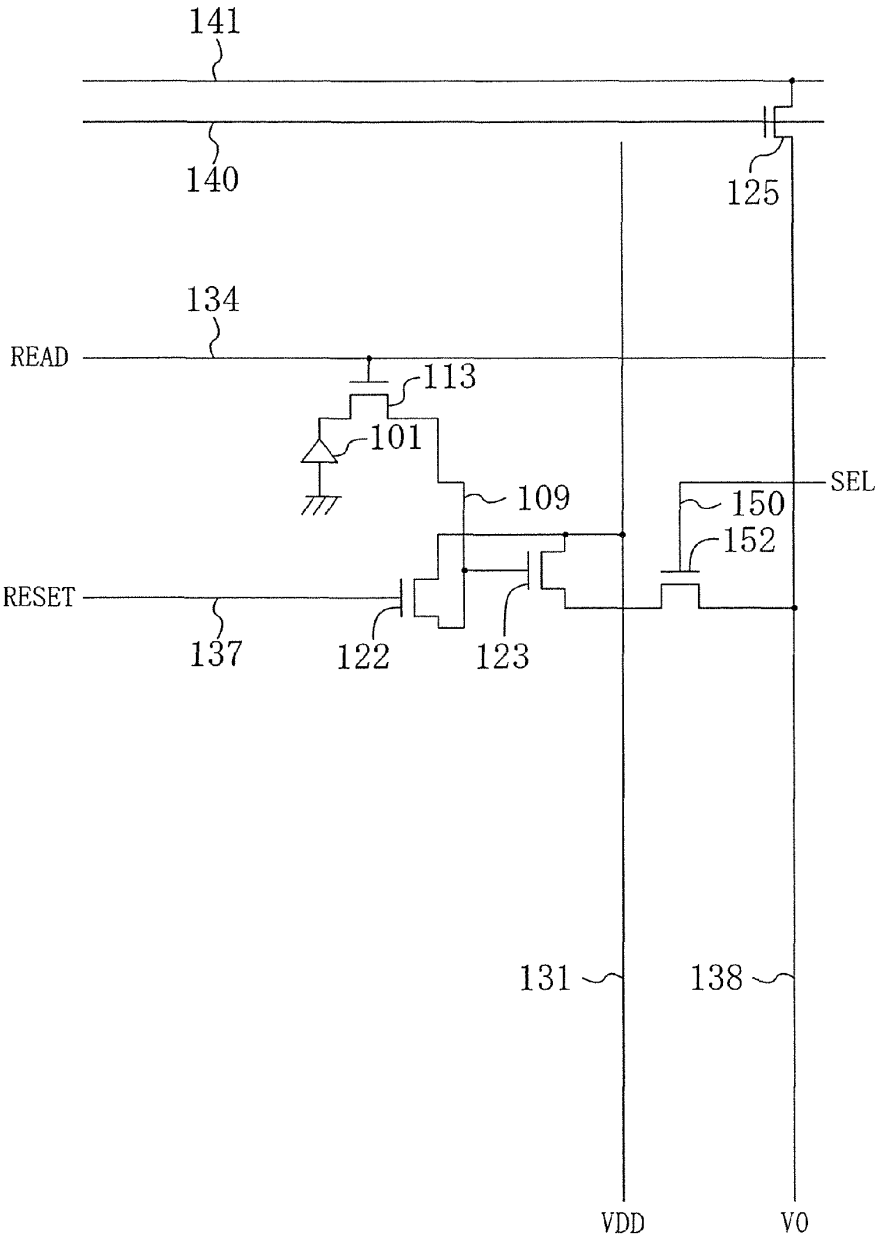


FIG. 9

FD SECTION	PIXEL AMPLIFIER	RESET GATE	APERTURE RATIO
A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	10%
		D REGION、B REGION、E REGION	25%
	D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	35%
D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	20%
	D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	20%

FIG. 10

PRIOR ART



SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

RELATED APPLICATIONS

This application is a Divisional of U.S. application Ser. No. 12/178,250, filed on Jul. 23, 2008 now U.S. Pat. No. 8,106,431, which is a Continuation of U.S. application Ser. No. 10/706,918, filed on Nov. 14, 2003, now U.S. Pat. No. 7,436,010, claiming priority of Japanese Patent Application No. 2003-034692, filed on Feb. 13, 2003, the entire contents of each of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a solid state imaging apparatus in which a plurality of photoelectric conversion sections are arranged in an array, a method for driving the solid state imaging apparatus and a camera using the solid state imaging apparatus.

FIG. **10** is a diagram illustrating a general circuit configuration for a MOS type image sensor, i.e., a known solid imaging apparatus (e.g., see M. H. White, D. R. Lange, F. C. Blaha and I. A. Mach, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels", IEEE J. Solid-State Circuits, SC-9, pp. 1-13 (1974)).

As shown in FIG. **10**, a photoelectric conversion cell includes a photodiode (PD) section **101**, a transfer transistor **113**, a reset transistor **122**, a pixel amplifier transistor **123**, a select transistor **152**, a floating diffusion (FD) section **109**, a power supply line **131** and an output signal line **138**.

The PD section **101** of which the anode is grounded is connected to the drain of the transfer transistor **113** at the cathode. The source of the transfer transistor **113** is connected to the respective sources of the FD section **109**, the gate of the pixel amplifier transistor **123** and the source of the reset transistor **122**. The gate of the transfer transistor **113** is connected to a read-out line **134**. The reset transistor **122** which receives a reset signal **137** at the gate includes a drain connected to the drain of the pixel amplifier transistor **123** and the power supply line **131**. The source of the pixel amplifier transistor **123** is connected to the drain of the select transistor **152**. The select transistor **152** receives a selection signal SEL at the gate and includes a source connected to the output signal line **138**.

The output signal line **138** is connected to the source of a load gate **125**. The gate of the load gate **125** is connected to a load gate line **140** thereof and the drain is connected to a source power supply line **141**.

In this configuration, a predetermined voltage is applied to the load gate line **140** so that the load gate **125** becomes a constant current source, and then the transfer transistor **113** is temporarily turned ON to transfer charge photoelectric-converted in the PD section **101** to the FD section **109**. Then, the potential of the PD section **101** is detected by the pixel amplifier transistor **123**. In this case, by turning the select transistor **152** ON, signal charge can be detected through the output signal line **138**.

However, in the known solid state apparatus, four transistors **113**, **122**, **123** and **152** and five lines **131**, **134**, **137**, **138** and **150** are required for total in each photoelectric conversion cell. Accordingly, the areas of transistor and line sections in a cell are increased. For example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD section **101** to the photoelectric conversion cell is only about 5%. Therefore, it is difficult to ensure a sufficiently large area of opening of the PD section **101** and also to reduce the size of the photoelectric conversion cell.

SUMMARY OF THE INVENTION

It is an object of the present invention to solve the above-described problems and, to reduce, in a FDA (floating diffusion amplifier) system, the size of a photoelectric conversion cell while increasing an aperture area of a photoelectric conversion section.

To achieve the above-described object, the present invention has been devised, so that a configuration in which a transistor and an interconnect can be shared by a plurality of photoelectric conversion (PD) sections is used in a solid state imaging apparatus.

Specifically, a first solid sate imaging apparatus includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections which are included in the same row; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. In the apparatus, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

In the first solid imaging apparatus, each said floating diffusion section is shared by ones of the photoelectric conversion sections included in the same row, and furthermore, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections. Thus, the number of read-out lines per photoelectric conversion cell becomes 0.5. As a result, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in the same column. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in the same column can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

Moreover, in the first solid state imaging apparatus, it is preferable that wherein each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in two adjacent columns, respectively. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in two adjacent columns, respectively, can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by a row which is read out by a transfer transistor connected to one of the read-out line and another row which is adjacent to the read-out row.

It is preferable that the first solid state imaging apparatus further includes: a signal line for outputting a signal from each said pixel amplifier transistor to the outside; and a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line. Thus, charges from one of the photoelectric conversion sections which are included in adjacent rows, respectively, can be detected through a shared signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by photoelectric conversion sections which are adjacent to each other in the row direction or in the column direction. Thus, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that in each said floating diffusion section, a reset section for resetting charge stored in the floating diffusion section is provided. Thus, it is possible to stop, after charge read out from a photoelectric conversion section has been detected by an amplifier, detection of charge by the pixel amplifier transistor.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction. Thus, a high quality image can be obtained from signals read out from the photoelectric conversion sections.

It is preferable that the first solid state imaging apparatus further includes a signal processing circuit for processing an output signal from each said pixel amplifier transistor. Thus, a high quality image can be obtained.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film. Thus, a power supply line can be formed in a different interconnect layer from an interconnect layer in which an output signal line connected to a pixel amplifier transistor is formed. Therefore, the size of a photoelectric conversion cell can be further reduced and also the aperture area can be increased.

A method for driving a solid state imaging apparatus according to the present invention is directed to a method for driving the first solid state imaging apparatus of the present invention and includes: a first step of transferring, in each said photoelectric conversion cell, by a first read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which are not included in the same row but included in two columns adjacent to each other, respectively, to one of the floating diffusion sections connected to said ones of the photoelectric conversion sections; and a second step of transferring, by a second read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which have not been read out in the first step to the same floating diffusion section connected to said ones of the photoelectric conversion sections as that in the first step.

A second solid state imaging apparatus according to the present invention includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows; a plurality of floating diffusion sections each being connected, via each of a plurality of transfer transistors, to each of ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same column in each said photoelectric conversion cell, and each being shared by said ones of the photoelectric conversion sections; a plurality of read-out lines each being connected to one of the transfer transistors and independently reading out charge from each of said ones of the photoelectric conversion sections to each said floating diffusion section shared by said ones of the photoelectric conversion sections; and a plurality of pixel amplifier transistors each detecting and outputting the potential of the floating diffusion section.

In the second solid state apparatus, each said floating diffusion section is connected to some of the plurality of transfer transistors, is shared by ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same. Furthermore, some of the plurality of read-out lines each independently reading out charge from each of said ones of the photoelectric conversion sections are connected to each said transfer transistor. Thus, a row-select transistor which is usually provided is not needed. As a result, the number of interconnects per photoelectric conversion section is reduced from 5 to 3.5. Therefore, the area of the photoelectric conversion cell itself can be reduced while increasing the area of the photoelectric sections.

It is preferable that the second solid state imaging apparatus further includes a reset transistor for resetting charge stored in each said floating diffusion section and the drain of the reset transistor is connected to the drain of the pixel amplifier transistor so that a drain is shared by the reset transistor and the pixel amplifier transistor. Thus, an interconnect connecting between the drain of the reset transistor and the drain of the pixel amplifier transistor can be shared. Accordingly, the number of interconnects per the photoelectric conversion cell can be further reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion sections which are adjacent to each other in the row direction in each said photoelectric conversion cell. Thus, the area of floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and a gate of the MIS transistor is arranged in the column direction. Thus, each said the read-out line can be also function as an interconnect of a transfer transistor, so that the area of the read-out lines occupying the photoelectric conversion cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the area of the pixel amplifier transistor per photoelectric conversion cell can be reduced whereas the area of the photoelectric conversion sections can be increased. Therefore, light sensitivity is increased.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor and each said floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect connecting between the pixel amplifier transistor and the floating diffusion section can be shortened, so that the areas of the pixel amplifier transistor and the floating diffusion section per photoelectric conversion cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between ones of the photoelectric cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so as to

have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

Moreover, in the second solid state imaging apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and each said pixel amplifier transistor is arranged between respective gates of the MIS transistor and another MIS transistor. Thus, an empty region located in an area of the cell in which a row and a column intersect to each other can be utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the area of the reset transistors per photoelectric conversion section can be reduced. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said pixel amplifier transistor and the floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect between the floating diffusion section can be omitted and the source of the reset transistor and the floating diffusion section can be connected to each other to be shared. Therefore, the areas of the reset transistors and the floating diffusion sections per photoelectric conversion cell can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is connected to a line arranged between ones of the photoelectric cells which are adjacent to each other in the row direction. Thus, pitches of the photoelectric sections in row directions can be matched in a simple manner, so that resolution is improved.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so as to have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

In this case, it is preferable that each said transfer transistor is made of an MIS transistor, and each said reset transistor is arranged between respective gate of the MIS transistor and another MIS transistor. Thus, an empty region located in an area of the cell in which a row and a column intersect to each other can be utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, the area of the floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in at least one of the row direction and the column direction. Thus, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that the line connecting respective drains of the reset transistor and the pixel amplifier transistor also functions as a light-shielding film. Thus, the number of interconnects per photoelectric conversion cell can be reduced. Therefore, the area of the photoelectric sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

It is preferable that each of the first and second solid state imaging apparatus further includes a signal processing circuit for processing an output signal output from each said pixel amplifier transistor. Thus, a high resolution image can be obtained.

A camera according to the present invention includes the first or second solid state imaging apparatus of the present invention. Thus, the camera of the present invention can achieve a high resolution image.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a first embodiment of the present invention.

FIG. **2** is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment.

FIG. **3** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment.

FIG. **4** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a second embodiment of the present invention.

FIG. **5** is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment.

FIG. **6** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention.

FIG. **7** is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment.

FIG. **8** is a plane view schematically illustrating a layout of the photoelectric conversion cell in the solid state imaging apparatus of the third embodiment.

FIG. **9** is a table showing the aperture ratio of PD sections to a photoelectric conversion cell in each of regions A through E of FIG. **8** where a transistor and the like are arranged.

FIG. **10** is a circuit diagram illustrating a photoelectric conversion cell in a known solid imaging apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

A first embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **1** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to the first embodiment of the present invention.

As shown in FIG. **1**, for example, photoelectric conversion (PD) sections **1**, **2**, **3** and **4** each of which is made of a photodiode and converts incident light to electric energy are arranged in this order in the row direction. Furthermore, PD sections **5**, **6**, **7** and **8** are arranged in this order in the row direction so that the PD sections **5**, **6**, **7** and **8** are adjacent to the PD sections **1**, **2**, **3** and **4**, respectively, in the column direction.

Here, in this application, the row direction means to be the direction in which a row number increases and the column direction means to be the direction in which a column number increases.

Between the first and 0^{th} rows (not shown), a first floating diffusion (FD) section **9** for storing photoelectric-converted charges from the PD sections **1** and **5** included in the first row and PD sections included in the 0^{th} row is provided. Between the second and third rows, a second floating diffusion section **10** for storing photoelectric-converted charges from the PD sections **2** and **6** included in the second row and the PD sections **3** and **7** included in the third row is provided so as to be surrounded by the PD sections **2**, **3**, **6** and **7**. Between the fourth and fifth rows (not shown), a third floating diffusion section **11** for storing photoelectric-converted charges from the PD sections **4** and **8** included in the fourth row and PD sections included in the fifth row is provided. In this manner, each of the FD sections **9**, **10** and **11** is shared by four PD sections.

In this case, a cell including the PD sections **1**, **2**, **5** and **6** is a first photoelectric conversion cell **91** and a cell including the PD sections **3**, **4**, **7** and **8** is a second photoelectric conversion cell **92**.

In the first photoelectric conversion cell **91**, a transfer transistor **13** made of an N channel FET for transferring charge from the PD section **1** to the first FD section **9** is connected between the PD section **1** included in the first row and the first FD section **9**, and a transfer transistor **17** made of an N channel FET for transferring charge from the PD section **5** to the first FD section **9** is connected between the PD section **5** and the first FD section **9**.

Moreover, in the first photoelectric conversion cell **91**, a transfer transistor **14** made of an N channel FET for transferring charges from the PD section **2** to the second FD section **10** is connected between the PD section **2** included in the second row and the second FD section **10**, and a transfer transistor **18** made of an N channel FET for transferring charges from the PD section **6** to the second FD section **10** is connected between the PD section **6** and the second FD section **10**.

As a characteristic of the first embodiment, the transfer transistor **13** included in the first row and the transfer transistor **14** included in the second row are connected to a first read-out (READ) line **32** while the transfer transistor **17** included in the first row and the transfer transistor **18** included in the second row are connected to a second READ line **33**.

In the second photoelectric conversion cell **92**, a transfer transistor **15** made of an N channel FET for transferring charge from the PD section **3** to the second FD section **10** is connected between the PD section **3** included in the third row and the second FD section **10**, and a transfer transistor **19** made of an N channel FET for transferring charge from the PD section **7** to the second FD section **10** is connected between the PD section **7** and the second FD section **10**.

Moreover, in the second photoelectric conversion cell **92**, a transfer transistor **16** made of an N channel FET for transferring charges from the PD section **4** to the third FD section **11** is connected between the PD section **4** included in the fourth row and the third FD section **11**, and a transfer transistor **20** made of an N channel FET for transferring charges from the PD section **8** to the third FD section **11** is connected between the PD section **8** and the third FD section **11**.

Also, in this cell, the transfer transistor **15** included in the third row and the transfer transistor **16** included in the fourth row are connected to the third READ line **34** while the transfer transistor **19** included in the third row and the transfer transistor **20** are connected to the fourth READ line **35**.

To the first FD section **9**, a first reset transistor **21** made of an N channel FET is connected. The first reset transistor **21** includes a source connected to the first FD section **9**, a drain connected to a photoelectric conversion cell power supply (VDDCELL) line **31** and a gate connected to a first reset pulse (RSCELL) line **36**. Thus, charge stored in the first FD section **9** is made to flow through the VDDCELL line **31** by a RSCELL signal.

In the same manner, a second reset transistor **22** made of an N channel FET is connected to the second FD section **10**. The second reset transistor **22** includes a source connected to the second FD section **10**, a drain connected to the VDDCELL line **31** and a gate connected to a second RSCELL line **37**. Note that although not shown in FIG. **1**, a reset transistor of the same configuration as that of the first reset transistor **21** or the like is provided in the third FD section **11**.

To the first FD section **9** and the first reset transistor **21**, a first pixel amplifier transistor **23** made of an N channel FET is connected. The first pixel amplifier transistor **23** includes a gate connected to the first FD section **9**, a drain connected to the VDDCELL line **31** and a source connected to a first output signal (VO) line **38**.

In the same manner, a second pixel amplifier transistor **24** made of an N channel FET is connected to the second FD section **10** and the second reset transistor **22**. The second pixel amplifier transistor **24** includes a gate connected to the second FD section **10**, a drain connected to the VDDCELL line **31** and a source connected to a second VO line **39**.

The first VO line **38** and the second VO line **39** are connected to not only the pixel amplifier transistors **23** and **24**, respectively, but also first and second load transistors **25** and **26**, respectively. Each of the first and second load transistor **25** and **26** is made of an N channel for constituting a source follower amplifier. A load gate (LGCELL) line **40** is connected to each of the gates of the first and second load transistors **25** and **26**. A source power supply (SCLL) line **41** is connected to each of the respective drains of first and second load transistors **25** and **26**.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **2** is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment. In this case, a series of operations is completed in a horizontal blanking period (=**1**H).

Moreover, as for the detection order of signal charges from the PD sections **1** through **8** arranged in an array, detection is simultaneously carried out in the first and second rows and then detection is simultaneously carried out in the third and fourth rows.

As shown in FIG. **2**, first, high level voltage is applied to the LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source, and then during a period in which the potential of the VDDCELL line **31** is high level, each of the RSCELL lines **36** and **37** is set to be a high level in a pulse state to temporarily turn each of the reset transistors **21** and **22** ON. Thus, each of charges stored in the first FD section **9** in the first photoelectric conversion cell **91** and in the second FD section **10** in the second photoelectric conversion cell **92** is made to flow through the VDDCELL line **31**. In this case, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to

the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **2** is transferred to the second FD section **10**. For charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

Subsequently, when the VDDCELL line **31** is turned to be in a low level OFF state and each of the RSCELL lines **36** and **37** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **10** becomes in the same OFF level state as that of the VDDCELL line **31**. Thus, each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **24** is not operated and thus the vertical line scanning circuit is in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at a reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **17** and **18** ON. Thus, charge stored in the PD section **5** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the second FD section **10**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

In this manner, charges detected during the first horizontal blanking period **1**H and charges detected during the second horizontal blanking period **2**H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges.

Subsequently, by driving the PD sections in the third and fourth rows in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

Note that in the first embodiment, the circuit configuration and driving method in which after every second column, i.e., every odd-numbered column including the PD sections **1** and **2** have been read out, charges in every even-numbered column including the PD sections **5** and **6** are detected have been described. However, this embodiment is not limited thereto but READ lines can be increased to detect charge in every third column at the same timing as described above.

In the solid state imaging apparatus of the first embodiment, as shown in the circuit configuration of FIG. **1**, for example, four PD sections share a FD section, a pixel amplifier transistor and a reset transistor. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 1.5. The number of interconnects can be reduced from 5 (required in the known solid state imaging apparatus) to 2.5. For example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections to the photoelectric conversion cell is about 35%. Therefore, it is possible to reduce the cell sizes of the photoelectric conversion cells **91** and **92** and to largely increase the aperture ratio of the PD section at the same time.

In this connection, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are detected by a READ line at the same timing is applied to the known circuit configuration. If a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 10%.

Moreover, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are read out by a READ line, and a FD section and a pixel amplifier transistor included in a row which adjacent to an unread row in a photoelectric conversion cell are shared by two photoelectric sections to detect signal charge is applied to the known circuit configuration. With a driving method in which signal charges are simultaneously detected in the two photoelectric conversion sections, for example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 15%.

Modified Example of First Embodiment

FIG. **3** is a diagram illustrating a circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment of the present invention. Also, in this modified example, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. **3**, for example, in the first photoelectric conversion cell **91**, the first READ line **32** is connected to the transfer transistor **13** and the transfer transistor **18** included in adjacent columns, respectively, while the second READ line **33** is connected to the transfer transistor **14** and the transfer transistor **17** included in adjacent columns, respectively. Thus, even if connections are made with respect to the PD sections **1**, **2**, **5** and **6** included in two adjacent rows with the first and second READ lines **32** and **33** interposed between the PD sections **1** and **5** and the PD sections **2** and **6** so that signal charges from the PD sections which are not included in

the same columns are transferred, charge can be detected at the same timing as that shown in FIG. **2**.

For example, when the first READ line **32** is temporarily turned ON, signal charge is transferred from the PD section **1** to the first FD section **9** via the transfer transistor **13** and, at the same time, signal charge is transferred from the PD section **6** to the second FD section **10** via the transfer transistor **18**.

Note that in the modified example of the first embodiment, signal charges from two of the four PD sections included in a photoelectric conversion cell **91** are read out during the horizontal blanking period **1**H. However, instead of this, signal charges from all of the four PD sections may be read out.

Moreover, by performing signal processing to signal charges from all of the photoelectric conversion cells which have been read out during different horizontal blanking periods, a high quality image with a large number of pixels can be obtained.

Second Embodiment

Hereinafter, a second embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **4** is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a second embodiment of the present invention. In FIG. **4**, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

First, differences of the solid state imaging apparatus of FIG. **4** from that of the first embodiment shown in FIG. **1** will be described.

In the second embodiment, an configuration in which the first and second pixel amplifier transistors **23** and **24** are connected to the first and second output signal (VO) lines **38** and **39**, respectively, via the first and second select transistors **52** and **53** each of which made of an N channel FET, respectively, is used.

To the respective gates of the first and second select transistors **52** and **53**, first and second select (SO) lines **50** and **51** to which a switching pulse is applied are connected, respectively.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **5** is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment. In this case, a series of operations is completed in a horizontal blanking period (=**1**H).

As shown in FIG. **5**, first, a predetermined voltage is applied to the LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source and the potential of the VDDCELL line **31** is set to be a high level. Subsequently, each of the RSCELL lines **36** and **37** is set to be a high level in a pulse state to temporarily turn each of the reset transistors **21** and **22** ON. Thus, each of charges stored in the first FD section **9** and in the second FD section **10** is made to flow through the VDDCELL line **31**. In this case, in each of the pixel amplifier transistors **23** and **24**, each of the select transistors **52** and **53** has been turned ON in advance, so that a signal level at a reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **2** is transferred to the second FD section **10**. Thereafter, for charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively.

Subsequently, by changing each of the first and second SO lines **50** and **51** to a high level to keep the first and second transistors **52** and **53** ON, stored charge signals of the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24** are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit.

Thereafter, each of the first and second SO lines **50** and **51** is set back to be a low level to turn the first and second select transistors **52** and **53** OFF, so that each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** is selected, each of the pixel amplifier transistors **23** and **24** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of the FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **17** and **18** ON. Thus, charge stored in the PD section **5** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the second FD section **10**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the stored signals whose voltage level have been detected selectively conducts the first and second VO lines **38** and **39** and are introduced to the noise cancellation circuit. Then, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

Thus, with the first and second select transistors **52** and **53** between the FD section **9** and the first VO line **38** and between the FD section **10** and the second VO line **39**, respectively. Thus, the number of transistors per photoelectric conversion cell is 1.75. Moreover, the number of interconnects is 2.75. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells **91** and **92** and also to largely improve the aperture ratio of PD sections.

Note that also in the second embodiment, as in the modified example of the first embodiment, for example, a configuration in which the transfer transistor **13** and the transfer transistor **18** located diagonally to the transfer transistor **13** are connected to the first READ line **32**, and the transfer transistor **14**

and the transfer transistor **17** located diagonally to the transfer transistor **14** are connected to the second READ line **33** may be used.

Moreover, in the photoelectric conversion cell **91**, the PD sections are arranged in two rows and two columns. However, the present invention is not limited thereto, but the PD sections may be arranged in two rows and three columns and, furthermore, may be arranged in three or more rows and three or more columns.

Third Embodiment

Hereinafter, a third embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **6** is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention. In FIG. **6**, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. **6**, in the solid state imaging apparatus of the third embodiment, first through fourth photoelectric conversion cells **91**, **92**, **93** and **94** are arranged in a matrix.

For example, the first photoelectric conversion cell **91** includes photoelectric conversion (PD) sections **1** and **2** arranged in regions which is located in the first column of an array and the first row and which is located in the first column of and the second rows of the array, respectively. The PD sections **1** and **2** share a first FD section **9** via transfer transistors **13** and **14** each of which is made of an N channel FET, respectively.

To the first FD section **9**, the first reset transistor **21** made of an N channel FET is connected. The first reset transistor **21** includes a source connected to the first FD section **9**, a drain connected to the first FD section **9** and a gate connected to a first RSCELL line **36**. Thus, charge stored in the first FD section **9** is made to flow through a first VDDCELL line **30** by a RSCELL signal.

To the first FD section **9** and the first reset transistor **21**, a first pixel amplifier transistor **23** of an N channel FET is connected. The first pixel amplifier transistor made of an N channel FET includes a gate connected to the first FD section **9**, a drain connected to the first VDDCELL line **30** and a source connected to a first VO line **38**.

In the same manner, PD sections **3** and **4** arranged in regions of an array forming a second photoelectric conversion cell **92** which is located in the first column and the third row and which is located in the first column and the fourth row, respectively, share a second FD section **10** via transfer transistors **15** and **16**, respectively. A second reset transistor **22** selectively conducts the second FD section **10** and the first VDDCELL line **30**. Moreover, a second pixel amplifier transistor **24** which receives the signal potential of the second FD section **10** at the gate and receives the power supply potential of the first VDDCELL line **30** at the drain outputs a detected signal corresponding to a received signal potential to the first VO line **38**.

PD sections **5** and **6** arranged in regions of an array forming a third photoelectric conversion cell **93** which is located in the second column and the first row and which is located in the second column and the second row, respectively, share a third FD section **11** via transfer transistors **17** and **18**, respectively. A third reset transistor **61** selectively conducts the third FD section **11** and a second VDDCELL line **31**. Moreover, a third pixel amplifier transistor **63** which receives the signal potential of the third FD section **11** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs a detected signal corresponding to a received signal potential to a second VO line **39**.

PD sections **7** and **8** arranged in regions of an array forming a fourth photoelectric conversion cell **94** which is located in the second column and the third row and which is located in the second column and the fourth row, respectively, share a fourth FD section **12** via transfer transistors **19** and **20**, respectively. A fourth reset transistor **62** selectively conducts the fourth FD section **12** and a second VDDCELL line **31**. Moreover, a fourth pixel amplifier transistor **64** which receives the signal potential of the fourth FD section **12** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs a detected signal corresponding to a received signal potential to a second VO line **39**.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **7** is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment. In this case, a series of operations is completed in a horizontal blanking period (=**1**H).

Moreover, as for the detection order of signal charges from the PD sections **1** through **8** arranged in an array, detection is carried out sequentially from the first row to the second row and so on.

As shown in FIG. **7**, first, high level voltage is applied to a LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source, and then during a period in which the potentials of the first VDDCELL line **30** and the VDDCELL line **31** are set to be high level, the first RSCELL lines **36** is set to be high level in a pulse state to temporarily turn each of the reset transistors **21** and **61** ON. Thus, charges stored in the first FD section **9** in the first photoelectric conversion cell **91** and in the third FD section **11** in the third photoelectric conversion cell **93** are made to flow through the first VDDCELL line **30** and the VDDCELL line **31**, respectively. In this case, in each of the pixel amplifier transistors **23** and **63**, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **61** has been turned OFF, high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **5** in the second row is transferred to the third FD section **11**. For charges transferred to the first FD section **9** and the third FD section **11**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the third pixel amplifier transistor **63**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **63** can be detected.

Subsequently, when each of the VDDCELL lines **30** and **31** is turned to be in a low level OFF state and the first RSCELL line **36** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **11** becomes in the same

OFF level state as that of each of the VDDCELL lines **30** and **31**. Then, each of the pixel amplifier transistors **23** and **63** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL line **36** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **63** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **61** is temporarily turned ON to reset charges of the FD sections **9** and **11**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **63**, a signal level at the reset time is detected, detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **61** has bee turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **14** and **18** ON. Thus, charge stored in the PD section **2** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the third FD section **11**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the third FD section **11**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the third pixel amplifier transistor **63**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **63** can be detected

In this manner, charges detected during the first horizontal blanking period **1**H and charges detected during the second horizontal blanking period **2**H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges. Thus, in the third embodiment, for example, the power supply potentials which are to be applied to the respective drains of the first reset transistor **21** and the first pixel amplifier transistor **23** vary in the same manner. Therefore, the known row selection transistor **152** is not necessarily provided.

Subsequently, if the PD sections in the third and fourth rows are driven in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

As has been described, the solid state imaging apparatus of the third embodiment has, for example, a configuration in which the two PD sections **1** and **2** share the first FD section **9**, the first pixel amplifier transistor **23** and the first reset transistor **21**. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 2. Moreover, the number of interconnects can be reduced from 5 (required in the known apparatus) to 3.5. Accordingly, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD sections **1** and **2** is about 30%. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells and also to largely improve the aperture ratio of the PD section.

Note that each of the reset transistors **21**, **22**, **61** and **62** is made of an N channel type MOS transistor. However, in each of the reset transistors **21**, **22**, **61** and **62** made of, instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second RSCELL lines **36** and **37**, each of the reset transistors **21**, **22**, **61** and **62** is turned ON.

In the same manner, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is made of an N channel type MOS transistor. However, in each of the pixel amplifier transistors **23**, **24**, **63** and **64** made of, instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second VDDVELL lines **30** and **31**, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is turned ON to be in a potential detection period in which signal potentials from the corresponding FD sections **9**, **10**, **11** and **12** are detected.

Hereinafter, in the layout in which each of the PD sections **1**, **2**, **3**, **5**, **6** and **7** arranged as shown in FIG. **8**, a region of the cell located between the PD sections **1** and **2** is referred to as an "A region"; a region of the cell surrounded by the PD sections **1**, **2**, **5** and **6** is referred to as a "B region"; a region of the cell located between the PD sections **5** and **6** is referred to as a "C region"; a region of the cell located between the PD sections **2** and **6** is referred to as a "D region"; and a region of the cell located between the PD sections **1** and **5** is referred to as an "E region". Then, by arranging the FD sections **9** and **11**, the pixel amplifier transistors **23** and **63**, and the reset transistors **21** and **61** in regions in the cell indicated in the FIG. **9**, respectively, the aperture ratio of the PD sections to the photoelectric conversion cell can be improved in any case, compared to the known solid state imaging apparatus. Moreover, the size of the cell can be reduced.

Furthermore, as also shown in FIG. **9**, if the FD sections **9** and **11** are arranged in the A and C regions, respectively, the aperture of the PD sections can be improved to be about 30% by arranging in parallel the READ lines **32** and **33** for driving the transfer transistors **13** and **14**, respectively.

Moreover, as shown in FIG. **9**, for example, the aperture of the PD sections can be improved to be about 30% by arranging the first RSCELL line **36** between the PD sections **2** and **3**.

Moreover, as shown in FIG. **8**, by arranging the PD sections so as to be spaced apart from one another by a certain distance at least in one of the row direction and the column direction, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

Moreover, although not shown in the drawings, by using the first VDDCELL line **30** and the second VDDCELL line **31** as light-shielding films for separating the photoelectric conversion cells from one another, the first VO line **38** and the second VO line **39** can be formed in different interconnect layers. Thus, the sizes of the photoelectric conversion cells **91** and **92** can be reduced and also the aperture area of the PD sections can be increased.

Moreover, with the solid state imaging apparatus of any one of the first through third embodiments, a camera which is small-sized and provides a high resolution image can be obtained.

What is claimed is:

1. A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the plurality of photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors;

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of pixel amplifier transistors each detecting and outputting the potential of one of the plurality of floating diffusion sections;

a plurality of signal lines each transferring an output from one of the plurality of pixel amplifier transistors,

wherein the plurality of photodiodes include a first photodiode, a second photodiode, a third photodiode and a fourth photodiode,

the plurality of transfer transistors include a first transfer transistor, a second transfer transistor, a third transfer transistor and a fourth transfer transistor,

the plurality of read-out lines include a first read-out line, a second read-out line, a third read-out line and a fourth read-out line,

the first read-out line is adjacent to the second read-out line,

the second read-out line is disposed between the first read-out line and the third read-out line,

the third read-out line is disposed between the second read-out line and the fourth read-out line,

the first read-out line is connected to the first photodiode in row m via the first transfer transistor, where m is a positive integer,

the second read-out line is connected to the second photodiode in the row m via the second transfer transistor,

the third read-out line is connected to the third photodiode in row m+1 via the third transfer transistor,

the fourth read-out line is connected to the fourth photodiode in the row m+1 via the fourth transfer transistors,

the first photodiode and the third photodiode are disposed in one of column n and column n+1, where n is a positive integer,

the second photodiode and the fourth photodiode are disposed in the other of the column n and the column n+1, and

one of the column n and the column n+1 is disposed between one of the plurality of signal lines and the other of the column n and the column n+1.

2. The solid state imaging apparatus of claim **1**, wherein the row m is adjacent to the row m+1, and

the column n is adjacent to the column n+1.

3. The solid state imaging apparatus of claim **1**, wherein no read-out line is disposed between the second read-out line and the third read-out line, and

no read-out line is disposed between the third read-out line and the fourth read-out line.

4. The solid state imaging apparatus of claim **1**, wherein one of the plurality of floating diffusion sections is connected to the first photodiode via the first transfer transistor,

the one of the plurality of floating diffusion sections is connected to the second photodiode via the second transfer transistor,

the one of the plurality of floating diffusion sections is connected to the third photodiode via the third transfer transistor, and

the one of the plurality of floating diffusion sections is connected to the fourth photodiode via the fourth transfer transistor.

5. The solid state imaging apparatus of claim **1**, wherein one of the plurality of floating diffusion sections is disposed between the column n and the column n+1.

6. The solid state imaging apparatus of claim **1**, wherein one of the plurality of pixel amplifier transistors is disposed between the row m and the row m+1.

7. The solid state imaging apparatus of claim **1**, wherein one of the plurality of floating diffusion sections is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

8. The solid state imaging apparatus of claim **1**, wherein the plurality of read-out lines and one of the plurality of signal lines intersect with each other.

9. The solid state imaging apparatus of claim **1**, further comprising a plurality of row select transistors each being connected to one of the plurality of pixel amplifier transistors.

10. The solid state imaging apparatus of claim **9**, wherein one of the plurality of row select transistors is disposed between the row m and the row m+1.

11. The solid state imaging apparatus of claim **9**, wherein one of the plurality of row select transistors is disposed between one of the plurality of pixel amplifier transistors and one of the plurality of signal lines.

12. The solid state imaging apparatus of claim **9**, wherein one of the plurality of row select transistors is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

13. The solid state imaging apparatus of claim **9**, wherein one of the plurality of row select transistors is adjacent to one of the plurality of pixel amplifier transistors.

14. The solid state imaging apparatus of claim **1**, further comprising a plurality of VDDCELL lines each being connected to one of the plurality of the reset transistors,

wherein one of the column n and the column n+1 is disposed between one of the plurality of VDDCELL lines and the other of the column n and the column n+1.

15. A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the plurality of photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors;

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of pixel amplifier transistors each detecting and outputting the potential of one of the plurality of floating diffusion sections;

a plurality of signal lines each transferring an output from one of the plurality of pixel amplifier transistors,

wherein the plurality of photodiodes include a first photodiode, a second photodiode, a third photodiode and a fourth photodiode,

the plurality of transfer transistors include a first transfer transistor, a second transfer transistor, a third transfer transistor and a fourth transfer transistor,

the plurality of read-out lines include a first read-out line, a second read-out line, a third read-out line and a fourth read-out line,

the first photodiode is in row m and column n, where m and n are a positive integer respectively,

the second photodiode is in row m and column n+1,

the third photodiode is in row m+1 and column n,

the fourth photodiode is in row m+1 and column n+1,

the first read-out line is adjacent to the second read-out line,

the second read-out line is disposed between the first read-out line and the third read-out line,

the third read-out line is disposed between the second read-out line and the fourth read-out line,

the first read-out line is connected to the second photodiode via the first transfer transistor,

the second read-out line is connected to the first photodiode via the second transfer transistor,

the third read-out line is connected to the fourth photodiode via the third transfer transistor,

the fourth read-out line is connected to the third photodiode via the fourth transfer transistor, and

one of the column n and the column n+1 is disposed between one of the plurality of signal lines and the other of the column n and the column n+1.

16. The solid state imaging apparatus of claim **15**, wherein the row m is adjacent to the row m+1, and

the column n is adjacent to the column n+1.

17. The solid state imaging apparatus of claim **15**, wherein no read-out line is disposed between the second read-out line and the third read-out line, and

no read-out line is disposed between the third read-out line and the fourth read-out line.

18. The solid state imaging apparatus of claim **15**, wherein one of the plurality of floating diffusion sections is connected to the first photodiode via the second transfer transistor,

the one of the plurality of floating diffusion sections is connected to the second photodiode via the first transfer transistor,

the one of the plurality of floating diffusion sections is connected to the third photodiode via the fourth transfer transistor, and

the one of the plurality of floating diffusion sections is connected to the fourth photodiode via the third transfer transistor.

19. The solid state imaging apparatus of claim **15**, wherein one of the plurality of floating diffusion sections is disposed between the column n and the column n+1.

20. The solid state imaging apparatus of claim **15**, wherein one of the plurality of pixel amplifier transistors is disposed between the row m and the row m+1.

21. The solid state imaging apparatus of claim **15**, wherein one of the plurality of floating diffusion sections is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

22. The solid state imaging apparatus of claim **15**, wherein the plurality of read-out lines and one of the plurality of signal lines intersect with each other.

23. The solid state imaging apparatus of claim **15**, further comprising a plurality of row select transistors each being connected to one of the plurality of pixel amplifier transistors.

24. The solid state imaging apparatus of claim **23**, wherein one of the plurality of row select transistors is disposed between the row m and the row m+1.

25. The solid state imaging apparatus of claim **23**, wherein one of the plurality of row select transistors is disposed between one of the plurality of pixel amplifier transistors and one of the plurality of signal lines.

26. The solid state imaging apparatus of claim **23**, wherein one of the plurality of row select transistors is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

27. The solid state imaging apparatus of claim **23**, wherein one of the plurality of row select transistors is adjacent to one of the plurality of pixel amplifier transistors.

28. The solid state imaging apparatus of claim **15**, further comprising a plurality of VDDCELL lines each being connected to one of the plurality of the reset transistors,

wherein one of the column n and the column n+1 is disposed between one of the plurality of VDDCELL lines and the other of the column n and the column n+1.

29. A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the plurality of photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors;

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of pixel amplifier transistors each detecting and outputting the potential of one of the plurality of floating diffusion sections;

a plurality of signal lines each transferring an output from one of the plurality of pixel amplifier transistors,

wherein the plurality of photodiodes include a first photodiode, a second photodiode, a third photodiode and a fourth photodiode,

the plurality of transfer transistors include a first transfer transistor, a second transfer transistor, a third transfer transistor and a fourth transfer transistor,

the plurality of read-out lines include a first read-out line, a second read-out line, a third read-out line and a fourth read-out line,

the first photodiode is in row m and column n, where m and n are a positive integer respectively,

the second photodiode is in row m and column n+1,

the third photodiode is in row m+1 and column n,

the fourth photodiode is in row m+1 and column n+1,

the first read-out line is adjacent to the second read-out line,

the second read-out line is disposed between the first read-out line and the third read-out line,

the third read-out line is disposed between the second read-out line and the fourth read-out line,

the first read-out line is connected to the first photodiode via the first transfer transistor,

the second read-out line is connected to the second photodiode via the second transfer transistor,

the third read-out line is connected to the third photodiode via the third transfer transistor,

the fourth read-out line is connected to the fourth photodiode via the fourth transfer transistor, and

one of the column n and the column n+1 is disposed between one of the plurality of signal lines and the other of the column n and the column n+1.

30. The solid state imaging apparatus of claim of claim **29**, wherein the row m is adjacent to the row m+1, and

the column n is adjacent to the column n+1.

31. The solid state imaging apparatus of claim **29**, wherein no read-out line is disposed between the second read-out line and the third read-out line, and

no read-out line is disposed between the third read-out line and the fourth read-out line.

32. The solid state imaging apparatus of claim **29**, wherein one of the plurality of floating diffusion sections is connected to the first photodiode via the first transfer transistor,

the one of the plurality of floating diffusion sections is connected to the second photodiode via the second transfer transistor,

the one of the plurality of floating diffusion sections is connected to the third photodiode via the third transfer transistor, and

the one of the plurality of floating diffusion sections is connected to the fourth photodiode via the fourth transfer transistor.

33. The solid state imaging apparatus of claim 29, wherein one of the plurality of floating diffusion sections is disposed between the column n and the column n+1.

34. The solid state imaging apparatus of claim 29, wherein one of the plurality of pixel amplifier transistors is disposed between the row m and the row m+1.

35. The solid state imaging apparatus of claim 29, wherein one of the plurality of floating diffusion sections is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

36. The solid state imaging apparatus of claim 29, wherein the plurality of read-out lines and one of the plurality of signal lines intersect with each other.

37. The solid state imaging apparatus of claim 29, further comprising a plurality of row select transistors each being connected to one of the plurality of pixel amplifier transistors.

38. The solid state imaging apparatus of claim 37, wherein one of the plurality of row select transistors is disposed between the row m and the row m+1.

39. The solid state imaging apparatus of claim 37, wherein one of the plurality of row select transistors is disposed between one of the plurality of pixel amplifier transistors and one of the plurality of signal lines.

40. The solid state imaging apparatus of claim 37, wherein one of the plurality of row select transistors is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

41. The solid state imaging apparatus of claim 37, wherein one of the plurality of row select transistors is adjacent to one of the plurality of pixel amplifier transistors.

42. The solid state imaging apparatus of claim 29, further comprising a plurality of VDDCELL lines each being connected to one of the plurality of the reset transistors,

wherein one of the column n and the column n+1 is disposed between one of the plurality of VDDCELL lines and the other of the column n and the column n+1.

* * * * *

Docket No.: 085393-0727 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Mitsuyoshi MORI, et al.	:	Confirmation Number: 3190
Application No.: 13/335,537	:	Group Art Unit: 2897
Filed: December 22, 2011	:	Examiner: John C. Ingham

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated May 30, 2012, having a three-month shortened statutory period for response set to expire on August 30, 2012, reconsideration of the above-identified application is respectfully requested in view of the following amendment and remarks.

AMENDMENT TO THE CLAIMS

1-30. (Canceled)

31. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the plurality of photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors;

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of pixel amplifier transistors each detecting and outputting the potential of one of the plurality of floating diffusion sections;

a plurality of signal lines each transferring an output from one of the plurality of pixel amplifier transistors,

wherein the plurality of photodiodes include a first photodiode, a second photodiode, a third photodiode and a fourth photodiode,

the plurality of transfer transistors include a first transfer transistor, a second transfer transistor, a third transfer transistor and a fourth transfer transistor,

the plurality of read-out lines include a first read-out line, a second read-out line, a third read-out line and a fourth read-out line,

the first read-out line is adjacent to the second read-out line,

the second read-out line is disposed between the first read-out line and the third read-out line,

the third read-out line is disposed between the second read-out line and the fourth read-out line,

the first read-out line is connected to the first photodiode in row m via the first transfer transistor, where m is a positive integer,

the second read-out line is connected to the second photodiode in the row m via the second transfer transistor,

the third read-out line is connected to the third photodiode in row m+1 via the third transfer transistor,

the fourth read-out line is connected to the fourth photodiode in the row m+1 via the fourth transfer transistors,

the first photodiode and the third photodiode are disposed in one of column n and column n+1, where n is a positive integer, [[and]]

the second photodiode and the fourth photodiode are disposed in the other of the column n and the column n+1, and

one of the column n and the column n+1 is disposed between one of the plurality of signal lines and the other of the column n and the column n+1.

32. (Previously presented) The solid state imaging apparatus of claim 31, wherein the row m is adjacent to the row m+1, and

the column n is adjacent to the column n+1.

33. (Previously presented) The solid state imaging apparatus of claim 31, wherein no read-out line is disposed between the second read-out line and the third read-out line, and

no read-out line is disposed between the third read-out line and the fourth read-out line.

34. (Previously presented) The solid state imaging apparatus of claim 31, wherein one of the plurality of floating diffusion sections is connected to the first photodiode via the first transfer transistor,

the one of the plurality of floating diffusion sections is connected to the second photodiode via the second transfer transistor,

the one of the plurality of floating diffusion sections is connected to the third photodiode via the third transfer transistor, and

the one of the plurality of floating diffusion sections is connected to the fourth photodiode via the fourth transfer transistor.

35. (Previously presented) The solid state imaging apparatus of claim 31, wherein one of the plurality of floating diffusion sections is disposed between the column n and the column n+1.

36. (Previously presented) The solid state imaging apparatus of claim 31, wherein one of the plurality of pixel amplifier transistors is disposed between the row m and the row m+1.

37. (Previously presented) The solid state imaging apparatus of claim 31, wherein one of the plurality of floating diffusion sections is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

38. (Previously presented) The solid state imaging apparatus of claim 31, wherein the plurality of read-out lines and one of the plurality of signal lines intersect with each other.

39. (Previously presented) The solid state imaging apparatus of claim 31, further comprising a plurality of row select transistors each being connected to one of the plurality of pixel amplifier transistors.

40. (Previously presented) The solid state imaging apparatus of claim 39, wherein one of the plurality of row select transistors is disposed between the row m and the row m+1.

41. (Previously presented) The solid state imaging apparatus of claim 39, wherein one of the plurality of row select transistors is disposed between one of the plurality of pixel amplifier transistors and one of the plurality of signal lines.

42. (Previously presented) The solid state imaging apparatus of claim 39, wherein one of the plurality of row select transistors is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

43. (Previously presented) The solid state imaging apparatus of claim 39, wherein one of the plurality of row select transistors is adjacent to one of the plurality of pixel amplifier transistors.

44. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the plurality of photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors;

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of pixel amplifier transistors each detecting and outputting the potential of one of the plurality of floating diffusion sections;

a plurality of signal lines each transferring an output from one of the plurality of pixel amplifier transistors,

wherein the plurality of photodiodes include a first photodiode, a second photodiode, a third photodiode and a fourth photodiode,

the plurality of transfer transistors include a first transfer transistor, a second transfer transistor, a third transfer transistor and a fourth transfer transistor,

the plurality of read-out lines include a first read-out line, a second read-out line, a third read-out line and a fourth read-out line,

the first photodiode is in row m and column n, where m and n are a positive integer respectively,

the second photodiode is in row m and column n+1,

the third photodiode is in row m+1 and column n,

the fourth photodiode is in row m+1 and column n+1,

the first read-out line is adjacent to the second read-out line,

the second read-out line is disposed between the first read-out line and the third read-out line,

the third read-out line is disposed between the second read-out line and the fourth read-out line,

the first read-out line is connected to the second photodiode via the first transfer transistor,

the second read-out line is connected to the first photodiode via the second transfer transistor,

the third read-out line is connected to the fourth photodiode via the third transfer transistor, [[and]]

the fourth read-out line is connected to the third photodiode via the fourth transfer transistor, and

one of the column n and the column n+1 is disposed between one of the plurality of signal lines and the other of the column n and the column n+1.

45. (Previously presented) The solid state imaging apparatus of claim 44, wherein the row m is adjacent to the row m+1, and

the column n is adjacent to the column n+1.

46. (Previously presented) The solid state imaging apparatus of claim 44, wherein no read-out line is disposed between the second read-out line and the third read-out line, and

no read-out line is disposed between the third read-out line and the fourth read-out line.

47. (Previously presented) The solid state imaging apparatus of claim 44, wherein one of the plurality of floating diffusion sections is connected to the first photodiode via the second transfer transistor,

the one of the plurality of floating diffusion sections is connected to the second photodiode via the first transfer transistor,

the one of the plurality of floating diffusion sections is connected to the third photodiode via the fourth transfer transistor, and

the one of the plurality of floating diffusion sections is connected to the fourth photodiode via the third transfer transistor.

48. (Previously presented) The solid state imaging apparatus of claim 44, wherein one of the plurality of floating diffusion sections is disposed between the column n and the column n+1.

49. (Previously presented) The solid state imaging apparatus of claim 44, wherein one of the plurality of pixel amplifier transistors is disposed between the row m and the row m+1.

50. (Previously presented) The solid state imaging apparatus of claim 44, wherein one of the plurality of floating diffusion sections is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

51. (Previously presented) The solid state imaging apparatus of claim 44, wherein the plurality of read-out lines and one of the plurality of signal lines intersect with each other.

52. (Previously presented) The solid state imaging apparatus of claim 44, further comprising a plurality of row select transistors each being connected to one of the plurality of pixel amplifier transistors.

53. (Previously presented) The solid state imaging apparatus of claim 52, wherein one of the plurality of row select transistors is disposed between the row m and the row m+1.

54. (Previously presented) The solid state imaging apparatus of claim 52, wherein one of the plurality of row select transistors is disposed between one of the plurality of pixel amplifier transistors and one of the plurality of signal lines.

55. (Previously presented) The solid state imaging apparatus of claim 52, wherein one of the plurality of row select transistors is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

56. (Previously presented) The solid state imaging apparatus of claim 52, wherein one of the plurality of row select transistors is adjacent to one of the plurality of pixel amplifier transistors.

57. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photodiodes arranged in an array;

a plurality of floating diffusion sections each being connected to ones of the plurality of photodiodes via each of a plurality of transfer transistors;

a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors;

a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;

a plurality of pixel amplifier transistors each detecting and outputting the potential of one of the plurality of floating diffusion sections;

a plurality of signal lines each transferring an output from one of the plurality of pixel amplifier transistors,

wherein the plurality of photodiodes include a first photodiode, a second photodiode, a third photodiode and a fourth photodiode,

the plurality of transfer transistors include a first transfer transistor, a second transfer transistor, a third transfer transistor and a fourth transfer transistor,

the plurality of read-out lines include a first read-out line, a second read-out line, a third read-out line and a fourth read-out line,

the first photodiode is in row m and column n, where m and n are a positive integer respectively,

the second photodiode is in row m and column n+1,

the third photodiode is in row m+1 and column n,

the fourth photodiode is in row m+1 and column n+1,

the first read-out line is adjacent to the second read-out line,

the second read-out line is disposed between the first read-out line and the third read-out line,

the third read-out line is disposed between the second read-out line and the fourth read-out line,

the first read-out line is connected to the first photodiode via the first transfer transistor,

the second read-out line is connected to the second photodiode via the second transfer transistor,

the third read-out line is connected to the third photodiode via the third transfer transistor, [[and]]

the fourth read-out line is connected to the fourth photodiode via the fourth transfer transistor, and

one of the column n and the column n+1 is disposed between one of the plurality of signal lines and the other of the column n and the column n+1.

58. (Previously presented) The solid state imaging apparatus of claim of claim 57, wherein the row m is adjacent to the row m+1, and

the column n is adjacent to the column n+1.

59. (Previously presented) The solid state imaging apparatus of claim 57, wherein no read-out line is disposed between the second read-out line and the third read-out line, and

no read-out line is disposed between the third read-out line and the fourth read-out line.

60. (Previously presented) The solid state imaging apparatus of claim 57, wherein one of the plurality of floating diffusion sections is connected to the first photodiode via the first transfer transistor,

the one of the plurality of floating diffusion sections is connected to the second photodiode via the second transfer transistor,

the one of the plurality of floating diffusion sections is connected to the third photodiode via the third transfer transistor, and

the one of the plurality of floating diffusion sections is connected to the fourth photodiode via the fourth transfer transistor.

61. (Previously presented) The solid state imaging apparatus of claim 57, wherein one of the plurality of floating diffusion sections is disposed between the column n and the column n+1.

62. (Previously presented) The solid state imaging apparatus of claim 57, wherein one of the plurality of pixel amplifier transistors is disposed between the row m and the row m+1.

63. (Previously presented) The solid state imaging apparatus of claim 57, wherein one of the plurality of floating diffusion sections is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

64. (Previously presented) The solid state imaging apparatus of claim 57, wherein the plurality of read-out lines and one of the plurality of signal lines intersect with each other.

65. (Previously presented) The solid state imaging apparatus of claim 57, further comprising a plurality of row select transistors each being connected to one of the plurality of pixel amplifier transistors.

66. (Previously presented) The solid state imaging apparatus of claim 65, wherein one of the plurality of row select transistors is disposed between the row m and the row m+1.

67. (Previously presented) The solid state imaging apparatus of claim 65, wherein one of the plurality of row select transistors is disposed between one of the plurality of pixel amplifier transistors and one of the plurality of signal lines.

68. (Previously presented) The solid state imaging apparatus of claim 65, wherein one of the plurality of row select transistors is disposed between one of the plurality of reset transistors and one of the plurality of signal lines.

69. (Previously presented) The solid state imaging apparatus of claim 65, wherein one of the plurality of row select transistors is adjacent to one of the plurality of pixel amplifier transistors.

70. (New) The solid state imaging apparatus of claim 31, further comprising a plurality of VDDCELL lines each being connected to one of the plurality of the reset transistors,

wherein one of the column n and the column n+1 is disposed between one of the plurality of VDDCELL lines and the other of the column n and the column n+1.

71. (New) The solid state imaging apparatus of claim 44, further comprising a plurality of VDDCELL lines each being connected to one of the plurality of the reset transistors,

wherein one of the column n and the column n+1 is disposed between one of the plurality of VDDCELL lines and the other of the column n and the column n+1.

72. (New) The solid state imaging apparatus of claim 57, further comprising a plurality of VDDCELL lines each being connected to one of the plurality of the reset transistors,

wherein one of the column n and the column n+1 is disposed between one of the plurality of VDDCELL lines and the other of the column n and the column n+1.

REMARKS

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Ingham. As a result of the interview, it was agreed that the enclosed amendment would obviate the pending rejection. Applicants and Applicants' representative would like to thank Examiner Ingham for his courtesy in conducting the interview and for his assistance in resolving issues. A summary of the interview discussion follows.

Claims 31-69 stand rejected under 35 U.S.C. § 102 as being anticipated by Hashimoto '906 ("Hashimoto"). Claims 31, 44 and 57 are independent. This rejection is respectfully traversed for the following reasons.

Each of independent claims 31, 44 and 57 embody a configuration in which one of the column n and the column n+1 is disposed between one of the plurality of signal lines and the other of the column n and the column n+1. In contrast, as shown in Figure 10 of Hashimoto, neither of column n (containing a11 or a12) and column n+1 (containing other of a11 or a12) is disposed between the signal line (unlabeled SO) and the other of the column n and the column n+1. Rather, the signal line SO is disposed between column n and column n+1.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Hashimoto does not anticipate claims 31, 44 and 57, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination. Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

Ramyar M. Farid
Registration No. 46,692
Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 RMF:MWE
Facsimile: 202.756.8087
Date: August 27, 2012

Notice of Allowability	Application No.	Applicant(s)	
	13/335,537	MORI ET AL.	
	Examiner	Art Unit	
	JOHN C. INGHAM	2897	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendments filed 27 Aug. 2012*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *31-72*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/JOHN C INGHAM/
Examiner, Art Unit 2897

Allowable Subject Matter

1. Claims 31-72 are allowed.

2. The following is an examiner's statement of reasons for allowance: the prior art does not disclose or make obvious the solid state imaging apparatus of claims 31, 44 and 57, including each of the limitations and specifically: a plurality of read-out lines each being selectively connected to at least two of the plurality of transfer transistors; the first read-out line is adjacent to the second read-out line; the second read-out line is disposed between the first and third read-out lines; the third read-out line is disposed between the second and fourth read-out lines; and one of the column n and the column n+1 is disposed between one of the plurality of signal lies and the other of the column n and n+1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on Monday to Friday, 9AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on 571-272-1867. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOHN C INGHAM/
Examiner, Art Unit 2897

US007436010B2

(12) **United States Patent**
Mori et al.

(10) **Patent No.: US 7,436,010 B2**
(45) **Date of Patent: Oct. 14, 2008**

(54) **SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME**

(75) Inventors: **Mitsuyoshi Mori**, Kyoto (JP); **Takumi Yamaguchi**, Kyoto (JP); **Takahiko Murata**, Osaka (JP)

(73) Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 233 days.

(21) Appl. No.: **10/706,918**

(22) Filed: **Nov. 14, 2003**

(65) **Prior Publication Data**

US 2004/0159861 A1 Aug. 19, 2004

(30) **Foreign Application Priority Data**

Feb. 13, 2003 (JP) 2003-034692

(51) **Int. Cl.**
H01L 31/062 (2006.01)

(52) **U.S. Cl.** **257/292**; 257/222; 257/444; 257/E27.132

(58) **Field of Classification Search** 257/444–445, 257/223, 291, 292, E27.132
See application file for complete search history.

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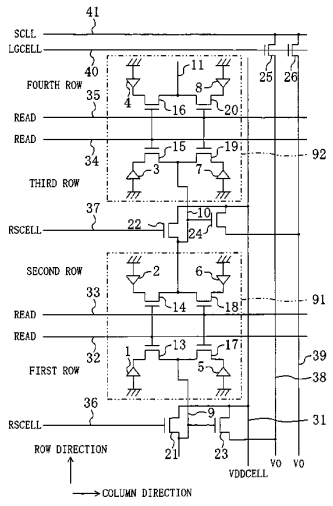
Primary Examiner—Howard Weiss
Assistant Examiner—John Ingham
(74) *Attorney, Agent, or Firm*—McDermott Will & Emery LLP

(57) **ABSTRACT**

A solid state imaging apparatus includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the same row of each said photoelectric conversion via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. Charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

17 Claims, 10 Drawing Sheets



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Japanese Office Action issued in corresponding Japanese Patent Application No. JP 2004-034818, dated Oct. 24, 2006.

* cited by examiner

FIG. 1

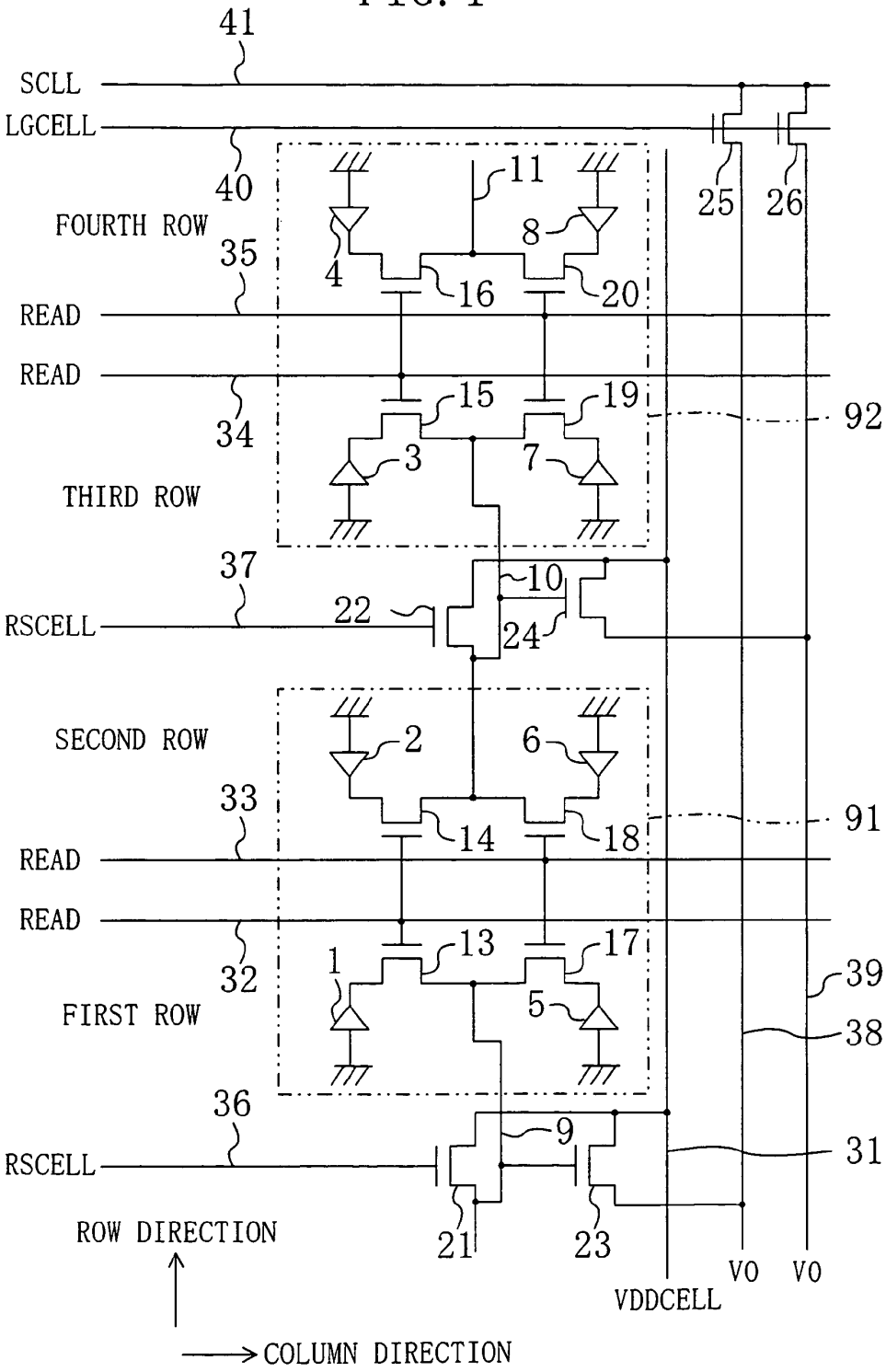

41
SCLL
LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
33
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
2
6
14
18
91
13
17
1
5
39
38
9
31
21
23
VO
VO
VDDCELL

FIG. 2

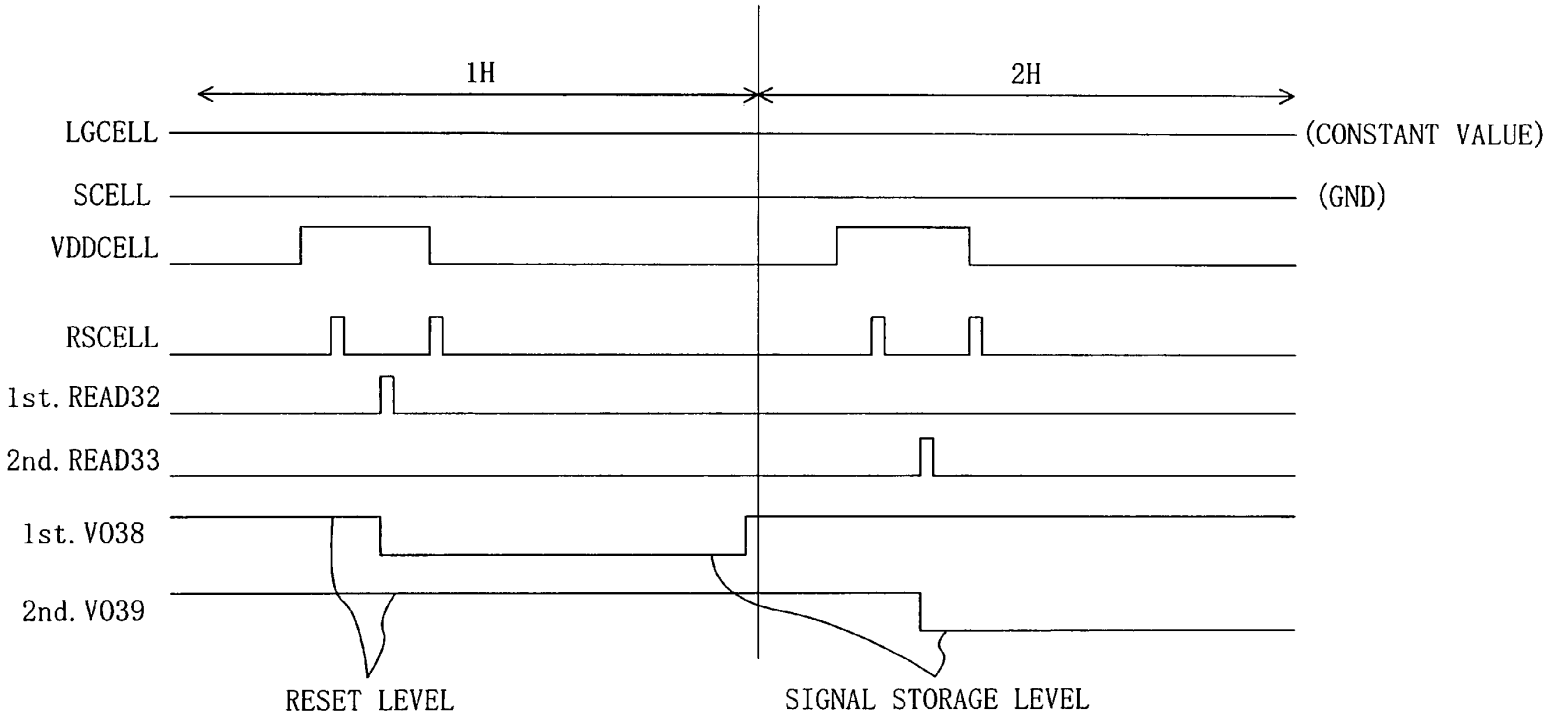

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
RSCELL
1st. READ32
2nd. READ33
1st. VO38
2nd. VO39
RESET LEVEL
SIGNAL STORAGE LEVEL

FIG. 3

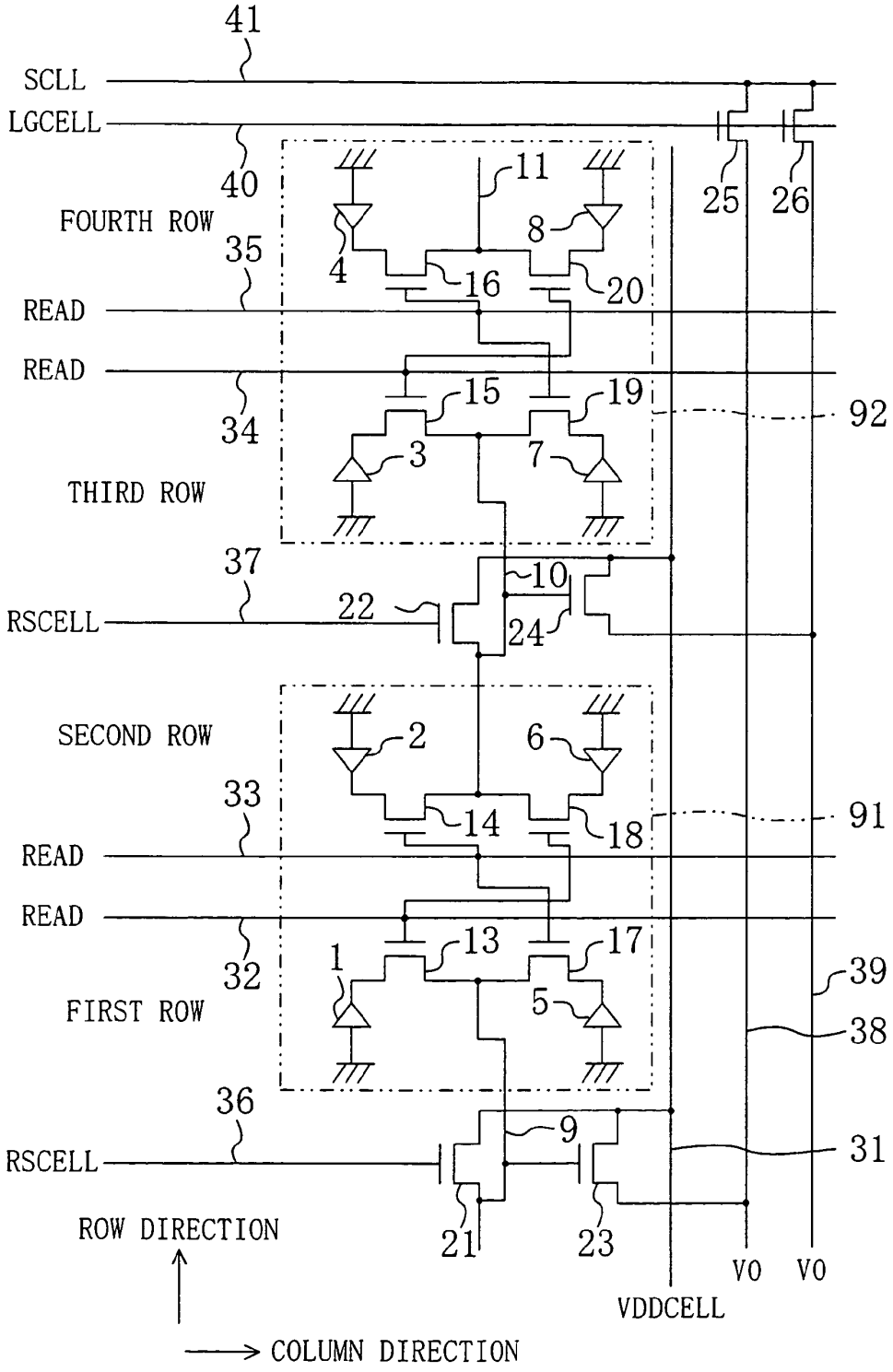

41
SCLL
LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
33
READ
READ
32
FIRST ROW
36
RSCELL
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
15
19
3
7
10
22
24
2
6
14
18
1
13
17
5
9
21
23
25
26
92
91
39
38
31
VO
VO
VDDCELL

FIG. 4

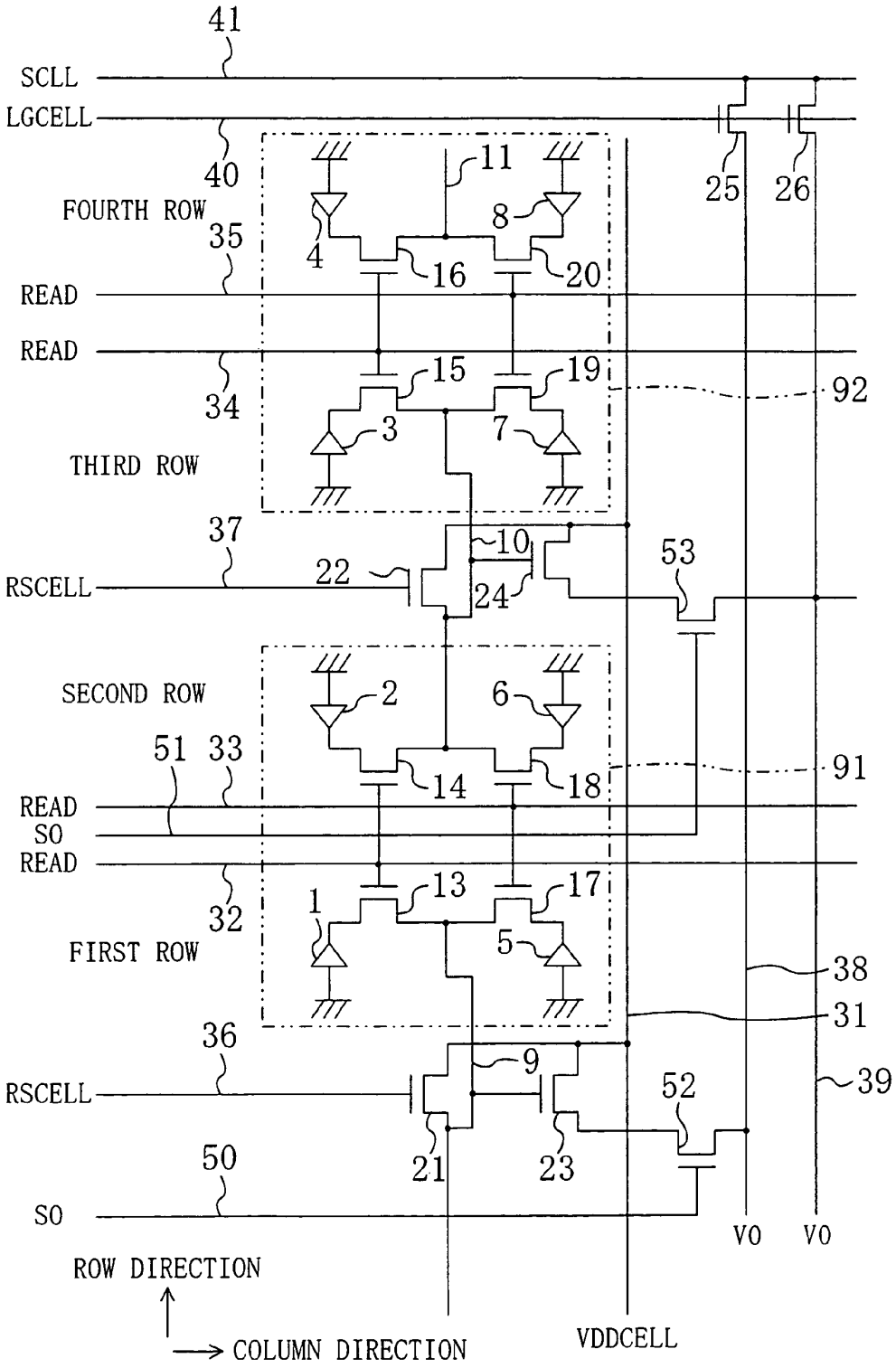

41
SCLL
LGCELL
40
FOURTH ROW
35
READ
READ
34
THIRD ROW
37
RSCELL
SECOND ROW
51
33
READ
SO
READ
32
FIRST ROW
36
RSCELL
50
SO
ROW DIRECTION
COLUMN DIRECTION
11
8
4
16
20
25
26
15
19
92
3
7
10
22
24
53
2
6
14
18
91
13
17
1
5
38
31
9
52
39
21
23
VO
VO
VDDCELL

FIG. 5

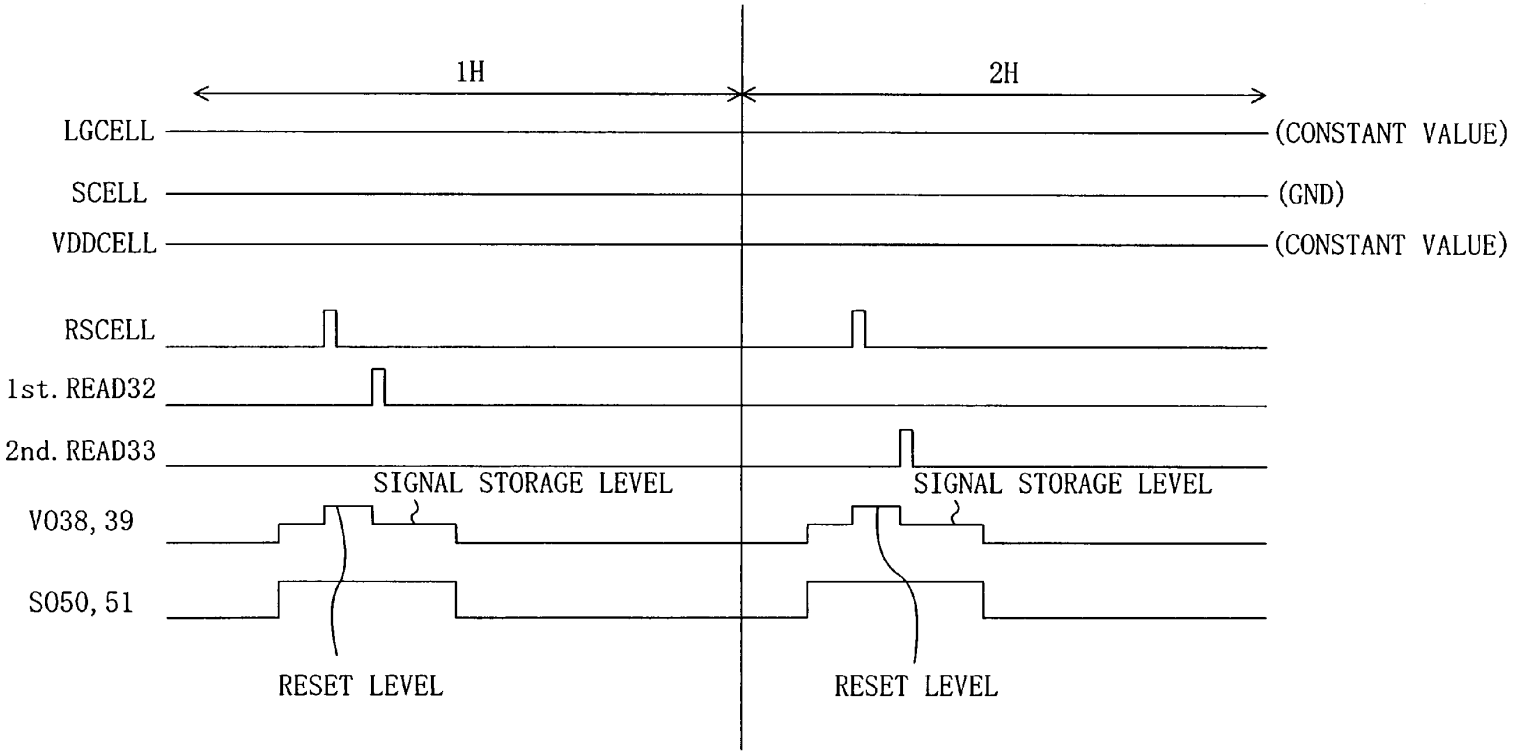

1H
2H
LGCELL
(CONSTANT VALUE)
SCELL
(GND)
VDDCELL
(CONSTANT VALUE)
RSCELL
1st. READ32
2nd. READ33
SIGNAL STORAGE LEVEL
SIGNAL STORAGE LEVEL
VO38, 39
SO50, 51
RESET LEVEL
RESET LEVEL

FIG. 6

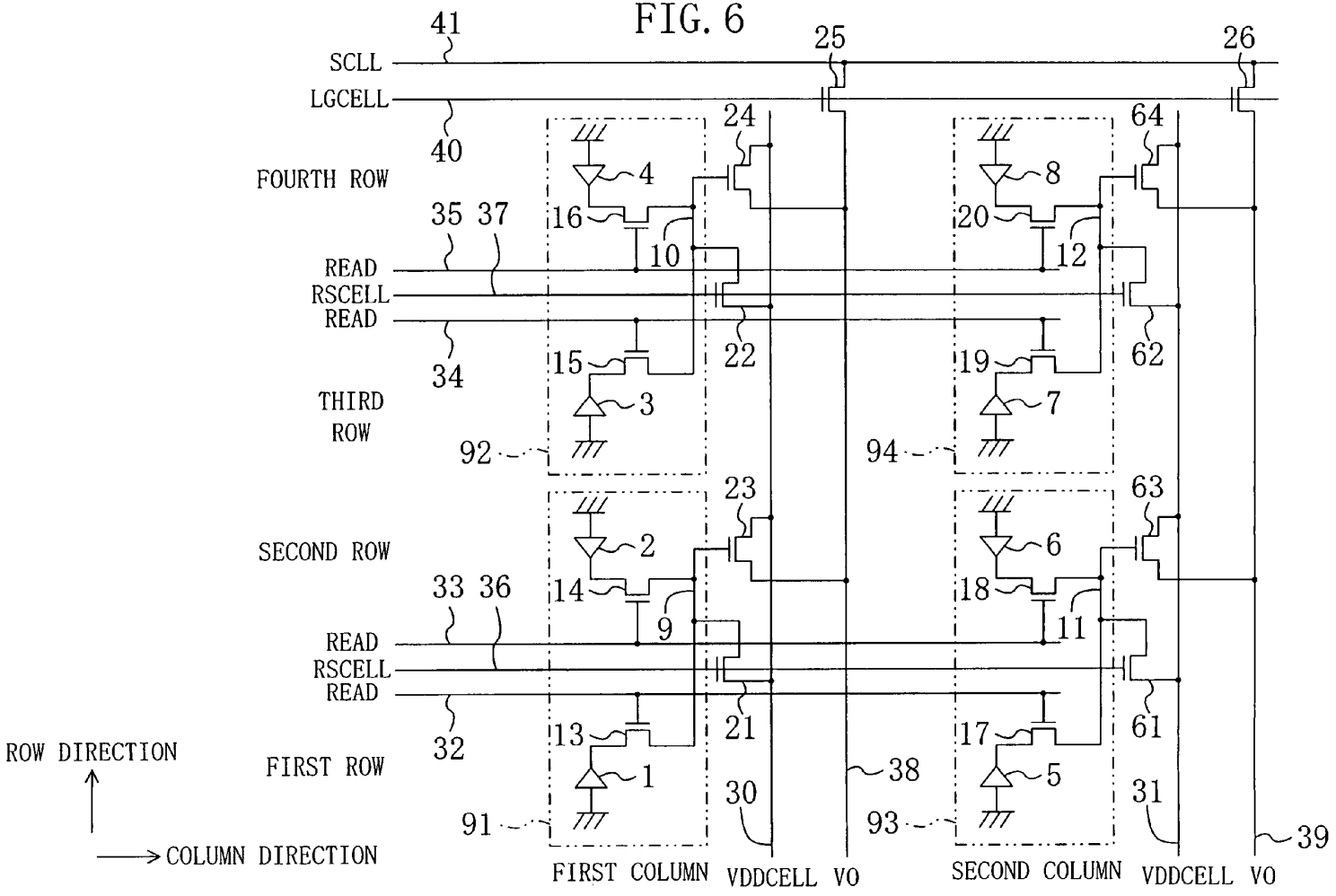

41
SCLL
LGCELL
40
FOURTH ROW
35 37
READ
RSCELL
READ
34
THIRD ROW
SECOND ROW
33 36
READ
RSCELL
READ
32
FIRST ROW
ROW DIRECTION
COLUMN DIRECTION
25
26
24
64
4
8
16
20
10
12
22
62
15
19
3
7
92
94
23
63
2
6
14
18
9
11
21
61
13
17
1
5
38
30
31
39
91
93
FIRST COLUMN
VDDCELL VO
SECOND COLUMN
VDDCELL VO

FIG. 7

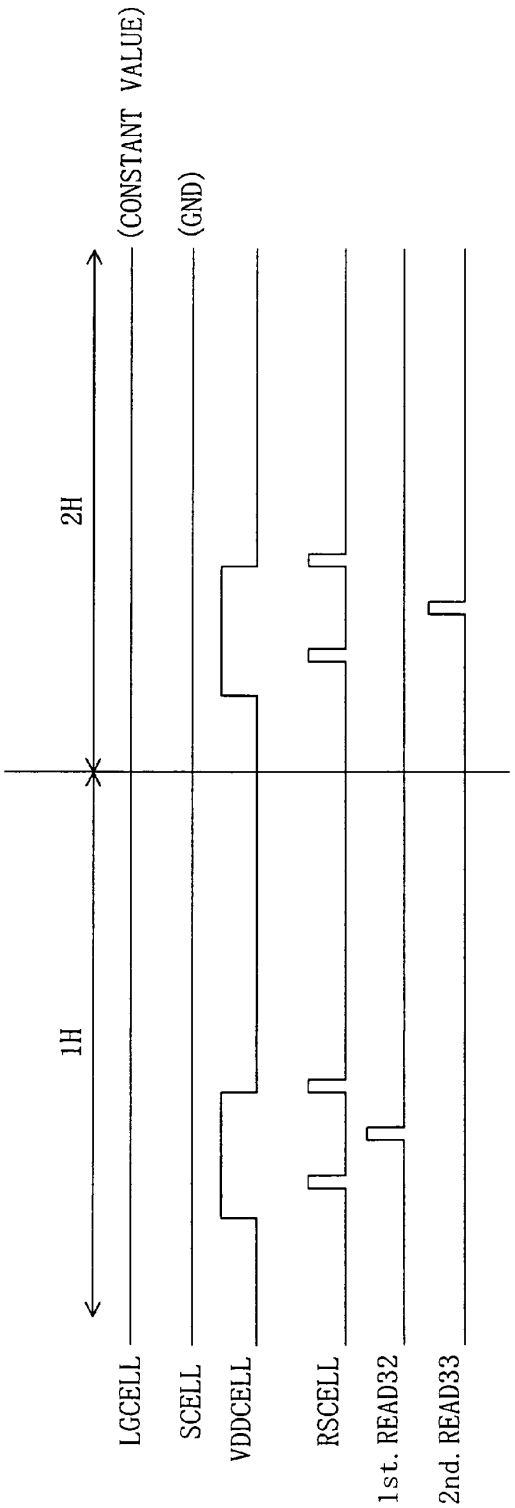

(CONSTANT VALUE)
(GND)
2H
1H
LGCELL
SCELL
VDDCELL
RSCELL
1st. READ32
2nd. READ33

FIG. 8

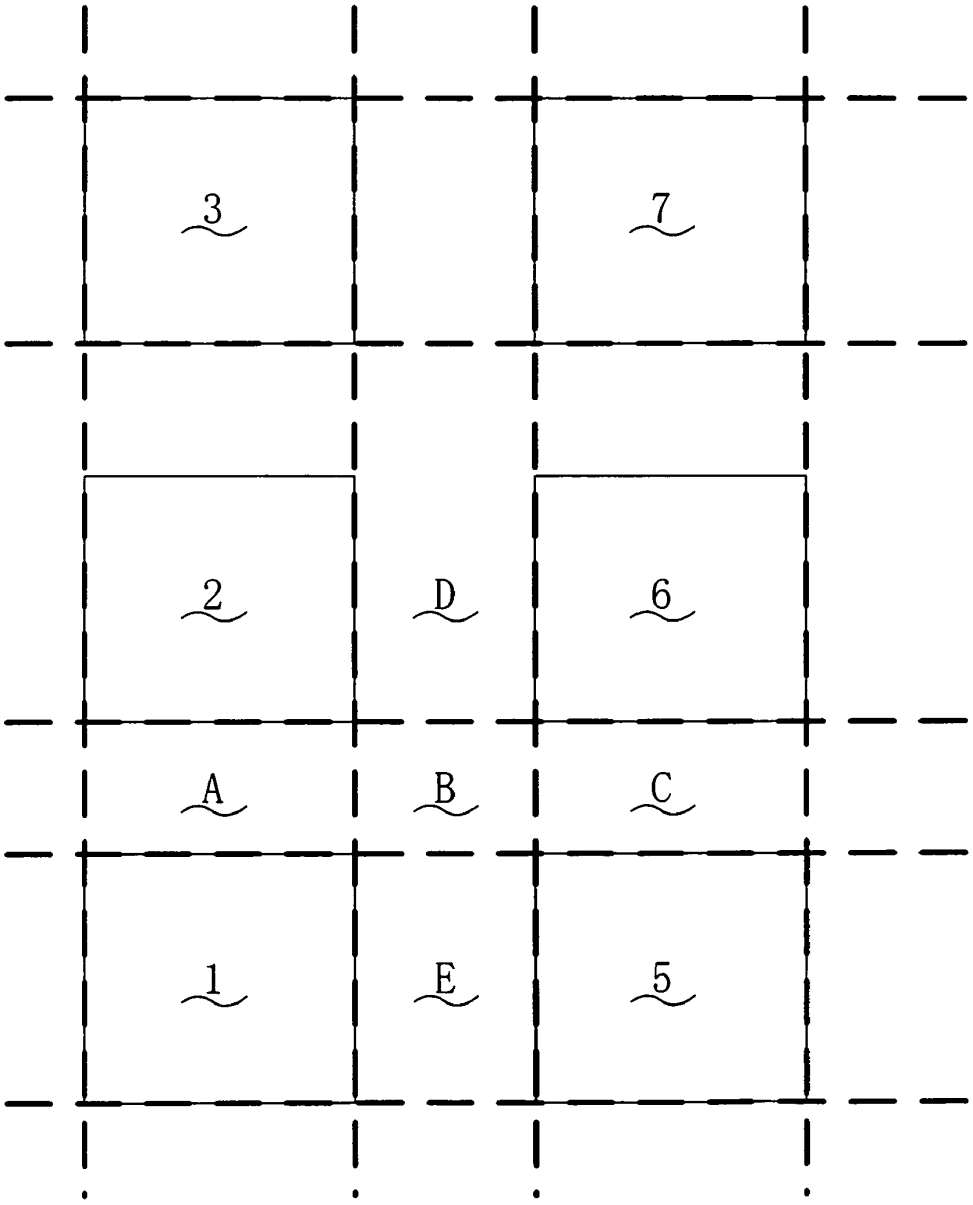
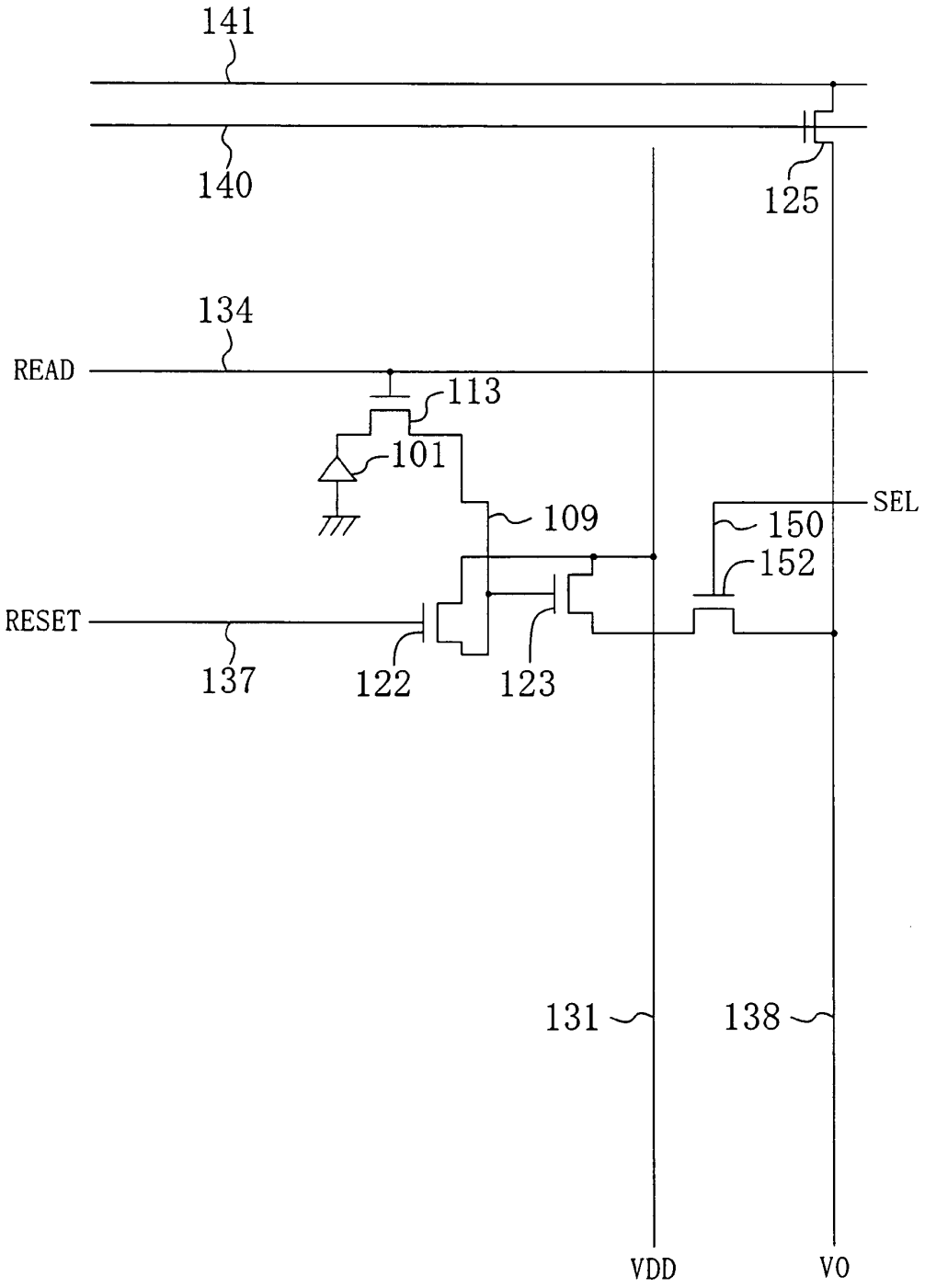


FIG. 9

FD SECTION	PIXEL AMPLIFIER	RESET GATE	APERTURE RATIO
A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	10%
		D REGION、B REGION、E REGION	25%
	D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	35%
D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	20%
	D REGION、B REGION、E REGION	A REGION、B REGION、C REGION	20%
		D REGION、B REGION、E REGION	20%

FIG. 10

PRIOR ART



SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

BACKGROUND OF THE INVENTION

The present invention relates to a solid state imaging apparatus in which a plurality of photoelectric conversion sections are arranged in an array, a method for driving the solid state imaging apparatus and a camera using the solid state imaging apparatus.

FIG. **10** is a diagram illustrating a general circuit configuration for a MOS type image sensor, i.e., a known solid imaging apparatus (e.g., see M. H. White, D. R. Lange, F. C. Blaha and I. A. Mach, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels", IEEE J. Solid-State Circuits. SC-9, pp. 1-13 (1974)).

As shown in FIG. **10**, a photoelectric conversion cell includes a photodiode (PD) section **101**, a transfer transistor **113**, a reset transistor **122**, a pixel amplifier transistor **123**, a select transistor **152**, a floating diffusion (FD) section **109**, a power supply line **131** and an output signal line **138**.

The PD section **101** of which the anode is grounded is connected to the drain of the transfer transistor **113** at the cathode. The source of the transfer transistor **113** is connected to the respective sources of the FD section **109**, the gate of the pixel amplifier transistor **123** and the source of the reset transistor **122**. The gate of the transfer transistor **113** is connected to a read-out line **134**. The reset transistor **122** which receives a reset signal **137** at the gate includes a drain connected to the drain of the pixel amplifier transistor **123** and the power supply line **131**. The source of the pixel amplifier transistor **123** is connected to the drain of the select transistor **152**. The select transistor **152** receives a selection signal SEL at the gate and includes a source connected to the output signal line **138**.

The output signal line **138** is connected to the source of a load gate **125**. The gate of the load gate **125** is connected to a load gate line **140** thereof and the drain is connected to a source power supply line **141**.

In this configuration, a predetermined voltage is applied to the load gate line **140** so that the load gate **125** becomes a constant current source, and then the transfer transistor **113** is temporarily turned ON to transfer charge photoelectric-converted in the PD section **101** to the FD section **109**. Then, the potential of the PD section **101** is detected by the pixel amplifier transistor **123**. In this case, by turning the select transistor **152** ON, signal change can be detected through the output signal line **138**.

However, in the known solid state apparatus, four transistors **113** **122**, **123** and **152** and five lines **131**, **134**, **137**, **138** and **150** are required for total in each photoelectric conversion cell. Accordingly, the areas of transistor and line sections in a cell are increased. For example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD section **101** to the photoelectric conversion cell is only about 5% Therefore, it is difficult to ensure a sufficiently large area of opening of the PD section **101** and also to reduce the size of the photoelectric conversion cell.

SUMMARY OF THE INVENTION

It is an object of the present invention to solve the above-described problems and, to reduce in a FDA (floating diffusion amplifier) system, the size of a photoelectric conversion cell while increasing an aperture area of a photoelectric conversion section.

To achieve the above-described object, the present invention has been deviced, so that a configuration in which a transistor and an interconnect can be shared by a plurality of photoelectric conversion (PD) sections is used in a solid state imaging apparatus.

Specifically, a first solid sate imaging apparatus includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows and two columns; a plurality of floating diffusion sections each being connected to each of ones of the photoelectric sections which are included in the sane row of each said photoelectric conversion cell via each of a plurality of transfer transistors, and being shared by said ones of the photoelectric sections which are included in the same row; a plurality of read-out lines each being selectively connected to at least two of the transfer transistors; and a plurality of pixel amplifier transistors each detecting and outputting the potential of each said the floating diffusion section. In the apparatus, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections.

In the first solid imaging apparatus, each said floating diffusion section is shared by ones of the photoelectric conversion sections included in the same row, and furthermore, respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by different floating diffusion sections. Thus, the number of read-out lines per photoelectric conversion cell becomes 0.5. As a result, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in the same column. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in the same column can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

Moreover, in the first solid state imaging apparatus, it is preferable that wherein each said read-out line is connected to a transfer transistor connected to ones of the photoelectric conversion sections which are included in two adjacent columns, respectively. Thus, charges of at least two of said ones of the photoelectric conversion sections which are included in two adjacent columns, respectively, can be output through a floating diffusion section, a pixel amplifier transistor and a signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by a row which is read out bar a transfer transistor connected to one of the read-out line and another row which is adjacent to the read-out row.

It is preferable that the first solid slate imaging apparatus further includes: a signal line for outputting a signal from each said pixel amplifier transistor to the outside; and a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line. Thus, charges from one of the photoelectric conversion sections which are included in adjacent rows, respectively, can be detected through a shared signal line.

In the first solid state imaging apparatus, it is preferable that each said floating diffusion section and each said pixel amplifier transistor are shared by photoelectric conversion sections which are adjacent to each other in the row direction or in the column direction. Thus, the aperture ratio of the photoelectric conversion sections to the photoelectric conversion cell can be increased and also the size of the photoelectric cell can be reduced.

In the first solid state imaging apparatus, it is preferable that in each said floating diffusion section, a reset section for resetting charge stored in the floating diffusion section is provided. Thus, it is possible to stop, after charge read out from a photoelectric conversion section has been detected by an amplifier, detection of charge by the pixel amplifier transistor.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction. Thus, a high quality image can be obtained from signals read out from the photoelectric conversion sections.

It is preferable that the first solid state imaging apparatus further includes a signal processing circuit for processing an output signal from each said pixel amplifier transistor. Thus, a high quality image can be obtained.

In the first solid state imaging apparatus, it is preferable that the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film. Thus, a power supply line can be formed in a different interconnect layer from an interconnect layer in which an output signal line connected to a pixel amplifier transistor is formed. Therefore, the size of a photoelectric conversion cell can be further reduced and also the aperture area can be increased.

A method for driving a solid state imaging apparatus according to the present invention is directed to a method for driving the first solid state imaging apparatus of the present invention and includes: a first step of transferring, in each said photoelectric conversion cell, by a first read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which are not included in the same row but included in two columns adjacent to each other, respectively to one of the floating diffusion sections connected to said ones of the photoelectric conversion sections, and a second step or transferring, by a second read-out line of the read-out lines, signal charges from ones of the photoelectric conversion sections which have not been read out in the first step to the same floating diffusion section connected to said ones of the photoelectric conversion sections as that in the first step.

A second solid state imaging apparatus according to the present invention includes: a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in an array of at least two rows; a plurality of floating diffusion sections each being connected via each of a plurality of transfer transistors, to each of ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same column in each said photoelectric conversion cell, and each being shared by said ones of the photoelectric conversion sections; a plurality of read-out lines each being connected to one of the transfer transistors and independently reading out charge from each of said ones of the photoelectric conversion sections to each said floating diffusion section shared by said ones of the photoelectric conversion sections, and a plurality of pixel amplifier transistors each detecting and outputting the potential of the floating diffusion section.

In the second solid state apparatus each said floating diffusion section is connected to some of the plurality of transfer transistors, is shared by ones of the photoelectric conversion sections which are included in adjacent rows, respectively, and which are included in the same. Furthermore, some of the plurality of read-out lines each independently reading out charge from each of said ones of the photoelectric conversion sections are connected to each said transfer transistor. Thus, a row-select transistor which is usually provided is not needed. As a result, the number of interconnects per photoelectric conversion section is reduced from 5 to 3.5. Therefore, the area of the photoelectric conversion cell itself can be reduced while increasing the area of the photoelectric sections.

It is preferable that the second solid state imaging apparatus further includes a reset transistor for setting charge stored in each said floating diffusion section and the drain of the reset transistor is connected to the drain of the pixel amplifier transistor so that a drain is shared by the reset transistor and the pixel amplifier transistor. Thus, an interconnect connecting between the drain of the reset transistor and the drain of the pixel amplifier transistor can be shared. Accordingly, the number of interconnects per the photoelectric conversion cell can be further reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion sections which are adjacent to each other in the row direction in each said photoelectric conversion cell. Thus, the area of floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and a gate of the MIS transistor is arranged in the column direction. Thus, each said the read-out line can be also function as an interconnect of a transfer transistor, so that the area of the read-out lines occupying the photoelectric conversion cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the, area of the pixel amplifier transistor per photoelectric conversion cell can be reduced whereas the area of the photoelectric conversion sections can be increased. Therefore, light sensitivity is increased.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor and each said floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect connecting between the pixel amplifier transistor and the floating diffusion section can be shortened, so that the areas of the pixel amplifier transistor and the floating diffusion section per photoelectric conversion cell can be reduced.

Moreover, in the second solid state imaging apparatus, it is preferable that each said pixel amplifier transistor is arranged between ones of the photoelectric cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so as to have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

Moreover, in the second solid state imagine apparatus, it is preferable that each said transfer transistor is made of an MIS transistor, and each said pixel amplifier transistor is arranged between respective gates of the MIS transistor and another MIS transistor. Thus, an empty region located in an area of the cell in which a row and a column intersect to each other can be

utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell. Thus, the area of the reset transistors per photoelectric conversion section can be reduced. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said pixel amplifier transistor and the floating diffusion section are arranged between adjacent ones of the read out lines. Thus, an interconnect between the floating diffusion section can be omitted and the source of the reset transistor and the floating diffusion section can be connected to each other to be shared. Therefore, the areas of the reset transistors and the floating diffusion sections per photoelectric conversion cell can be reduced.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors it is preferable that each said reset transistor is connected to a line arranged between ones of the photoelectric cells which are adjacent to each other in the row direction. Thus, pitches of the photoelectric sections in row directions can be matched in a simple manner, so that resolution is improved.

Moreover, in the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that each said reset transistor is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, an opening for each said photoelectric conversion section can be formed so is to have a large area extending in the row direction. Therefore, even if the size of the cell is reduced, light sensitivity can be maintained.

In this case, it is preferable that each said transfer transistor is made of an MIS transistor, and each said reset transistor is arranged between respective gate of the MIS transistor and another MIS transistor. Thus, an empty region located in the area of the cell in which a row and a column intersect to each other can be utilized. Therefore, the area of the photoelectric conversion sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

In the second solid state imaging apparatus, it is preferable that each said floating diffusion section is arranged between ones of the photoelectric conversion cells which are adjacent to each other in the column direction. Thus, the area of the floating diffusion sections per photoelectric conversion cell can be reduced.

In the second solid state imaging apparatus, it is preferable that the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in at least one of the row direction and the column direction. Thus, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

In the case where the second solid state imaging apparatus includes the reset transistors, it is preferable that the line connecting respective drains of the reset transistor and the pixel amplifier transistor also functions as a light-shielding film. Thus, the number of interconnects per photoelectric conversion cell can be reduced. Therefore, the area of the photoelectric sections can be increased and the area of the photoelectric conversion cell itself can be reduced.

It is preferable that each of the first and second solid state imaging apparatus further includes a signal processing circuit for processing an output signal output from each said pixel amplifier transistor. Thus, a high resolution image can be obtained.

A camera according to the present invention includes the first or second solid state imaging apparatus of the present invention. Thus, the camera of the present invention can achieve a high resolution image.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a first embodiment of the present invention.

FIG. **2** is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment.

FIG. **3** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment.

FIG. **4** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a second embodiment of the present invention.

FIG. **5** is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment.

FIG. **6** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention.

FIG. **7** is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment.

FIG. **8** is a plane view schematically illustrating a layout of the photoelectric conversion cell in the solid state imaging apparatus of the third embodiment.

FIG. **9** is a table showing the aperture ratio of PD sections to a photoelectric conversion cell in each of regions A through E of FIG. **8** where a transistor and the like are arranged.

FIG. **10** is a circuit diagram illustrating a photoelectric conversion cell in a known solid imaging apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

A first embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **1** is a circuit diagram illustrating an exemplary photoelectric conversion cell in a solid state imaging apparatus according to the first embodiment of the present invention.

As shown in FIG. **1**, for example, photoelectric conversion (PD) sections **1**, **2**, **3** and **4** each of which is made of a photodiode and converts incident light to electric energy are arranged in this order in the row direction. Furthermore, PD sections **5**, **6**, **7** and **8** are arranged in this order in the row direction so that the PD sections **5**, **6**, **7** and **8** are adjacent to the PD sections **1**, **2**, **3** and **4**, respectively, in the column direction.

Here, in this application, the row direction means to be the direction in which a row number increases and the column direction means to be the direction in which a column number increases.

Between the first and 0^{th} rows (not shown), a first floating diffusion (FD) section **9** for storing photoelectric-converted charges from the PD sections **1** and **5** included in the first row and PD sections included in the 0^{th} row is provided. Between the second and third rows, a second floating diffusion section **10** for storing photoelectric-converted charges from the PD

sections **2** and **6** included in the second row and the PD sections **3** and **7** included in the third row is provided so as to be surrounded by the PD sections **2**, **3**, **6** and **7**. Between the fourth and fifth rows (not shown), a third floating diffusion section **11** for storing photoelectric-converted charges from the PD sections **4** and **8** included in the fourth row and PD sections included in the fifth row is provided. In this manner, each of the FD sections **9**, **10** and **11** is shared by four PD sections.

In this case, a cell including the PD sections **1**, **2**, **5** and **6** is a first photoelectric conversion cell **91** and a cell including the PD sections **3**, **4**, **7** and **8** is a second photoelectric conversion cell **92**.

In the first photoelectric conversion cell **91**, a transfer transistor **13** made of an N channel FET for transferring charge from the PD section **1** to the first FD section **9** is connected between the PD section **1** included in the first row and the first FD section **9**, and a transfer transistor **17** made of an N channel FET for transferring charge from the PD section **5** to the first FD section **9** is connected between the PD section **5** and the first FD section **9**.

Moreover, in the first photoelectric conversion cell **91**, a transfer transistor **14** made of an N channel FET for transferring charges from the PD section **2** to the second FD section **10** is connected between the PD section **2** included in the second row and the second FD section **10**, and a transfer transistor **18** made of an N channel FET for transferring charges from the PD section **6** to the second FD section **10** is connected between the PD section **6** and the second FD section **10**.

As a characteristic of the first embodiment, the transfer transistor **13** included in the first row, and the transfer transistor **14** included in the second row are connected to a first read-out (READ) line **32** while the transfer transistor **17** included in the first row and the transfer transistor **18** included in the second row are connected to a second READ line **33**.

In the second photoelectric conversion cell **92**, a transfer transistor **15** made of an N channel FET for transferring charge from the PD section **3** to the second FD sections **10** is connected between the PD section **3** included in the third row and the second FD section **10**, and a transfer transistor **19** made of an N channel FET for transferring charge from the PD section **7** to the second FD section **10** is connected between the PD section **7** and the second FD section **10**.

Moreover, in the second photoelectric conversion cell **92**, a transfer transistor **16** made of an N channel FET for transferring charges from the PD section **4** to the third FD section **11** is connected between the PD section **4** included in the fourth row and the third FD section **11**, and a transfer transistor **20** made of an N channel FET for transferring charges from the PD section **8** to the third FD section **11** is connected between the PD section **8** and the third FD section **11**.

Also, in this cell, the transfer transistor **15** included in the third row and the transfer transistor **16** included in the fourth row are connected to the third READ line **34**, while the transfer transistor **19** included in the third row and the transfer transistor **20** are connected to the fourth READ line **35**.

To the first FD section **9**, a first reset transistor **21** made of an N channel FET is connected. The first reset transistor **21** includes a source connected to the first FD section **9**, a drain connected to a photoelectric conversion cell power supply (VDDCELL) line **31** and a gate connected to a first reset pulse (RSCELL) line **36**. Thus, charge stored in the first FD section **9** is made to flow through the VDDCELL line **31** by a RSCELL signal.

In the same manner, a second reset transistor **22** made of an N channel FET is connected to the second FD section **10**. The second reset transistor **22** includes a source connected to the second FD section **10**, a drain connected to the VDDCELL line **31** and a gate connected to a second RSCELL line **37**. Note that although not shown in FIG. **1**, a reset transistor of the same configuration as that of the first reset transistor **21** or the like is provided in the third FD section **11**.

To the first FD section **9** and the first reset transistor **21**, a first pixel amplifier transistor **23** made of an N channel FET is connected. The first pixel amplifier transistor **23** includes a gate connected to the first FD section **9** a drain connected to the VDDCELL line **31** and a source connected to a first output signal (VO) line **38**.

In the same manner, a second pixel amplifier transistor **24** made of an N channel FET is connected to the second FD section **10** and the second reset transistor **22**. The second pixel amplifier transistor **24** includes a gate connected to the second FD section **10**, a drain connected to the VDDCELL line **31** and a source connected to a second VO line **39**.

The first VO line **38** and the second VO line **39** are connected to not only the pixel amplifier transistors **23** and **24**, respectively, but also first and second load transistors **25** and **26**, respectively. Each of the first and second load transistor **25** and **26** is made of an N channel for constituting a source follower amplifier. A load gate (LGCELL) line **40** is connected to each of the gates of the first and second load transistors **25** and **26**. A source power supply (SCLL) line **41** is connected to each of the respective drains of first and second load transistors **25** and **26**.

Hereinafter the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **2** is a timing chart showing timing for driving the solid state imaging apparatus of the first embodiment. In this case, a series of operations is completed in a horizontal blanking period (=1 H).

Moreover, as for the detection order of signal charges from the PD sections **1** through **8** arranged in an array, detection is simultaneously carried out in the first and second rows and then detection is simultaneously carried out in the third and fourth rows.

As shown in FIG. **2**, first, high level voltage is applied to the LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source, and then during a period in which the potential of the VDDCELL line **31** is high level, each of the RSCELL lines **36** and **37** is set to be a high level in a pulse state to temporarily turn each of the reset transistors **21** and **22** ON. Thus, each of charges stored in the first FD section **9** in the first photoelectric conversion cell **91** and in the second FD section **10** in the second photoelectric conversion cell **92** is made to flow through the VDDCELL line **31**. In this case, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF; high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the ID section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **2** is transferred to the second FD section **10**. For charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the

second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

Subsequently, when the VDDCELL line **31** is turned to be in a low level OFF state and each of the RSCELL lines **36** and **37** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **10** becomes in the same OFF level state as that of the VDDCELL line **31**. Thus, each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **24** is not operated and thus the vertical line scanning circuit is in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at a reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **17** and **18** ON. Thus, charge stored in the PI) section **4** in the first row is transferred to the first FD section **9** while charge stored in the PD) section **6** in the second row is transferred to the second FD section **10**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

In this manner, charges detected during the first horizontal blanking period **1**H and charges detected during the second horizontal blanking, period **2**H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges.

Subsequently by driving the PD sections in the third and fourth rows in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

Note that in the first embodiment, the circuit configuration and driving method in which after every second column, i.e., every odd-numbered column including the PD sections **1** and **2** have been read out, charges in every even-numbered column including the PD sections **5** and **6** are detected have been described. However, this embodiment is not limited thereto but READ lines can be increased to detect charge in every third column at the same timing as described above.

In the solid state imaging apparatus of the first embodiment as shown in the circuit configuration of FIG. **1**, for example, four PD sections share a FD section, a pixel amplifier transistor and a reset transistor. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 1.5. The number of interconnects can be reduced from 5 (required in the known solid state imaging apparatus) to 2.5. For example, if photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections to the photoelectric conversion cell is about 35%. Therefore, it is possible to reduce the cell sizes of the photoelectric conversion cells **91** and **92** and to largely increase the aperture ratio of the PD section at the same time.

In this connection, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are detected by a READ line at the same timing is applied to the known circuit configuration. If a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 10%.

Moreover, assume that a configuration in which signal charges from two photoelectric conversion sections included in adjacent rows are read out by a READ line, and a FD section and a pixel amplifier transistor included in a row which adjacent to an unread row in a photoelectric conversion cell are shared by two photoelectric sections to detect signal charge is applied to the known circuit configuration. With a driving method in which signal charges are simultaneously detected in the two photoelectric conversion sections, for example, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of PD sections is about 15%.

Modified Example of First Embodiment

FIG. **3** is a diagram illustrating a circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a modified example of the first embodiment of the present invention. Also, in this modified example each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. **3**, for example, in the first photoelectric conversion cell **91**, the first READ line **32** is connected to the transfer transistor **13** and the transfer transistor **18** included in adjacent columns, respectively, while the second READ line **33** is connected to the transfer transistor **14** and the transfer transistor **17** included in adjacent columns, respectively. Thus, even if connections are made with respect to the PD sections **1**, **2**, **5** and **6** included in two adjacent rows with the first and second READ lines **32** and **33** interposed between the PD sections **1** and **5** and the PD sections **2** and **6** so that signal charges from the PD sections which are not included in the same column are transferred, charge can be deflected at the same timing as that shown in FIG. **2**.

For example, when the first READ line **32** is temporarily turned ON, signal charge is transferred from the PD section **1** to the first FD section **9** via the transfer transistor **13** one, at the same time signal charge is transferred from the PD section **6** to the second FD section **10** via the transfer transistor **18**.

Note that in the modified example of the first embodiment, signal charges from two of the four PD sections included in a photoelectric conversion cell **91** are read not during the horizontal blanking period **1**H. However, instead of this, signal charges from all of the four PD sections may be read out.

Moreover, by performing signal processing to signal charges from all of the photoelectric conversion cells which have been read out during different horizontal blanking periods, a high quality image with a large number of pixels can be obtained.

Second Embodiment

Hereinafter, a second embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **4** is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a second embodiment of the present invention. In FIG. **4**, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

First, differences of the solid state imaging apparatus of FIG. **4** from that of the first embodiment shown in FIG. **1** will be described.

In the second embodiment, an configuration in which the first and second pixel amplifier transistors **23** and **24** are connected to the first and second output signal (VO) lines **38** and **39**, respectively, via the first and second select transistors **52** and **53** each of which made of an N channel FET, respectively, is used.

To the respective gates of the first and second select transistors **52** and **53**, first and second select (SO) lines **50** and **51** to which a switching pulse is applied are connected, respectively.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **5** is a timing chart showing timing for driving the solid state imaging apparatus of the second embodiment. In this case, a series of operations is completed in a horizontal blanking period (=1 H).

As shown in FIG. **5**, first, a predetermined voltage is applied to the LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source and the potential of the VDDCELL line **31** is set to be a high level. Subsequently, each of the RSCELL lines **36** and **37** is set to be a high level in a pulse state to temporarily turn each of the reset transistors **21** and **22** ON. Thus, each of charges stored in the first FD section **9** and in the second FD section **10** is made to flow through the VDDCELL line **31**. In this case, in each of the pixel amplifier transistors **23** and **24**, each of the select transistors **52** and **53** has been turned ON in advance, so that a signal level at a reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **2** is transferred to the second FD section **10**. Thereafter, for charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively.

Subsequently, by changing each of the first and second SO lines **50** and **51** to a high level to keep the first and second transistors **52** and **53** ON, stored charge signals of the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24** are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit.

Thereafter, each of the first and second SO lines **50** and **51** is set back to be a low level to turn the first and second select transistors **52** and **53** OFF, so that each of the pixel amplifier transistors **23** and **24** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL lines **36** and **37** and the first READ line **32** is selected, each of the pixel amplifier transistors **23** and **24** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **22** is temporarily turned ON to reset charges of the FD sections **9** and **10**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **24**, a signal level at the reset time is detected, the detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively. The introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **22** has been turned OFF, high level voltage is applied in all pulse state to the second READ line **33** to simultaneously turn transfer transistors **17** and **18** ON. Thus, charge stored in the PD section **5** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the second FD section **10**.

Thereafter, in the same manner as in the first horizontal blanking period **1**H, for respective charges transferred to the first FD section **9** and the second FD section **10**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the second pixel amplifier transistor **24**, respectively. Furthermore, the stored signals whose voltage level have been detected selectively conducts the first and second VO lines **38** and **39** and are introduced to the noise cancellation circuit. Then; sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **24** can be detected.

Thus, with the first and second select transistors **52** and **53** between the FD section **9** and the first VO line **38** and between the FD section **10** and the second VO line **39**, respectively. Thus, the number of transistors per photoelectric conversion cell is 1.75. Moreover, the number of interconnects is 2.75. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells **91** and **92** and also to largely improve the aperture ratio of PD sections.

Note that also in the second embodiment, as in the modified example of the first embodiment, for example, a configuration in which the transfer transistor **13** and the transfer transistor **18** located diagonally to the transfer transistor **13** are connected to the first READ line **32**, and the transfer transistor **14** and the transfer transistor **17** located diagonally to the transfer transistor **14** are connected to the second READ line **33** may be used.

Moreover, in the photoelectric conversion cell **91**, the PD sections are arranged in two rows and two columns. However, the present invention is not limited thereto, but the PD sections may be arranged in two rows and three columns and, furthermore, may be arranged in three or more rows and three or more columns.

Third Embodiment

Hereinafter, a third embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. **6** is a diagram illustrating an example of circuit configuration of a photoelectric conversion cell in a solid state imaging apparatus according to a third embodiment of the present invention. In FIG. **6**, each member also shown in FIG. **1** is identified by the same reference numeral, and therefore, description thereof will be omitted.

As shown in FIG. **6**, in the solid state imaging apparatus of the third embodiment, first through fourth photoelectric conversion cells **91**, **92**, **93** and **94** are arranged in a matrix.

For example, the first photoelectric conversion cell **91** includes photoelectric conversion (PD) sections **1** and **2** arranged in regions which is located in the first column of an array and the first row and which is located in the first column of and the second rows of the array, respectively. The PD sections **1** and **2** share a first FD section **9** via transfer transistors **13** and **14** each of which is made of an N channel FET, respectively.

To the first FD section **9**, the first reset transistor **21** made of an N channel FET is connected. The first reset transistor **21** includes a source connected to the first FD section **9**, a drain connected to the first FD section **9** and a gate connected to a first RSCELL line **36**. Thus, charge stored in the first FD section **9** is made to flow through a first VDDCELL line **30** by a RSCELL signal.

To the first FD section **9** and the first reset transistor **21**, a first pixel amplifier transistor **23** of an N channel FET is connected. The first pixel amplifier transistor made of an N channel FET includes a gate connected to the first FD section **9**, a drain connected to the first VDDCELL line **30** and a source connected to a first VO line **38**.

In the same manner, PD sections **3** and **4** arranged in regions of an array forming a second photoelectric conversion cell **92** which is located in the first column and the third row and which is located in the first column and the fourth row, respectively, share a second FD section **10** via transfer transistors **15** and **16**, respectively. A second reset transistor **22** selectively conducts the second FD section **10** and the first VDDCELL line **30**. Moreover, a second pixel amplifier transistor **24** which receives the signal potential of the second FD section **10** at the gate and receives the power supply potential of the first VDDCELL line **30** at the drain outputs a detected signal corresponding to a received signal potential to the first VO line **38**.

PD sections **5** and **6** arranged in regions of an array forming a third photoelectric conversion cell **93** which is located in the second column and the first row and which is located in the second column and the second row, respectively, share a third FD section **11** via transfer transistors **17** and **18**, respectively. A third reset transistor **61** selectively conducts the third FD section **11** and a second VDDCELL line **31**. Moreover, a third pixel amplifier transistor **63** which receives the signal potential of the third FD section **11** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs a detected signal corresponding to a received signal potential to a second VO line **39**.

PD sections **7** and **8** arranged in regions of an array forming a fourth photoelectric conversion cell **94** which is located in the second column and the third row and which is located in the second column and the fourth row, respectively, share a fourth FD section **12** via transfer transistors **19** and **20**, respectively. A fourth reset transistor **62** selectively conducts the fourth FD section **12** and a second VDDCELL line **31**. Moreover, a fourth pixel amplifier transistor **64** which receives the signal potential of the fourth FD section **12** at the gate and receives the power supply potential of the second VDDCELL line **31** at the drain outputs **3** detected signal corresponding to a received signal potential to a second VO line **39**.

Hereinafter, the operation of the solid state imaging apparatus having the above-described configuration will be described with reference to the accompanying drawings.

FIG. **7** is a timing chart showing timing for driving the solid state imaging apparatus of the third embodiment. In this case, a series of operations is completed in a horizontal blanking period (=1 H).

Moreover, as for the detection order of signal charges from the PD sections **1** through **8** arranged in an array, detection is carried out sequentially from the first row to the second row and so on.

As shown in FIG. **7**, first, high level voltage is applied to a LGCELL line **40** so that each of the load transistors **25** and **26** becomes a constant current source, and then during a period in which the potentials of the first VDDCELL line **30** and the VDDCELL line **31** are set to be high level, the first RSCELL lines **36** is set to be high level in a pulse state to temporarily turn each of the reset transistors **21** and **61** ON. Thus, charges stored in the first FD section **9** in the first photoelectric conversion cell **91** and in the third FD section **11** in the third photoelectric conversion cell **93** are made to flow through the first VDDCELL line **30** and the VDDCELL line **31**, respectively. In this case, in each of the pixel amplifier transistors **23** and **63**, a signal level at the reset time is detected, the detected signal level is introduced to a noise cancellation circuit (not shown) via each of the VO lines **38** and **39**. The introduced signal level is clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **61** has been turned OFF, high level voltage is applied in an pulse state to the first READ line **32** to simultaneously turn transfer transistors **13** and **14** ON. Thus, charge stored in the PD section **1** in the first row is transferred to the first FD section **9** while charge stored in the PD section **5** in the second row is transferred to the third FD section **11**. For charges transferred to the first FD section **9** and the third FD section **11**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the third pixel amplifier transistor **63**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively, Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **63** can be detected.

Subsequently, when each of the VDDCELL lines **30** and **31** is turned to be in a low level OFF state and the first RSCELL line **36** is temporarily turned ON, each of the respective potentials of the FD sections **9** and **11** becomes in the same OFF level state as that of each of the VDDCELL lines **30** and **31**. Then, each of the pixel amplifier transistors **23** and **63** stops its operation.

After this, in a vertical line scanning circuit, until each of the first RSCELL line **36** and the first READ line **32** are selected, each of the pixel amplifier transistors **23** and **63** is not operated. Thus, the vertical line scanning circuit becomes in a non-select state.

In a subsequent horizontal blanking period **2**H, each of the reset transistors **21** and **61** temporarily turned ON to reset charges of the FD sections **9** and **11**. In this case, as has been described, in each of the pixel amplifier transistors **23** and **63**,

a signal level at the reset time is detected, detected signal levels are introduced to the noise cancellation circuit via each of the VO lines **38** and **39**, respectively the introduced signal levels are clamped by the noise cancellation circuit.

Next, after each of the reset transistor **21** and **61** has bee turned OFF, high level voltage is applied in an pulse state to the second READ line **33** to simultaneously turn transfer transistors **14** and **18** ON. Thus, charge stored in the PD section **2** in the first row is transferred to the first FD section **9** while charge stored in the PD section **6** in the second row is transferred to the third FD section **11**.

Thereafter, in the same manner as in the first horizontal blanking period **1** H, for respective charges transferred to the first FD section **9** and the third FD section **11**, voltage levels of stored signals are detected in the first pixel amplifier transistor **23** and the third pixel amplifier transistor **63**, respectively. Furthermore, the detected voltage levels are introduced to the noise cancellation circuit via the first VO line **38** and the second VO line **39**, respectively. Thus, sampling of each of the signals is performed by the noise cancellation circuit. By this series of operations, output signals from which variations in threshold and noise components have been removed and which are held by the pixel amplifier transistors **23** and **63** can be detected

In this manner, charges detected during the first horizontal blanking period **1** H and charges detected during the second horizontal blanking period **2** H are processed in signal processing circuits (not shown), respectively, so that charges photoelectric-converted in the first and second rows can be detected as an image corresponding to actual positions of the charges. Thus, in the third embodiment, for example, the power supply potentials which are to be applied to the respective drains of the first reset transistor **21** and the first pixel amplifier transistor **23** vary in the same manner. Therefore, the known row selection transistor **152** is not necessarily provided.

Subsequently, if the PD sections in the third and fourth rows are driven in the same manner as that of driving the PD sections in the first and second rows, signals can be detected throughout the array.

As has been described, the solid state imaging apparatus of the third embodiment has for example, a configuration in which the two PD sections **1** and **2** share the first FD section **9**, the first pixel amplifier transistor **23** and the first reset transistor **21**. Thus, the number of transistors per photoelectric conversion cell can be finally reduced from 4 (required in the known solid state imaging apparatus) to 2. Moreover, the number of interconnects can be reduced from 5 (required in the known apparatus) to 3.5. Accordingly, if a photoelectric conversion cell is designed, assuming that the area of a photoelectric conversion cell is 4.1 μm×4.1 μm, with the design rule of 0.35 μm, the aperture ratio of the PD sections **1** and **2** is about 30%. Therefore, it is possible to reduce the cell size of each of the photoelectric conversion cells and also to largely improve the aperture ratio of the PD section.

Note that each of the reset transistors **21**, **22**, **61** and **62** is made of an N channel type MOS transistor. However, in each of the reset transistors **21**, **22**, **61** and **62** made of instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second RSCELL lines **36** and **37**, each of the reset transistors **21**, **22**, **61** and **62** is turned ON.

In the same manner, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is made of an N channel type MOS transistor. However, in each of the pixel amplifier transistors **23**, **24**, **63** and **64** made of, instead of an N channel type MOS transistor, a P channel type MOS transistor, when low level voltage is applied to the first and second VDDVELL lines **30** and **31**, each of the pixel amplifier transistors **23**, **24**, **63** and **64** is turned ON to be in a potential detection period in which signal potentials from the corresponding FD sections **9**, **10**, **11** and **12** are detected.

Hereinafter, in the layout in which each of the PD sections **1**, **2**, **3**, **5**, **6** and **7** arranged as shown in FIG. **8**, a region of the cell located between the PD sections **1** and **2** is referred to as an "A region"; a region of the cell surrounded by the PD sections **1**, **2**, **5** and **6** is referred to as a "B region"; a region of the cell located between the PD sections **5** and **6** is referred to as a "C region"; a region of the cell located between the PD sections **2** and **6** is referred to as a "D region"; and a region of the cell located between the PD sections **1** and **5** is referred to as an "E region". Then, by arranging the FD sections **9** and **11**, the pixel amplifier transistors **23** and **63**, and the reset transistors **21** and **61** in regions in the cell indicated in the FIG. **9**, respectively, the aperture ratio of the PD sections to the photoelectric conversion cell can be improved in any case, compared to the known solid state imaging apparatus. Moreover, the size of the cell can be reduced.

Furthermore, as also shown in FIG. **9**, if the FD sections **9** and **11** are arranged in the A and C regions, respectively, the aperture of the PD sections can be improved to be about 30% by arranging in parallel the READ lines **32** and **33** for driving the transfer transistors **13** and **14**, respectively.

Moreover, as shown in FIG **9**, for example, the aperture of the PD sections can be improved to be about 30% by arranging the first RSCELL line **36** between the PD sections **2** and **3**.

Moreover, as shown in FIG. **8**, by arranging the PD sections so as to be spaced apart from one another by a certain distance at least in one of the row direction and the column direction, inclination in the resolution of an image taken can be corrected. Therefore, a high quality image can be obtained.

Moreover, although not shown in the drawings, by using the first VDDCELL line **30** and the second VDDCELL line **31** as light-shielding films for separating the photoelectric conversion cells from one another, the first VO line **38** and the second VO line **39** can be formed in different interconnect layers. Thus, the sizes of the photoelectric conversion cells **91** and **92** can be reduced and also the aperture area of the PD sections can be increased.

Moreover, with the solid state imaging apparatus of any one of the first through third embodiments, a camera which is small-sized and provides a high resolution image can be obtained.

The invention claimed is:

1. A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistors included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines,

each floating diffusion section is disposed across the two photoelectric conversion cells adjacent to each other in row direction, and

only two read-out lines are disposed within the photoelectric conversion cells.

2. The solid state imaging apparatus of claim **1**, wherein,

the first and second pixel amplifier transistors are coupled to the first and second floating diffusion sections, respectively; and

each of the first and second pixel amplifier transistors comprises a source follower transistor which detects and outputs a voltage potential converted from one of said first floating diffusion section and said second floating diffusion section.

3. The solid state imaging apparatus of claim **1**, wherein the plurality of read lines are connected to a vertical scanning circuit.

4. The solid state imaging apparatus of claim **1**, further comprising:

a plurality of a pair of signal lines outputting signals from the first pixel amplifier transistors and the second pixel amplifier transistors, respectively, to the outside.

5. The solid state imaging apparatus of claim **1**, wherein each floating diffusion section and each pixel amplifier transistor are shared by the photoelectric sections in the first row of one of the photoelectric conversion cells and the photoelectric sections in the second row of another of the photoelectric conversion cells.

6. The solid state imaging apparatus of claim **1**, further comprising:

a signal line for outputting a signal from each pixel amplifier transistor to the outside; and

a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line.

7. The solid state imaging apparatus of claim **1**, wherein each floating diffusion section and each pixel amplifier transistor are shared by photoelectric conversion section which are adjacent to each other in the row direction or in the column direction.

8. The solid state imaging apparatus of claim **1**, wherein in each floating diffusion section, a reset section for resetting charge stored in the floating diffusion section.

9. The solid state imaging apparatus of claim **1**, wherein the photoelectric conversion section are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction.

10. The solid state imaging apparatus of claim **1**, further comprising a signal processing circuit for processing an output signal from each pixel amplifier transistor.

11. The solid state imaging apparatus of claim **1**, wherein the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film.

12. The solid state imaging apparatus of claim **1**, wherein respective charges of the photoelectric conversion section each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

13. A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric section arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoeletric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines, and

wherein in each photoelectric conversion cell, a first read-out line is connected to a gate of a transfer transistor included in the first row and the first column and a gate of a transfer transistor included in the second row and the column, and a second read-out line is connected to a gate of a transfer transistor included in the first row and the second column and a gate of a transfer transistor included in the second row and the second column.

14. A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoeletric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines, and

wherein in each photoelectric conversion cell, a first read-out line is connected to a gate of a transfer transistor included in the first row and the first column and a gate of a transfer transistor included in the second row and the second column, and a second read-out line is connected to a gate of a transfer transistor included in the first row and the second column and a gate of a transfer transistor included in the second row and the first column.

15. The solid state imaging apparatus of claim **14**, wherein the plurality of photoelectric elements are photo diodes.

16. A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoeletric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines,

each floating diffusion section is disposed across the two photoelectric conversion cells adjacent to each other in a row direction, and

only two read-out lines are disposed within the photoelectric conversion cells.

17. The camera of claim **16**, wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

* * * * *

ZFW

Docket No.: 060188-0710 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mitsuyoshi MORI, et al.	:	Confirmation Number: 7667
Application No.: 10/706,918	:	Group Art Unit: 2814
Filed: November 14, 2003	:	Examiner: John C. Ingham

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an Amendment in the above-identified application.
☒ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	34	34	0	$50.00 =	$0.00
Independent Claims	4	5	0	$200.00 =	$0.00
		Multiple dependent claims newly presented			$0.00
		Fee for extension of time			$0.00
					$0.00
		Total of Above Calculations			$0.00

☐ Please charge my Deposit Account No. 500417 in the amount of $0.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

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WDC99 1230997-1.060188.0710

Docket No.: 060188-0710 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mitsuyoshi MORI, et al.	:	Confirmation Number: 7667
Application No.: 10/706,918	:	Group Art Unit: 2814
Filed: November 14, 2003	:	Examiner: John C. Ingham

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of February 7, 2006, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 13 of this paper.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Canceled)

2. (Currently amended) The solid state imaging apparatus of claim 31, wherein one of two switching elements which are coupled to the first floating diffusion section ~~storage node~~ and one of two switching elements are coupled to the second floating diffusion section ~~storage node~~ are included in the same column.

3. (Currently amended) The solid state imaging apparatus of claim 31, wherein one of two switching elements which are coupled to the first floating diffusion section ~~storage node~~ and one of two switching elements which are coupled to the second floating diffusion section ~~storage node~~ are included in two adjacent columns.

4. (Currently amended) The solid state imaging apparatus of claim 35, wherein [[each]] said floating diffusion section ~~storage node~~ and [[each]] said pixel amplifier ~~output~~ transistor are shared by the two switching elements which are coupled to the first read line and the second read line, respectively.

5. (Currently amended) The solid state imaging apparatus of claim 35, further comprising:

a signal line for outputting a signal from said pixel amplifier ~~output~~ transistor to the outside; and

a select transistor which is provided between the pixel amplifier ~~output~~ transistor and the signal line.

6. (Currently amended) The solid state imaging apparatus of claim 35 [[34]], wherein the first floating diffusion section ~~storage node~~ and the pixel amplifier ~~output~~ transistor are shared by photoelectric elements which are adjacent to each other in the row direction or in the column direction.

7. (Currently amended) The solid state imaging apparatus of claim 31, further comprising:

a reset element for resetting charge stored in the first floating diffusion section ~~storage node~~.

8. (Previously presented) The solid state imaging apparatus of claim 31, wherein the photoelectric elements are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction.

9. (Currently amended) The solid state imaging apparatus of claim 35 [[33]], further comprising:

a signal processing circuit for processing an output signal from said pixel amplifier ~~output~~ transistor.

10. (Previously presented) The solid state imaging apparatus of claim 31, wherein:

the plurality of photoelectric elements arranged in an array of at least two rows and two columns define a unit of a photoelectric section; and

a plurality of the photoelectric sections are separated from one another by a power supply line which also functions as a light-shielding film.

11. (Canceled)

12. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photoelectric elements arranged in an array of at least two rows and two columns;

a plurality of switching elements~~, each of which is connected to one of said plurality of photoelectric elements, each of said switching elements operative~~ for transferring charges from one of said photoelectric elements ~~to one of a plurality of storage nodes~~;

a plurality of floating diffusion sections which are connected to the photoelectric elements via the switching elements and store the charges; and

a plurality of a pair ~~plurality~~ of read lines coupled to the switching elements ~~including a first read line coupled to a first switching element which is coupled to a storage node, and a second read line coupled to a second switching elements which is coupled to the storage node,~~

wherein one of the pair of read lines is connected to a switching element at an odd-numbered column and the other is connected to a switching element at an even-numbered column, and

one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction.

13. (Currently amended) The solid state imaging apparatus of claim 12, further comprising:

a reset transistor for resetting charge stored in each said floating diffusion section ~~storage node~~ and ~~an output~~ a pixel amplifier transistor for detecting and outputting a voltage potential converted from said floating diffusion section ~~the storage node~~;

wherein a drain of the reset transistor is connected to a drain of the pixel amplifier ~~output~~ transistor so that the drain is shared by the reset transistor and the pixel amplifier ~~output~~ transistor.

14. (Currently amended) The solid state imaging apparatus of claim 12, wherein the floating diffusion section ~~storage node~~ is arranged between the two photoelectric elements which are adjacent to each other in the row direction.

15. (Currently amended) The solid state imaging apparatus of claim 13, wherein said switching elements are ~~transistor is~~ made of an MIS transistor, and

a gate of the MIS transistor is arranged in the row direction.

16. (Currently amended) The solid state imaging apparatus of claim 13, wherein said pixel amplifier ~~output~~ transistor is arranged between rows which include some of the photoelectric elements adjacent to each other.

17. (Currently amended) The solid state imaging apparatus of claim 13, wherein said pixel amplifier ~~output~~ transistor and said floating diffusion section ~~storage node~~ are arranged between the first read line and the second read line.

18. (Currently amended) The solid state imaging apparatus of claim 12, wherein the plurality of photoelectric elements arranged in an array of at least two columns ~~column~~ which define a photoelectric section; and [[the]] a pixel amplifier ~~output~~ transistor is arranged between the two photoelectric sections which are adjacent to each other in the column direction.

19. (Currently amended) The solid state imaging apparatus of claim 15, wherein each said pixel amplifier ~~output~~ transistor is arranged between the gate of a first MIS transistor and the gate of a second MIS transistor.

20. (Previously presented) The solid state imaging apparatus of claim 13, wherein each said reset transistor is arranged between the first read line and the second read line.

21. (Currently amended) The solid state imaging apparatus of claim 18, wherein the pixel amplifier ~~output~~ transistor and the floating diffusion section ~~storage node~~ are arranged between the two photoelectric sections which are adjacent to each other.

22. (Previously presented) The solid state imaging apparatus of claim 18, wherein said reset transistor is arranged between the two photoelectric sections, which are adjacent to each other in the row direction.

23. (Previously presented) The solid state imaging apparatus of claim 18, wherein said reset transistor is arranged between the two photoelectric sections, which are adjacent to each other in the column direction.

24. (Previously presented) The solid state imaging apparatus of claim 15, wherein said reset transistor is arranged between the gate of a first MIS transistor and the gate of a second MIS transistor.

25. (Currently amended) The solid state imaging apparatus of claim 18, wherein said floating diffusion section ~~storage node~~ is arranged between the two photoelectric sections which are adjacent to each other in the column direction.

26. (Previously presented) The solid state imaging apparatus of claim 12, wherein the photoelectric elements are arranged so as to be spaced apart from one another by a certain distance in at least one of the row direction and the column direction.

27. (Currently amended) The solid state imaging apparatus of claim 13, wherein a line of the drain shared by the reset transistor and the pixel amplifier ~~output~~ transistor also functions as a light-shielding film.

28. (Currently amended) The solid state imaging apparatus of claim 13 [[12]], further comprising a signal processing circuit for processing an output signal from said pixel amplifier ~~output~~ transistor.

29. (Currently amended) A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric elements arranged in an array of at leas two rows and two columns;

a plurality of switching elements~~, each of which is connected to one of said plurality of photoelectric elements, each of said switching elements operative~~ for transferring charges from one of said photoelectric elements ~~photosensitive devices to one of a plurality of storage nodes~~;

a plurality of floating diffusion sections which are connected to the photoelectric elements via the switching elements and store the charges; and

a plurality of a pair ~~plurality~~ of read lines coupled to the switching elements ~~including a first read line coupled to one of two switching elements which are coupled to a first storage node, and a second read line coupled to one of two switching elements which are coupled to a second storage node; and~~

~~said first read line also coupled to one of said two switching elements coupled to said second storage node, said second read line also coupled to one of said two switching elements coupled to said first storage node~~

wherein one of the pair of read lines connects between a switching element at an odd-numbered row and an odd-numbered column and a switching element at an even-numbered row

and an even-numbered column, and the other connects between a switching element at the odd-numbered row and the even-numbered column and a switching element at the even-numbered row and the odd-numbered column, and

one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction.

30. (Currently amended) A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric elements arranged in an array of at least two rows and two columns;

a plurality of switching elements~~, each of which is connected to one of said plurality of photoelectric elements, each of said switching elements operative~~ for transferring charges from one of said photoelectric elements ~~to one of a plurality of storage nodes~~;

a plurality of floating diffusion sections which are connected to the photoelectric elements via the switching elements and store the charges; and

a plurality of a pair ~~plurality~~ of read lines coupled to the switching elements ~~including a first read line coupled to a first switching element which are coupled to a storage node, and a second read line coupled to a second switching element which is coupled to the storage node~~

wherein one of the pair of read lines is connected to a switching element at an odd-numbered column and the other is connected to a switching element at an even-numbered column, and

one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction.

31. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photoelectric elements arranged in an array of at least two rows and two columns;

a plurality of switching elements~~, each of which is connected to one of said plurality of photoelectric elements, each of said switching elements operative~~ for transferring charges from one of said photoelectric elements ~~to one of a plurality of storage nodes~~;

a plurality of floating diffusion sections which are connected to the photoelectric elements via the switching elements and store the charges; and

a plurality of a pair ~~plurality~~ of read lines coupled to the switching elements ~~including a first read line coupled to one of two switching elements which are coupled to a first storage node, and a second read line coupled to one of two switching elements which are coupled to a second storage node; and~~

~~said first read line also coupled to one of said two switching elements coupled to said second storage node, said second read line also coupled to one of said two switching elements coupled to said first storage node,~~

wherein one of the pair of read lines connects between a switching element at an odd-numbered row and an odd-numbered column and a switching element at an even-numbered row and an even-numbered column, and the other connects between a switching element at the odd-numbered row and the even-numbered column and a switching element at the even-numbered row and the odd-numbered column, and

one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction□

32-33. (Canceled)

34. (Previously presented) The solid state imaging apparatus of claim 3, wherein the plurality of photoelectric elements are photo diodes.

35. (Currently amended) The solid state imaging apparatus of claim 31, further comprising:

a pixel amplifier ~~an output~~ transistor which is coupled to the first floating diffusion section ~~storage node~~; and

the pixel amplifier ~~output~~ transistor comprises of a source follower transistor which detects and outputs a voltage potential converted from said [[the]] first floating diffusion section ~~storage node~~.

36. (Previously presented) The solid state imaging apparatus of claim 31, wherein the plurality of read lines are connected to a vertical scanning circuit.

37. (New) The solid state imaging apparatus of claim 12, further comprising:

a plurality of pixel amplifier transistors detecting and outputting a potential of the floating diffusion section, and

a plurality of a pair of signal lines outputting a signal from the pixel amplifier transistors to the outside,

wherein one of the pair of signal lines is connected to a pixel amplifier transistor which is adjacent to another pixel amplifier transistor in the row direction to which the other is connected.

38. (New) The solid state imaging apparatus of claim 31, further comprising:

a plurality of pixel amplifier transistors detecting and outputting a potential of the floating diffusion section, and

a plurality of a pair of signal lines outputting a signal from the pixel amplifier transistors to the outside,

wherein one of the pair of signal lines is connected to a pixel amplifier transistor which is adjacent to another pixel amplifier transistor in the row direction to which the other is connected.

REMARKS

I. Introduction

At the time of the Office Action dated February 7, 2006, claims 2-10 and 12-36 were pending in this application. In this Amendment, claims 2-7, 9, 12-19, 21, 25, 27-31 and 35 have been amended, claims 32 and 33 have been canceled, and new claims 37 and 38 have been added. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the amendment of independent claims 12, 29, 30 and 31 can be found in, for example, Figs. 1 and 3 and relevant description of the specification. Claims 2-7, 9, 13-19, 21, 25, 27, 28 and 35 have been amended to improve wording. Claims 6 and 9 have respectively been amended to be dependent on claim 35, and claim 28 have been amended to be dependent on claim 13. In addition, adequate descriptive support for new claim 37 can be found in, for example, original claim 5, Fig.1 and relevant description of the specification, and adequate descriptive support for new claim 38 can be found in, for example, original claim 5, Fig.3 and relevant description of the specification.

II. The Rejection of Claims 3, 7-9, 12, 14, 26, 28, 31-34 and 36 under 35 U.S.C. §102(b)

Claims 3, 7-9, 12, 14, 26, 28, 31-34 and 36 have been rejected under 35 U.S.C. §102(b) as being anticipated by Guidash (U.S. Patent No. 6,552,323 ("Guidash 323")). In the statement of the rejection, the Examiner asserted that Guidash 323 discloses an image sensor with a shared output signal line identically corresponding to what is claimed.

In response, Applicants submit that Guidash 323 does not identically disclose a solid state imaging apparatus including all the limitations recited in independent claims 12 and 31, as amended. Specifically, Guidash 323 does not disclose, among other things, a solid state imaging

apparatus wherein "one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction," recited in claims 12 and 31. The claimed invention makes it possible to reduce the number of the floating diffusion sections per one photoelectric cell (pixel). Therefore, the aperture ratio of a photoelectric element to a photoelectric cell is increased, and the size of a photoelectric cell can be reduced. In other words, the size of the photoelectric cell can be reduced, while the photoelectric cell maintains a large aperture of the photoelectric element.

Guidash 323 in Fig. 2a discloses a solid state imaging apparatus comprising photoelectric elements 30a, 30b arranged in an array; switching elements TG transferring charges from the photoelectric elements; FD sections 10a, 10b connected to the photoelectric elements via the switching elements; and read lines TG coupled to the switching elements. As shown in Fig. 2a, every pixel 5 (photoelectric cell) has one FD section 10 in Guidash 323. This configuration is the same as that described in the background section of the specification. Accordingly, Guidash 323 does not disclose a solid state imaging apparatus in which a floating diffusion section is shared by four photoelectric sections which are adjacent to the floating diffusion section in the row and column directions, as claimed.

Guidash 323 describes that "the present invention shares the pixel output node and output signal line between at least two rows adjacent pixels 5" (see column 2, lines 53-60). However, such description does not suggest a floating diffusion section is shared by four photoelectric sections which are adjacent to the floating diffusion section in the row and column directions, as claimed.

Accordingly, Guidash 323 does not disclose a solid state imaging apparatus including all the limitations recited in independent claims 12 and 31, as amended, under 35 U.S.C. §102.

Dependent claims 3, 7-9, 14, 26, 28, 32-34 and 36 are also patentably distinguishable over Guidash 323 at least because these claims respectively include all the limitations recited in independent claims 12 and 31. Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims under 35 U.S.C. §102(b) and favorable consideration thereof.

III. The Rejection of Claims 2, 4-6, 13, 15-25 and 35 under 35 U.S.C. §103(a)

Claims 2, 4-6, 13, 15-25 and 35 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash 323 and Guidash (U.S. Patent No. 6,352,869 ("Guidash 869")).

Guidash 869 in Fig. 3b teaches a solid state imaging apparatus comprising photoelectric elements 71, 73, 72, 74 arranged in arrays; switching elements 51, 61, 52, 62 transferring charges from the photoelectric elements; FD sections 42, 41 connected to the photoelectric elements via the switching elements; and read lines coupled to the switching elements, wherein the FD section 42 is shared by the photoelectric elements 71 and 73, and the FD section 41 is shared by the photoelectric elements 72 and 74. Moreover, as shown in Fig. 3a, two pixels (or photoelectric cells) 11 and 12 adjacent to each other in the column direction share one FD section 41. Similarly, two pixels 21 and 22 adjacent to each other in the column direction share one FD section 42. However, there is a reset transistor 36 provided between the FD sections 41 and 42, and the reset transistor 36 isolates the FD sections 41 and 42 from each other. Accordingly, Guidash 869 does not teach that the four pixels 11, 12, 21 and 22 adjacent to each other share one FD section.

Based on the foregoing, Applicants submit that Guidash 869 does not teach, among other things, a solid state imaging apparatus wherein "one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row

direction and a column direction," recited in independent claims 12 and 31. It is, thus, apparent that Guidash 869 does not cure the above discussed deficiencies of Guidash 323. Therefore, dependent claims 2, 4-6, 13, 15-25 and 35 are patentably distinguishable over Guidash 323 and Guidash 869 at least because these claims respectively include all the limitations recited in independent claims 12 and 31. Applicants respectfully solicit withdrawal of the rejection of the claims under 35 U.S.C. §103(a) and favorable consideration thereof.

IV. The Rejection of Claims 29 and 30 under 35 U.S.C. §103(a)

Claims 29 and 30 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash 323 in view of Patterson et al.

In response, Applicants submit that Guidash 323 and Patterson et al., either individually or in combination do not teach a camera comprising a solid state imaging apparatus including all the limitations recited in independent claims 29 and 30, as amended. Specifically, the applied combination does not teach, among other things, a camera comprising a solid state imaging apparatus wherein "one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction," recited in claims 29 and 30.

As discussed with respect to claims 12 and 31, Guidash 323 does not teach that "one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction," recited in claim 29 and 30. The secondary reference, Patterson et al., teaches an imaging device which may be used in cameras, but is silent on a floating diffusion section shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction.

Accordingly, Guidash 323 and Patterson et al., either individually or in combination do not teach a camera comprising a solid state imaging apparatus including all the limitations recited in independent claims 29 and 30, as amended. Applicants, therefore, respectfully solicit withdrawal of the rejection of claims 29 and 30 under 35 U.S.C. §103(a) and favorable consideration thereof.

V. The Rejection of Claims 10 and 27 under 35 U.S.C. §103(a)

Claims 10 and 27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash 323 in view of Yamazaki et al.

In response, Applicants submit that dependent claims 10 and 27 are patentably distinguishable over Guidash 323 and Yamazaki et al. at least because these claims respectively include all the limitations recited in independent claims 32 and 12. It is noted that Yamazaki et al. does not teach a floating diffusion section shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction, and thus, does not cure the deficiencies of Guidash 323.

Therefore, Applicants respectfully solicit withdrawal of the rejection of claims 10 and 27 under 35 U.S.C. §103(a) and favorable consideration thereof.

VI. New Claims 37 and 38

New claims 37 and 38 recite a plurality of a pair of signal lines for outputting signals from pixel amplifier transistors. Applicants specifically note that Guidash 323 and Guidash 869 disclose a single signal line (not a pair) as a signal line connected to pixel amplifier transistors, which is different from the claimed invention.

Since new claims 37 and 38 are not disclosed or taught by the cited references, Applicants, therefore, respectfully solicit favorable consideration of new claims 37 and 38.

VII. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

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WDC99 1229803-1.060188.0710

Docket No.: 060188-3410

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mitsuyoshi MORI, et al.	:	Confirmation Number: 7667
Application No.: 10/706,918	:	Group Art Unit: 2814
Filed: November 14, 2003	:	Examiner: John C. Ingham

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

AMENDMENT FILED WITH REQUEST FOR CONTINUED EXAMINATION

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of July 24, 2006, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 12 of this paper.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-33. (Cancelled)

34. (Currently Amended) The solid state imaging apparatus of claim [[3]] 41, wherein the plurality of photoelectric elements are photo diodes.

35. (Currently Amended) The solid state imaging apparatus of claim [[31]] 39, wherein, ~~further comprising:~~

[[a]] the first and second pixel amplifier transistors are ~~transistor which is~~ coupled to the first and second floating diffusion sections, respectively ~~section~~; and

each of the first and second pixel amplifier transistors ~~transistor~~ comprises [[of]] a source follower transistor which detects and outputs a voltage potential converted from one of said first floating diffusion section and said second floating diffusion section.

36. (Currently Amended) The solid state imaging apparatus of claim [[31]] 39, wherein the plurality of read lines are connected to a vertical scanning circuit.

37. (Currently Amended) The solid state imaging apparatus of claim [[12]] 39, further comprising:

~~a plurality of pixel amplifier transistors detecting and outputting a potential of the floating diffusion section, and~~

a plurality of a pair of signal lines outputting ~~a signal~~ signals from the first pixel amplifier transistors and the second pixel amplifier transistors, respectively, to the outside[[,]].

~~wherein one of the pair of signal lines is connected to a pixel amplifier transistor which is adjacent to another pixel amplifier transistor in the row direction to which the other is connected.~~

38. (Currently Amended) The solid state imaging apparatus of claim [[31]] 49, further comprising:

~~a plurality of pixel amplifier transistors detecting and outputting a potential of the floating diffusion section, and~~

a plurality of a pair of signal lines outputting ~~a signal~~ signals from the pixel amplifier transistors adjacent to each other, respectively to the outside[[,]].

~~wherein one of the pair of signal lines is connected to a pixel amplifier transistor which is adjacent to another pixel amplifier transistor in the row direction to which the other is connected.~~

39. (New) A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section.

40. (New) The solid state imaging apparatus of claim 39, wherein each read-out line is connected to the transfer transistors connected to the photoelectric conversion sections which are included in one of the first and second columns.

41. (New) The solid state imaging apparatus of claim 39, wherein each read-out line is connected to the transfer transistors connected to the photoelectric conversion sections which are included in the first and second columns, respectively.

42. (New) The solid state imaging apparatus of claim 39, wherein each floating diffusion section and each pixel amplifier transistor are shared by the photoelectric sections in the first row of one of the photoelectric conversion cells and the photoelectric sections in the second row of another of the photoelectric conversion cells.

43. (New) The solid state imaging apparatus of claim 39, further comprising:

a signal line for outputting a signal from each pixel amplifier transistor to the outside; and

a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line.

44. (New) The solid state imaging apparatus of claim 39, wherein each floating diffusion section and each pixel amplifier transistor are shared by photoelectric conversion sections which are adjacent to each other in the row direction or in the column direction.

45. (New) The solid state imaging apparatus of claim 39, wherein in each floating diffusion section, a reset section for resetting charge stored in the floating diffusion section.

46. (New) The solid state imaging apparatus of claim 39, wherein the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction.

47. (New) The solid state imaging apparatus of claim 39, further comprising a signal processing circuit for processing an output signal from each pixel amplifier transistor.

48. (New) The solid state imaging apparatus of claim 39, wherein the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film.

49. (New) A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells arranged in a matrix, each photoelectric conversion cell including a plurality of photoelectric sections arranged in a matrix including at least two rows and at least one column;

a plurality of floating diffusion sections each being provided between said photoelectric conversion cells, each floating diffusion section being shared by, and being connected to, the photoelectric conversion sections which are respectively included in the at least two rows and the at least one column in each photoelectric conversion cell via transfer transistor, respectively;

a plurality of read-out lines each being connected to one of the transfer transistors and independently reading out charge from the one of the photoelectric conversion sections of each photoelectric conversion cell to each floating diffusion section shared by said photoelectric conversion sections; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each floating diffusion section.

50. (New) The solid state imaging apparatus of claim 49, further comprising reset transistors for resetting charge stored in said floating diffusion sections,

wherein the drain of the reset transistor is connected to the drain of the pixel amplifier transistor so that a drain is shared by the reset transistor and the pixel amplifier transistor.

51. (New) The solid state imaging apparatus of claim 49, wherein each floating diffusion section is arranged between the photoelectric conversion sections which are adjacent to each other in the row direction in each said photoelectric conversion cell.

52. (New) The solid state imaging apparatus of claim 49, wherein each said transfer transistor is made of an MIS transistor, and

wherein a gate of the MIS transistor is arranged in the row direction.

53. (New) The solid state imaging apparatus of claim 49, wherein each pixel amplifier transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell.

54. (New) The solid state imaging apparatus of claim 49, wherein each pixel amplifier transistor and each floating diffusion section are arranged between the read out lines.

55. (New) The solid state imaging apparatus of claim 49, wherein each pixel amplifier transistor is arranged between the photoelectric cells which are adjacent to each other in the column direction.

56. (New) The solid state imaging apparatus of claim 55, wherein each transfer transistor is made of an MIS transistor, and

wherein each pixel amplifier transistor is arranged between respective gates of the MIS transistor and another MIS transistor.

57. (New) The solid state imaging apparatus of claim 50, wherein each reset transistor is arranged between rows which include some of the photoelectric conversion sections and are adjacent to each other in each said photoelectric conversion cell.

58. (New) The solid state imaging apparatus of claim 50, wherein each pixel amplifier transistor and the floating diffusion section are arranged between the read out lines.

59. (New) The solid state imaging apparatus of claim 50, wherein each reset transistor is connected to a line arranged between the photoelectric cells which are adjacent to each other in the row direction.

60. (New) The solid state imaging apparatus of claim 50, wherein each reset transistor is arranged between the photoelectric conversion cells which are adjacent to each other in the column direction.

61. (New) The solid state imaging apparatus of claim 60, wherein each transfer transistor is made of an MIS transistor, and

wherein each reset transistor is arranged between respective gates of the MIS transistor and another MIS transistor.

62. (New) The solid state imaging apparatus of claim 49, wherein each floating diffusion section is arranged between the photoelectric conversion cells which are adjacent to each other in the column direction.

63. (New) The solid state imaging apparatus of claim 49, wherein the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in at least one of the row direction and the column direction.

64. (New) The solid state imaging apparatus of claim 50, wherein the line connecting respective drains of the reset transistor and the pixel amplifier transistor also functions as a light-shielding film.

65. (New) The solid state imaging apparatus of claim 49, further comprising a signal processing circuit for processing an output signal output from each pixel amplifier transistor.

66. (New) A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section.

67. (New) A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric conversion cells arranged in a matrix, each photoelectric conversion cell including a plurality of photoelectric sections arranged in a matrix including at least two rows and at least one column;

a plurality of floating diffusion sections each being provided between said photoelectric conversion cells, each floating diffusion section being shared by, and being connected to, the photoelectric conversion sections which are respectively included in the at least two rows and the at least one column in each photoelectric conversion cell via transfer transistor, respectively;

a plurality of read-out lines each being connected to one of the transfer transistors and independently reading out charge from the one of the photoelectric conversion sections of each photoelectric conversion cell to each floating diffusion section shared by said photoelectric conversion sections; and

a plurality of pixel amplifier transistors each detecting and outputting the potential of each floating diffusion section.

68. (New) The solid state imaging apparatus of claim 39, wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

69. (New) The camera of claim 66, wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

REMARKS

I. Introduction

At the time of the Office Action dated July 24, 2006, claims 2-10, 12-31, and 34-38 are pending in this application. In this Amendment, claims 34-38 have been amended, claims 2-10 and 12-31 have been canceled, and new claims 39-69 have been added. Care has been exercised to avoid the introduction of new matter. New claims 39-69 are prepared based on original claims 1-30, which are supported in, for example, Figs. 1 and 4 and relevant description of the specification. Entry of the present Amendment is respectfully solicited. A Request for Continuing Examination is filed herewith.

Now, claims 34-69 are active in this application, of which claims 39, 49, 66, and 67 are independent.

II. The Rejection of Claims 37 and 38 under U.S.C. §112, First Paragraph

The Examiner asserted that the claims contain subject matter which is not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In response, claims 37 and 38 have been amended based on Fig. 1 and the First Embodiment of the specification. Withdrawal of the rejection of claims 37 and 38 is, therefore, respectfully solicited.

III. The Rejection of Claims 2-10, 12-31 and 34-38

The rejection of claims 2-10 and 12-31 under 35 U.S.C. §103(a) has been rendered moot by cancellation of these claims. The rejection of claims 34-38 under 35 U.S.C. §103(a) has also been rendered moot by amending these claims to be dependent on new claims 39 and 49,

respectively. Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims under 35 U.S.C. §103(a).

IV. New Claims

Independent claims 39 and 49 are directed to a solid state imaging apparatus, while claims 66 and 67 are directed to a camera comprising a solid state imaging apparatus of claims 39 and 49, respectively. One aspect of the present invention is that a floating diffusion section (FD section), a transistor (pixel amplifier) and a line (output signal line) are shared by a plurality of photoelectric (photodiode: PD) sections. Accordingly, it is possible to reduce the number of locations of the floating diffusion sections per one photoelectric cell (i.e. pixel), and therefore to increase the aperture ratio of the photoelectric section to the photoelectric cell. As a result, it is possible to reduce the size of the photoelectric cell while increasing the aperture area of the photoelectric section to the photoelectric cell.

Comparison between the Present Invention and References

i) Guidash (USP 6,352,869; "Guidash '869")

Guidash '869 discloses in Fig. 3b, a solid state imaging apparatus comprising: a pixel architecture 30 having photodetectors 71, 73, 72 and 74 arranged in arrays; transfer gates 51, 61, 52 and 62 transferring charges from the respective photodetectors; a first FD section 41 connected to the photodetectors 72 and 74 via the transfer gates 52 and 62, a second DF section 42 connected to the photodetectors 71 and 73 via the transfer gates 51 and 61; and an amplifier 32 connected to the first and second FD sections. It is apparent from Fig. 3b, the amplifier 32 is shared by two FD sections 41 and 42, and the two FD sections are included in one pixel architecture 30 (see Fig. 3b and column 3, lines 55-59).

Accordingly, the FD sections of Guidash '869 are not connected to different amplifiers, respectively. This is different from the present invention in claim 39, where a first pixel amplifier for detecting charges of a first PD section and a second pixel amplifier for detecting charges of a second FD section are provided separately. Guidash '869 does not disclose, at a minimum, "a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section," recited in claim 39.

In addition, each of the FD sections of Guidash '869 is not provided between the pixel architectures and not shared by the photodetectors included in adjacent rows and in the same column. This structure is different from the structure of the present invention according to claim 49, in which each of the FD sections is provided between the photoelectric conversion cells and shared by the photoelectric conversion sections included in adjacent rows and in the same column. That is, Guidash '869 does not disclose, at a minimum, a plurality of floating diffusion sections each being provided between the photoelectric conversion cells, each floating diffusion section being shared by, and being connected to, the photoelectric conversion sections which are respectively included in the at least two rows and the at least one column in each photoelectric conversion cell via transfer transistor, respectively, recited in claim 49.

ii) Hashimoto (USP 6,956,605)

Hashimoto discloses in its Figs. 2 and 21, a solid state imaging apparatus comprising: unit cells 81 having photoelectric conversion sections 82a to 82d arranged in arrays; transfer gates 83a to 83d transferring charges from the respective photoelectric conversion sections; an FD section 85 connected to the respective photoelectric conversion sections via the transfer

gates; an amplifier 86 connected to the FD section; and read-out interconnections 88a to 88d connected to the respective transfer gates.

It is apparent from Figs. 2 and 21 of Hashimoto, the photoelectric conversion sections, which are included in different rows in the respective unit cells, are not connected to FD sections different from (or independent of) each other. This is different from the present invention in claim 39, where the photoelectric conversion sections included in a first row are connected to first floating diffusion sections and that the photoelectric sections included in a second row are connected to second floating diffusion sections. Thus, Hashimoto does not disclose, at a minimum, "a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively," and "a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively," recited in claim 39.

In addition, each of the FD sections of Hashimoto is not provided between the unit cells and not shared by the photoelectric conversion sections included in adjacent rows and in the same column. This structure is different from the structure of the present invention according to claim 49, in which each of the FD sections is provided between the photoelectric conversion cells and shared by the photoelectric conversion sections included in adjacent rows and in the same column. That is, Hashimoto does not disclose, at a minimum, a plurality of floating diffusion sections each being provided between the photoelectric conversion cells, each floating diffusion section being shared by, and being connected to, the photoelectric conversion sections

which are respectively included in the at least two rows and the at least one column in each photoelectric conversion cell via transfer transistor, respectively, recited in claim 49.

iii) Guidash et al. (USP 6,552,323; "Guidash '323")

Guidash '323 discloses that an FD section and an amplifier are shared between two pixels adjacent to each other. The problem is that this structure makes it difficult to perform an electronic shutter. Guidash '323 aims to solve this problem and discloses a structure of sharing a pixel output node and an output signal line between at least two rows adjacent pixels (see column 2 lines 55-57).

Accordingly, as shown in Fig. 2a, Guidash '323 provides one FD section for one pixel. This structure is the same as that of the conventional art in the present specification and thus, different from what is claimed in claims 39 and 49.

iv) Patterson (USP 6,541,794)

Patterson relates to an imaging capturing circuits to be used in copiers, scanners, digital cameras, and other devices. Patterson does not cure the deficiencies of Guidash '869, Hashimoto, and Guidash '323.

v) Yamazaki et al. (US patent application publication No. 2002/0145582)

Yamazaki et al. are directed to a display device which includes a pixel section and a driving circuit for transmitting a signal to the pixel section, both of which are provided on the same insulator. Yamazaki et al. do not cure the deficiencies of Guidash '869, Hashimoto, and Guidash '323.

Accordingly, Applicants submit that independent claims 39 and 49 are patentably distinguishable over Guidash '869, Hashimoto, Guidash '323, Patterson, and Yamazaki et al. The above discussion is applicable to independent claims 66 and 67. It is also noted that

dependent claims 40-48, 50-65, 67, and 68, as well as claims 34-38, are patentably distinguishable over Guidash '869, Hashimoto, Guidash '323, Patterson, and Yamazaki et al., at least because these claims include all the limitations recited in independent claims 39 and 49, respectively.

Applicants, therefore, respectfully solicit favorable consideration of claims 34-69.

V. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

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Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/706,918
Filing Date	November 14, 2003
First Named Inventor	Mitsuyoshi MORI, et al.
Art Unit	2814
Examiner Name	John C. Ingham
Attorney Docket Number	060188-0710

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Education (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b. ☒ Enclosed

      i. ☒ Amendment/Reply

      ii. ☐ Affidavit(s)/Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action of the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 500417. I have enclosed a duplicate copy of this sheet.

      i. ☒ RCE fee required under 37 CFR 1.17(e) $790

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☒ Other $100 (Additional claim fee)

   10/25/2006 SZEWDIE1 00000092 500417 10706918
   01 FC:1801 790.00 DA
   02 FC:1202 100.00 DA

   b. ☐ Check in the amount of $ _____ enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	October 24, 2006
Name (Print/Type)	Michael E. Fogarty	Registration No.	36,139

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

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This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Docket No.: 060188-0710 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Mitsuyoshi MORI, et al.	:	Confirmation Number: 7667
Application No.: 10/706,918	:	Group Art Unit: 2814
Filed: November 14, 2003	:	Examiner: John C. Ingham

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of December 29, 2006, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-33. (Cancelled)

34. (Previously Presented) The solid state imaging apparatus of claim 41, wherein the plurality of photoelectric elements are photo diodes.

35. (Previously Presented) The solid state imaging apparatus of claim 39, wherein,

the first and second pixel amplifier transistors are coupled to the first and second floating diffusion sections, respectively; and

each of the first and second pixel amplifier transistors comprises a source follower transistor which detects and outputs a voltage potential converted from one of said first floating diffusion section and said second floating diffusion section.

36. (Previously Presented) The solid state imaging apparatus of claim 39, wherein the plurality of read lines are connected to a vertical scanning circuit.

37. (Previously Presented) The solid state imaging apparatus of claim 39, further comprising:

a plurality of a pair of signal lines outputting signals from the first pixel amplifier transistors and the second pixel amplifier transistors, respectively, to the outside.

38. (Cancelled)

39. (Currently Amended) A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein each first floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and each second floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and

substantially one floating diffusion section is included in the adjacent photoelectric conversion cells.

40. (Previously Presented) The solid state imaging apparatus of claim 39, wherein each read-out line is connected to the transfer transistors connected to the photoelectric conversion sections which are included in one of the first and second columns.

41. (Previously Presented) The solid state imaging apparatus of claim 39, wherein each read-out line is connected to the transfer transistors connected to the photoelectric conversion sections which are included in the first and second columns, respectively.

42. (Previously Presented) The solid state imaging apparatus of claim 39, wherein each floating diffusion section and each pixel amplifier transistor are shared by the photoelectric sections in the first row of one of the photoelectric conversion cells and the photoelectric sections in the second row of another of the photoelectric conversion cells.

43. (Previously Presented) The solid state imaging apparatus of claim 39, further comprising:

a signal line for outputting a signal from each pixel amplifier transistor to the outside; and

a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line.

44. (Previously Presented) The solid state imaging apparatus of claim 39, wherein each floating diffusion section and each pixel amplifier transistor are shared by photoelectric conversion sections which are adjacent to each other in the row direction or in the column direction.

45. (Previously Presented) The solid state imaging apparatus of claim 39, wherein in each floating diffusion section, a reset section for resetting charge stored in the floating diffusion section.

46. (Previously Presented) The solid state imaging apparatus of claim 39, wherein the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction.

47. (Previously Presented) The solid state imaging apparatus of claim 39, further comprising a signal processing circuit for processing an output signal from each pixel amplifier transistor.

48. (Previously Presented) The solid state imaging apparatus of claim 39, wherein the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film.

49-65. (Cancelled)

66. (Currently Amended) A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein each first floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and each second floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and

substantially one floating diffusion section is included in the adjacent photoelectric conversion cells.

67. (Cancelled)

68. (Previously Presented) The solid state imaging apparatus of claim 39, wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

69. (Previously Presented) The camera of claim 66, wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

70. (New) The solid state imaging apparatus of claim 39, wherein

each floating diffusion section and each pixel amplifier transistor are disposed between the two photoelectric conversion cells adjacent to each other in a row direction, and

the read-out lines are disposed within the photoelectric conversion cells.

71. (New) The camera of claim 66, wherein

each floating diffusion section and each pixel amplifier transistor are disposed between the two photoelectric conversion cells adjacent to each other in a row direction, and

the read-out lines are disposed within the photoelectric conversion cells.

REMARKS

I. Introduction

At the time of the Office Action of December 29, 2006, claims 34-69 were pending in this application. In this Amendment, claims 39 and 66 have been amended, and claims 38, 49-65, and 67 have been canceled, and new claims 70 and 71 have been added. Care has been exercised to avoid the introduction of new matter. Support for the amendment of claims 39 and 66 can be found in, for example, page 12, lines 8-17 of the specification and Fig. 1. Support for the new claims can be found in, for example, page 12, lines 8-12; and page 13, lines 8-11 of the specification, and Fig. 1.

Claims 34-37, 39-48, 66, and 68-71 are now active in this application, of which claims 39 and 66 are independent.

II. The Rejection of Claims 34-47, 49-63, 65, and 68

Claims 34-47, 49-63, 65, and 68 have been rejected under 35 U.S.C. §102(b) as being anticipated by Guidash. It is noted that the rejection of claims 38 and 49-63 has been rendered moot by cancellation of those claims.

Applicants submit that Guidash does not disclose a solid state imaging apparatus including all the limitations recited in independent claim 39. Specifically, Guidash does not disclose, at a minimum, "each first floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and each second floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and substantially one floating diffusion section is included in the adjacent photoelectric conversion cells," recited in claim 39.

In the present invention, a floating diffusion section can be shared by photoelectric conversion cells each including a plurality of photodiode sections. For example, in Fig. 1 of the present application, four photodiode sections (two photodiode sections are in one photoelectric conversion cell, while the other two photodiode sections are in another photoelectric conversion cell) share one floating diffusion section. It may be said that there is a 0.25 floating diffusion section per photodiode section. Accordingly, the present invention can reduce the number of floating diffusion sections per photodiode section. As a result, it is possible to increase an aperture ratio, i.e., an opening area of the photodiode section (photoelectric element) to the photoelectric conversion cell and downsize plane dimensions of the photoelectric conversion cell itself.

Guidash in Figs. 2A and 2B discloses a solid state imaging apparatus comprising: picture architecture 20 (picture cell) including two photodetectors 24 arranged in two rows and one column; transfer gates TG1 and TG2 for transferring charges from the photodetectors 24; floating diffusion section 26 connected to photodetectors 24 through transfer gates TG1 and G2; and amplifier 27 connected to floating diffusion section 26.

As shown in Figs. 2A and 2B of Guidash, floating diffusion section 26 is owned exclusively by one picture cell (picture cell 20), i.e., two photodiode sections in one picture cell share one floating diffusion section, but the floating diffusion section is not shared by picture cells adjacent to each other. This means that there is a 0.5 floating diffusion section per photodiode section in Guidash.

In contrast, the claimed floating diffusion section is shared by photoelectric conversion cells adjacent to each other. Since each photoelectric conversion cell includes a plurality of photoelectric sections, as claimed, the floating diffusion section is further shared by the plurality

of photoelectric sections in one photoelectric conversion cell. For example, in the case of Fig. 1, it can be said that there is a 0.25 floating diffusion section per photodiode section in the present invention. Accordingly, Guidash does not disclose, at a minimum, the claimed floating diffusion section.

According to one aspect of the present invention, since the number of floating diffusion sections can be reduced, it is possible to increase the aperture ratio of the photodiode section to the photoelectric conversion cell and downsize the plane dimensions of the photoelectric conversion cell. As a result, sensitivity of the solid state imaging apparatus can be improved. Guidash cannot provide the same benefit.

Based on the foregoing, Applicants submit that Guidash does not identically disclose a solid state imaging apparatus including all the limitations recited in independent claim 39, within the meaning of 35 U.S.C. §102. Dependent claims 34-37, 40-47, and 68 are also patentably distinguishable over Guidash at least because these claims respectively include all the limitations recited in independent claim 39. Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims and favorable consideration thereof.

III. The Rejection of Claims 66, 67, and 69

Claims 66, 67, and 69 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash and Patterson. The rejection of claim 67 has been rendered moot by cancellation of the claim.

The Examiner admitted that Guidash does not disclose that the solid state imaging apparatus is part of a camera. However, the Examiner asserted that Patterson et al. teaches the

missing feature of Guidash, and concluded that it would have been obvious to modify Guidash's device based on the teachings of Patterson et al. to arrive at the claimed invention.

Applicants submit that Guidash does not disclose a camera including all the limitations recited in independent claim 66. Specifically, Guidash does not teach, at a minimum, "each first floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and each second floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and substantially one floating diffusion section is included in the adjacent photoelectric conversion cells," recited in independent claim 66. Applicants incorporate herein the arguments previously advanced in responding to the rejection of claim 39 under 35 U.S.C. §102 for anticipation evidenced by Guidash. The Examiner's additional comments and secondary reference to Patterson et al. do not cure the previously argued deficiencies in Guidash.

Accordingly, Guidash and Patterson et al., either individually or in combination, do not teach a camera including all the limitations recited in independent claim 66, within the meaning of 35 U.S.C. §103. Dependent claim 69 is also patentably distinguishable over Guidash and Patterson et al. at least because the claim includes all the limitations recited in independent claim 66. Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims and favorable consideration thereof.

IV. The Rejection of Claims 48 and 64

Claims 48 and 64 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash in view of Yamazaki et al. It is noted that the rejection of claim 64 has been rendered moot by cancellation of the claim.

Since claim 48 depends from independent claim 39, Applicants incorporate herein the arguments previously advanced in responding to the rejection of claim 39 under 35 U.S.C. §102(b) for anticipation evidence by Guidash. The Examiner's additional comments and secondary reference to Yamazaki et al. do not cure the previously argued deficiencies in Guidash. Applicants, therefore, respectfully solicit withdrawal of the rejection of the claim and favorable consideration thereof.

V. New Claims 70 and 71

Applicants believe that new claims 70 and 71 are patentably distinguishable over Guidash, Patterson et al., and Yamazaki et al. Favorable consideration is, therefore, respectfully solicited.

VI. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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WDC99 1368972-1 060188.0710

Docket No.: 060188-0710 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Mitsuyoshi MORI, et al.	:	Confirmation Number: 7667
Application No.: 10/706,918	:	Group Art Unit: 2814
Filed: November 14, 2003	:	Examiner: John C. Ingham

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

AMENDMENT WITH REQUEST FOR CONTINUED EXAMINATION

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of June 22, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-33. (Cancelled)

34. (Previously Presented) The solid state imaging apparatus of claim 41, wherein the plurality of photoelectric elements are photo diodes.

35. (Previously Presented) The solid state imaging apparatus of claim 39, wherein,

the first and second pixel amplifier transistors are coupled to the first and second floating diffusion sections, respectively; and

each of the first and second pixel amplifier transistors comprises a source follower transistor which detects and outputs a voltage potential converted from one of said first floating diffusion section and said second floating diffusion section.

36. (Previously Presented) The solid state imaging apparatus of claim 39, wherein the plurality of read lines are connected to a vertical scanning circuit.

37. (Previously Presented) The solid state imaging apparatus of claim 39, further comprising:

a plurality of a pair of signal lines outputting signals from the first pixel amplifier transistors and the second pixel amplifier transistors, respectively, to the outside.

38. (Cancelled)

39. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines ~~each first floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and each second~~

~~floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and~~

~~substantially one floating diffusion section is included in the adjacent photoelectric conversion cells~~.

40. (Currently amended) The solid state imaging apparatus of claim 39, wherein in each photoelectric conversion cell, a first read-out line is connected to a gate of a transfer transistor included in the first row and the first column and a gate of a transfer transistor included in the second row and the first column, and a second read-out line is connected to a gate of a transfer transistor included in the first row and the second column and a gate of a transfer transistor included in the second row and the second column ~~each read-out line is connected to the transfer transistors connected to the photoelectric conversion sections which are included in one of the first and second columns~~.

41. (Currently amended) The solid state imaging apparatus of claim 39, wherein in each photoelectric conversion cell, a first read-out line is connected to a gate of a transfer transistor included in the first row and the first column and a gate of a transfer transistor included in the second row and the second column, and a second read-out line is connected to a gate of a transfer transistor included in the first row and the second column and a gate of a transfer transistor included in the second row and the first column ~~each read-out line is connected to the transfer transistors connected to the photoelectric conversion sections which are included in the first and second columns, respectively~~.

42. (Previously Presented) The solid state imaging apparatus of claim 39, wherein each floating diffusion section and each pixel amplifier transistor are shared by the photoelectric sections in the first row of one of the photoelectric conversion cells and the photoelectric sections in the second row of another of the photoelectric conversion cells.

43. (Previously Presented) The solid state imaging apparatus of claim 39, further comprising:

a signal line for outputting a signal from each pixel amplifier transistor to the outside; and

a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line.

44. (Previously Presented) The solid state imaging apparatus of claim 39, wherein each floating diffusion section and each pixel amplifier transistor are shared by photoelectric conversion sections which are adjacent to each other in the row direction or in the column direction.

45. (Previously Presented) The solid state imaging apparatus of claim 39, wherein in each floating diffusion section, a reset section for resetting charge stored in the floating diffusion section.

46. (Previously Presented) The solid state imaging apparatus of claim 39, wherein the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction.

47. (Previously Presented) The solid state imaging apparatus of claim 39, further comprising a signal processing circuit for processing an output signal from each pixel amplifier transistor.

48. (Previously Presented) The solid state imaging apparatus of claim 39, wherein the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film.

49-65. (Cancelled)

66. (Currently amended) A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row; and

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section, and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines ~~each first floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and each second floating diffusion section is shared by the photoelectric conversion cells adjacent to each other, and~~

~~substantially one floating diffusion section is included in the adjacent photoelectric conversion cells~~.

67. (Cancelled)

68. (Previously Presented) The solid state imaging apparatus of claim 39, wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

69. (Previously Presented) The camera of claim 66, wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

70. (Currently amended) The solid state imaging apparatus of claim 39, wherein

each floating diffusion section ~~and each pixel amplifier transistor are~~ is disposed across ~~between~~ the two photoelectric conversion cells adjacent to each other in a row direction, and

[[the]] only two read-out lines are disposed within the photoelectric conversion cells.

71. (Currently amended) The camera of claim 66, wherein

each floating diffusion section ~~and each pixel amplifier transistor are~~ is disposed across ~~between~~ the two photoelectric conversion cells adjacent to each other in a row direction, and

[[the]] only two read-out lines are disposed within the photoelectric conversion cells.

REMARKS

I. Introduction

Claims 34-37, 39-48, 66, and 68-71 are pending in this application, of which claims 39 and 66 are independent. In this Amendment, claims 39-41, 66, 70, and 71 have been amended. Care has been exercised to avoid the introduction of new matter. Support for the amendment of claims 39 and 66 can be found in, for example, page 13, lines 8-11 of the specification and Fig. 1. Support for the amendment of claims 40, 70, and 71 can be found in, for example, Fig. 1 and relevant description of the specification. Support for the amendment of claim 41 can be found in, for example, Fig. 3 and relevant description of the specification.

II. Information Disclosure Statement

Applicants note that the Information Disclosure Statement filed December 21, 2006 has not been acknowledged. Applicants respectfully request the Examiner to clarify the record by acknowledging receipt of the IDS when reviewed and provide a copy of the PTO-1449 form appropriately initialed indicating consideration of the cited reference. An additional copy of the previously submitted PTO-1449 form is enclosed for the Examiner's convenience.

III. The Present Application

The present application describes a solid state imaging apparatus in which each of photoelectric conversion cells comprises a plurality of photoelectric sections (photodiode (PD) sections), configured to be able to share a floating diffusion (FD) section, a pixel amplifier transistor, and a read-out line.

For example, four photoelectric sections share one floating diffusion (PD) section, and two transfer transistors share one read-out line in each photoelectric conversion cell (see Fig. 1). In this case, there are a 0.25 floating diffusion section per PD section and a 0.5 read-out line per PD section (or transfer transistor).

Accordingly, the number of floating diffusion sections, pixel amplifier transistors, and read-out lines per PD section can be reduced in the solid state imaging apparatus. Therefore, it may be possible to increase an aperture ratio of the PD section (photoelectric element) to the photoelectric conversion cell (pixel), and downsize plane dimensions of the photoelectric conversion cell itself.

IV. The Rejection of Claims 34-37, 39-47, 68, and 70

Claims 34-37, 39-47, 68, and 70 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash. The Examiner asserted that Guidash, describing an active pixel image sensor, teaches the claimed subject matter.

Applicants submit that Guidash does not disclose or suggest a solid state imaging apparatus including all the limitations recited in independent claim 39. Specifically, Guidash does not teach, at a minimum, "in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines," as recited in independent claim 39.

In the Office Action, the Examiner, referring to Fig. 3b of Guidash, asserted that the reference teaches the claimed solid state imaging apparatus. Fig. 3b of Guidash illustrates pixel architecture 30 having four photodetectors (PD) 71-74 arranged in two rows and two columns;

transfer gates 51, 52, 61 and 62 for transferring charges from respective photodetectors 71-74; floating diffusion (FD) sections 41 and 42 connected to photodetectors 71-74 through transfer gates 51, 52, 61 and 62; and amplifier 32 connected to floating diffusion sections 41 and 42.

Applicants invite the Examiner's attention to terminals TG1b, TG1a, TG2b and TG2a connected to transfer gates 51, 52, 61 and 62, respectively, shown in Fig. 3b and a timing chart of Fig. 4 showing control pulses applied to the respective terminals. Fig. 4 shows that terminals TG1b, TG1a, TG2b and TG2a are respectively supplied with control pulses different from each other. Guidash teaches that there are four control signal lines connected to transfer gates 51, 52, 61 and 62, respectively, to provide the gates with different pulses, respectively. In other words, one control signal line (read-out line) is necessary for one photodetector (transfer gates) in Guidash.

In more detail, each photoelectric conversion cell (pixel) has four photoelectric sections (photodiodes) sharing substantially one floating diffusion (FD) section, and is provided with one control signal line (read-out line) per transfer gate in Guidash. Thus, there is one read-out line per photodiode section.

In contrast, claim 39 recites that a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines. For example, each photoelectric conversion cell has four photoelectric sections (PD sections) sharing one FD section, and two transfer transistors included in the same row or rows adjacent to each other share one read-out line in the each photoelectric conversion cell (see Figs. 1 and 3 of the present application). There is a 0.5 read-out line per photodiode section. Accordingly, it is possible to reduce wiring regions in one

pixel and thereby increase an opening area of the photodiode section with respect to one pixel. As a result, it can further possible to increase sensitivity of the solid state imaging apparatus.

Based on the foregoing, Applicants submit that Guidash does not disclose or suggest a solid state imaging apparatus including all the limitations recited in independent claim 39, within the meaning of 35 U.S.C. §103. Dependent claims 34-37, 40-47, 68, and 70 are also patentably distinguishable over Guidash at least because these claims respectively include all the limitations recited in independent claim 39. Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims and favorable consideration thereof.

V. The Rejection of Claim 48

Claim 48 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash in view of Yamazaki et al. This rejection is respectfully traversed.

Claim 48 depends from independent claim 39. Applicants thus incorporate herein the arguments made in response to the rejection of claim 39 under 35 U.S.C. §103 for obviousness predicated upon Guidash. The Examiner's additional comments and secondary reference to Yamazaki et al. do not cure the deficiencies of Guidash. Yamazaki et al. simply discloses a display device in which a channel formation region in the semiconductor film is covered with the gate wiring, thereby shielding the channel formation region. Applicants, therefore, respectively solicit withdrawal of the claim and favorable consideration thereof.

VI. The Rejection of Claims 66, 69, and 71

Claims 66, 69, and 71 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash and Patterson et al. The Examiner admitted that Guidash does not disclose that the

solid state imaging apparatus is part of a camera. However, the Examiner asserted that Patterson et al. teaches the missing feature of Guidash, and concluded that it would have been obvious to modify Guidash's device based on the teachings of Patterson et al. to arrive at the claimed invention.

Applicants submit that Guidash and Patterson et al., either individually or in combination, do not disclose or suggest a camera comprising a solid state image apparatus including all the limitations recited in independent claim 66. Specifically, the applied combination of Guidash and Patterson et al. does not teach, at a minimum, a solid state image apparatus "wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines," as recited in claim 66. Claim 66 recites a camera comprising a solid state imaging apparatus similar to that recited in independent claim 39.

Applicants thus incorporate herein the arguments made in response to the rejection of claim 39 under 35 U.S.C. §103 for obviousness predicated upon Guidash. The Examiner's additional comments and secondary reference to Patterson et al. do not cure the deficiencies of Guidash. Patterson et al. simply teaches using a solid state imaging apparatus in electronic cameras. The reference does not teach that in a solid state imaging apparatus, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines, as claimed. Dependent claims 69 and 71 are also patentably distinguishable over Guidash and Patterson et al. al least because these claims include all the limitations recited in independent claims 66.

Applicants, therefore, respectively solicit withdrawal of the rejection of claim 66, 69, and 71, and favorable consideration thereof.

VII. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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WDC99 1463704-1.060188.0710

Docket No.: 060188-0710 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Mitsuyoshi MORI, et al.	:	Confirmation Number: 7667
Application No.: 10/706,918	:	Group Art Unit: 2814
Filed: November 14, 2003	:	Examiner: John C. Ingham

For: SOLID STATE IMAGING APPARATUS, METHOD FOR DRIVING THE SAME AND CAMERA USING THE SAME

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated December 21, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 10 of this paper.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-33. (Cancelled)

34. (Previously Presented) The solid state imaging apparatus of claim 41, wherein the plurality of photoelectric elements are photo diodes.

35. (Previously Presented) The solid state imaging apparatus of claim 39, wherein,

the first and second pixel amplifier transistors are coupled to the first and second floating diffusion sections, respectively; and

each of the first and second pixel amplifier transistors comprises a source follower transistor which detects and outputs a voltage potential converted from one of said first floating diffusion section and said second floating diffusion section.

36. (Previously Presented) The solid state imaging apparatus of claim 39, wherein the plurality of read lines are connected to a vertical scanning circuit.

37. (Previously Presented) The solid state imaging apparatus of claim 39, further comprising:

a plurality of a pair of signal lines outputting signals from the first pixel amplifier transistors and the second pixel amplifier transistors, respectively, to the outside.

38. (Cancelled)

39. (Currently amended) A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines,

each floating diffusion section is disposed across the two photoelectric conversion cells adjacent to each other in a row direction, and

only two read-out lines are disposed within the photoelectric conversion cells.

40. (Currently amended) ~~The solid state imaging apparatus of claim 39,~~ A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines, and

wherein in each photoelectric conversion cell, a first read-out line is connected to a gate of a transfer transistor included in the first row and the first column and a gate of a transfer transistor included in the second row and the first column, and a second read-out line is connected to a gate of a transfer transistor included in the first row and the second column and a gate of a transfer transistor included in the second row and the second column.

41. (Currently amended) ~~The solid state imaging apparatus of claim 39,~~ A solid state imaging apparatus comprising:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row;

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines, and

wherein in each photoelectric conversion cell, a first read-out line is connected to a gate of a transfer transistor included in the first row and the first column and a gate of a transfer transistor included in the second row and the second column, and a second read-out line is connected to a gate of a transfer transistor included in the first row and the second column and a gate of a transfer transistor included in the second row and the first column.

42. (Previously Presented) The solid state imaging apparatus of claim 39, wherein each floating diffusion section and each pixel amplifier transistor are shared by the photoelectric sections in the first row of one of the photoelectric conversion cells and the photoelectric sections in the second row of another of the photoelectric conversion cells.

43. (Previously Presented) The solid state imaging apparatus of claim 39, further comprising:

a signal line for outputting a signal from each pixel amplifier transistor to the outside; and

a select transistor which is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier transistor and the signal line.

44. (Previously Presented) The solid state imaging apparatus of claim 39, wherein each floating diffusion section and each pixel amplifier transistor are shared by photoelectric

conversion sections which are adjacent to each other in the row direction or in the column direction.

45. (Previously Presented) The solid state imaging apparatus of claim 39, wherein in each floating diffusion section, a reset section for resetting charge stored in the floating diffusion section.

46. (Previously Presented) The solid state imaging apparatus of claim 39, wherein the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction or in the column direction.

47. (Previously Presented) The solid state imaging apparatus of claim 39, further comprising a signal processing circuit for processing an output signal from each pixel amplifier transistor.

48. (Previously Presented) The solid state imaging apparatus of claim 39, wherein the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film.

49-65. (Cancelled)

66. (Currently amended) A camera comprising a solid state imaging apparatus, the apparatus including:

a plurality of photoelectric conversion cells each including a plurality of photoelectric sections arranged in a matrix including at least first and second rows and first and second columns;

a plurality of first floating diffusion sections each being shared by, and being connected to, the photoelectric sections which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of second floating diffusion sections each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively;

a plurality of read-out lines each being selectively connected to at least two of the transfer transistors that are not included in the same row; [[and]]

a plurality of first pixel amplifier transistors each detecting and outputting the potential of each first floating diffusion section[[,]]; and

a plurality of second pixel amplifier transistors each detecting and outputting the potential of each second floating diffusion section,

wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines,

each floating diffusion section is disposed across the two photoelectric conversion cells adjacent to each other in a row direction, and

only two read-out lines are disposed within the photoelectric conversion cells.

67. (Cancelled)

68. (Previously Presented) The solid state imaging apparatus of claim 39, wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

69. (Previously Presented) The camera of claim 66, wherein respective charges of the photoelectric conversion sections each being connected to one of the read-out lines and being read out by the transfer transistors are read out by said first floating diffusion sections or said second floating diffusion sections.

70. (Cancelled)

71. (Cancelled)

REMARKS

I. Introduction

At the time of the Office Action December 21, 2007, claims 34-37, 39-48, 66, and 68-71 were pending in this application. Applicants acknowledge, with appreciation, the Examiner's indication that claims 40, 41, 70, and 71 would be allowable if written in independent form including all of the limitations of the base claim and any intervening claims.

In this Amendment, claims 39, 40, 41, and 66 have been amended, and claims 70 and 71 have been canceled. Care has been exercised to avoid the introduction of new matter. Specifically, claims 39 and 66 have been amended to include the limitations recited in dependent claims 70 and 71, respectively. Claims 40 and 41 have been amended to be in independent form based on claim 39.

Claims 34-37, 39-48, 66, 68, and 69 are now active in this application, of which claims 39, 40, 41, and 66 are independent.

II. The Rejection of the Claims

Claims 34-37, 39, 42-47, and 68 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash and Wong; claim 48 has been rejected under 35 U.S.C. §103(a) as being a patentable over Guidash, Wong, and Yamazaki; and claims 66 and 69 have been rejected under 35 U.S.C. §103(a) as being a patentable over Guidash, Wong, and Patterson.

The above rejections have been rendered moot by the amendment of claims 39 and 66 to include the limitations of allowable claims 70 and 71, respectively. Applicants, therefore, respectively solicit withdrawal of the rejections of the claims and favorable consideration thereof.

III. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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US006160281A

United States Patent [19]

Guidash

[11] **Patent Number: 6,160,281**

[45] **Date of Patent: *Dec. 12, 2000**

[54] **ACTIVE PIXEL SENSOR WITH INTER-PIXEL FUNCTION SHARING**

[75] Inventor: **Robert M. Guidash**, Rush, N.Y.

[73] Assignee: **Eastman Kodak Company**, Rochester, N.Y.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/808,444**

[22] Filed: **Feb. 28, 1997**

[51] **Int. Cl.**[7] **H01L 27/146**; H03K 3/42

[52] **U.S. Cl.** **257/292**; 327/515

[58] **Field of Search** 257/291, 292; 327/515

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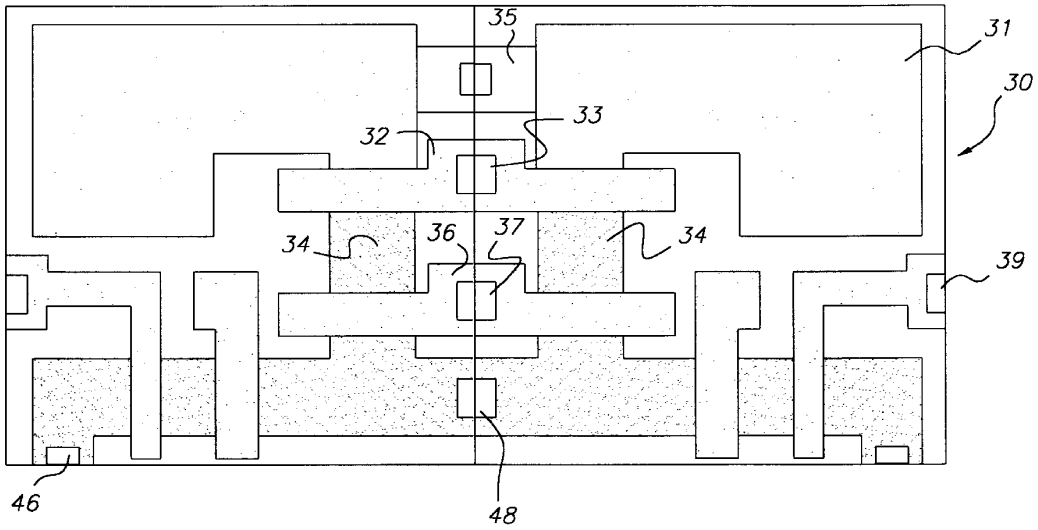
Primary Examiner—Gene M. Munson
Attorney, Agent, or Firm—James D. Leimbach

[57] **ABSTRACT**

An image sensor having a plurality of pixels comprising a semiconductor material of a first conductivity type with at least two adjacent pixels, each of the pixels has a photodetector formed within the substrate and an electrical function that is shared between the adjacent pixels integrated within the adjacent pixels. The electrical function can be: a transfer gate, a reset gate, a row select gate, an amplifier drain, an output node, a floating diffusion, a reset drain, a lateral overflow gate, an overflow drain or an amplifier, that is shared between multiple pixels resulting in a saving of space.

6 Claims, 11 Drawing Sheets



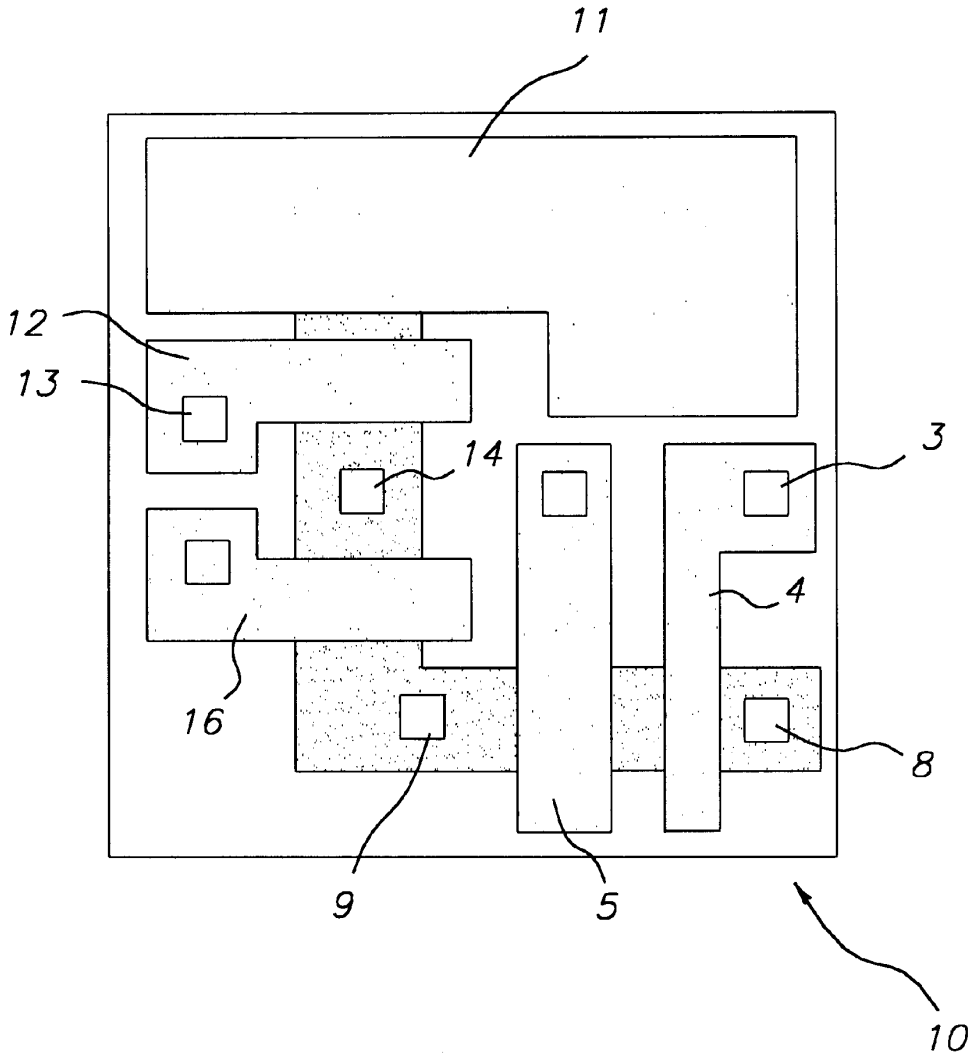


FIG. 1
(PRIOR ART)

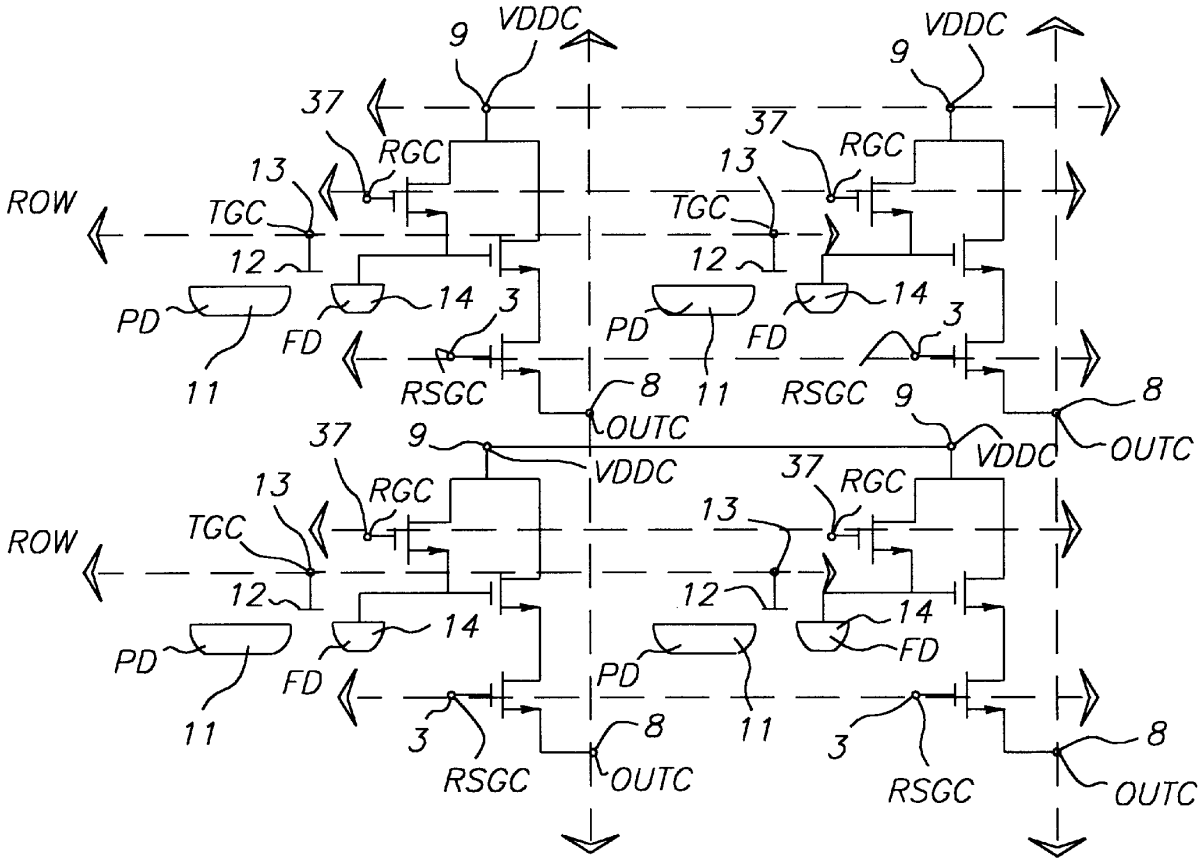


FIG. 2
(PRIOR ART)

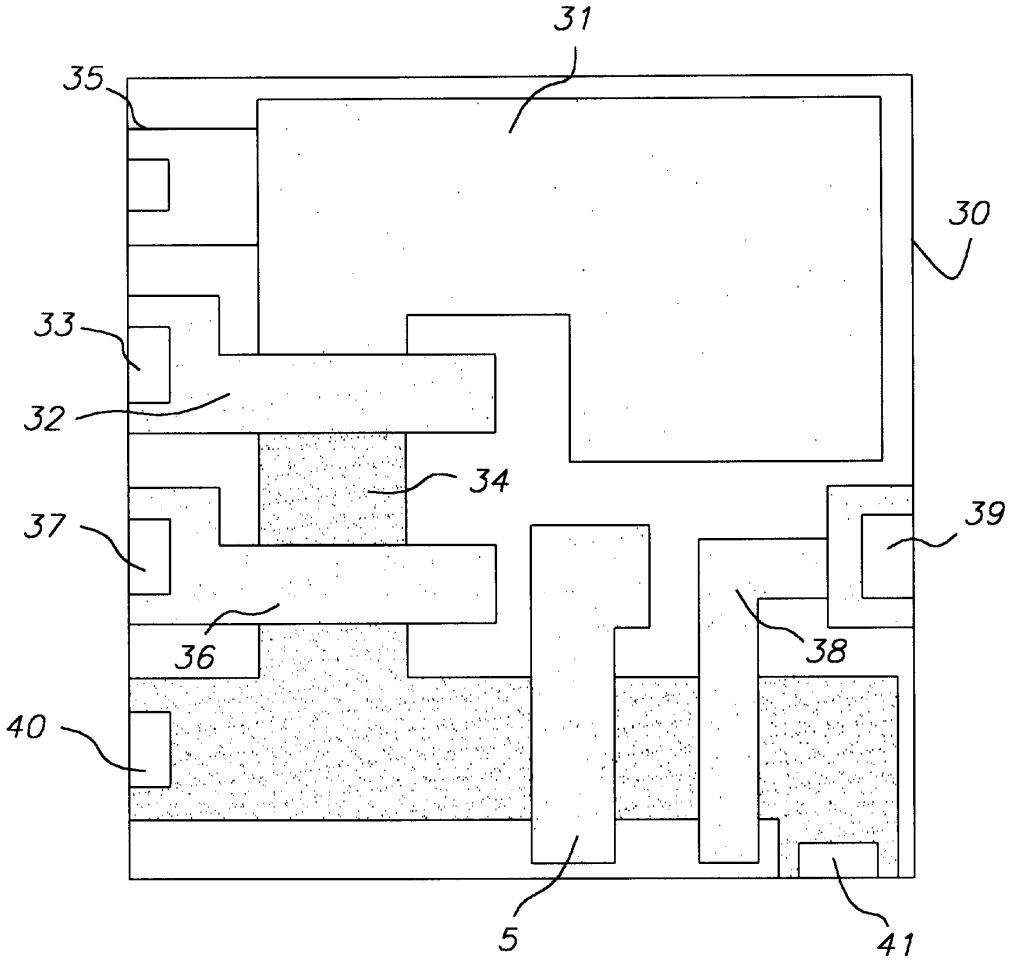


FIG. 3

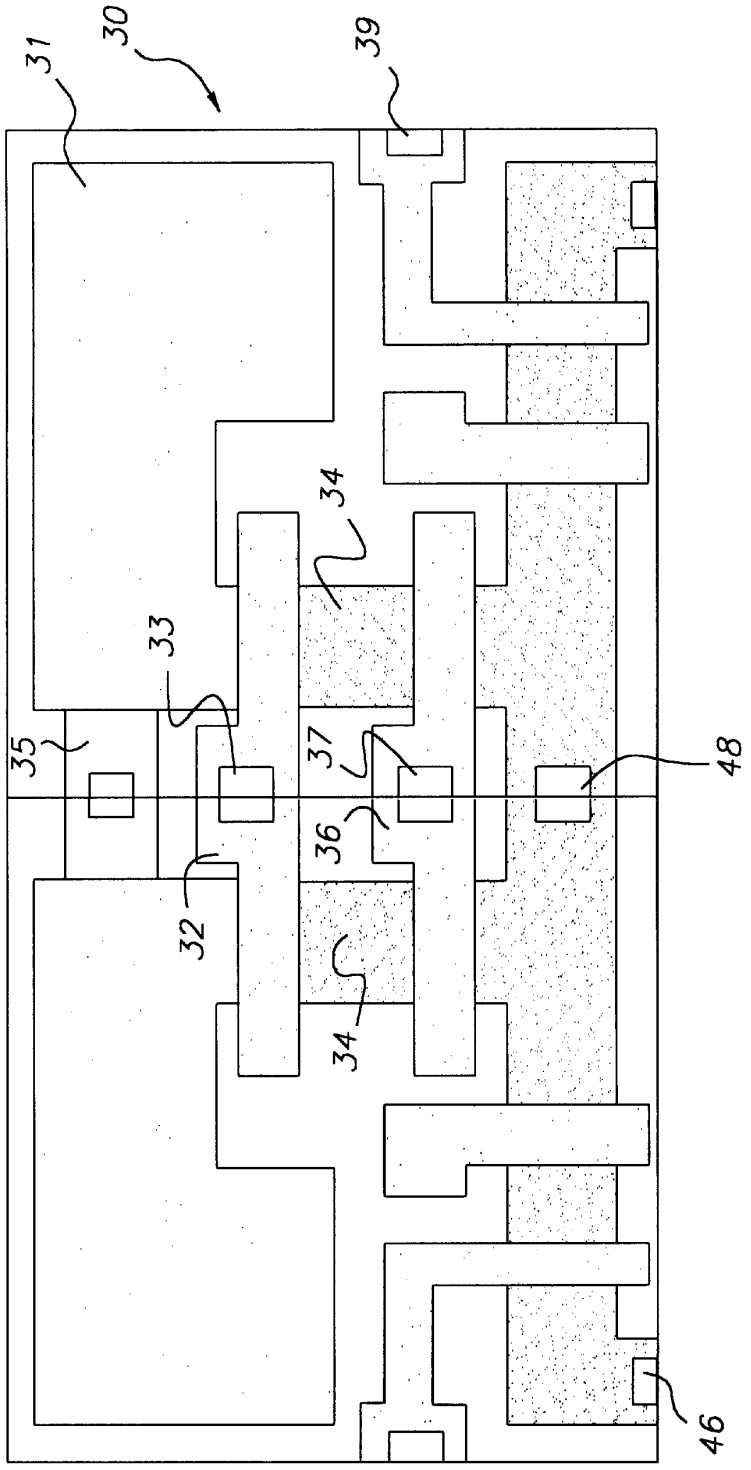


FIG. 4A

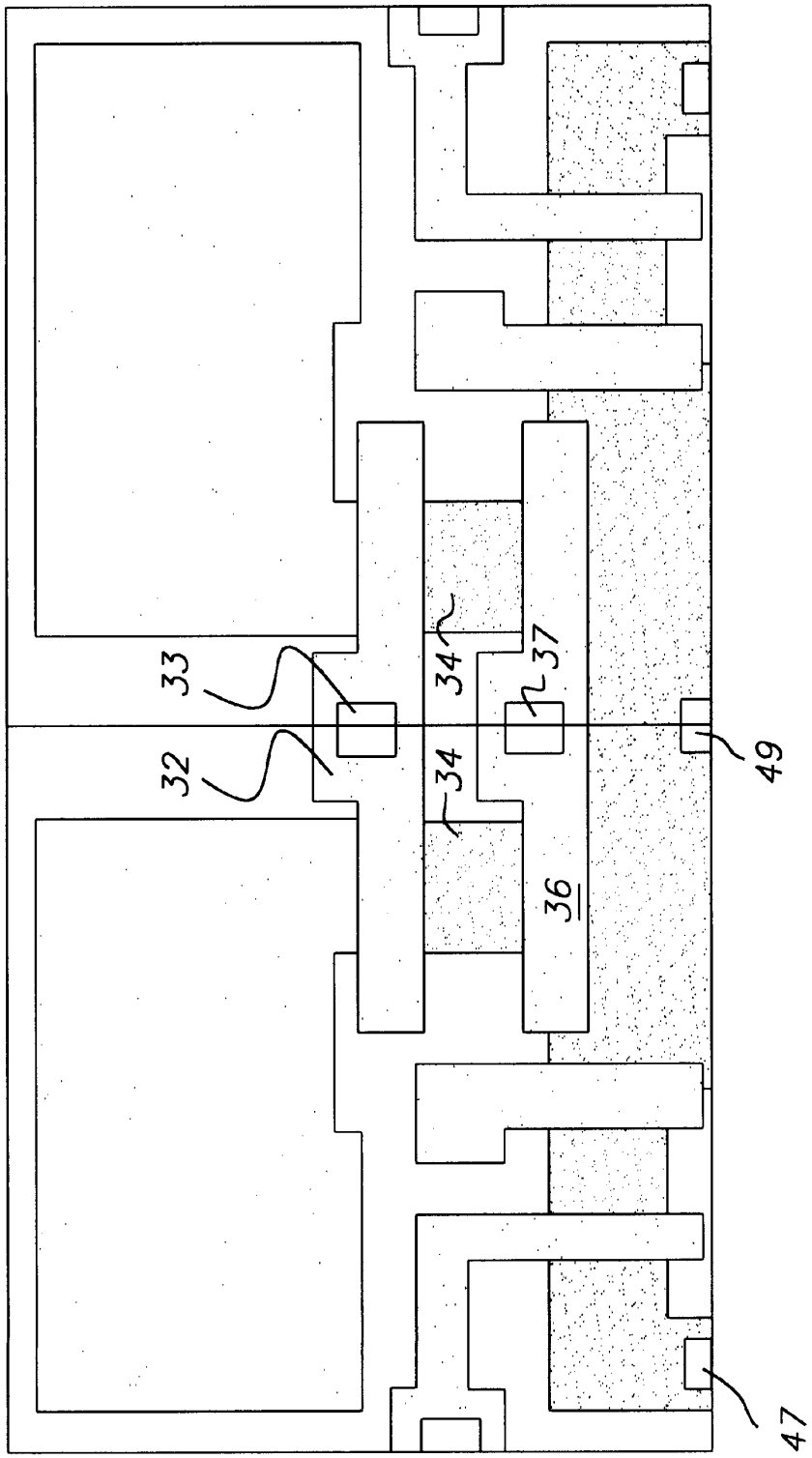


FIG. 4B

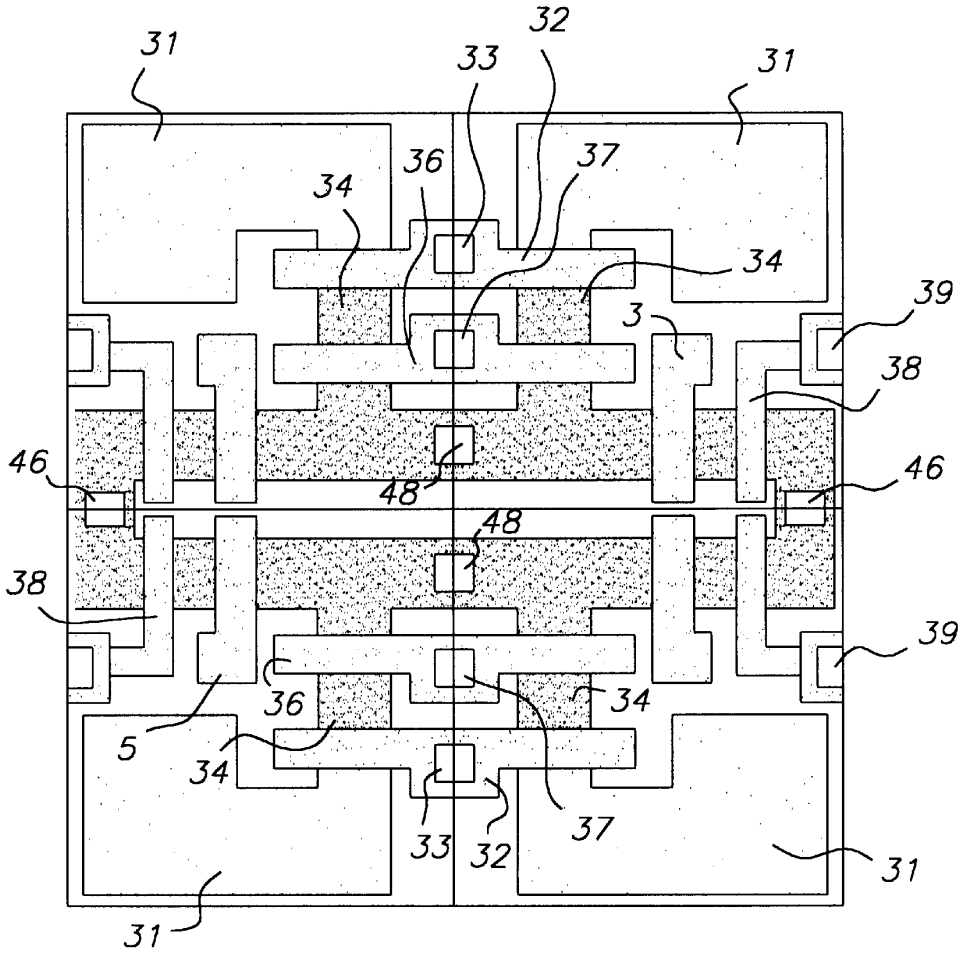

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FIG. 5A

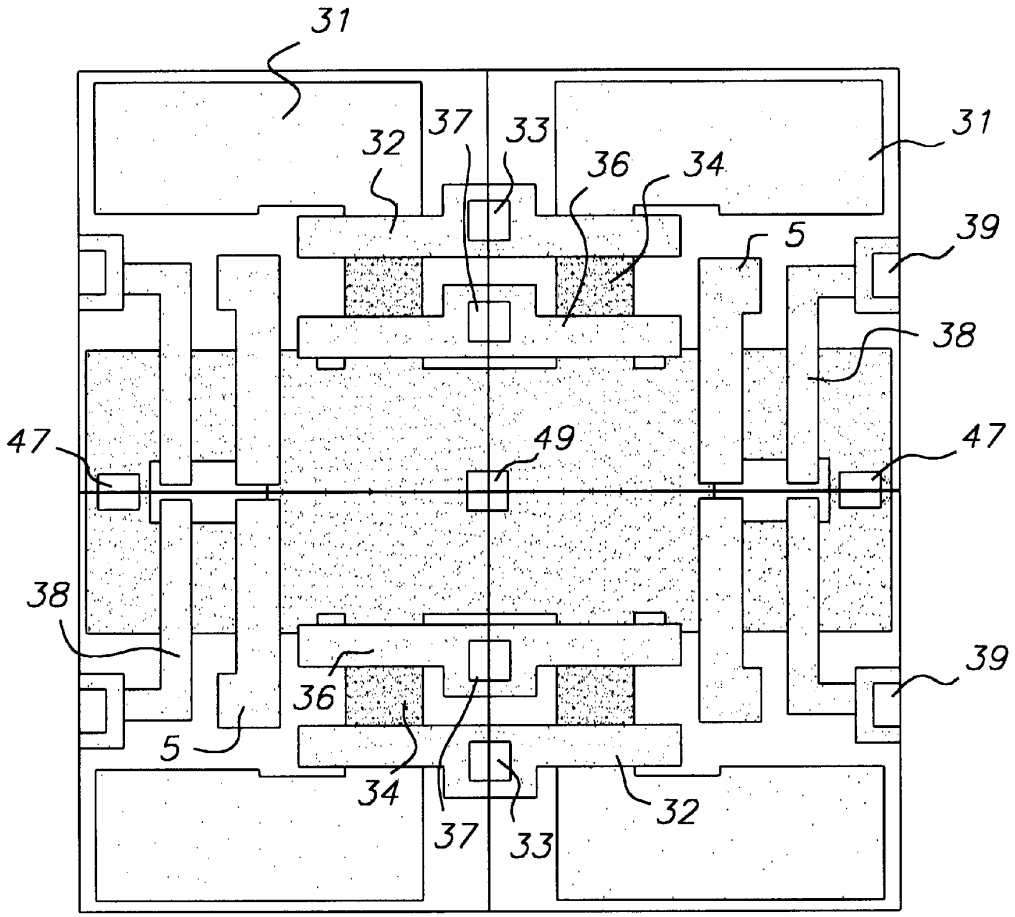

FIG. 5B

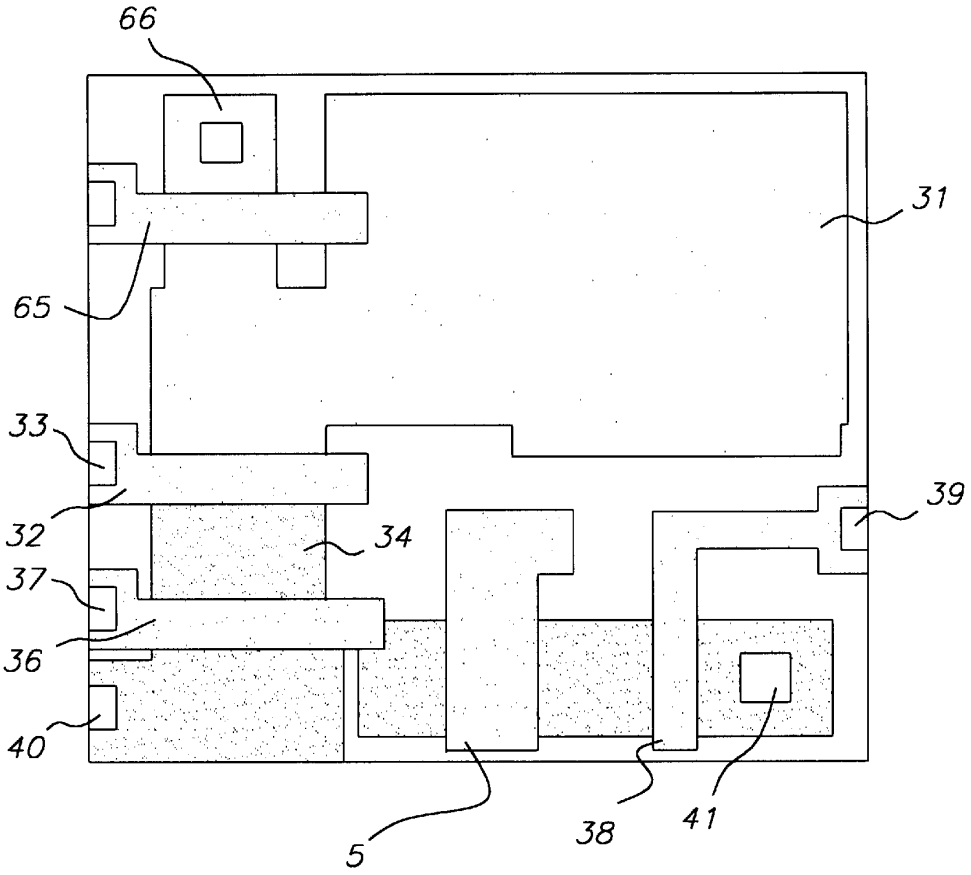

FIG. 6

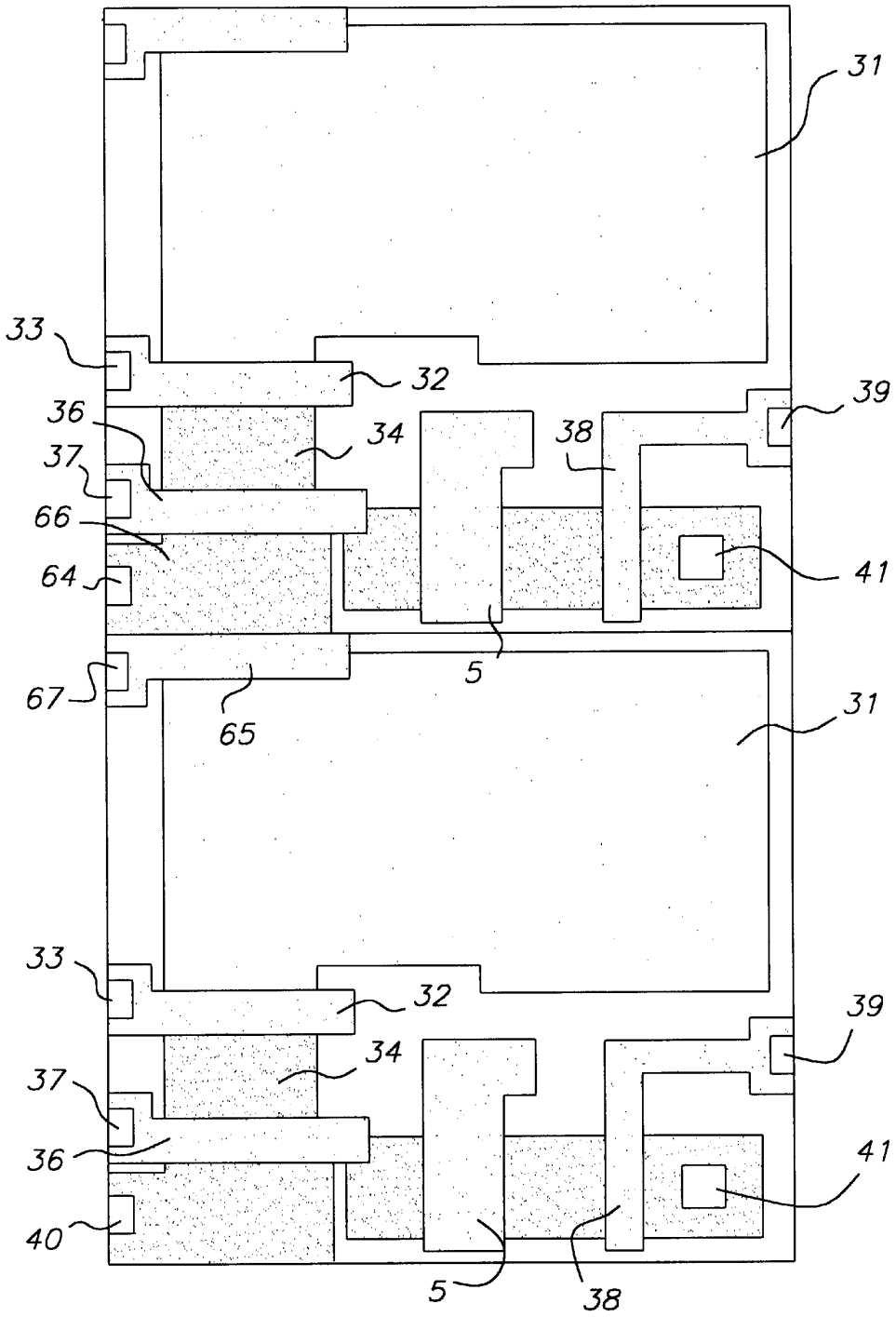

FIG. 7

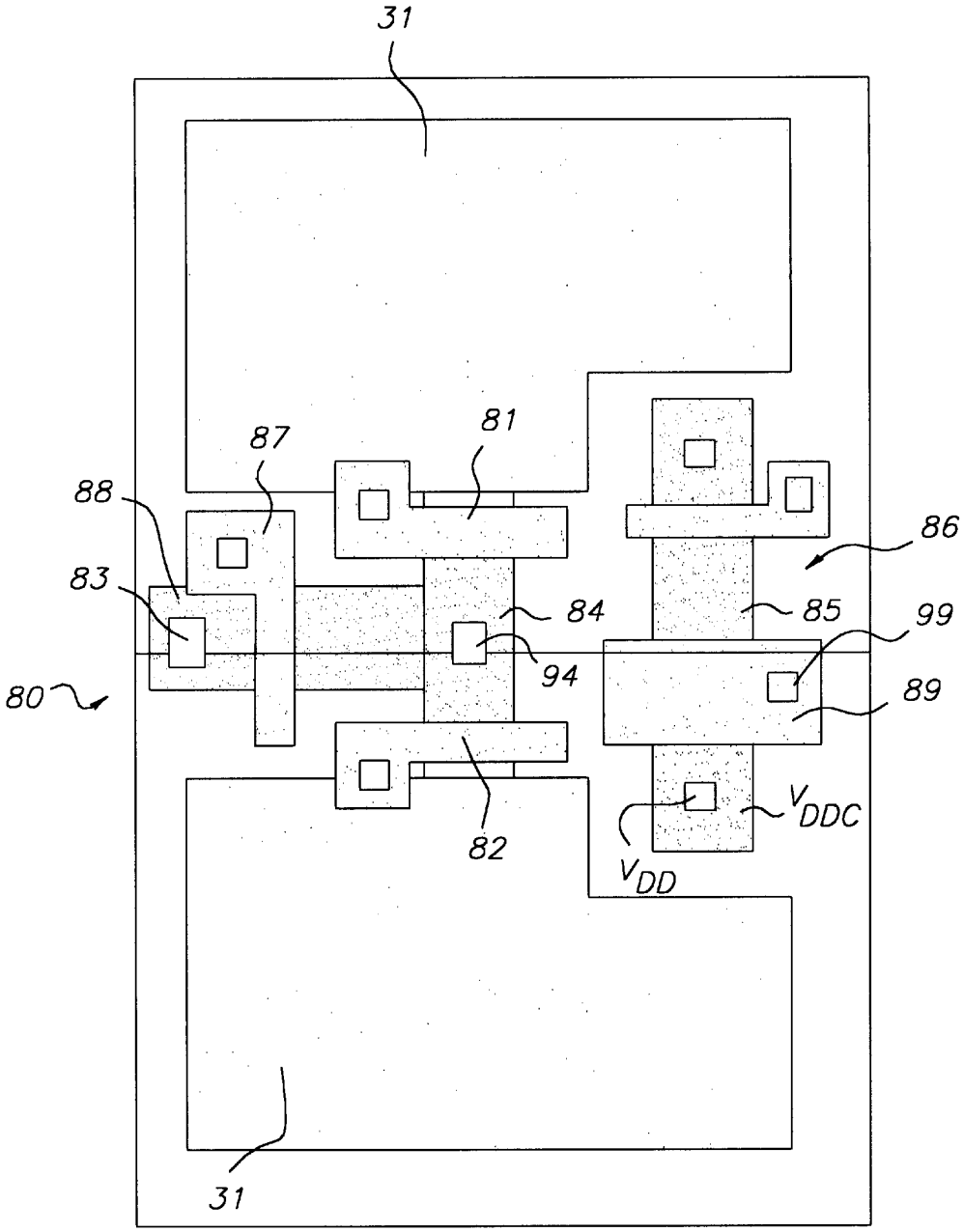

FIG. 8

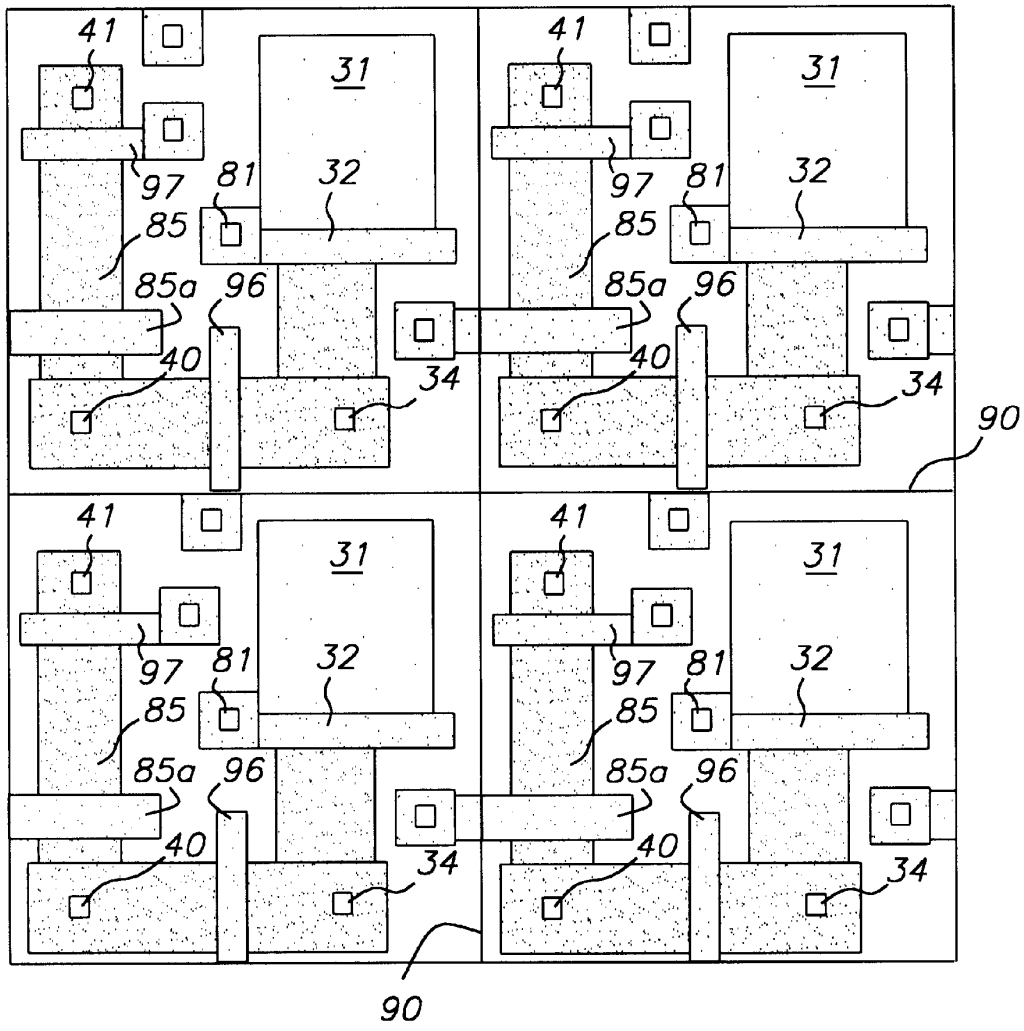

FIG. 9

ACTIVE PIXEL SENSOR WITH INTER-PIXEL FUNCTION SHARING

FIELD OF THE INVENTION

The invention relates generally to the field of solid state image sensors, specifically imagers referred to as Active Pixel Sensors, (APS), and to providing greater fill factors within APS sensors.

BACKGROUND OF THE INVENTION

DESCRIPTION OF THE PRIOR ART

APS are solid state imagers wherein each pixel typically contains a photo-sensing means, reset means, a charge transfer means, a charge to voltage conversion means, and all of part of an amplifier. Prior art APS devices have been operated in a manner where each line, or row, of the imager is selected and then read out using a column select signal (analogous to the selection and reading of a memory device). In prior art devices the connection, or contact, to the various nodes within the pixels of a given row is accomplished on a per pixel basis. This is true even though the pixels exist on the same electrical node within a row (see FIG. **1**). Since these contact regions are placed in each pixel, and contact regions typically consume a large amount of pixel area due to the overlap of metal layers required, inclusion of these contact regions in each pixel reduces the fill factor for the pixel because it takes up area that could otherwise be used for the photodetector. This reduces the sensitivity and saturation signal of the sensor. This adversely affects the photographic speed and dynamic range of the sensor, performance measures that are critical to obtaining good image quality. In addition prior art APS pixels have included the entire amplifier, address and reset transistors within a single pixel, and have made operative interconnection of these components and the photodetector entirely within a single pixel boundary. This leads to inefficiencies of layout and produces pixels with small fill factors.

In order to build high resolution, small pixel APS devices, it is necessary to use sub-μm CMOS processes in order to minimize the area of the pixel allocated to the row select transistor and other parts of the amplifier in the pixel. In essence, it takes a more technologically advanced and more costly process to realize the same resolution and sensitivity in an APS device as compared to a standard charge coupled device (CCD) sensor. However, APS devices have the advantages of single 5V supply operation, lower power consumption, x-y addressability, image windowing, and the ability to effectively integrate signal processing electronics on-chip, when compared to CCD sensors.

A typical prior art APS pixel **10** is shown in FIG. **1**. The pixel comprises a photodetector (PDET) **11**, that can be either a photodiode or photogate, a transfer gate (TG) **12**, floating diffusion (FD) **14**, reset transistor with a reset gate (RG) **16**, row select transistor with a row select gate (RSG) **4**, and signal transistor (SIG) **5**. Note that all of the electrical components required to readout and address the pixel are contained entirely within a single pixel boundary, and are operatively connected entirely within a single pixel boundary. Regions to provide contact to each of the various electrical nodes within the pixel that are common to a row are designated in FIG. **1** and shown schematically in FIG. **2**. These are Transfer Gate Contact (TGC) **13**, Reset Gate Contact (RGC) **17**, and Row Select Gate Contact (RSGC) **3**. Additionally there are contact regions that are common to a column. These are also shown in FIGS. **1** and **2**. These are

power supply contacts (VDDC) **9** and the pixel output node contact (OUTC) **8**. Note that there are separate and individual contact regions in each pixel even though some are common to a row or column. It is evident that the area consumed by these contact regions is a significant portion of the pixel area, thus limiting the area available for the photodetector, which reduces the fill factor and sensitivity of the pixel.

It should be apparent, from the foregoing discussion, that there remains a need in the art for APS sensors that have increased fill factors. This and other problems are addressed by the present invention.

SUMMARY OF THE INVENTION

The present invention addresses the foregoing problems. Briefly summarized, according to one aspect of the present invention the an image sensor having a plurality of pixels comprising: a semiconductor material of a first conductivity type; and at least two adjacent pixel having photodetectors formed within the substrate such that each pixel has at least one electrical function that is shared by the adjacent pixels.

The pixel layout innovation provided by the present invention yields a higher fill factor for the pixel. One approach to providing an image sensor with the sensitivity of a CCD and the advantages of an APS device is to improve the fill factor, thereby, increasing the corresponding sensitivity of the APS device. This is accomplished by the present invention in several ways: first by eliminating the need for a separate signal line contact areas in each pixel. Secondly, by sharing electrical components between pixels. Finally, fill factor can be increased by operatively interconnecting the electrical components by traversing pixel boundaries and using the array to complete the routing. These are all accomplished while maintaining the ability to selectively address specific pixels of the APS device.

The invention provides a means for reducing the area per pixel required for these contact regions. Conceptually, it can be described in the following manner. The design of each pixel is done to place the contact regions of the row related nodes along or near the left and right edges of the pixel, and the column related contact regions along or near the top or bottom edge of the pixel, (see FIG. **3**), allowing neighboring pixels to share these contact regions and alleviating the requirement of having separate contact regions in each pixel. In the case of the preferred embodiment of the present invention, contact regions are required for every 2 pixels as compared to each pixel as required by prior art devices. Hence, the area required per pixel by the present invention is reduced, resulting in an increase in fill factor for the pixel.

Additionally, one can use the VDD drain region of an adjacent pixel as a lateral overflow drain. This is a similar "pixel sharing" concept where the VDD drain region serves as the drain of the signal transistor for one pixel and the lateral overflow drain for the adjacent pixel or pixels. Since a separate lateral overflow drain region is not needed for each pixel, more area can be allocated to the photodetector, providing increased fill factor.

Another means to realize fill factor improvement is to utilize the row at a time read out operation, and provide a floating diffusion and amplifier for every two pixels instead of for each pixel. Since only one row is read out at a given time, a single floating diffusion and amplifier can be used for 2 adjacent pixels that are in separate rows. Once again the photodetector area per pixel can be increased, or the fill factor can be maintained to produce a smaller pixel.

Finally, by operatively interconnecting the pixel components such that the components orientation traverse pixel

boundaries (rather than providing a schematically complete layout within a single pixel boundary) layout efficiencies can be utilized to improve the fill factor of the pixel.

These and other aspects, objects, features, and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

ADVANTAGEOUS EFFECT OF THE INVENTION

The present invention has the following advantages. All of the features and advantages of prior art APS devices are maintained while requiring less pixel area for contact regions. This provides the following advantages:

higher fill factor, sensitivity and saturation signal for the same pixel size;

smaller pixel and device size for the same fill factor.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a top view of prior art APS pixel;

FIG. **2** is a schematic of an array of four prior art pixels as shown in FIG. **1**;

FIG. **3** is a top view of a pixel as envisioned by the present invention; having reduced contact area;

FIG. **4**A is a top view of two pixels of the present invention that illustrates the sharing of contact regions;

FIG. **4**B is a top view of the present invention as shown if FIG. **4***a* with reduced VDD contact region;

FIG. **5**A is a top view of 4 pixels of the present invention that are a mirror duplication of the two pixels in FIG. **4**A that illustrates the sharing of contact regions that are common to a column;

FIG. **5**B is a top view of 4 pixels of the present invention that are a mirror duplication of the two pixels in FIG. **4**B that illustrates the sharing of contact regions that are common to a column;

FIG. **6** is the pixel of FIG. **4**A that includes a lateral overflow gate and drain;

FIG. **7** is a diagram of 2 of the pixels as shown in FIG. **4**A with a lateral overflow gate for each pixel and VDD of the adjacent pixel used as a lateral overflow drain;

FIG. **8** is an illustration of 2 pixels sharing floating diffusion, reset gate, reset drain VDD, amplifier, row select gate, and output contact region.

FIG. **9** is a top view of 4 pixels illustrating operative interconnection of electrical components across pixel boundaries.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION OF THE INVENTION

One physical embodiment of the new pixel architecture is shown in FIG. **3**. Other specific physical embodiments are realizable. This one is chosen for illustration. The pixel **30** has a photodetecting area **31** that accumulates charge from incident light and transfers the stored charge under control of the transfer gate **32** to a floating diffusion **34**.

There are various contact regions that are associated with the circuit elements recited within the above description. The transfer gate **32** has a transfer gate contact **33**, the reset gate **36** has a reset gate contact **37** and the row select gate **38** has a row select gate contact (RSGC) **39**. These contact regions are row common contact regions, and are placed appropriately along the left and right side of pixel **30** boundaries. In the preferred embodiment as shown if FIG. **3**, half of the contact region for reset gate contact **37** and transfer gate contact **33** are placed on the left edge of the pixel. Half of a contact region for the row select gate contact **39** is placed along the right edge of the pixel. Next the column common contact regions VDDC **40** and OUTC **41** are placed appropriately along the bottom edge of the pixel. This architecture allows these various elements to be shared between pixels, in terms of function and also in terms of pixel area used to construct these elements. In the case where the photodetector **31** is a photogate, the photogate contact region **35** can be shared between photogates of adjacent pixels.

An array of pixels is then constructed in the following manner. First, a new pixel is created by mirroring the original pixel shown in FIG. **3** in the x-dimension. The new pixel is then butted with the original pixel by placing the half contact regions adjacent to each other. This is shown in FIGS. **4**A and **4**B. In FIG. **4**A, VDDC **48** is shared by 2 pixels. OUTC **46** is placed along a pixel border so that it may be shared with another pixel. In FIG. **4**B, VDDC **49** is placed along the bottom edge of the pixel so that it can be shared by 4 pixels. This can be done since the VDDC **49** node is common to all pixels, rows and columns. OUTC **47** is placed along a pixel border so that it may be shared by another pixel. The transfer gate **32** and the transfer gate contact **33** are also mirrored and shared by the two pixels shown in FIGS. **4**A and **4**B Next this group 2 pixels mirrored in the y-dimension then created another set of 2 pixels. These sets of 2 pixels are then butted so that the half contact regions for VDDC and OUTC are adjacent to each other. This is shown in FIGS. **5**A and **5**B, corresponding to FIGS. **4**A and **4**B, respectively. This set of 4 pixels is then arrayed to produce the desired number of pixels in the image sensor.

In order to provide antiblooming control during readout of the sensor, it is necessary to provide an overflow drain for the photodetector. The simplest approach in a CMOS process is to provide a lateral overflow drain that is separated from the photodetector **31** by a gate **65**. If one were to include a lateral overflow drain **66** in each pixel, this would further reduce the fill factor of the pixel, and adversely affect the sensitivity of the pixel. This is shown in FIG. **6**. However, by placing the VDD region appropriately within the pixel, this can be used as the lateral overflow drain for the adjacent pixel or pixels. One example of this is shown in FIG. **7**. This VDD serves as the power source for the amplifier for the top pixel in FIG. **7** while serving as the overflow drain for the bottom pixel in FIG. **7**. Since the lateral overflow drain **66** is now in another pixel, the pixel fill factor is not affected. By using this approach, antiblooming control during readout is achieved without impacting pixel fill factor.

Finally, FIG. **8** illustrates a new design of a pixel **80** that shares the floating diffusion **84**, with associated floating diffusion contact **94** amplifier **85**, with associated drain contact VDDC row select transistor **86**, and reset gate **87** with an adjacent pixel that is in a separate row. In this case the row select signal for 2 consecutive rows is actually the same. Image signal separation is achieved by having separate Transfer Gates **81**, **82** in each pixel. The operation occurs in the following manner. Row A is integrated, and the gate of the row select transistor **85** is turned on. The floating diffusion **84** is then reset by pulsing the reset gate **87**. This

reset signal is then read out for row A. Transfer Gate **81** is then pulsed on and the signal charge from photodetector A is transferred onto the floating diffusion **84**. The signal level is the read out for row A. Next the floating diffusion **84** is reset by pulsing on reset gate **87** again. The reset level for row B is then read out. TGB is then pulsed on to transfer the signal charge from photodetector B onto the floating diffusion. The signal level is then read out for row B. This procedure is then repeated for the remaining pairs of rows on the device.

In the embodiment as shown if FIG. **8**, the reset drain **88** is separate from the amplifier drain VDD. As shown in FIG. **8**, the reset drain **88** is shared between both adjacent pixels, as is the reset drain contact.

FIG. **9** is a top view of 4 pixels of the present invention illustrating the concept of routing or interconnecting across pixel boundaries. A contact region for the signal transistor is placed to the right side of the floating diffusion and ends at the right side of the pixel boundary **90**. When another pixel is butted to the right side, this completes the connection of the floating diffusion to the signal transistor. This is done similarly with the reset gate using the top and bottom boundaries of the pixel. This concept provides the ability to have minimum routing and interconnect area.

Although not shown in these examples, it is desirable to design the pixel so the photodetector occupies the same site within the pixel even when the pixel is mirrored so the modulation transfer function of the imager is constant throughout the device.

It should be noted that although not shown in the drawings, each of the features detailed in this invention can be used in conjunction with each other to produce other physical layouts and embodiments that provide the advantages discussed.

The invention has been described with reference to a preferred embodiment, however, it will be appreciated that variations and modifications can be effected by a person of ordinary skill in the art without departing from the scope of the invention.

PARTS LIST:

3	row select gate contact 3
4	row select transistor
5	signal transistor
8	output node contact
9	power supply contact (VDDC)
10	prior art pixel
11	photodetector
12	transfer gate
13	transfer gate contact
14	floating diffusion
16	reset gate
17	reset gate contact
30	pixel
31	photodetector
32	transfer gate
33	transfer gate contact
34	floating diffusion
36	reset gate
37	reset gate contact
38	row select gate
39	row select gate contact
40	VDDC
41	OUTC
45	OUTC
46	OUTC
47	OUTC

-continued

48	VDDC
49	VDDC
65	lateral overflow gate
66	lateral overflow drain
80	pixel
81	transfer gate
82	transfer gate
83	reset drain contact
84	floating diffusion
85	amplifier
86	row select transistor
87	reset gate
88	reset drain
90	pixe boundary

What is claimed is:

1. An image sensor having a plurality of pixels comprising:

a semiconductor material of a first conductivity type;

at least two adjacent pixels each of the pixels having photodetectors formed within the substrate; and

at least one electrical function integrated within the adjacent pixels that is shared between the adjacent pixels, wherein the electrical function is an electrical contact that is selected from one of the following components (a photogate contact, a transfer gate contact, a row select gate contact, an output node contact, or an amplifier contact).

2. An image sensor having a plurality of pixels comprising:

a semiconductor material of a first conductivity type; and

at least two adjacent pixels, each of the pixels having a photodetector formed within the substrate with a sense node, an amplifier, row select transistor, and reset transistor are integrated within the adjacent pixels such that they are shared by the adjacent pixels.

3. The image sensor of claim **2** further comprising a contact region formed on at least one of the electrical components that are shared by the adjacent pixels.

4. The image sensor of claim **2** further comprising a contact region formed on each of the adjacent pixels for operation of one of the electrical components that is shared.

5. An image sensor having a plurality of pixels comprising:

a semiconductor material of a first conductivity type;

at least two adjacent pixels having photodetectors formed within the substrate such that each pixel has at least one electrical component integrated within the pixel, and

a contact region that is shared by the electrical components of the adjacent pixels, wherein the electrical contact is selected from one of the following (a photogate contact, a transfer gate contact, a row select gate contact, an amplifier drain contact, or an amplifier contact).

6. The image sensor of claim **5** wherein in addition to sharing the contact region, the electrical component is constructed with at least a portion of the electrical component formed along a common border of the adjacent pixels.

* * * * *

US006310366B1

(12) **United States Patent**
Rhodes et al.

(10) **Patent No.: US 6,310,366 B1**
(45) **Date of Patent: Oct. 30, 2001**

(54) **RETROGRADE WELL STRUCTURE FOR A CMOS IMAGER**

(75) Inventors: **Howard E. Rhodes**; **Mark Durcan**, both of Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/334,261**

(22) Filed: **Jun. 16, 1999**

(51) **Int. Cl.**[7] **H01L 31/062**; H01L 31/12
(52) **U.S. Cl.** **257/185**; 257/431; 257/655
(58) **Field of Search** 257/185, 431, 257/655, 917

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(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin & Oshinsky LLP

(57) **ABSTRACT**

A retrograde well structure for a CMOS imager that improves the quantum efficiency and signal-to-noise ratio of the imager. The retrograde well comprises a doped region with a vertically graded dopant concentration that is lowest at the substrate surface, and highest at the bottom of the well. A single retrograde well may have a single pixel sensor cell, multiple pixel sensor cells, or even an entire array of pixel sensor cells formed therein. The highly concentrated region at the bottom of the retrograde well repels signal carriers from the photosensor so that they are not lost to the substrate, and prevents noise carriers from the substrate from diffusing up into the photosensor. Also disclosed are methods for forming the retrograde well.

45 Claims, 8 Drawing Sheets

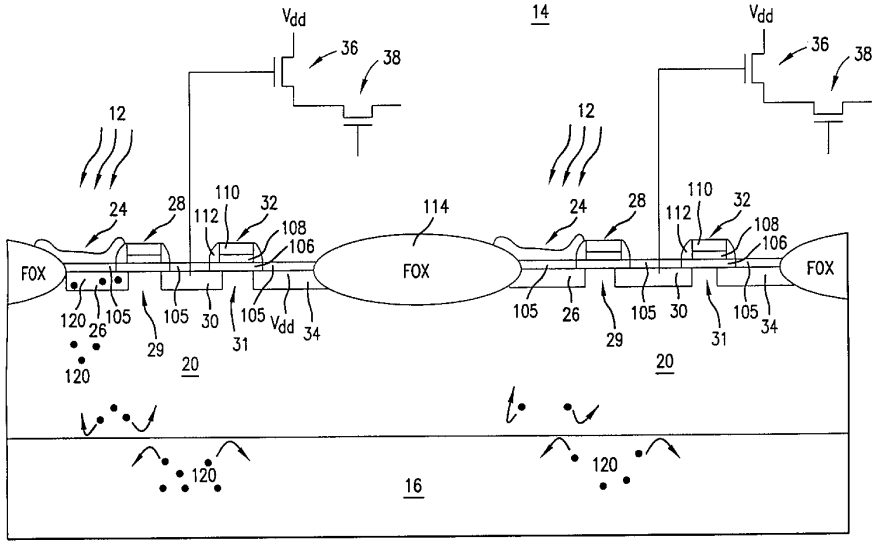

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FIG. 1

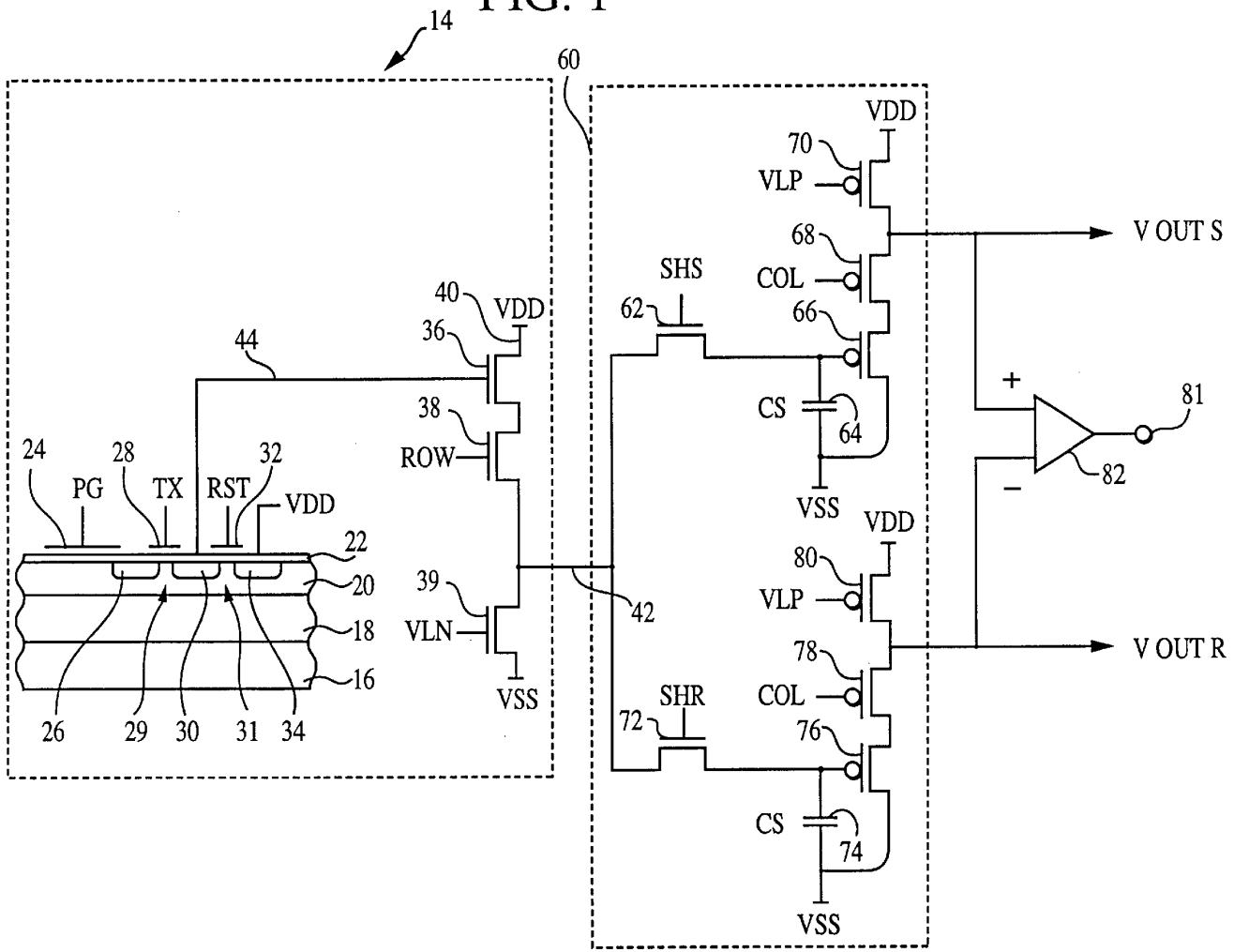

14
60
VDD
70
VLP
68
COL
66
V OUT S
SHS
62
40
VDD
36
44
CS
64
81
38
ROW
+
82
−
24
28
32
PG
TX
RST
VDD
VSS
VDD
22
80
20
VLP
39
42
18
VLN
78
V OUT R
16
SHR
COL
72
76
VSS
CS
74
26
29
30
31
34
VSS

FIG. 2

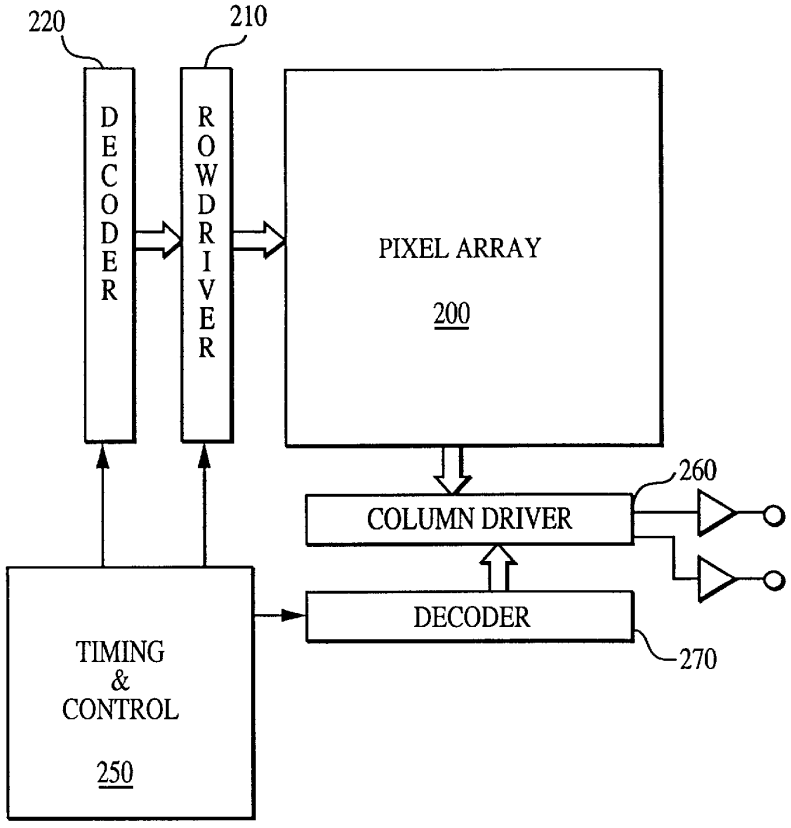

220
210
DECODER
ROW DRIVER
PIXEL ARRAY
200
260
COLUMN DRIVER
DECODER
270
TIMING
&
CONTROL
250

FIG. 3

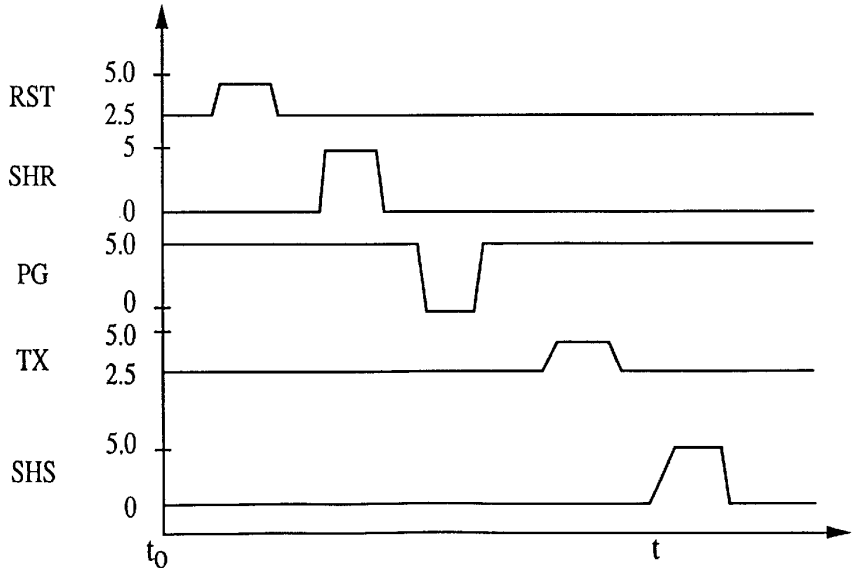
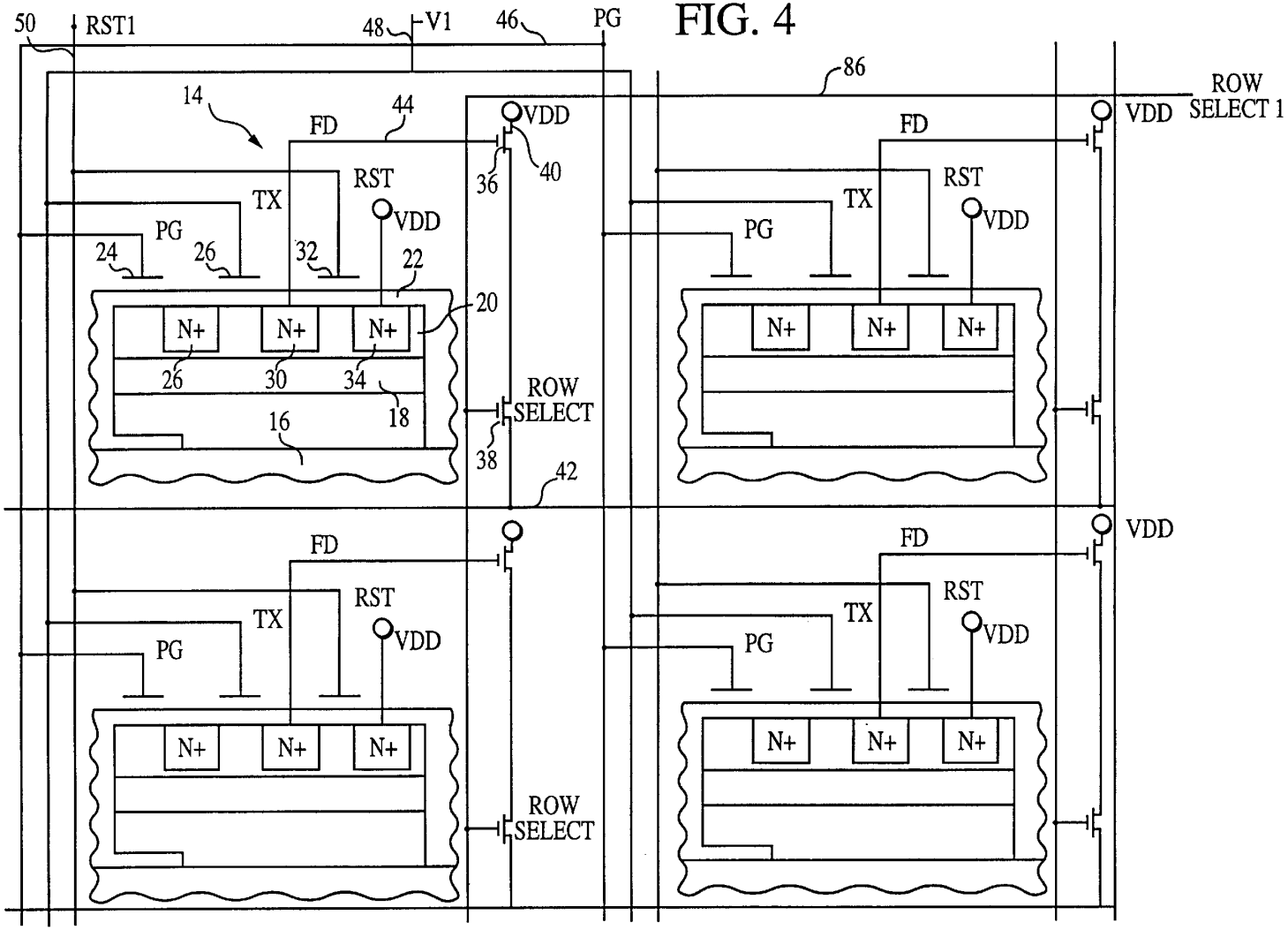

RST
5.0
2.5
SHR
5
0
PG
5.0
0
TX
5.0
2.5
SHS
5.0
0
t_0
t

FIG. 4


50
RST1
48
V1
46
PG
86
ROW SELECT 1
14
FD
44
VDD
36
40
TX
RST
VDD
PG
24
26
32
22
20
N+
N+
N+
26
30
34
18
16
ROW SELECT
38
42
FD
VDD
TX
RST
VDD
PG
N+
N+
N+
ROW SELECT
FD
VDD
TX
RST
VDD
PG
N+
N+
N+
VDD

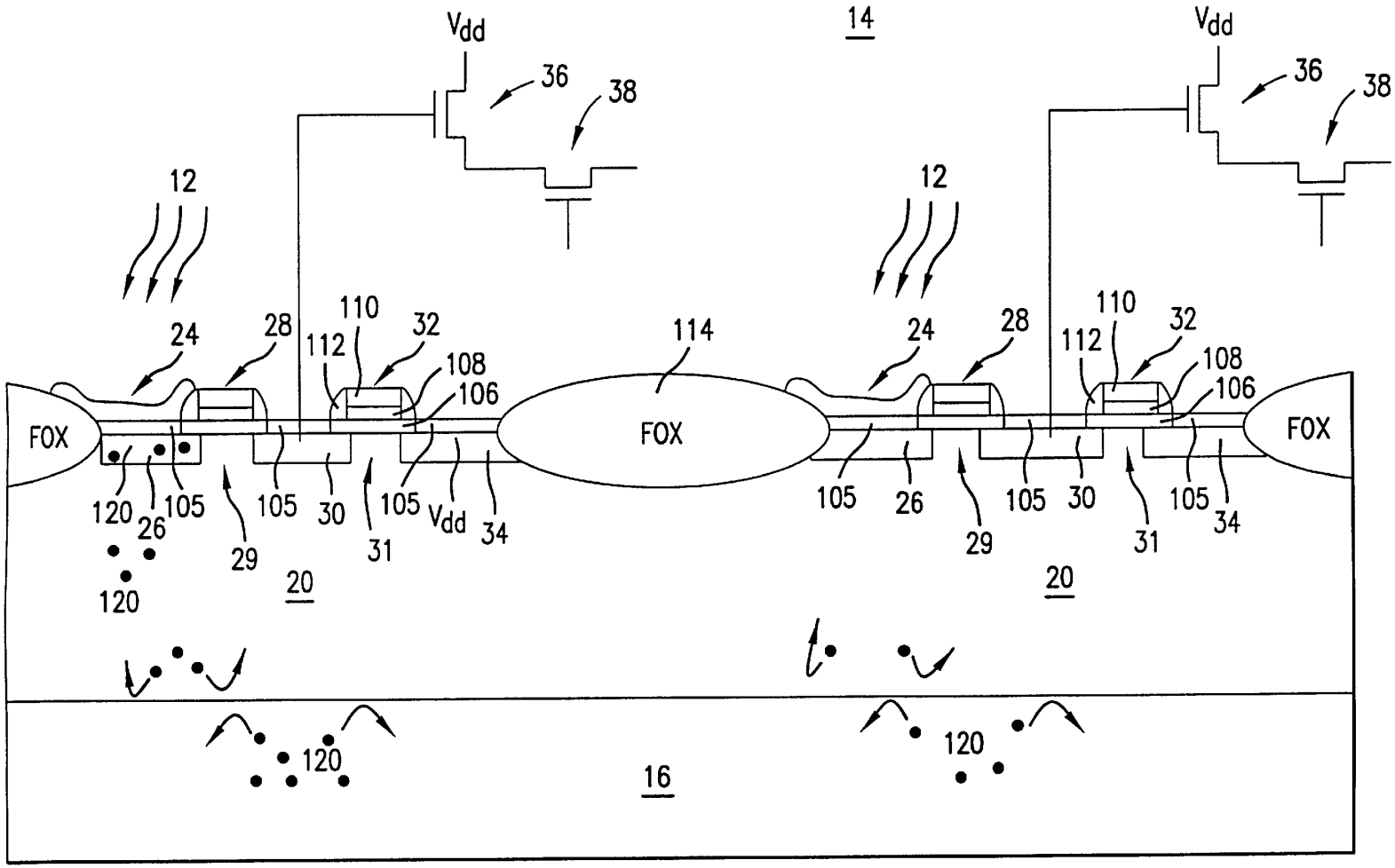

14
Vdd
36
38
12
24
28
110
112
32
108
106
114
FOX
120
26
105
29
30
31
34
20
16

FIG.5

FIG. 6

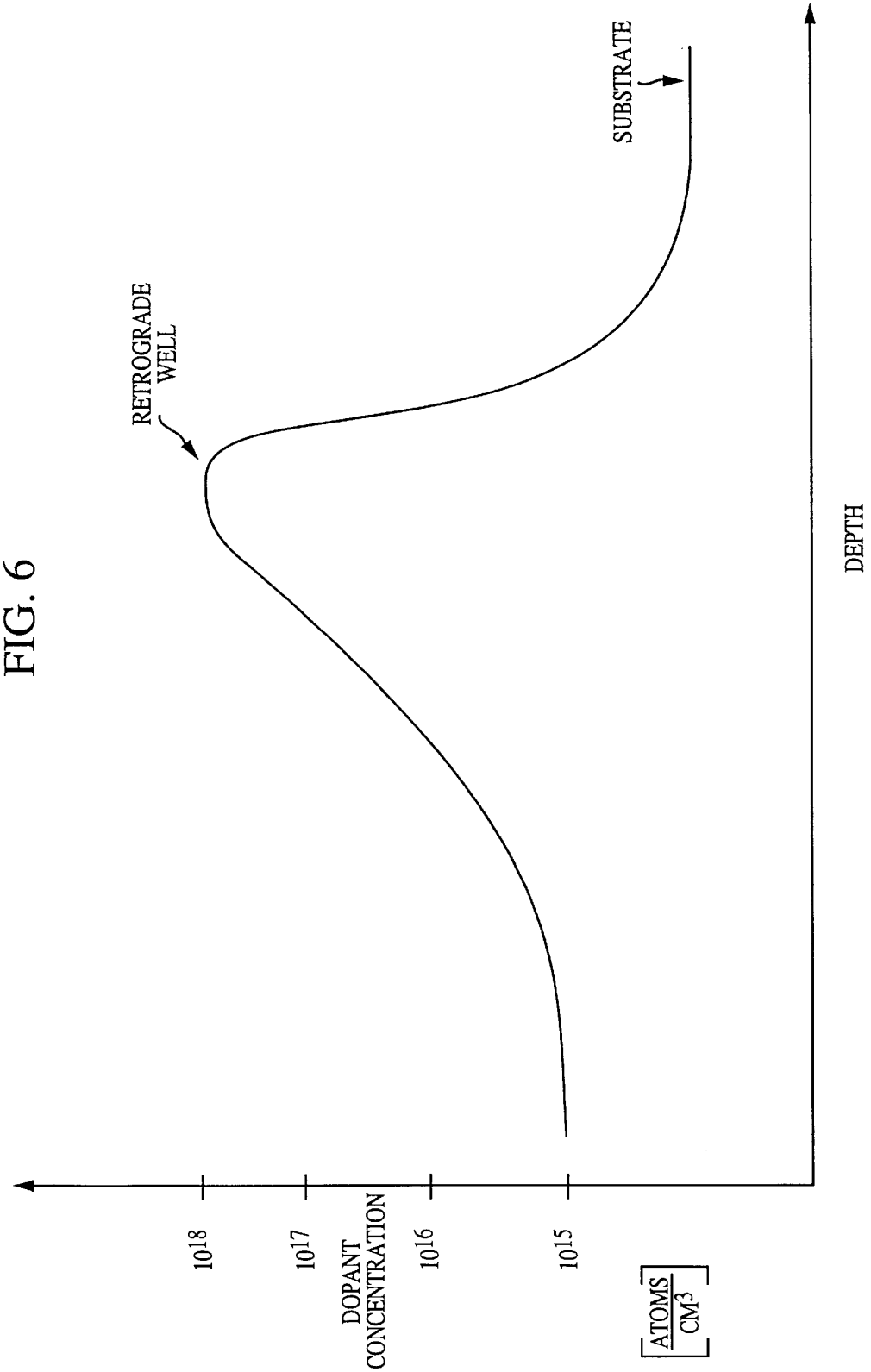

SUBSTRATE
RETROGRADE WELL
DEPTH
DOPANT CONCENTRATION
10^{18}
10^{17}
10^{16}
10^{15}
[ATOMS / CM^3]

FIG. 7

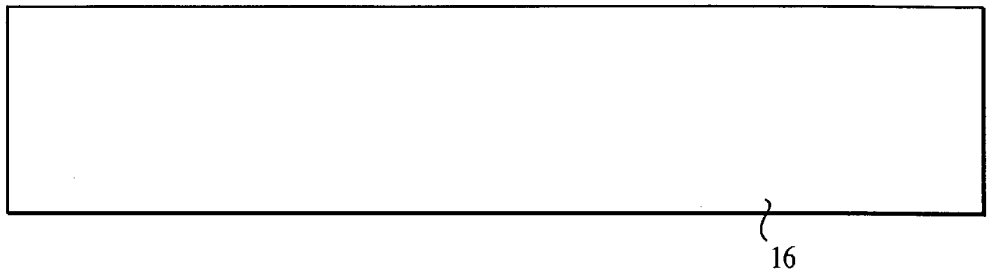


FIG. 8

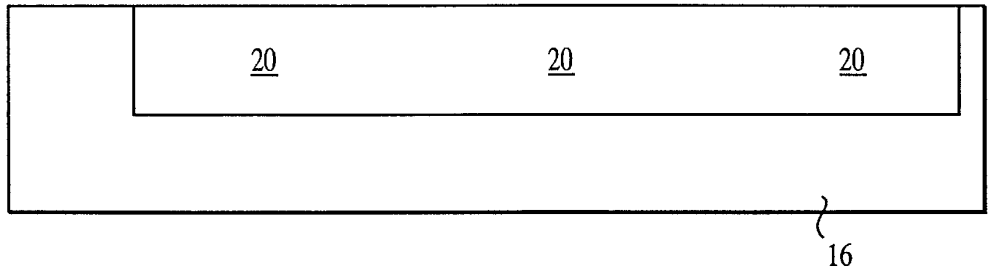


FIG. 9

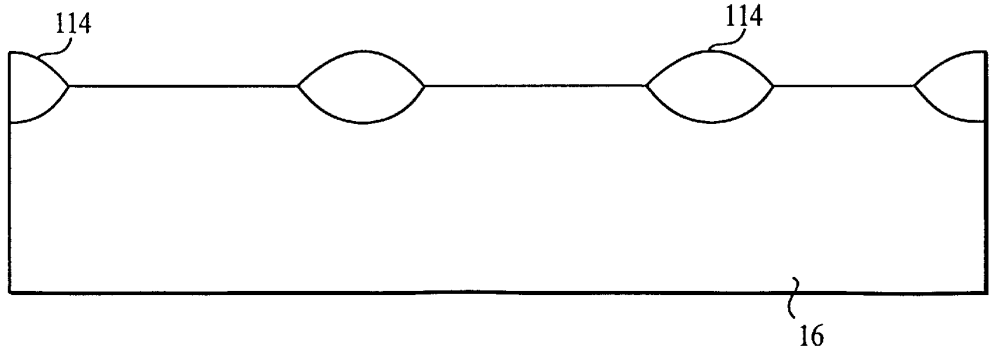


FIG. 10

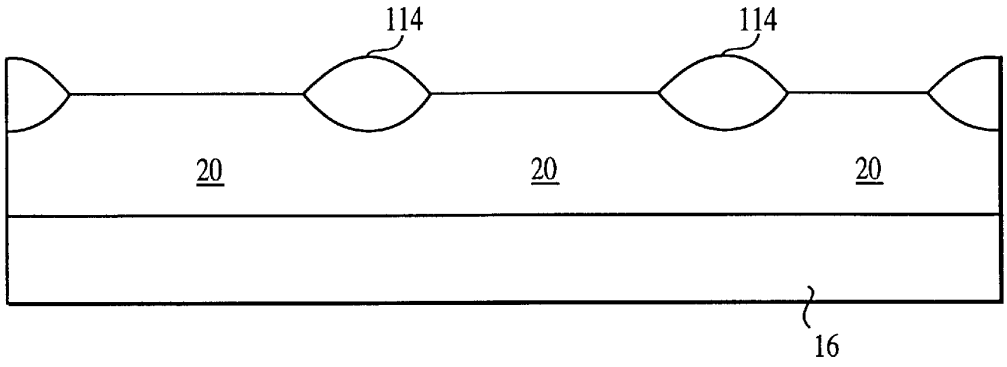
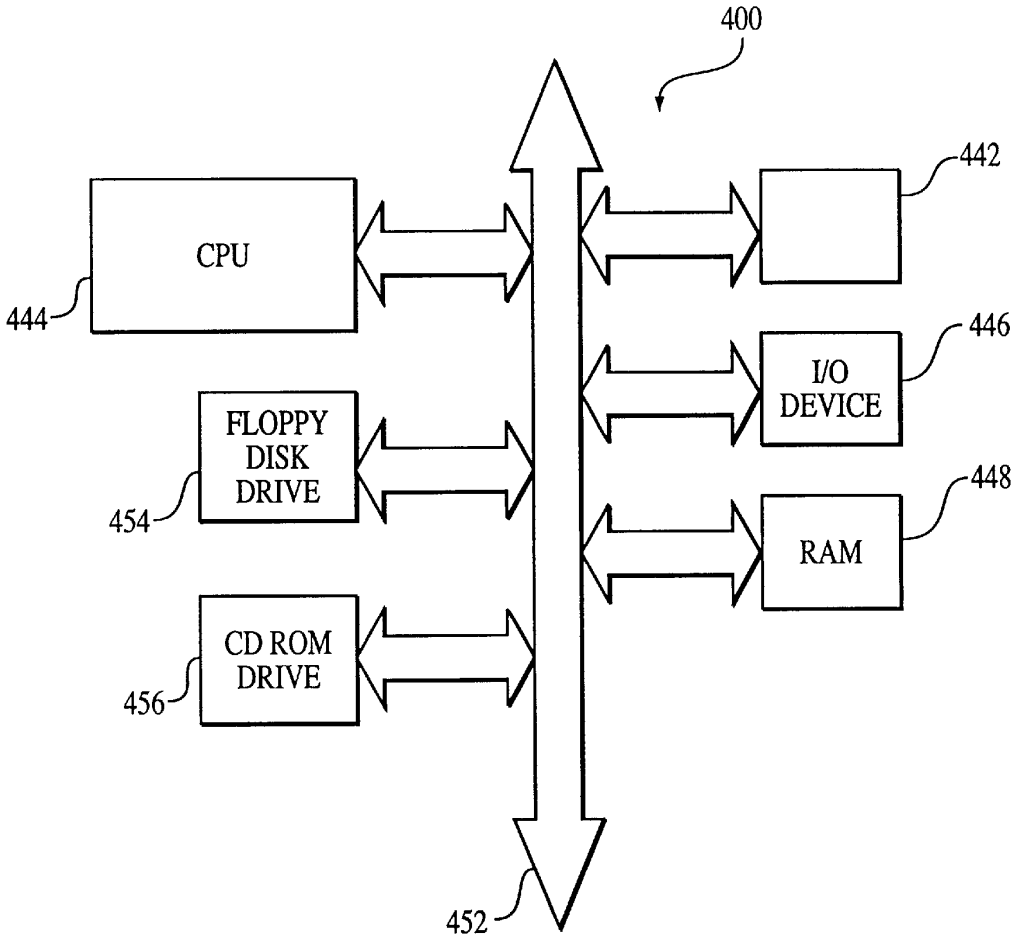


FIG. 11


400
442
CPU
444
446
I/O DEVICE
FLOPPY DISK DRIVE
454
448
RAM
CD ROM DRIVE
456
452

RETROGRADE WELL STRUCTURE FOR A CMOS IMAGER

FIELD OF THE INVENTION

The present invention relates generally to improved semiconductor imaging devices and in particular to a silicon imaging device that can be fabricated using a standard CMOS process.

BACKGROUND OF THE INVENTION

There are a number of different types of semiconductor-based imagers, including charge coupled devices (CCDs), photodiode arrays, charge injection devices and hybrid focal plane arrays. CCD technology is often employed for image acquisition and enjoys a number of advantages which makes it the incumbent technology, particularly for small size imaging applications. CCDs are capable of large formats with small pixel size and they employ low noise charge domain processing techniques.

However, CCD imagers also suffer from a number of disadvantages. For example, they are susceptible to radiation damage, they exhibit destructive read-out over time, they require good light shielding to avoid image smear and they have a high power dissipation for large arrays. Additionally, while offering high performance, CCD arrays are difficult to integrate with CMOS processing in part due to a different processing technology and to their high capacitances, complicating the integration of on-chip drive and signal processing electronics with the CCD array. While there have been some attempts to integrate on-chip signal processing with CCD arrays, these attempts have not been entirely successful. CCDs also must transfer an image by line charge transfers from pixel to pixel, requiring that the entire array be read out into a memory before individual pixels or groups of pixels can be accessed and processed. This takes time. CCDs may also suffer from incomplete charge transfer from pixel to pixel which results in image smear.

Because of the inherent limitations in CCD technology, there is an interest in CMOS imagers for possible use as low cost imaging devices. A fully compatible CMOS sensor technology enabling a higher level of integration of an image array with associated processing circuits would be beneficial to many digital applications such as, for example, in cameras, scanners, machine vision systems, vehicle navigation systems, video telephones, computer input devices, surveillance systems, auto focus systems, star trackers, motion detection systems, image stabilization systems and data compression systems for high-definition television.

The advantages of CMOS imagers over CCD imagers are that CMOS imagers have a low voltage operation and low power consumption; CMOS imagers are compatible with integrated on-chip electronics (control logic and timing, image processing, and signal conditioning such as A/D conversion); CMOS imagers allow random access to the image data; and CMOS imagers have lower fabrication costs as compared with the conventional CCD because standard CMOS processing techniques can be used. Additionally, low power consumption is achieved for CMOS imagers because only one row of pixels at a time needs to be active during the readout and there is no charge transfer (and associated switching) from pixel to pixel during image acquisition. On-chip integration of electronics is particularly advantageous because of the potential to perform many signal conditioning functions in the digital domain (versus analog signal processing) as well as to achieve a reduction in system size and cost.

A CMOS imager circuit includes a focal plane array of pixel cells, each one of the cells including either a photogate, photoconductor or a photodiode overlying a substrate for accumulating photo-generated charge in the underlying portion of the substrate. A readout circuit is connected to each pixel cell and includes at least an output field effect transistor formed in the substrate and a charge transfer section formed on the substrate adjacent the photogate, photoconductor or photodiode having a sensing node, typically a floating diffusion node, connected to the gate of an output transistor. The imager may include at least one electronic device such as a transistor for transferring charge from the underlying portion of the substrate to the floating diffusion node and one device, also typically a transistor, for resetting the node to a predetermined charge level prior to charge transference.

In a CMOS imager, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) transfer of charge to the floating diffusion node accompanied by charge amplification; (4) resetting the floating diffusion node to a known state before the transfer of charge to it; (5) selection of a pixel for readout; and (6) output and amplification of a signal representing pixel charge. Photo charge may be amplified when it moves from the initial charge accumulation region to the floating diffusion node. The charge at the floating diffusion node is typically converted to a pixel output voltage by a source follower output transistor. The photosensitive element of a CMOS imager pixel is typically either a depleted p–n junction photodiode or a field induced depletion region beneath a photogate. For photodiodes, image lag can be eliminated by completely depleting the photodiode upon readout.

CMOS imagers of the type discussed above are generally known as discussed, for example, in Nixon et al., "256×256 CMOS Active Pixel Sensor Camera-on-a-Chip," IEEE Journal of Solid-State Circuits, Vol. 31(12), pp. 2046–2050 (1996); Mendis et al., "CMOS Active Pixel Image Sensors," IEEE Transactions on Electron Devices, Vol. 41(3), pp. 452–453 (1994), as well as U.S. Pat. No. 5,708,263 and U.S. Pat. No. 5,471,515, which are herein incorporated by reference.

To provide context for the invention, an exemplary CMOS imaging circuit is described below with reference to FIG. **1**. The circuit described below, for example, includes a photogate for accumulating photo-generated charge in an underlying portion of the substrate. It should be understood that the CMOS imager may include a photodiode or other image to charge converting device, in lieu of a photogate, as the initial accumulator for photo-generated charge.

Reference is now made to FIG. **1** which shows a simplified circuit for a pixel of an exemplary CMOS imager using a photogate and having a pixel photodetector circuit **14** and a readout circuit **60**. It should be understood that while FIG. **1** shows the circuitry for operation of a single pixel, that in practical use there will be an M×N array of pixels arranged in rows and columns with the pixels of the array accessed using row and column select circuitry, as described in more detail below.

The photodetector circuit **14** is shown in part as a cross-sectional view of a semiconductor substrate **16** typically a p-type silicon, having a surface well of p-type material **20**. An optional layer **18** of p-type material may be used if desired, but is not required. Substrate **16** may be formed of, for example, Si, SiGe, Ge, or GaAs. Typically the entire substrate **16** is p-type doped silicon substrate and may contain a surface p-well **20** (with layer **18** omitted), but

many other options are possible, such as, for example p on p− substrates, p on p+ substrates, p-wells in n-type substrates or the like. The terms wafer or substrate used in the description includes any semiconductor-based structure having an exposed surface in which to form the circuit structure used in the invention. Wafer and substrate are to be understood as including silicon-on-insulator (SOI) technology, silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure or foundation.

An insulating layer **22** such as, for example, silicon dioxide is formed on the upper surface of p-well **20**. The p-type layer may be a p-well formed in substrate **16**. A photogate **24** thin enough to pass radiant energy or of a material which passes radiant energy is formed on the insulating layer **22**. The photogate **24** receives an applied control signal PG which causes the initial accumulation of pixel charges in n+region **26**. The n+type region **26**, adjacent one side of photogate **24**, is formed in the upper surface of p-well **20**. A transfer gate **28** is formed on insulating layer **22** between n+ type region **26** and a second n+ type region **30** formed in p-well **20**. The n+regions **26** and **30** and transfer gate **28** form a charge transfer transistor **29** which is controlled by a transfer signal TX. The n+ region **30** is typically called a floating diffusion region. It is also a node for passing charge accumulated thereat to the gate of a source follower transistor **36** described below.

A reset gate **32** is also formed on insulating layer **22** adjacent and between n+ type region **30** and another n+region **34** which is also formed in p-well **20**. The reset gate **32** and n+ regions **30** and **34** form a reset transistor **31** which is controlled by a reset signal RST. The n+ type region **34** is coupled to voltage source V_{DD}, e.g., 5 volts. The transfer and reset transistors **29**, **31** are n-channel transistors as described in this implementation of a CMOS imager circuit in a p-well. It should be understood that it is possible to implement a CMOS imager in an n-well in which case each of the transistors would be p-channel transistors. It should also be noted that while FIG. **1** shows the use of a transfer gate **28** and associated transistor **29**, this structure provides advantages, but is not required.

Photodetector circuit **14** also includes two additional n-channel transistors, source follower transistor **36** and row select transistor **38**. Transistors **36**, **38** are coupled in series, source to drain, with the source of transistor **36** also coupled over lead **40** to voltage source V_{DD} and the drain of transistor **38** coupled to a lead **42**. The drain of row select transistor **38** is connected via conductor **42** to the drains of similar row select transistors for other pixels in a given pixel row. A load transistor **39** is also coupled between the drain of transistor **38** and a voltage source V_{SS}, e.g. 0 volts. Transistor **39** is kept on by a signal V_{LN} applied to its gate.

The imager includes a readout circuit **60** which includes a signal sample and hold (S/H) circuit including a S/H n-channel field effect transistor **62** and a signal storage capacitor **64** connected to the source follower transistor **36** through row transistor **38**. The other side of the capacitor **64** is connected to a source voltage V_{SS}. The upper side of the capacitor **64** is also connected to the gate of a p-channel output transistor **66**. The drain of the output transistor **66** is connected through a column select transistor **68** to a signal sample output node V_{OUTS} and through a load transistor **70** to the voltage supply V_{DD}. A signal called "signal sample and hold" (SHS) briefly turns on the S/H transistor **62** after the charge accumulated beneath the photogate electrode **24** has been transferred to the floating diffusion node **30** and from there to the source follower transistor **36** and through row select transistor **38** to line **42**, so that the capacitor **64** stores a voltage representing the amount of charge previously accumulated beneath the photogate electrode **24**.

The readout circuit **60** also includes a reset sample and hold (S/H) circuit including a S/H transistor **72** and a signal storage capacitor **74** connected through the S/H transistor **72** and through the row select transistor **38** to the source of the source follower transistor **36**. The other side of the capacitor **74** is connected to the source voltage V_{SS}. The upper side of the capacitor **74** is also connected to the gate of a p-channel output transistor **76**. The drain of the output transistor **76** is connected through a p-channel column select transistor **78** to a reset sample output node V_{OUTR} and through a load transistor **80** to the supply voltage V_{DD}. A signal called "reset sample and hold" (SHR) briefly turns on the S/H transistor **72** immediately after the reset signal RST has caused reset transistor **31** to turn on and reset the potential of the floating diffusion node **30**, so that the capacitor **74** stores the voltage to which the floating diffusion node has been reset.

The readout circuit **60** provides correlated sampling of the potential of the floating diffusion node **30**, first of the reset charge applied to node **30** by reset transistor **31** and then of the stored charge from the photogate **24**. The two samplings of the diffusion node **30** charges produce respective output voltages V_{OUTR} and V_{OUTS} of the readout circuit **60**. These voltages are then subtracted (V_{OUTS}−V_{OUTR}) by subtractor **82** to provide an output signal terminal **81** which is an image signal independent of pixel to pixel variations caused by fabrication variations in the reset voltage transistor **31** which might cause pixel to pixel variations in the output signal.

FIG. **2** illustrates a block diagram for a CMOS imager having a pixel array **200** with each pixel cell being constructed in the manner shown by element **14** of FIG. **1**. FIG. **4** shows a 2×2 portion of pixel array **200**. Pixel array **200** comprises a plurality of pixels arranged in a predetermined number of columns and rows. The pixels of each row in array **200** are all turned on at the same time by a row select line, e.g., line **86**, and the pixels of each column are selectively output by a column select line, e.g., line **42**. A plurality of rows and column lines are provided for the entire array **200**. The row lines are selectively activated by the row driver **210** in response to row address decoder **220** and the column select lines are selectively activated by the column driver **260** in response to column address decoder **270**. Thus, a row and column address is provided for each pixel. The CMOS imager is operated by the control circuit **250** which controls address decoders **220**, **270** for selecting the appropriate row and column lines for pixel readout, and row and column driver circuitry **210**,**260** which apply driving voltage to the drive transistors of the selected row and column lines.

FIG. **3** shows a simplified timing diagram for the signals used to transfer charge out of photodetector circuit **14** of the FIG. **1** CMOS imager. The photogate signal PG is nominally set to 5V and pulsed from 5V to 0V during integration. The reset signal RST is nominally set at 2.5V. As can be seen from the figure, the process is begun at time t_0 by briefly pulsing reset voltage RST to 5V. The RST voltage, which is applied to the gate **32** of reset transistor **31**, causes transistor **31** to turn on and the floating diffusion node **30** to charge to the V_{DD} voltage present at n+ region **34** (less the voltage drop V_{TH} of transistor **31**). This resets the floating diffusion node **30** to a predetermined voltage (V_{DD}−V_{TH}). The charge

on floating diffusion node **30** is applied to the gate of the source follower transistor **36** to control the current passing through transistor **38**, which has been turned on by a row select (ROW) signal, and load transistor **39**. This current is translated into a voltage on line **42** which is next sampled by providing a SHR signal to the S/H transistor **72** which charges capacitor **74** with the source follower transistor output voltage on line **42** representing the reset charge present at floating diffusion node **30**. The PG signal is next pulsed to 0 volts, causing charge to be collected in n+ region **26**.

A transfer gate voltage TX, similar to the reset pulse RST, is then applied to transfer gate **28** of transistor **29** to cause the charge in n+ region **26** to transfer to floating diffusion node **30**. It should be understood that for the case of a photogate, the transfer gate voltage TX may be pulsed or held to a fixed DC potential. For the implementation of a photodiode with a transfer gate, the transfer gate voltage TX must be pulsed. The new output voltage on line **42** generated by source follower transistor **36** current is then sampled onto capacitor **64** by enabling the sample and hold switch **62** by signal SHS. The column select signal is next applied to transistors **68** and **70** and the respective charges stored in capacitors **64** and **74** are subtracted in subtractor **82** to provide a pixel output signal at terminal **81**. It should also be noted that CMOS imagers may dispense with the transfer gate **28** and associated transistor **29**, or retain these structures while biasing the transfer transistor **29** to an always "on" state.

The operation of the charge collection of the CMOS imager is known in the art and is described in several publications such as Mendis et al., "Progress in CMOS Active Pixel Image Sensors," SPIE Vol. 2172, pp. 19–29 (1994); Mendis et al., "CMOS Active Pixel Image Sensors for Highly Integrated Imaging Systems," IEEE Journal of Solid State Circuits, Vol. 32(2) (1997); and Eric K Fossum, "CMOS Image Sensors: Electronic Camera on a Chip," IEDM Vol. 95, pp. 17–25 (1995) as well as other publications. These references are incorporated herein by reference.

Quantum efficiency is a problem in some imager applications due to the diffusion of signal carriers out of the photosite and into the substrate, where they become effectively lost. The loss of signal carriers results in decreased signal strength, increased cross talk, and the reading of an improper value for the adjacent pixels.

There is needed, therefore, an improved pixel sensor cell for use in an imager that exhibits improved quantum efficiency, a better signal-to-noise ratio, and reduced cross talk. A method of fabricating a pixel sensor cell exhibiting these improvements is also needed.

SUMMARY OF THE INVENTION

The present invention provides a pixel sensor cell formed in a retrograde well in a semiconductor substrate having improved quantum efficiency, an improved signal-to-noise ratio, and reduced cross talk. The retrograde well comprises a doped region with a vertically graded dopant concentration that is lowest at the substrate surface, and highest at the bottom of the well. The retrograde well would have an entire array of pixels formed therein, and may also have peripheral circuitry formed therein. If the peripheral circuitry is formed in the retrograde well, the well may have a different dopant profile in the peripheral region than in the array region. The highly concentrated region at the bottom of the retrograde well reflects signal carriers back to the photosensor so that they are not lost to the substrate. Also provided are methods for forming a pixel sensor cell in the retrograde well of the present invention.

Additional advantages and features of the present invention will be apparent from the following detailed description and drawings which illustrate preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a representative circuit of a CMOS imager.

FIG. **2** is a block diagram of a CMOS pixel sensor chip.

FIG. **3** is a representative timing diagram for the CMOS imager.

FIG. **4** is a representative pixel layout showing a 2×2 pixel layout.

FIG. **5** is a cross-sectional view of two pixel sensor cells according to an embodiment of the present invention.

FIG. **6** is a graph depicting the dopant concentration as a function of the depth of the retrograde well.

FIG. **7** is a cross-sectional view of a semiconductor wafer undergoing the process of a preferred embodiment of the invention.

FIG. **8** shows the wafer of FIG. **7** at a processing step subsequent to that shown in FIG. **7**.

FIG. **9** is a cross-sectional view of a semiconductor wafer undergoing the process of a second embodiment of the invention.

FIG. **10** shows the wafer of FIG. **9** at a processing step subsequent to that shown in FIG. **9**.

FIG. **11** is an illustration of a computer system having a CMOS imager according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention.

The terms "wafer" and "substrate" are to be understood as including silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous process steps may have been utilized to form regions or junctions in the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, germanium, or gallium arsenide. For exemplary purposes an imager formed of n-channel devices in a retrograde p-well is illustrated and described, but it should be understood that the invention is not limited thereto, and may include other combinations such as an imager formed of p-channel devices in a retrograde n-well.

The term "pixel" refers to a picture element unit cell containing a photosensor and transistors for converting electromagnetic radiation to an electrical signal. For purposes of illustration, a representative pixel is illustrated in the figures and description herein, and typically fabrication

of all pixels in an imager will proceed simultaneously in a similar fashion. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

The structure of pixel cells **14** formed in retrograde wells **20** of the first embodiment are shown in more detail in FIG. **5**. A pixel cell **14** may be formed in a substrate **16** having a retrograde layer or well **20** of a first conductivity type, which for exemplary purposes is treated as p-type. The retrograde well **20** has a vertically graded dopant concentration that is lowest at the substrate surface, and highest at the bottom of the well, as is shown in FIG. **6**. The dopant concentration at the top of the retrograde well **20** is within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3, and is preferably within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3, and most preferably is about 5×10^{15} atoms per cm^3. At the bottom of the retrograde well **20**, the dopant concentration is within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3, and is preferably within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3, and most preferably is about 3×10^{17} atoms per cm^3. A single retrograde well **20** as depicted in FIG. **5**, spans all pixels in the array of pixels.

A second retrograde well (not shown) may be formed in the substrate **16**, and may have peripheral circuitry, such as, e.g., logic circuitry, formed therein. This second well may be doped similarly or differently from the first retrograde well **20**, for example, the first retrograde well **20** may be doped to a first dopant level such as about 3×10^{17} atoms per cm^3 at the bottom of the well and the second well may be doped to a second dopant level such as 5×10^{16} at the bottom of the well.

The transistor gates form the pixel cell **14** as shown: a photogate **24**, a transfer gate **28** for transfer transistor **29**, and a reset transistor gate **32** for the reset transistor **31**. In addition, the photosensitive element in the pixel cell **14** is shown to be a photogate **24**, but other photosensitive elements such as a photodiode or a photoconductor could be used. The source follower transistor and the row select transistor are not shown. The transfer gate **28** and the reset gate **32** include a gate oxide layer **106** on the retrograde well **20**, and a conductive layer **108** of doped polysilicon, tungsten, or other suitable material over the gate oxide layer **106**. An insulating cap layer **110** of, for example, silicon dioxide, silicon nitride, or ONO (oxide-nitride-oxide), may be formed if desired; also a more conductive layer such as a silicide layer (not shown) may be used between the conductive layer **108** and the cap **110** of the transfer gate stack **28**, source follower gate, row select gate, and reset gate stack **32**, if desired. Insulating sidewalls **112** are also formed on the sides of the gate stacks **28**, **32**. These sidewalls may be formed of, for example, silicon dioxide or silicon nitride or ONO. The transfer gate is not required but may advantageously be included. The photogate **24** is a semitransparent conductor and is shown as an overlapping gate. In this case there is a second gate oxide **105** over the retrograde well and under the photogate.

Underlying the photogate **24** is a doped region **26** called the photosite, where photogenerated charges are stored. In between the reset transistor gate **32** and the transfer gate **28** is a doped region **30** that is the source for the reset transistor **31**, and on the other side of the reset transistor gate **32** is a doped region **34** that acts as a drain for the reset transistor **31**. The doped regions **26**, **30**, **34** are doped to a second conductivity type, which for exemplary purposes is treated as n-type. The second doped region **30** is the floating diffusion region, sometimes also referred to as a floating diffusion node, and it serves as the source for the reset transistor **31**. The third doped region **34** is the drain of the reset transistor **31**, and is also connected to voltage source Vdd.

As shown in FIG. **5**, as light radiation **12** in the form of photons strikes the photosite **26**, photo-energy is converted to electrical signals, i.e., carriers **120**, which are stored in the photosite **26**. The absorption of light creates electron-hole pairs. For the case of an n-doped photosite in a p-well, it is the electrons that are stored. For the case of a p-doped photosite in an n-well, it is the holes that are stored. In the exemplary pixel cell **14** having n-channel devices formed in a p-type retrograde well **20**, the carriers **120** stored in the photosite **26** are electrons. The retrograde well **20** acts to reduce carrier loss to the substrate **16** by forming a concentration gradient that modifies the band diagram and serves to reflect electrons back towards the photosite **26**, thereby increasing quantum efficiency of the pixel **14**.

The retrograde well **20** is manufactured through a process described as follows, and illustrated by FIGS. **7** and **8**. Referring now to FIG. **7**, a substrate **16**, which may be any of the types of substrates described above, is provided. Retrograde well **20** is then formed by suitable means such as blanket ion implantation of the entire wafer. The retrograde well **20** may be implanted at a later stage of the process such as after field oxide formation. The implant may be patterned so that the array well and the periphery logic well could have different doping profiles.

Ion implantation is performed by placing the substrate **16** in an ion implanter, and implanting appropriate dopant ions into the substrate **16** at an energy of 100 keV to 5 MeV to form retrograde wells **20** having a dopant concentration that is lowest at the surface, and highest at the bottom of the well. The dopant concentration at the top of the retrograde well **20** is within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3, and is preferably within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3, and most preferably is about 5×10^{15} atoms per cm^3. At the bottom of the retrograde well **20**, the dopant concentration is within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3, and is preferably within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3, and most preferably is about 3×10^{17} atoms per cm^3. If the retrograde well is to be a p-type well, a p-type dopant, such as boron, is implanted, and if the well **20** is to be an n-type well, an n-type dopant, such as arsenic, antimony, or phosphorous is implanted. The resultant structure is shown in FIG. **8**. Multiple high energy implants may be used to tailor the profile of the retrograde well **20**.

Referring now to FIGS. **9** and **10**, field oxide regions **114** may be formed around the pixel cell **14** prior to the formation of the retrograde well **20**. The field oxide regions are formed by any known technique such as thermal oxidation of the underlying silicon in a LOCOS process or by etching trenches and filling them with oxide in an STI process. Following field oxide **114** formation, the retrograde wells **20** may then be formed by blanket implantation as shown in FIG. **10** or by masked implantation (not shown).

Subsequent to formation of the retrograde well **20**, the devices of the pixel sensor cell **14**, including the photogate **24**, the transfer gate **28**, reset transistor **31**, the source follower **36** and the row select transistor **38** are formed by well-known methods. Doped regions **26**, **30**, and **34** are formed in the retrograde well **20**, and are doped to a second conductivity type, which for exemplary purposes will be considered to be n-type. The doping level of the doped regions **26**, **30**, **34** may vary but should be higher than the doping level at the top of the retrograde well **20**, and greater

than 5×10^{16} atoms per cm^3. If desired, multiple masks and resists may be used to dope these regions to different levels. Doped region **26** may be variably doped, such as either n+ or n− for an n-channel device. Doped region **34** should be strongly doped, i.e., for an n-channel device, the doped region **34** will be doped as n+. Doped region **30** is typically strongly doped (n+), and would not be lightly doped (n−) unless a buried contact is also used.

The pixel sensor cell **14** is essentially complete at this stage, and conventional processing methods may be used to form contacts and wiring to connect gate lines and other connections in the pixel cell **14**. For example, the entire surface may then be covered with a passivation layer of, e.g., silicon dioxide, BSG, PSG, or BPSG, which is CMP planarized and etched to provide contact holes, which are then metallized to provide contacts to the photogate, reset gate, and transfer gate. Conventional multiple layers of conductors and insulators may also be used to interconnect the structures in the manner shown in FIG. **1**.

A typical processor based system which includes a CMOS imager device according to the present invention is illustrated generally at **400** in FIG. **11**. A processor based system is exemplary of a system having digital circuits which could include CMOS imager devices. Without being limiting, such a system could include a computer system, camera system, scanner, machine vision system, vehicle navigation system, video telephone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system and data compression system for high-definition television, all of which can utilize the present invention.

A processor system, such as a computer system, for example generally comprises a central processing unit (CPU) **444**, e.g., a microprocessor, that communicates with an input/output (I/O) device **446** over a bus **452**. The CMOS imager **442** also communicates with the system over bus **452**. The computer system **400** also includes random access memory (RAM) **448**, and, in the case of a computer system may include peripheral devices such as a floppy disk drive **454** and a compact disk (CD) ROM drive **456** which also communicate with CPU **444** over the bus **452**. CMOS imager **442** is preferably constructed as an integrated circuit which includes pixels containing a photosensor such as a photogate or photodiode formed in a retrograde well, as previously described with respect to FIGS. **5** through **10**. The CMOS imager **442** may be combined with a processor, such as a CPU, digital signal processor or microprocessor, with or without memory storage in a single integrated circuit, or may be on a different chip than the processor.

As can be seen by the embodiments described herein, the present invention encompasses a pixel sensor cell formed in a retrograde well. The pixel sensor cell has improved quantum efficiency and an improved signal-to-noise ratio due to the presence of a doping gradient induced electric field created in the bottom of the retrograde well which reflects signal carriers back to the photosensitive node. By reflecting photogenerated carriers back to the storage node the retrograde p-well also reduces the number of carriers diffusing to adjacent pixels and so also reduces cross talk.

It should again be noted that although the invention has been described with specific reference to CMOS imaging circuits having a photogate and a floating diffusion region, the invention has broader applicability and may be used in any CMOS imaging apparatus. Similarly, the process described above is but one method of many that could be used. The above description and drawings illustrate preferred embodiments which achieve the objects, features and advantages of the present invention. It is not intended that the present invention be limited to the illustrated embodiments. Any modification of the present invention which comes within the spirit and scope of the following claims should be considered part of the present invention.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A CMOS imager comprising:

a substrate having at least one retrograde well of a first conductivity type, wherein said at least one retrograde well has a vertically graded dopant of said first conductivity type between a bottom of said at least one retrograde well having a highest concentration of said dopant of said first conductivity type and a top of said at least one retrograde well;

an array of pixel sensor cells formed in said at least one retrograde well, wherein each pixel sensor cell has a photosensor; and

a circuit electrically connected to receive and process output signals from said array.

2. The CMOS imager of claim **1**, wherein said CMOS imager comprises a single retrograde well.

3. The CMOS imager of claim **1**, wherein said at least one retrograde well comprises a plurality of retrograde wells, wherein said array is formed in a first retrograde well of said plurality and said circuit is formed in a second retrograde well of said plurality.

4. The CMOS imager of claim **3**, wherein said first retrograde well is doped to a first dopant level, and said second retrograde well is doped to a second dopant level.

5. The CMOS imager of claim **1**, wherein each pixel sensor further comprises a floating diffusion region of a second conductivity type located in said at least one retrograde well.

6. The CMOS imager of claim **5**, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

7. The CMOS imager of claim **6**, wherein said at least one retrograde well is doped with boron.

8. The CMOS imager of claim **5**, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

9. The CMOS imager of claim **8**, wherein said at least one retrograde well is doped with a dopant selected from the group consisting of arsenic, antimony, and phosphorous.

10. The CMOS imager of claim **1**, wherein each pixel sensor cell further comprises a transfer gate located between said photosensor and a floating diffusion region.

11. The CMOS imager of claim **10**, wherein the photosensors are photogate sensors.

12. The CMOS imager of claim **1**, wherein said at least one retrograde well has a dopant concentration within a range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of said at least one retrograde well.

13. The CMOS imager of claim **12**, wherein said at least one retrograde well has a dopant concentration within a range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of said at least one retrograde well.

14. The CMOS imager of claim **1**, wherein said at least one retrograde well has a dopant concentration within a range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of said at least one retrograde well.

15. The CMOS imager of claim **14**, wherein said at least one retrograde well has a dopant concentration within a range of about 1×10^{15} to about 5×10^{16} atoms per cm^3 at the top of said at least one retrograde well.

16. The CMOS imager of claim **1**, wherein said at least one retrograde well has a dopant concentration of about

3×10^{17} atoms per cm^3 at the bottom of said at least one retrograde well.

17. The CMOS imager of claim **16**, wherein said at least one retrograde well has a dopant concentration of about 5×10^{15} atoms per cm^3 at the top of said at least one retrograde well.

18. The CMOS imager of claim **1**, wherein the photosensors are photodiode sensors.

19. The CMOS imager of claim **1**, wherein the photosensors are photoconductor sensors.

20. An imager comprising:

an array of pixel sensor cells formed in a substrate having at least one retrograde well of a first conductivity type, wherein each pixel sensor cell has a photosensor and said at least one retrograde well comprises a dopant of said first conductivity type which is at a highest concentration at a bottom of said at least one retrograde well;

a circuit formed in the substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing the image; and

a processor for receiving and processing data representing the image.

21. The imager of claim **20**, wherein said array, said circuit, and said processor are formed on a single substrate.

22. The imager of claim **20**, wherein said array and said circuit are formed on a first substrate, and said processor is formed on a second substrate.

23. The imager of claim **20**, wherein said imager comprises a single retrograde well.

24. The imager of claim **20**, wherein said at least one retrograde well comprises a plurality of retrograde wells, wherein said array is formed in a first retrograde well of said plurality and said circuit is formed in a second retrograde well of said plurality.

25. The imager of claim **24**, wherein said first retrograde well is doped to a first dopant level, and said second retrograde well is doped to a second dopant level.

26. The imager of claim **20**, wherein each pixel sensor cell further comprises a floating diffusion region of a second conductivity type located in said at least one retrograde well.

27. The imager of claim **26**, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

28. The imager of claim **26**, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

29. The imager of claim **20**, wherein each pixel sensor cell further comprises a transfer gate located between said photosensor and a floating diffusion region.

30. The imager of claim **29**, wherein the photosensors are photogate sensors.

31. The imager of claim **20**, wherein said at least one retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of said at least one retrograde well, and within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of said at least one retrograde well.

32. The imager of claim **20**, wherein said at least one retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of said at least one retrograde well, and within the range of about 1×10^{15} to about 5×10^{16} atoms per cm^3 at the top of said at least one retrograde well.

33. The imager of claim **20**, wherein said at least one retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3at the bottom of said at least one retrograde well, and about 5×10^{15} atoms per cm^3 at the top of said at least one retrograde well.

34. The imager of claim **20**, wherein the photosensors are photodiode sensors.

35. The imager of claim **20**, wherein the photosensors are photoconductor sensors.

36. An imager comprising:

a CMOS imager comprising

an array of pixel sensor cells formed in a retrograde well defined by a dopant of a first conductivity type on a substrate having a second conductivity type, wherein each pixel sensor cell has a photosensitive region, a photosensor formed on the photosensitive region, and a floating diffusion region for receiving and outputting image charge received from the photosensitive region, and wherein said retrograde well has a vertical profile having a greatest concentration of said dopant of said first conductivity type at a bottom of said retrograde well and said concentration diminishes toward a top of said retrograde well;

a circuit formed in the substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing the image; and

a processor for receiving and processing data representing the image.

37. The imager of claim **36**, wherein said CMOS imager and said processor are formed on a single substrate.

38. The imager of claim **36**, wherein said CMOS imager is formed on a first substrate, and said processor is formed on a second substrate.

39. The imager of claim **36**, wherein the retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of the retrograde well.

40. The imager of claim **39**, wherein the retrograde well has a dopant concentration within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of the retrograde well.

41. The imager of claim **36**, wherein the retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of the retrograde well.

42. The imager of claim **41**, wherein the retrograde well has a dopant concentration within the range of about 1×10^{15} to 5×10^{16} atoms per cm^3 at the top of the retrograde well.

43. The imager of claim **36**, wherein the retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of the retrograde well.

44. The imager of claim **43**, wherein the retrograde well has a dopant concentration of about 5×10^{15} atoms per cm^3 at the top of the retrograde well.

45. The imager of claim **36**, wherein the retrograde well is a first retrograde well, and said circuit is formed in a second retrograde well.

* * * * *

US006794677B2

(12) **United States Patent**
Tamaki et al.

(10) **Patent No.: US 6,794,677 B2**
(45) **Date of Patent: Sep. 21, 2004**

(54) **SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD FOR FABRICATING THE SAME**

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(73) Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 168 days.

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(22) Filed: **Sep. 28, 2001**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**[7] **H01L 29/06**; H01L 31/0352

(52) **U.S. Cl.** **257/41**; 257/2; 257/390; 257/401

(58) **Field of Search** 257/41, 2, 202–211, 257/390, 401

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Primary Examiner—Duy-Vu Deo
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

Variations in the size of a linear pattern resulting from difference in mask pattern layout are prevented by setting the perimeter of the linear pattern per unit area in a specified range irrespective of the type of a semiconductor integrated circuit device or by adjusting a process condition in accordance with type-to-type difference in the perimeter of the linear pattern per unit area.

6 Claims, 9 Drawing Sheets

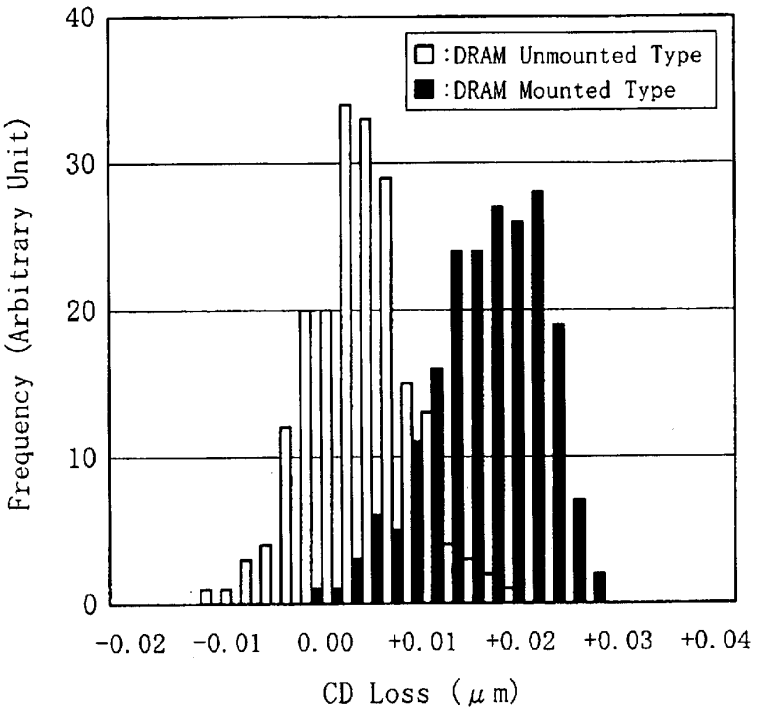


FIG. 1

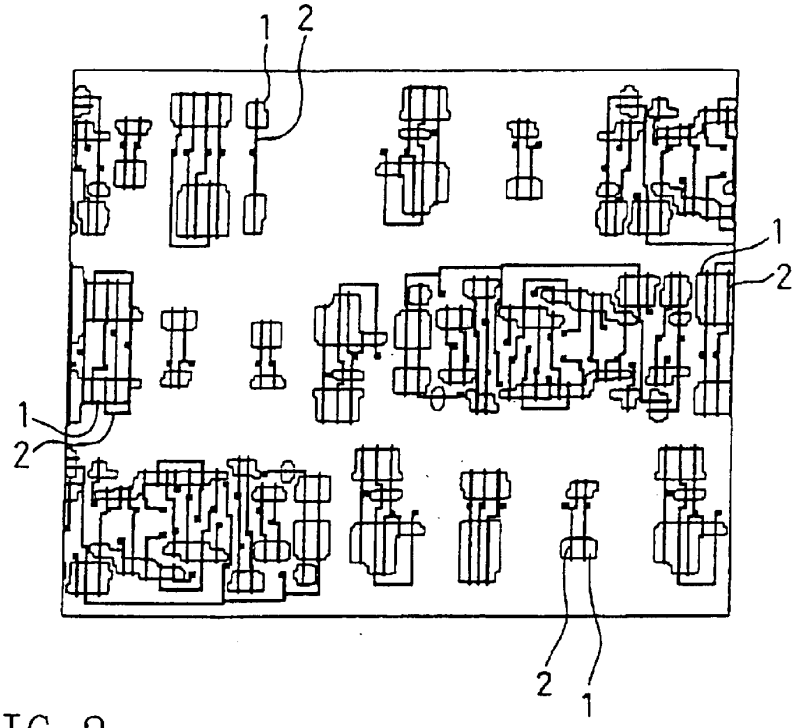


FIG. 2

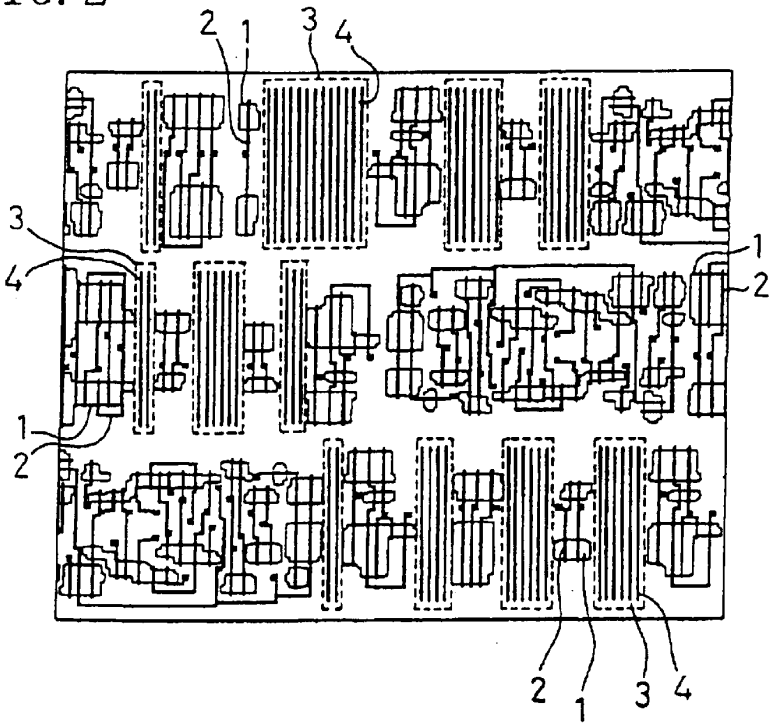


FIG. 3A

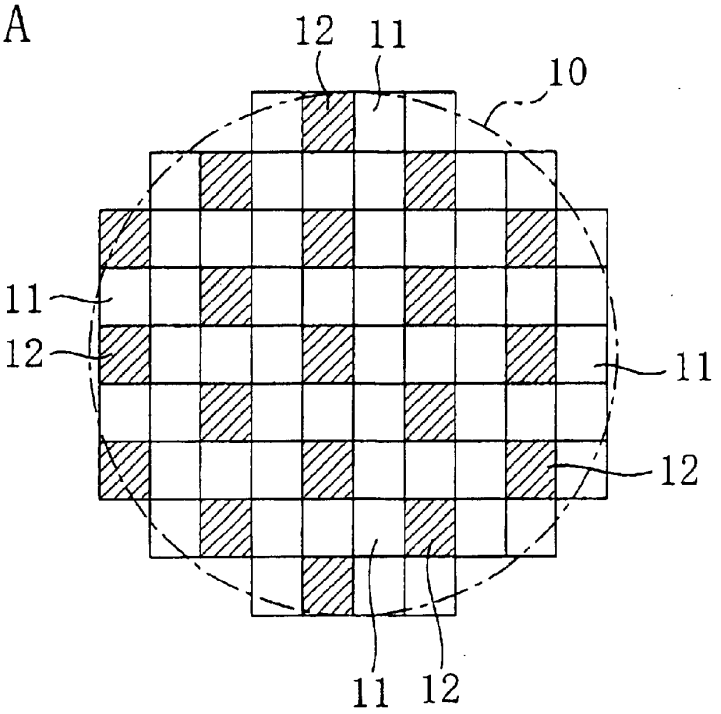


FIG. 3B

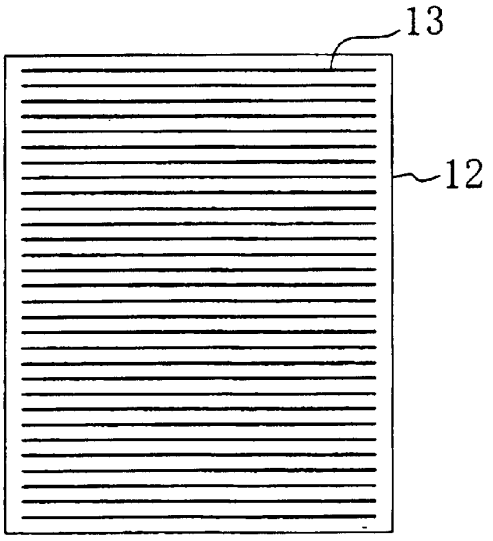


FIG. 4

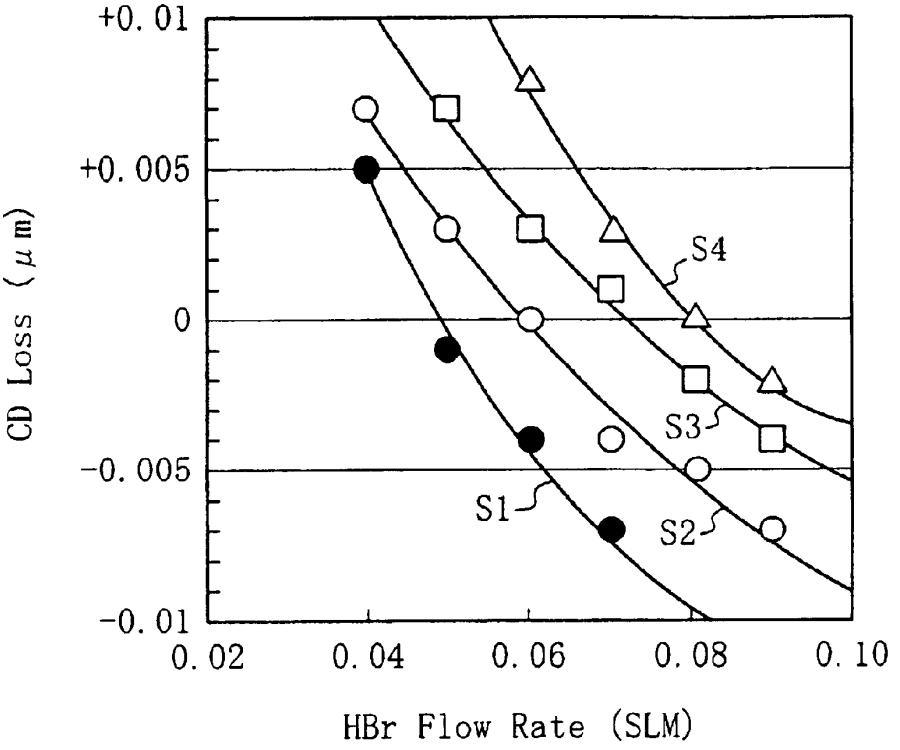

+0.01
+0.005
0
-0.005
-0.01
CD Loss (μm)
0.02
0.04
0.06
0.08
0.10
HBr Flow Rate (SLM)
S1
S2
S3
S4

FIG. 5A

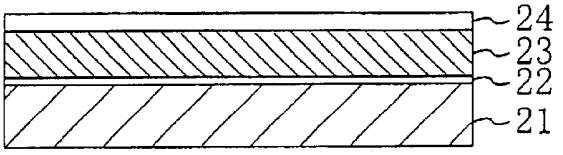


FIG. 5B

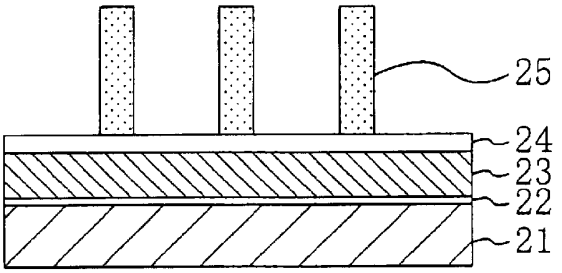


FIG. 5C

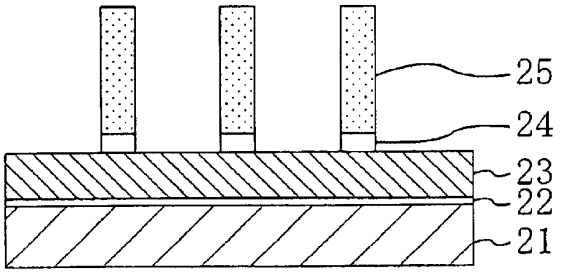


FIG. 5D

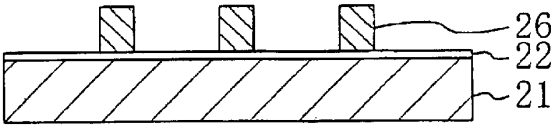


FIG. 6

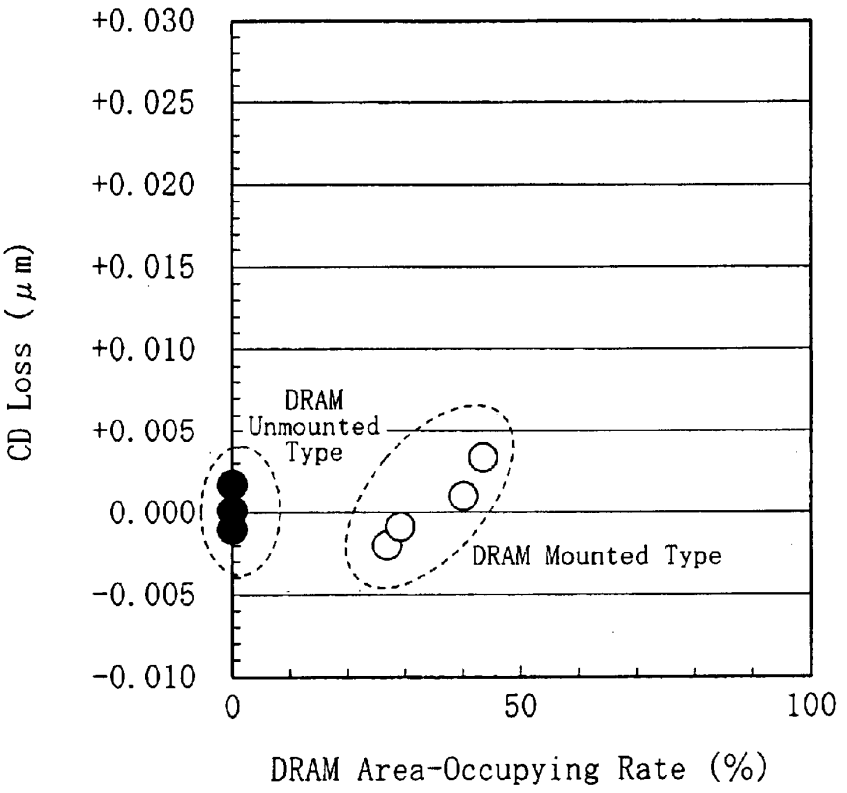

+0.030
+0.025
+0.020
+0.015
+0.010
+0.005
0.000
-0.005
-0.010
CD Loss (μm)
DRAM
Unmounted
Type
DRAM Mounted Type
0
50
100
DRAM Area-Occupying Rate (%)

FIG. 7

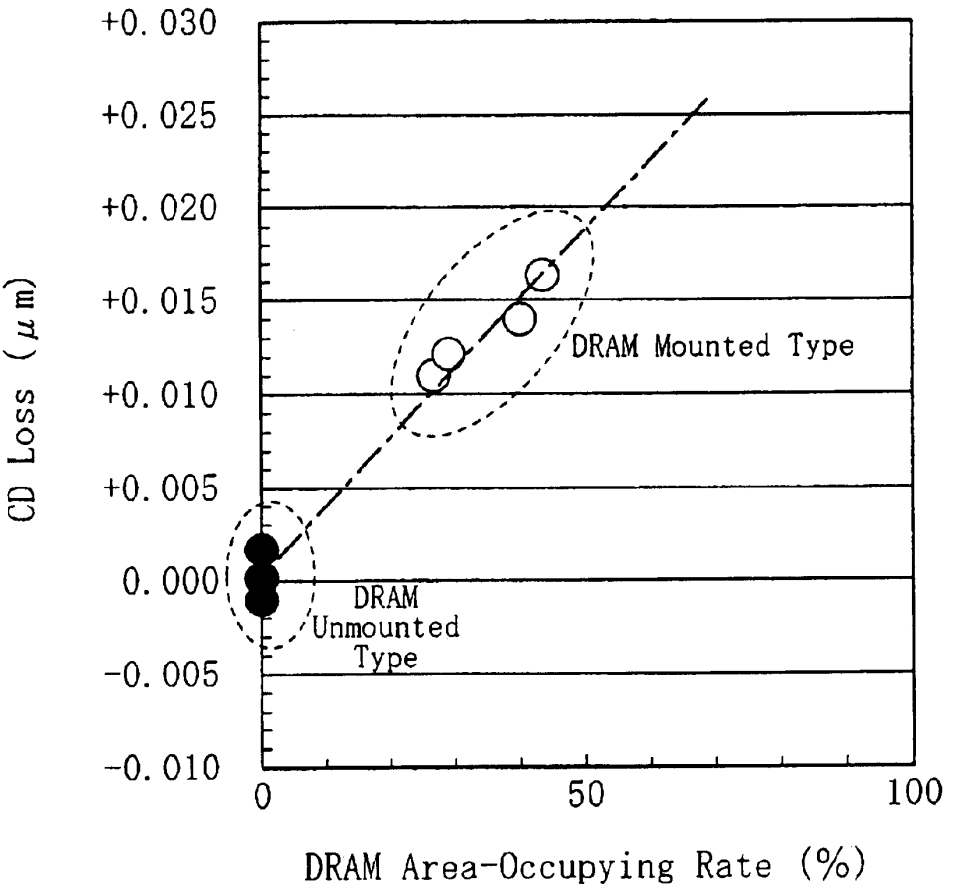

+0.030
+0.025
+0.020
+0.015
+0.010
+0.005
0.000
-0.005
-0.010
CD Loss (μm)
DRAM Mounted Type
DRAM Unmounted Type
0
50
100
DRAM Area-Occupying Rate (%)

FIG. 8

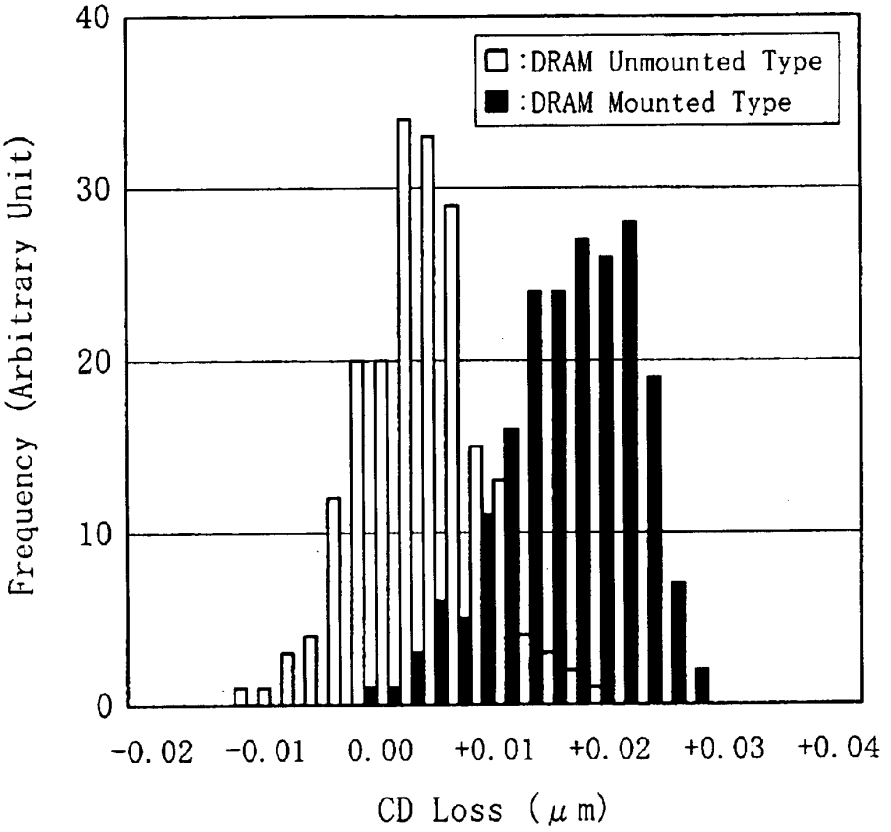

40
30
20
10
0
□ :DRAM Unmounted Type
■ :DRAM Mounted Type
Frequency (Arbitrary Unit)
-0.02
-0.01
0.00
+0.01
+0.02
+0.03
+0.04
CD Loss (μm)

FIG. 9

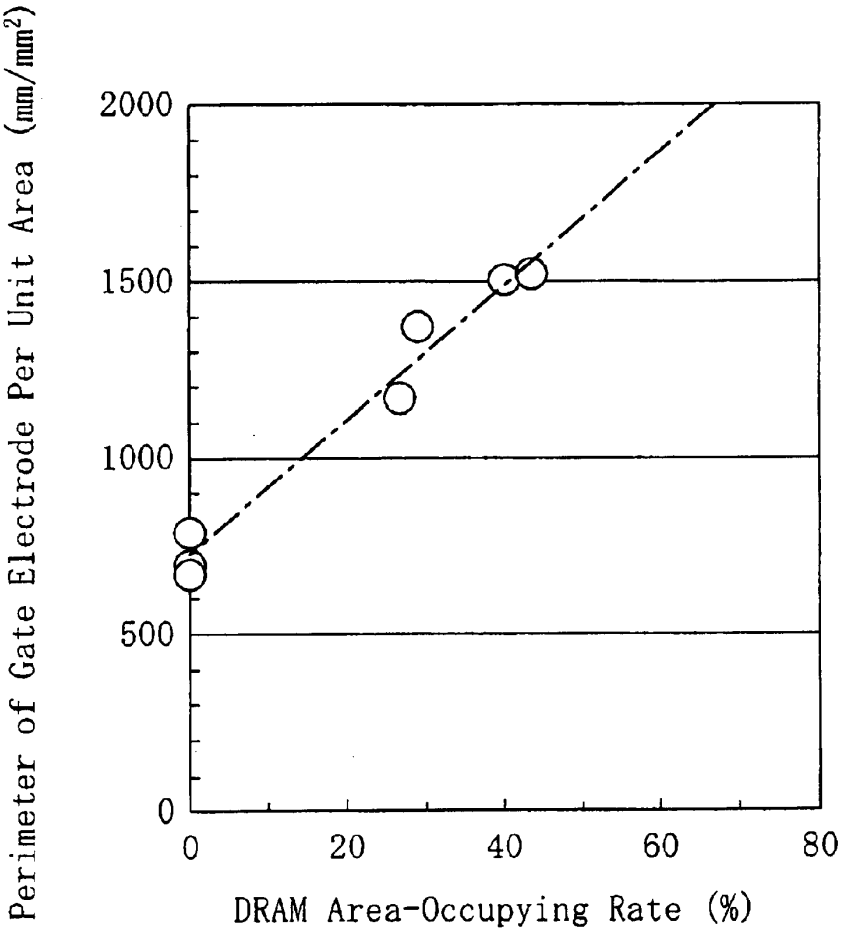
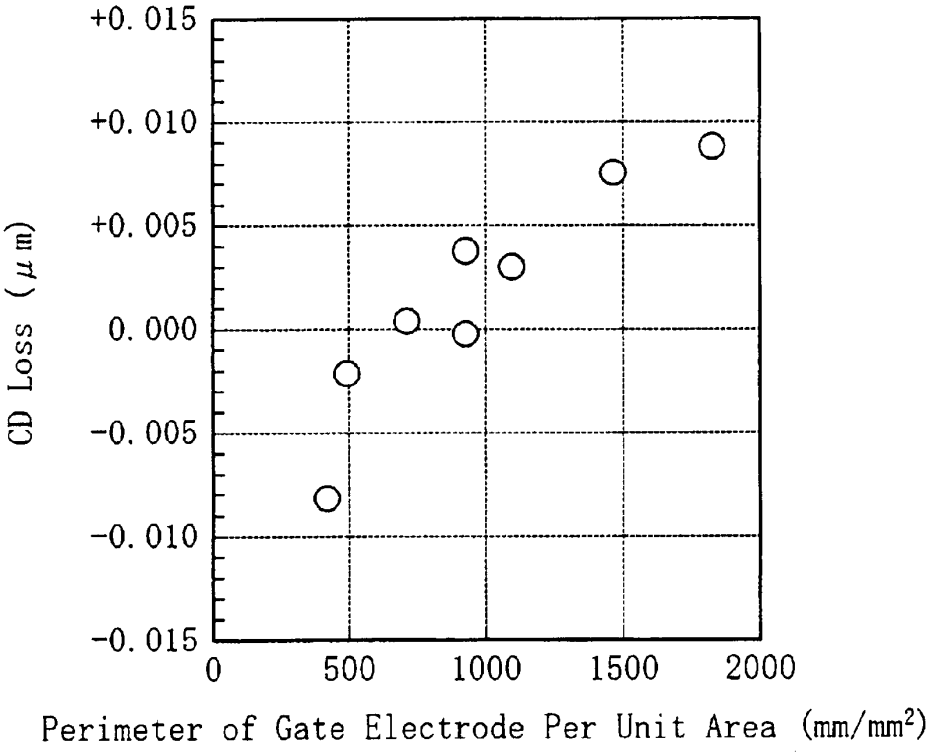

Perimeter of Gate Electrode Per Unit Area (mm/mm²)
2000
1500
1000
500
0
0
20
40
60
80
DRAM Area-Occupying Rate (%)

FIG. 10


+0.015
+0.010
+0.005
0.000
-0.005
-0.010
-0.015
CD Loss (μm)
0
500
1000
1500
2000
Perimeter of Gate Electrode Per Unit Area (mm/mm²)

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor integrated circuit device and a method for fabricating the same. More particularly, it relates to technology for forming a linear pattern composed of the gate electrode and wires of a MOS transistor, or metal wires, and the like in a system LSI in which a group of elements having an extremely fine repetitive pattern, such as DRAMs (Dynamic Random Access Memories), can be merged.

As an example of a semiconductor integrated circuit device in which DRAMs are merged, a system LSI on which DRAMs having a capacity over 20 megabits are mounted has been mass-produced in recent years.

In the fabrication steps for a semiconductor integrated circuit device represented by the system LSI in which the mounting rate of memory circuits such as DRAMs, SRAMs (Static Random Access Memories), or ROMs (Read Only Memories) on a single semiconductor chip (rate of an area occupied by the memory circuits to an area of the entire chip; hereinafter also referred to as an area-occupying rate) differs according to usage or specifications, the formation of a mask pattern having not only unit circuits which are simply and repeatedly arranged therein but also a variety of layouts has been required.

There has conventionally been known a phenomenon in which the configuration or size of a pattern obtained by etching a target film by using a mask pattern (hereinafter referred to as a formed pattern) differs depending on a mask pattern layout, i.e., the placement of an element pattern.

As an example of the phenomenon, a pattern proximity effect occurring during the formation of a resist pattern in a photolithographic step can be listed. This is the phenomenon in which even a pattern having the same design configuration and the same design size has different configurations and sizes after it is formed depending on the degree of proximity between the pattern and a pattern adjacent thereto or on the configuration of the adjacent pattern.

As another example, there can be listed a loading effect or a microloading effect occurring in a dry etching step. The loading effect is a phenomenon in which an etching rate varies depending on the size of a total etched area of a semiconductor chip, which may slightly affect variations in pattern size. The microloading effect is a phenomenon in which, when a pattern laid out in a single semiconductor chip shows an arrangement which is locally sparse and dense, an etching rate differs locally due to the locally dense and sparse arrangement. That is, the etching rate for even the single chip differs from the portion thereof on which the pattern is sparsely placed to the portion thereof on which the pattern is densely placed, which also indirectly affects variations in pattern size.

To solve the foregoing problem of variations in pattern size depending on the mask pattern layout, there have conventionally been adopted such design rules as to correct variations in pattern size only at a portion of a mask where the pattern size is considered to vary remarkably depending on the mask pattern layout due to the proximity effect or the loading effect.

On the other hand, the fabrication of a system LSI in which DRAMs can be merged has used the same processing

method or the same processing condition irrespective of the presence or absence of a mounted DRAM or of a DRAM area-occupying rate (the rate of an area occupied by the DRAMs to the area of an entire chip).

With the increasing miniaturization of the LSI, specifically as the size of an integrated circuit pattern is reduced to 0.25 μm or less, particularly to 0.15 μm or less, higher-precision size control has been required so that size variations resulting from difference in mask pattern layout are no more negligible.

FIG. **8** shows the frequency distribution of a CD (critical dimension) loss which is the difference between the size of a resist pattern prior to etching and the size of a completed gate electrode when the gate electrode is formed by dry etching by using the resist pattern as a mask in the fabrication of each of semiconductor integrated circuit devices on which 24 Mb DRAMs are mounted (hereinafter referred to as a DRAM mounted type) and a semiconductor integrated circuit device on which DRAMs are not mounted (hereinafter referred to as a DRAM unmounted type). The result shown in FIG. **8** was obtained by using the same gate-electrode forming process in the fabrication of each of the DRAM mounted type and the DRAM unmounted type. Each of the CD losses was calculated by subtracting the size of the completed gate electrode from the size of the resist pattern prior to etching.

As shown in FIG. **8**, mask-pattern-layout dependency is observed in pattern size though the same gate-electrode forming process was used to fabricate each of the types.

This indicates that, in accordance with the conventional method for fabricating a semiconductor integrated circuit device, the gate electrode size varies with difference in mask pattern layout associated with different types of semiconductor integrated circuit devices even if the same gate-electrode forming process is used. In other words, type dependency occurs in gate electrode size. As a result, the characteristics of a MOS transistor deviate from design specifications in a specified type of semiconductor integrated circuit device fabricated by using a specified mask, which causes the problem of a narrower operating margin. The problem cannot be ignored especially when the design rules are 0.18 μm or less.

SUMMARY OF THE INVENTION

In view of the foregoing, it is therefore an object of the present invention to prevent a size variation resulting from difference in mask pattern layout during the formation of a linear pattern composed of the gate electrode and wires of a MOS transistor, or metal wires, and the like.

To attain the object the present inventors have examined the cause of size variations resulting from difference in mask pattern layout.

As a result the examination, the present inventors have found that, in a semiconductor integrated circuit device on which a logic circuit composed of a CMOS (Complementary Metal-Oxide Semiconductor) is mounted and a memory circuit such as a DRAM composed of the gate electrode and wires that are densely arranged is mounted, pattern size varies with the area-occupying rate of the memory circuit.

The present inventors have also found that the phenomenon in which size variations result from difference in mask pattern layout is different in nature from the foregoing loading effect which results from the size of the etched area, i.e., the area of the pattern. As is obvious from FIG. **8**, the phenomenon is a phenomenon of novel nature in which the pattern size varies over the entire chip, which is also

different from the microloading effect resulting from the in-chip local denseness and sparseness of the pattern.

As described above, the type dependency of the size of the formed gate electrode or the like results from the CD loss. On the other hand, a dry etching step currently performed uses an etching gas having a sidewall protecting effect (hereinafter referred to as a deposition gas) or forms an etching reaction product having the sidewall protecting effect to achieve anisotropic dry etching by preventing side etching. If a gate electrode is formed by performing dry etching with respect to a polysilicon film, a chlorine-containing gas, e.g., is used frequently as the etching gas and HBr gas is used frequently as the deposition gas. As a result, a sidewall protecting film composed of $SiBr_4$, which is a reaction product between HBr and polysilicon and has low volatility, is formed on a sidewall of the polysilicon film. In the case of forming aluminium wires by performing dry etching with respect to an aluminium film, a CHF_3 gas has been used frequently as the deposition gas in recent years. The CHF_3 gas containing fluorine is a depositive gas added to form the sidewall protecting film but does not contribute to the etching of the aluminium film.

The present inventors have found that, if the configuration of the target film after etching is to be controlled with the sidewall protecting effect in the case of using the same gate-electrode forming process irrespective of the mask pattern layout, the sidewall protecting effect per unit area is reduced as the area of the sidewall of the target film to be protected increases, which increases the CD loss.

FIG. **9** shows the relationship between the perimeter of a gate electrode per unit area (the length of the peripheral portion of the gate electrode) and the DRAM area-occupying rate in each of various types of semiconductor integrated circuit devices having different DRAM area-occupying rates including the DRAM unmounted type. In the graph of FIG. **9**, "Perimeter of Gate Electrode Per Unit Area" represented by the vertical axis indicates the value obtained by dividing the total perimeter of the gate electrodes in a specified circuit region by the area of the specified circuit region. The specified circuit region may be the entire chip.

As shown in FIG. **9**, the perimeter of the gate electrode per unit area increases as the DRAM area-occupying rate increases.

FIG. **10** shows the relationship between the perimeter of the gate electrode per unit area and the CD loss in each of the various types.

As shown in FIG. **10**, the size of the gate electrode decreases as the perimeter of the gate electrode per unit area increases (the CD loss becomes positive). Conversely, the size of the gate electrode increases as the perimeter of the gate electrode per unit area decreases (the CD loss becomes negative). This is because the area of the sidewall to be protected increases as the perimeter of the gate electrode per unit area increases so that the sidewall protecting effect per unit area is reduced accordingly.

The present inventors have focused attention on the fact that the CD loss changes monotonously from a negative value to a positive value as the perimeter of the gate electrode per unit area increases (see FIG. **10**) and found that size variations in gate electrode pattern resulting from difference in mask pattern layout can be prevented by setting the perimeter of the gate electrode per unit area in a specified range irrespective of the type or adjusting a process condition in accordance with type-to-type difference in the perimeter per unit area of the gate electrode.

Specifically, a first semiconductor integrated circuit device according to the present invention assumes a semiconductor integrated circuit device comprising: a circuit pattern having a linear pattern, a perimeter of the linear pattern per unit area being set in a specified range.

In the first semiconductor integrated circuit device, the perimeter of the linear pattern per unit area is set in the specified range. Accordingly, even if a mask pattern layout differs greatly from one type of semiconductor integrated circuit device to another, size variations in linear pattern resulting from difference in mask pattern layout can be prevented. In a system LSI in which the mounting rate of DRAMs or the like is different depending on use or specifications also, it is possible to form gate electrode patterns, metal wires, or the like of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

A second semiconductor integrated circuit device according to the present invention assumes a semiconductor integrated circuit device comprising: a circuit pattern having a linear pattern, a dummy pattern being inserted in a region in which the circuit pattern is placed such that a sum perimeter of the linear pattern and the dummy pattern per unit area is set in a specified range.

In the second semiconductor integrated circuit device, the sum perimeter of the linear pattern and the dummy pattern per unit area is set in the specified range. Accordingly, even if a mask pattern layout differs greatly from one type of semiconductor integrated circuit device to another, size variations in linear pattern resulting from difference in mask pattern layout can be prevented. In a system LSI in which the mounting rate of DRAMs or the like is different depending on use or specifications also, it is possible to form gate electrode patterns, metal wires, or the like of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

In the second semiconductor integrated circuit device, the dummy pattern preferably has a strip-like configuration.

This allows easy formation of the dummy pattern.

A third semiconductor integrated circuit device according to the present invention assumes a semiconductor integrated circuit device comprising: a first circuit pattern having a first linear pattern and placed in a region in which a group of elements having a repetitive pattern are formed; and a second circuit pattern having a second linear pattern and placed in a region in which components other than the group of elements are formed, a dummy pattern being inserted in the region in which the second circuit pattern is placed such that a sum perimeter of the first linear pattern, the second linear pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first linear pattern per unit area.

In the third semiconductor integrated circuit device, the dummy pattern is inserted in the region in which the second circuit pattern corresponding to the components other than the group of elements is placed, whereby the sum perimeter per unit area of the first linear pattern of the first circuit pattern corresponding to the group of elements, the second linear pattern of the second circuit pattern, and the dummy pattern is set to the perimeter of the first linear pattern per unit area, i.e., the largest perimeter per unit area or less. Specifically, the sum perimeter per unit area is preferably set to 70% to 100% of the perimeter per unit area of the first linear pattern. Since the sum perimeter per unit area is set in

the specified range, even if a mask pattern layout differs greatly from one type of semiconductor integrated circuit device to another, size variations in linear pattern resulting from difference in mask pattern layout can be prevented. In a system LSI in which the mounting rate of DRAMs or the like is different depending on use or specifications also, it is possible to form gate electrode patterns, metal wires, or the like of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

In the third the semiconductor integrated circuit, the group of elements are preferably memories.

In the third the semiconductor integrated circuit, a perimeter of the dummy pattern per unit area is preferably 70% or more of the perimeter of the first linear pattern per unit area.

The insertion of the dummy pattern ensures the setting of the sum perimeter per unit area in the specified range, specifically 70% to 100% of the perimeter of the first linear pattern per unit area.

A first method for fabricating a semiconductor integrated circuit device assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern, at least one of fabrication steps for the semiconductor integrated circuit devices being common, the fabrication steps including the step of: inserting a dummy pattern in a region in which the circuit pattern is placed such that a sum perimeter of the linear pattern and the dummy pattern per unit area is set in a specified range.

In accordance with the first method for fabricating a semiconductor integrated circuit device, the dummy pattern is inserted such that the sum perimeter of the linear pattern and the dummy pattern per unit area is set in the specified range. Specifically, it is desirable to assume, as the specified range, 70% to 100% of the perimeter of the linear pattern per unit area in a memory circuit. To satisfy the standard, the perimeter of the inserted dummy pattern per unit area should be 70% or more of the perimeter of the linear pattern per unit area in the memory circuit. The present inventors have found that the CD loss in the formed pattern or the size of the formed pattern changes depending on the perimeter of the formed pattern per unit area. Accordingly, even if a mask pattern layout differs greatly from one type of semiconductor integrated circuit device to another, the sum perimeter of the linear pattern and the dummy pattern per unit area can be set in the specified range by forming an additional dummy pattern having a perimeter per unit area of 70% or more of that of the linear pattern of the memory circuit in a vacant region. For example, the perimeter of the gate electrode per unit area over the entire chip is largely dependent on a specified circuit such as a memory circuit since the specified circuit has a large perimeter of the gate electrode per unit area. Even if the in-chip area-occupying rate of such a specified circuit varies from one type to another, variations in the perimeter of the gate electrode per unit area over the entire chip can be suppressed by using the dummy pattern, as described above. As a result, size variations resulting from difference in mask pattern layout can be prevented. In short, the linear pattern can constantly be formed by etching with high precision. In a system LSI in which the mounting rate of DRAMs, SRAMs, ROMS, or the like is different depending on use or specifications also, it is possible to form the gate electrode and wires for MOS transistors, metal wires, or the like of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

A second method for fabricating a semiconductor integrated circuit device assumes a method for fabricating a semiconductor integrated circuit device, the method comprising the steps of: exposing each of a plurality of first regions of a semiconductor substrate to transfer a circuit pattern having a linear pattern onto the first region; exposing each of a plurality of second regions of the semiconductor substrate other than the first regions to transfer a dummy pattern onto the second region; and adjusting a ratio between the number of exposing shots for transferring the circuit pattern and the number of exposing shots for transferring the dummy pattern such that a sum perimeter of all the linear patterns transferred and all the dummy patterns transferred per unit area is set in a specified range.

In accordance with the second method for fabricating a semiconductor integrated circuit device, the ratio between the number of exposing shots for transferring the circuit pattern and the number of exposing shots for transferring the dummy pattern is adjusted such that the sum perimeter of all the linear patterns transferred and all the dummy patterns transferred per unit area is set in the specified range. Accordingly, even if a mask pattern layout differs greatly from one type of semiconductor integrated circuit device to another, size variations in linear pattern resulting from difference in mask pattern layout can be prevented. In a system LSI in which the mounting rate of DRAMs or the like is different depending on use or specifications also, it is possible to form gate electrode patterns, metal wires, or the like of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

A third method for fabricating a semiconductor integrated circuit devices assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern, at least one of fabrication steps for the semiconductor integrated circuit devices being common, the fabrication steps including the step of: performing dry etching with respect to a target film while adjusting a dry etching condition in accordance with a perimeter of the linear pattern per unit area.

In accordance with the third method for fabricating a semiconductor integrated circuit device, dry etching is performed with respect to the target film while adjusting the dry etching condition in accordance with the perimeter of the linear pattern per unit area. Accordingly, even if a mask pattern layout differs greatly from one type of semiconductor integrated circuit device to another, the size of the linear pattern can be held constantly at a specified value. In a system LSI in which the mounting rate of DRAMs or the like is different depending on use or specifications also, it is possible to form gate electrode patterns, metal wires, or the like of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

In the third method for fabricating a semiconductor integrated circuit device, the step of adjusting the dry etching condition preferably includes the step of: determining one dry etching condition when the perimeter of the linear pattern per unit area is within one range.

The arrangement allows easy adjustment of the dry etching condition.

A fourth method for fabricating a semiconductor integrated circuit device assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern, at least one of fabrication steps for the semiconductor integrated

circuit devices being common, the fabrication steps including the step of: forming a resist pattern corresponding to the linear pattern while adjusting a size of the resist pattern in accordance with a perimeter of the linear pattern per unit area.

In accordance with the fourth method for fabricating a semiconductor integrated circuit device, the resist pattern corresponding to the linear pattern is formed while the size of the resist pattern is adjusted in accordance with the perimeter of the linear pattern per unit area. Accordingly, even if a mask pattern layout differs greatly from one type of semiconductor integrated circuit device to another, the size of the linear pattern can be held constantly at a specified value. In a system LSI in which the mounting rate of DRAMs or the like is different depending on use or specifications also, it is possible to form gate electrode patterns, metal wires, or the like of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

A fifth method for fabricating a semiconductor integrated circuit devices assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern, at least one of fabrication steps for the semiconductor integrated circuit devices being common, the fabrication steps including: a first step of forming a resist pattern corresponding to the linear pattern on a target film; and a second step of performing dry etching with respect to the target film by using the resist pattern as a mask, the second step including the step of: using an etching gas having an effect of protecting a sidewall formed in the target film through the etching or forming an etching reaction product having the sidewall protecting effect, a processing method or a processing condition in at least one of the first and second steps being adjusted in accordance with a ratio between an area occupied by a group of elements contained in the circuit pattern and having a repetitive pattern and an area of a region in which the circuit pattern is placed.

In the first step of forming the resist pattern corresponding to the linear pattern or in the second step of performing dry etching with respect to the target film by using the resist pattern as a mask, the fifth method for fabricating a semiconductor integrated circuit device changes the processing method or the processing condition in accordance with the rate of the area occupied by the group of elements having the repetitive pattern to the area of the region in which the circuit pattern is placed (hereinafter referred to as a group-of-elements area-occupying rate). Accordingly, even if the area of the sidewall formed in the target film through etching differs according to difference in group-of-elements area-occupying rates, i.e., difference in mask pattern layout, it is possible to adjust the size of the resist pattern in the first step so as to eliminate difference in sidewall protecting effects per unit area in the second step or adjust the etching condition in the second step to achieve a desired sidewall protecting effect per unit area. This prevents size variations resulting from difference in mask pattern layout during the formation of the circuit pattern by using a lithographic or dry etching technique and thereby allows high-precision formation of a gate electrode or wires.

In the fifth method for fabricating a semiconductor integrated circuit device, the group of elements are preferably memories such as DRAMs.

In the fifth method for fabricating a semiconductor integrated circuit device, the first step preferably includes the step of: increasing a size of the resist pattern as the group-of-elements area-occupying rate increases.

In the arrangement, the area of the sidewall formed in the target film through etching increases as the group-of-elements area-occupying rate increases. Accordingly, even if the sidewall protecting effect per unit area decreases in the second step, the decrement in sidewall protecting effect can be compensated for so that size variations in components are surely suppressed.

In the fifth method for fabricating a semiconductor integrated circuit device, the second step preferably includes the step of: determining an etching condition such that the sidewall protecting effect increases as the group-of-elements area occupying rate increases.

In the arrangement, even if the area of the sidewall formed in the target film through etching increases as the group-of-elements area-occupying rate increases, a desired sidewall protecting effect per unit area is achievable in the second step that so that size variations in components are surely suppressed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows an example of the layout of a circuit pattern prior to the insertion of a dummy pattern in a semiconductor integrated circuit device according to a first embodiment of the present invention;

FIG. **2** shows an example of the layout of a circuit pattern after the insertion of the dummy pattern in the semiconductor integrated circuit device according to the first embodiment;

FIG. **3**A shows an example of a pattern-exposure shot map in a lithographic step for forming a polysilicon gate electrode pattern in accordance with a method for fabricating a semiconductor integrated circuit device according to a second embodiment of the present invention and

FIG. **3**B shows an example of a dummy pattern used in the lithographic step;

FIG. **4** shows the result of experimentally determining the relationship between the flow rate of a dry etching gas and a CD loss in a polysilicon gate electrode pattern by using, as a parameter, an on-chip perimeter of gate electrodes per unit area when the gate electrode pattern is formed by dry etching in the fabrication of plural types of semiconductor integrated circuit devices;

FIGS. **5**A to **5**D are cross-sectional views illustrating the individual steps of a method for fabricating a semiconductor integrated circuit device according to a fifth or sixth embodiment of the present invention;

FIG. **6** shows the relationship between a CD loss and a DRAM area-occupying rate when various types of semiconductor integrated circuit devices with different DRAM area-occupying rates, including a DRAM unmounted type, are fabricated by using the method for fabricating semiconductor integrated circuit devices according to the fifth embodiment;

FIG. **7** shows, as a comparative example, the relationship between a CD loss and a DRAM area-occupying rate when various types of semiconductor integrated circuit devices with different DRAM area-occupying rates, including a DRAM unmounted type, are fabricated by using the same etching condition irrespective of the presence or absence of a DRAM;

FIG. **8** shows the frequency distribution of a CD loss when a DRAM mounted type and a DRAM non-mounted type are fabricating by using the same gate-electrode forming process;

FIG. **9** shows the relationship between the perimeter of gate electrodes per unit area and a DRAM area-occupying rate in each of various types with different DRAM area-occupying rates including a DRAM unmounted type; and

FIG. **10** shows the relationship between the perimeter of gate electrodes per unit area and a CD loss in each of the various types.

DETAILED DESCRIPTION OF THE INVENTION

Embodiment 1

A semiconductor integrated circuit device and a method for fabricating the same according to a first embodiment of the present invention will be described with reference to the drawings. It is to be noted that the method for fabricating the semiconductor integrated circuit device according to the first embodiment assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern and at least one of fabrication process steps for the semiconductor integrated circuit devices is common.

The first embodiment features a dummy pattern inserted in a region in which a circuit pattern having a linear pattern is to be placed such that a sum perimeter of the linear pattern and the dummy pattern per unit area is set in a specified range.

FIG. **1** shows an example of the layout of the circuit pattern prior to the insertion of the dummy pattern in the semiconductor integrated circuit device according to the first embodiment. FIG. **2** shows an example of the layout of the circuit pattern after the insertion of the dummy pattern in the semiconductor integrated circuit device according to the first embodiment. Although the circuit pattern shown in each of FIGS. **1** and **2** is of a logic circuit, a memory circuit such as a RAM or ROM may also be mounted on a chip in addition to the logic circuit.

As shown in FIG. **1**, the circuit pattern is composed of an active region pattern **1** and a gate electrode pattern **2** for a MOS transistor. As shown in FIG. **2**, a strip-like or linear gate electrode dummy pattern **4** is inserted in a vacant region **3** in which the active region pattern **1** and the gate electrode pattern **2** are not provided.

This allows an increase in the perimeter of the gate electrode without increasing the chip area. Specifically, the perimeter of the gate electrodes per unit area in the circuit pattern after the insertion of the dummy pattern shown in FIG. **2** has increased to 1600 mm/mm^2, in contrast to the circuit pattern before the insertion of the dummy pattern shown in FIG. **1** in which the perimeter of the gate electrode per unit area is 500 mm/mm^2. Thus, in the first embodiment, the perimeter of the gate electrode per unit area was as small as 500 mm/mm^2 at a time prior to the insertion of the dummy patterns due to a low area-occupying rate of DRAMs, ROMs, or the like where the gate electrode patterns are dense (or due to the fact that the DRAMs, ROMs, or the like are not mounted). To bring the perimeter of the gate electrode per unit area of each of the gate electrode patterns **2** in the circuit pattern shown in FIG. **1** closer to the perimeter of the gate electrode per unit area in another type with a higher mounting rate of DRAMs or ROMs, therefore, a large number of gate electrode dummy patterns **4** are inserted such that a sum perimeter of the gate electrode patterns **2** and the gate electrode dummy patterns **4** per unit area is greatly increased to 1600 mm/mm^2, as shown in FIG. **2**.

To reduce variations in CD loss resulting from type-to-type difference in the perimeter of the gate electrode per unit area in the gate-electrode forming process (specifically in etching for forming the gate electrode) to an error range of 0 to 0.003 μm associated with size measurement, reticle formation, or the like, the type-to-type difference in the perimeter of the gate electrode per unit area should be limited to a range of about 500 mm/mm^2 (see FIG. **10**).

In a system LSI, on the other hand, the mounting rate of DRAMs, ROMS, or the like where the gate electrode patterns are dense differs greatly from one type to another so that the perimeter of the gate electrode per unit area varies significantly. The perimeter of the gate electrode per unit area is maximum in general-purpose DRAMs having DRAM cells where the gate electrode patterns are densest, the value of which is about 2500 mm/mm^2.

To reduce the type-to-type difference in the perimeter of the gate electrode per unit area to about 500 mm/mm^2, therefore, the standard (the foregoing specified range) may be set in about 2000 to 2500 mm/mm^2. However, there is a case where a type exists in which a dummy pattern cannot be inserted such that the required perimeter of the gate electrode per unit area, which is 2000 mm/mm^2, is satisfied depending on the layout prior to the insertion of the dummy pattern. In reality, it can be assumed that a system LSI on which DRAMs having an area-occupying rate of 70% or more are mounted will not be produced. Therefore, the present embodiment has determined 2000 mm/mm^2 which corresponds to the case where the DRAM area-occupying rate is 80% as the upper limit of the standard range of the perimeter of the gate electrode per unit area and determined 1600 to 2000 mm/mm^2 as the standard range of the perimeter of the gate electrode per unit area.

According to the first embodiment, a perimeter of the gate electrodes per unit area over the entire chip, i.e., a sum perimeter of the gate electrode patterns **2** and the gate electrode dummy patterns **4** per unit area (if a memory circuit not shown is mounted, a sum perimeter of the gate electrodes per unit area considering another gate electrode pattern included in the memory circuit) can be set in a specified range with the insertion of the gate electrode dummy patterns **4**. Specifically, it is desirable to assume, as the specified range, 70% to 100% of the perimeter of the gate electrode per unit area in the memory circuit, i.e., the maximum perimeter per unit area. To satisfy the standard, the perimeter per unit area of the gate electrode dummy patterns **4** to be inserted (a value obtained by, e.g., dividing the perimeter of the gate electrode dummy patterns **4** by the area of the vacant regions **3**) should be 70% or more of the perimeter of the gate electrode per unit area in the memory circuit. The arrangement ensures the setting of a perimeter of the gate electrode per unit area over the entire chip in the specified range even if the mask pattern layout differs greatly from one type of semiconductor integrated circuit device to another. For example, a perimeter of the gate electrode per unit area over the entire chip is greatly dependent on a specified circuit such as a memory circuit because of its large perimeter of the gate electrode per unit area. Even when the in-chip area-occupying rate of the specified circuit varies from one type to another, variations in the perimeter of the gate electrodes per unit area over the entire chip can be suppressed by using the dummy patterns, as described above. As a result, size variations resulting from difference in mask pattern layout can be prevented. In short, it becomes possible to form the gate electrode patterns **2** of constantly uniform sizes through etching. In a system LSI in which the mounting rate of DRAMs or the like is different depending

on use or specifications also, it is possible to form the gate electrode patterns **2** of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

In the first embodiment, the method of forming the gate electrode patterns **2** is not particularly limited. The gate electrode patterns **2** may also be formed by using, e.g., a parallel-plate RIE (Reactive Ion Etching) apparatus and setting the flow rate of a Cl_2 gas to 0.04 SLM (Standard Litter per Minute), the flow rate of HBr gas to 0.08 SLM, pressure to 20 Pa, and RF power to 300 W, which are main dry etching conditions, and performing etching with respect to the polysilicon film.

In the first embodiment, the perimeter per unit area of the linear pattern (for example, the gate electrode pattern) composing the circuit pattern may also be set in a specified range without using the dummy pattern.

Although the first embodiment has assumed the formation of the gate electrode, the present invention is not limited thereto. The present invention achieves equally high formation accuracy even in the microfabrication of a layer having another linear pattern, e.g., the formation of metal wires composed of, e.g., aluminium, copper, or the like.

Embodiment 2

A semiconductor integrated circuit device and a method for fabricating the same according to a second embodiment of the present invention will be described with reference to the drawings. It is to be noted that the method for fabricating the semiconductor integrated circuit device according to the second embodiment assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern and at least one of fabrication process steps for the semiconductor integrated circuit devices is common.

The second embodiment features the adjustment of a ratio between the number of exposing shots for transferring the circuit pattern having a linear pattern onto a wafer as a substrate to be exposed and the number of exposing shots for transferring a dummy pattern onto the wafer such that a sum perimeter of all linear patterns transferred and all dummy patterns transferred per unit area is set in a specified range.

FIG. **3**A shows an example of a pattern-exposure shot map in a lithographic step for forming a polysilicon gate electrode pattern in the method for fabricating the semiconductor integrated circuit devices according to the second embodiment. FIG. **3**B shows an example of a dummy pattern used in the lithographic step.

In the method for fabricating the semiconductor integrated circuit devices according to the second embodiment, the number of first exposed regions **11** on each of which the circuit pattern is transferred (i.e., the number of exposing shots for transferring the circuit pattern) and the number of second exposed regions **12** on each of which the dummy pattern is transferred (i.e., the number of exposing shots for transferring the dummy pattern) are adjusted on a wafer **10**, as shown in FIG. **3**A. Onto each of the second exposed regions **12**, a strip-like dummy pattern **13** composed of e.g., 0.2-μm lines and 0.2-μm spaces is transferred simply and entirely over the second exposed region **12**.

As a result, it becomes possible to limit, e.g., the perimeter of the gate electrodes per unit area over the wafer **10**, i.e., a sum perimeter of all gate electrode patterns transferred (included in all circuit patterns transferred) and all dummy patterns **13** transferred per unit area to a specified range which is not dependent on the mask pattern layout of the semiconductor integrated circuit device, i.e., on the mask pattern layout corresponding to the circuit pattern.

Specifically, the present embodiment uses a dummy reticle mask for transferring the dummy pattern **13** in addition to a reticle mask for forming the circuit pattern. This allows the perimeter of the gate electrode per unit area over the entire wafer **10** to be larger than in the first embodiment.

To limit the perimeter of the gate electrode per unit area over the entire wafer **10** to the range of, e.g., 1600 to 2000 mm/mm^2, similarly to the first embodiment, the present embodiment can calculate the rate A of the area occupied by the second exposed regions **12** to the area of the entire wafer as follows. In this case, it is assumed that the perimeter per unit area of the dummy pattern to be transferred onto each of the second exposed regions **12** is, e.g., 5000 mm/mm^2 and the perimeter of the gate electrode per unit area in the circuit pattern to be transferred onto each of the first exposed regions **12** is, e.g., 500 mm/mm^2. That is, the relation represented by the following expression:

$$1600 \leqq 5000 \times A + 500 \times (1-A) \leqq 2000$$

is established so that

$$0.244 \leqq A \leqq 0.333$$

is satisfied. This causes the necessity to set the number of exposing shots for transferring the dummy pattern such that the rate of the area occupied by the second exposing regions **12** to the area of the entire wafer **10** is about 24.5% or more. Specifically, as shown in FIG. **3**A, the first exposed regions **11** for transferring the circuit pattern are provided to occupy ¾ (75%) of the surface area of the wafer **10** and the second exposed regions **12** for transferring the dummy pattern are provided to occupy ¼ (25%) of the surface area of the wafer **10** in the present embodiment.

According to the second embodiment, the ratio between the number of exposing shots for transferring the circuit pattern and the number of exposing shots for transferring the dummy pattern is adjusted such that the perimeter of the gate electrode per unit area over the entire wafer **10** is set in a specified range. This prevents size variations in gate electrode pattern resulting from difference in mask pattern layout even if the mask pattern layout differs greatly from one type of semiconductor integrated circuit device to another. In a system LSI in which the mounting rate of DRAMs or the like is different depending on use or specifications also, it is possible to form gate electrode patterns of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

In the second embodiment, the perimeter of the dummy pattern per unit area is preferably 70% or more of the perimeter of the gate electrode per unit area in a memory circuit mounted on the semiconductor integrated circuit device.

In the second embodiment, the ratio between the number of exposing shots for transferring the circuit pattern and the number of exposing shots for transferring the dummy pattern is adjusted preferably such that the perimeter of the gate electrode per unit area over the entire wafer is set to 70% to 100% of the perimeter of the gate electrode per unit area in the memory circuit.

Although the second embodiment has assumed the formation of the gate electrode, the present invention is not limited thereto. The present invention achieves equally high formation accuracy even in the microfabrication of a layer having another linear pattern, e.g., the formation of metal wires composed of, e.g., aluminium, copper, or the like.

Embodiment 3

A semiconductor integrated circuit device and a method for fabricating the same according to a third embodiment of the present invention will be described with reference to the drawings. It is to be noted that the method for fabricating the semiconductor integrated circuit device according to the third embodiment assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern and at least one of fabrication process steps for the semiconductor integrated circuit devices is common.

The third embodiment features dry etching performed with respect to a target film while a dry etching condition is adjusted in accordance with the perimeter per unit area of the linear pattern composing a circuit pattern. By way of example, a description will be given herein below to the case where the size dependency of a gate electrode pattern on a mask pattern layout for the semiconductor integrated circuit device is suppressed by selectively using a dry etching condition for forming the gate electrode pattern.

FIG. **4** is a graph showing, when a polysilicon gate electrode pattern is formed by dry etching in the fabrication of plural types of semiconductor integrated circuit devices incorporating circuits of various layouts, the result of experimentally determining the relationship between the flow rate of a dry etching gas and a CD loss in a gate electrode pattern by using a perimeter of the gate electrode per unit area over a chip as parameters (parameter S1: 600 mm/mm^2, parameter S2: 1000 mm/mm^2, parameter S3: 1400 mm/mm^2, and parameter S4: 1800 mm/mm^2). The experimental result shown in FIG. **4** was obtained by using, as an etching gas, a gas mixture of HBr, Cl_2, and He serving as a cooling gas and varying the gas flow rate of HBr composing the gas mixture.

As shown in FIG. **4**, even though the gas flow rate of HBr is the same, if the perimeter of the gate electrode per unit area differs, the CD loss in the gate electrode pattern differs accordingly. On the other hand, by varying the gas flow rate of HBr, the CD loss can be reduced to nearly zero at a specified flow rate even at any value of the perimeter of the gate electrode per unit area.

Thus, the method for fabricating the semiconductor integrated circuit devices according to the third embodiment preliminarily calculates the perimeter of the gate electrode per unit area in a circuit pattern for each of the semiconductor integrated circuit devices and experimentally determines the relationship between the dry etching condition and the CD loss shown in FIG. **4**. Then, dry etching is performed with respect to the polysilicon film to be formed into the gate electrodes by selectively using such a dry etching condition (which is the flow rate of HBr gas in FIG. **4**) that, for the calculated perimeter of the gate electrode per unit area, the CD loss in the gate electrode pattern becomes substantially zero to a degree that can be permitted in terms of design. In other words, dry etching is performed with respect to the polysilicon film by selectively using a dry etching condition such that the size of the gate electrode pattern equals an objective size determined at the design stage.

In the fabrication of plural types of semiconductor integrated circuit devices on which, e.g., a memory circuit and a logic circuit are mounted, if the objective size of the formed pattern is the same for each of the types but the layout differs greatly from one type to another, accurate etching for pattern formation can be performed in principle irrespective of the layout. In practice, however, it is not preferred to individually determine the dry etching condition for each of the types with different layouts, i.e., to vary the dry etching condition from one type to another in terms of mass producibility.

To prevent this, the present embodiment may also divide the perimeter of the gate electrode per unit area into a plurality of ranges and set one dry etching condition for the perimeter of the gate electrode per unit area in each of the ranges.

Table 1 shows an optimum condition in the dry etching step for the perimeter of the gate electrode per unit area in each of the ranges in forming the polysilicon gate electrode pattern by dry etching.

TABLE 1

Perimeter of Gate Electrode Per Unit Area (mm/mm^2)	Recipe No. of Dry Etching Condition in Forming Gate Electrode Pattern	HBr Gas Flow Rate (SLM)
$400<S\leqq800$	PS1	0.05
$800<S\leqq1200$	PS2	0.06
$1200<S\leqq1600$	P53	0.07
$1600<S\leqq2000$	PS4	0.08

As shown in Table 1, the perimeter of the gate electrode per unit area is divided into a plurality of ranges such that dry etching conditions (specifically, the flow rates of HBr gas) different from one range to another are used. When the dry etching conditions shown in Table 1 are used, the CD loss in the gate electrode pattern for the perimeter of the gate electrode per unit area in each of the ranges (S1 to S4) is a small value substantially falling within 0±0.002 m, as is obvious from the correspondence with FIG. **4**. This provides sufficient pattern accuracy even in the fabrication of a device with design rules of 0.1 μm or less.

Since the third embodiment performs dry etching with respect to the polysilicon film while adjusting a dry etching condition for the polysilicon film formed into the gate electrodes in accordance with the perimeter of the gate electrode per unit area, the size of the gate electrode pattern can constantly be adjusted to a specified value even if the mask pattern layout greatly differs from one type of semiconductor integrated circuit device to another. In a system LSI in which the mounting rate of DRAMs or the like is different depending on use or specifications also, it is possible to form gate electrode patterns of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

Since the third embodiment has divided the perimeter of the gate electrode per unit area into the plurality of ranges and determined one dry etching condition for each of the ranges, the dry etching condition can be adjusted more easily than in the case where the dry etching condition is changed on a per type basis.

Although the third embodiment has controlled the CD loss in the gate electrode pattern by adjusting the flow rate of HBr gas in the dry etching step for forming the polysilicon gate electrode, it is also possible to determine the optimum dry etching condition by adjusting the total flow rate of all etching gases, the pressure of each etching gas, the RF power of a dry etching apparatus, or the like instead of adjusting the HBr flow rate.

In the third embodiment, if an organic coated film serving as a light-reflection preventing film in, e.g., a lithographic step is formed on the polysilicon film to be formed into the gate electrodes or if a silicon dioxide film or the like serving as a hard mask is formed by, e.g., CVD (Chemical Vapor Deposition) on the polysilicon film to be formed into the

gate electrodes, the etching condition for the organic coated film, the CVD silicon oxide film, or the like may also be adjusted instead of adjusting the etching condition for the polysilicon film.

Although the third embodiment has assumed the formation of the gate electrode, the present invention is not limited thereto. The present invention achieves equally high formation accuracy even in the microfabrication of a layer having another linear pattern, e.g., etching for forming metal wires, etching of an insulating film for forming a trench for a buried wire, or the like.

Embodiment 4

A semiconductor integrated circuit device and a method for fabricating the same according to a fourth embodiment of the present invention will be described with reference to the drawings. It is to be noted that the method for fabricating the semiconductor integrated circuit device according to the fourth embodiment assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern and at least one of fabrication process steps for the semiconductor integrated circuit devices is common.

The third embodiment has adjusted the dry etching condition in accordance with the perimeter per unit area of the linear pattern composing the circuit pattern. By contrast, the fourth embodiment features the formation of a resist pattern corresponding to the linear pattern composing the circuit pattern, while adjusting the size of the resist pattern in accordance with the perimeter of the linear pattern per unit area. By way of example, a description will be given herein below to the case where the size dependency of a gate electrode pattern on a mask pattern layout for the semiconductor integrated circuit device is suppressed by adjusting the size of the resist pattern corresponding to the gate electrode pattern.

Specifically, when a polysilicon gate electrode pattern is formed by dry etching in the fabrication of plural types of semiconductor integrated circuit devices incorporating circuits of various layouts, the fourth embodiment uses, as an etching gas, a gas mixture of HBr, Cl_2, and He serving as a cooling gas, while fixing the gas flow rate of HBr composing the gas mixture to 0.07 SLM. That is, the dry etching condition used in the fourth embodiment is fixed to the recipe No. PS3 (standard condition) shown in Table 1 of the third embodiment. When the dry etching condition is thus fixed, the value of the CD loss in the gate electrode pattern differs depending on the mask pattern layout, as shown in FIG. **4** of the third embodiment.

In the method for fabricating the semiconductor integrated circuit devices according to the fourth embodiment, therefore, the relationship between a perimeter of the gate electrode per unit area in a circuit pattern for each of the semiconductor integrated circuit devices and the CD loss in the gate electrode pattern is determined. Then, the size of the resist pattern serving as a dry etching mask is adjusted in accordance with, e.g., a photolithographic condition such as a dose such that a variation in pattern size which occurs depending on the magnitude of the determined CD loss, i.e., on the perimeter of the gate electrode per unit area is compensated for.

Table 2 shows the CD loss (A) in the gate electrode pattern, the objective size (B) in the photolithographic step, and the design size (C) of the gate electrode pattern after dry etching, which are for the perimeter of the gate electrode per unit area in each of the ranges in performing dry etching by forming the resist pattern corresponding to the polysilicon gate electrode pattern and performing the dry etching by using the formed resist pattern.

TABLE 2

Perimeter of Gate Electrode Per Unit Area (mm/mm^2)	CD Loss (A) in Recipe No. PS3 (μm)	Objectve Size (B) in lithographic Step (μm)	Design Size (C) After Dry Etching (μm)
$400<S\leqq800$	−0.007	0.143	0.150
$800<S\leqq1200$	−0.003	0.147	0.150
$1200<S\leqq1600$	0.001	0.151	0.150
$1600<S\leqq2000$	0.003	0.153	0.150

In Table 2, each CD loss (A) is a value obtained when the dry etching condition of the recipe No. PS3 shown in Table 1 is used. Each objective size (B) is the optimum size of the resist pattern adjusted in consideration of the magnitude of the CD loss (A), as described above. In the present embodiment, the design size (C) is determined to be 0.150 μm.

Since the relation given by the following expression:

$$\text{Objective Size } (B) = CD \text{ Loss } (A) + \text{Design size } (C)$$

is established, the objective size (B), i.e., the value of the optimum size of the resist pattern shown in Table 2 can be determined specifically. Conversely, an amount of adjustment and the CD loss (A) can be cancelled out by adjusting the objective size (B) in the photolithographic step.

In the present embodiment, the objective size (B) in the photolithographic step can also be determined easily by reading the CD loss corresponding to the perimeter per unit area of the gate electrode in each of the ranges (S1 to S4) when the flow rate of HBr gas is, e.g., 0.07 SLM in FIG. **4** by focusing attention on the fact that the design size (C) is 0.150 μm and the dry etching condition is the Recipe No. PS3 (Flow Rate of HBr Gas: 0.07 SLM) shown in Table 1. The reason that the recipe No. PS3 shown in Table 1 is used as the dry etching condition in the present embodiment is as follows. As is obvious from Table 2, when the recipe No. PS3 is used, the amount of adjustment of the objective size (B) corresponding to the magnitude of the CD loss (A) becomes minimum with respect to various perimeters of the gate electrodes per unit area implemented in the different types of semiconductor integrated circuit devices.

Since the fourth embodiment has thus formed the resist pattern corresponding to the gate electrode pattern while adjusting the size of the resist pattern in accordance with the perimeter of the gate electrode per unit area, the size of the gate electrode pattern can constantly be adjusted to a specified value even if the mask pattern layout greatly differs from one type of semiconductor integrated circuit device to another. In a system LSI in which the mounting rate of DRAMs or the like is different depending on use or specifications also, it is possible to form gate electrode patterns of uniform sizes irrespective of the mask pattern layout, so that a semiconductor integrated circuit device free of variations in operating margin is provided.

To adjust the objective size in the photolithographic step, i.e., adjust the size of the resist pattern corresponding to the gate electrode pattern in the fourth embodiment, it is an easiest method to increase or decrease, e.g., a dose during the exposure of the resist pattern. It is also possible to correct the size of a light shielding pattern (e.g., a chrome pattern) on a photo mask or the like. This obviates the necessity to increase or decrease the dose and reduces the number of the fabrication steps.

Although the fourth embodiment has assumed the formation of the gate electrode, the present invention is not limited thereto. The present invention achieves equally high formation accuracy even in the microfabrication of a layer having another linear pattern, e.g., the formation of metal wires composed of, e.g., aluminium, copper, or the like.

Embodiment 5

A semiconductor integrated circuit device and a method for fabricating the same according to a fifth embodiment of the present invention will be described with reference to the drawings. It is to be noted that the method for fabricating the semiconductor integrated circuit device according to the fifth embodiment assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern and at least one of fabrication process steps for the semiconductor integrated circuit devices is common. By way of example, a description will be given herein below to a method for forming gate electrodes in a system LSI in which memories such as DRAMs having a repetitive pattern can be merged.

FIGS. **5**A to **5**D are cross-sectional views illustrating the individual process steps of the method for fabricating the semiconductor integrated circuit device according to the fifth embodiment.

First, as shown in FIG. **5**A, a silicon oxide film **22** having a thickness of about 5 nm and serving as a gate insulating film is formed on a silicon substrate **21**. Then, a polysilicon film **23** having a thickness of about 200 nm and serving as the gate electrodes is formed on the silicon oxide film **22**. Thereafter, an organic coated film **24** having a thickness of about 100 nm and serving as a light-reflection preventing film in a lithographic step (see FIG. **5**B) is formed on the polysilicon film **23**.

Next, as shown in FIG. **5**B, a resist pattern **25** (with a thickness of about 600 nm) having a minimum line width (the objective size of the gate electrode) of 0.15 μm and corresponding to the gate electrodes **26** (see FIG. **5**D) having a linear pattern is formed on the organic coated film **24** by using a lithographic technique.

Next, as shown in FIG. **5**C, dry etching is performed with respect to the organic coated film **24** by using the resist pattern **25** as a mask.

If the semiconductor integrated circuit device is of a DRAM unmounted type, dry etching is performed by introducing, into a chamber in which a pressure is adjusted to, e.g., 10 Pa, an etching gas composed of a gas mixture of SO_2 gas and O_2 gas each at a flow rate of 20 cc/min and applying a radio-frequency power (RF power) of 200 W to a sample stage. If the semiconductor integrated circuit device is of a DRAM mounted type, dry etching is performed by introducing, into the chamber in which the pressure is adjusted to 10 Pa, an etching gas composed of a gas mixture of SO_2 gas at a flow rate of 25 cc/min and O_2 gas at a flow rate of 20 cc/min and applying an RF power of 200 W to a sample stage. In the present embodiment, a gas flow rate is expressed by using a flow rate per minute in a standard state (0° C., 1 atmospheric pressure).

Thus, in the dry etching step performed with respect to the organic coated film **24**, the etching condition is changed depending on the presence or absence of a mounted DRAM. Specifically, in the case of the DRAM mounted type, the flow rate of SO_2 gas having the effect of protecting a sidewall formed in the organic coated film **24** through etching is increased from 20 cc/min, which is used in the case of the DRAM unmounted type, to 25 cc/min. As a result, the organic coated film **24** can be patterned to have a desired size (0.15 μm) irrespective of the presence or absence of a mounted DRAM since a desired sidewall protecting effect per unit area is achievable even in the case where the area of the sidewall of the organic coated film **24** is increased by mounting a DRAM.

Next, dry etching is performed with respect to the polysilicon film **23** by using the resist pattern **25** or the patterned organic coated film **24** as a mask. Then, the resist pattern **25** and the organic coated film **24** are removed by ashing so that the gate electrodes **26** composed of the polysilicon film **23** are formed, as shown in FIG. **5**D. Since the organic coated film **24** has been patterned to have a desired size irrespective of the presence or absence of a mounted DRAM, the gate electrodes **26** having a desired size (0.15 μm) can be formed by preventing the occurrence of the CD loss.

In the dry etching step performed with respect to the polysilicon film **23**, dry etching is performed by introducing, into the chamber in which the pressure is adjusted to 20 Pa, an etching gas composed of a gas mixture of Cl_2 gas at a flow rate of 40 cc/min and HBr gas at a flow rate of 80 cc/min and applying an RF power of 300 W to the sample stage whether the semiconductor integrated circuit device is of the DRAM unmounted type or of the DRAM mounted type. In short, different facilities and conditions are used in the respective dry etching steps performed with respect to the polysilicon film **23** and to the organic coated film **24**.

Thus, according to the fifth embodiment, the etching condition is changed depending on the presence or absence of a mounted DRAM in the step of performing dry etching with respect to the organic coated film **24** by using the resist pattern **25** corresponding to the gate electrodes **26** each having the linear pattern. Specifically, in the case of the DRAM mounted type, the flow rate of SO_2 gas having the effect of protecting the sidewall formed in the organic coated film **24** through etching is increased compared with the case of the DRAM unmounted type. This achieves a desired sidewall protecting effect per unit area even in the case where the area of the sidewall of the organic coated film **24** is increased by mounting a DRAM, so that the organic coated film **24** is patterned to have a desired size. By performing dry etching with respect to the polysilicon film **23** by using the patterned organic coated film **24** as a mask, the gate electrodes **26** having a desired size can be formed. This ensures the suppression of size variations in gate electrodes **26** resulting from difference in mask pattern layout associated with the presence or absence of a mounted DRAM and allows high-precision formation of the gate electrodes.

FIG. **6** shows the relationship between the CD loss (value obtained by subtracting the size of the completed gate electrode from the size of the resist pattern prior to etching) and the DRAM area-occupying rate when various types of semiconductor integrated circuit devices having different DRAM area-occupying rates, including a DRAM unmounted type, are fabricated by using the method for fabricating semiconductor integrated circuit devices according to the fifth embodiment.

As shown in FIG. **6**, the fifth embodiment has achieved 0.15 m, which is the desired size of the gate electrode, by suppressing the occurrence of the CD loss irrespective of the presence or absence of a mounted DRAM.

FIG. **7** shows, as a comparative example, the relationship between the CD loss and the DRAM area-occupying rate when various types of semiconductor integrated circuit devices having different DRAM area-occupying rates, including a DRAM unmounted type, are fabricated by using the same etching condition irrespective of the presence or absence of a mounted DRAM.

As shown in FIG. **7**, the comparative example can suppress the occurrence of the CD loss in the DRAM unmounted type, while a CD loss of about 0.013 μm on average occurs in the DRAM mounted type.

Although the fifth embodiment has changed the etching condition for the organic coated film **24** depending on the presence or absence of a mounted DRAM (specifically, the flow rate of SO_2 gas having the effect of protecting the sidewall of the organic coated film **24**) and used the common etching condition for the polysilicon film **23** irrespective of the presence or absence of a mounted DRAM, it is also possible to use the common etching condition for the organic coated film **24** irrespective of the presence or absence of a mounted DRAM and change the etching condition for the polysilicon film **23** depending on the presence or absence of a mounted DRAM. In this case, it is also possible to change the flow rate of HBr gas for forming, e.g., an etching reaction product ($SiBr_4$ or the like) having the effect of protecting the sidewall of the polysilicon film **23** as the sidewall protecting film depending on the presence or absence of a mounted DRAM. If a structure in which a silicon dioxide film or the like is formed on a polysilicon film is used as a gate electrode structure, size variations in gate electrode resulting from the presence or absence of a mounted DRAM may also be suppressed by changing the etching condition for the silicon dioxide film.

Although the fifth embodiment has changed the etching condition depending on the presence or absence of a mounted DRAM, it is also possible to finely change the etching condition depending on the DRAM area-occupying rate.

Although the fifth embodiment has assumed the formation of the gate electrode, the present invention is not limited thereto. The present invention is also applicable to the formation of another linear pattern such as a metal wire.

Although the fifth embodiment has assumed the system LSI on which memories such as DRAMs can be mounted, the present invention is not limited thereto. The present invention is also applicable to a system LSI on which another group of elements composed of a plurality of semiconductor elements arranged in a repetitive pattern can be mounted.

Embodiment 6

A semiconductor integrated circuit device and a method for fabricating the same according to a sixth embodiment of the present invention will be described with reference to the drawings. It is to be noted that the method for fabricating the semiconductor integrated circuit device according to the sixth embodiment assumes a method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern and at least one of fabrication process steps for the semiconductor integrated circuit devices is common. By way of example, a description will be given herein below to a method for forming a gate electrode in a system LSI in which memories such as DRAMs having a repetitive pattern can be merged. Similarly to the fifth embodiment, FIGS. **5**A to **5**D illustrate the individual process steps of the method for fabricating the semiconductor integrated circuit device according to the sixth embodiment.

The sixth embodiment is different from the fifth embodiment as follows. The fifth embodiment has changed the etching condition depending on the presence or absence of a mounted DRAM in the step of performing dry etching with respect to the organic coated film **24** by using, as a mask, the resist pattern **25** corresponding to the gate electrodes **26** having the linear pattern (see FIGS. **5**C and **5**D). By contrast, the sixth embodiment changes the size of the resist pattern **25** in accordance with the DRAM area-occupying rate in the step of forming the resist pattern **25** (see FIG. **5**B).

Specifically, the sixth embodiment predetermines the relationship between the CD loss (a value obtained by subtracting the size of the completed gate electrode from the size of the resist pattern prior to etching from) and the DRAM area-occupying area and thereby determines the size of the resist pattern by using, e.g., the following expression:

(Size of Resist Pattern)=(Expected Value of *CD* Loss Corresponding to *DRAM* Area-occupying rate)+(objective Size of Gate Electrode).

As shown in FIG. **7**, the CD loss increases as the DRAM area-occupying rate increases. In accordance with the foregoing expression, therefore, the size of the resist pattern **25** is increased as the DRAM area-occupying rate increases, whereby the sixth embodiment achieves the following effect. That is, even if the area of a sidewall formed in the polysilicon film **23** or the organic coated film **24** through etching using the resist pattern **25** as a mask increases as the DRAM area-occupying rate increases and the sidewall protecting effect per unit area decreases accordingly, the decrement in sidewall protecting effect can be compensated for by adjusting the size of the resist pattern **25**. This ensures the suppression of variations in the size of the gate electrode **26** resulting from difference in mask pattern layout associated with different DRAM area-occupying rates and thereby allows high-precision formation of the gate electrode.

Table 3 shows the size of the resist pattern for forming the gate electrode having the objective size of 0.15 μm when various types of semiconductor integrated circuit devices with different DRAM occupying-area rates, including a DRAM unmounted type, are fabricated by using the method for fabricating semiconductor integrated circuit devices according to the sixth embodiment. For reference purposes, Table 3 shows expected values of the CD loss corresponding to the individual DRAM area-occupying rates.

TABLE 3

DRAM Area-occupying rate R (%)	CD Loss (μm)	Size of Resist Pattern (μm)
R = 0	0.000	0.150
0<R≦20	0.008	0.158
20<R≦40	0.016	0.166
40<R≦60	0.024	0.174

By determining the size of the resist pattern **25** as shown in Table 3, the sixth embodiment has achieved 0.15 μm which is the desired size of the gate electrode irrespective of the DRAM area-occupying rate.

Although the sixth embodiment has changed the size of the resist pattern **25** in accordance with the DRAM area-occupying rate, it is also possible to coarsely change the size of the resist pattern **25** depending on the presence or absence of a mounted DRAM instead.

In the sixth embodiment, it is also possible to use, e.g., a method of adjusting a dose or adjusting the size of a mask pattern on a reticle as a specific method for adjusting the size of the resist pattern **25**.

Although the sixth embodiment has assumed the formation of the gate electrode, the present invention is not limited thereto. The present invention is also applicable to the formation of another linear pattern such as a metal wire.

Although the sixth embodiment has assumed the system LSI on which memories such as DRAMs can be mounted, the present invention is not limited thereto. The present invention is also applicable to a system LSI on which another group of elements composed of a plurality of semiconductor elements arranged in a repetitive pattern can be mounted.

What is claimed is:

1. A semiconductor integrated circuit device comprising:

a first circuit pattern having a first linear pattern and placed in a region in which a group of elements having a repetitive pattern are formed; and

a second circuit pattern having a second linear pattern and placed in a region in which components other than the group of elements are formed,

a dummy pattern being inserted in the region in which the second circuit pattern is placed such that a sum perimeter of the first linear pattern, the second linear pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first linear pattern per unit area.

2. The semiconductor integrated circuit device of claim **1**, wherein the group of elements are memories.

3. The semiconductor integrated circuit device of claim **1**, wherein a perimeter of the dummy pattern per unit area is 70% or more of the perimeter of the first linear pattern per unit area.

4. A semiconductor integrated circuit device comprising:

a first circuit pattern having a first gate electrode pattern and placed in a memory circuit region; and

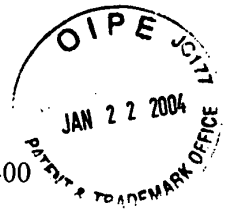
a second circuit pattern having a second gate electrode pattern and placed in a logic circuit region,

a dummy pattern being inserted in the logic region in which the second circuit pattern is placed such that a sum perimeter of the first gate electrode pattern, the second gate electrode pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first gate electrode pattern per unit area.

5. The semiconductor integrated circuit device of claim **4**, wherein the dummy pattern has a rectangular like shape.

6. The semiconductor integrated circuit device of claim **4**, wherein the perimeter of the dummy pattern per unit area is 70% or more of the perimeter of the first gate electrode pattern per unit area.

* * * * *



Docket No.: 60188-400 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
TAMAKI, TOKUHIKO, et al.	:	Confirmation Number: 1307
Serial No.: 09/964,868	:	Group Art Unit: 1765
Filed: September 28, 2001	:	Examiner: DUY VU NGUYEN DEO

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD FOR FABRICATING THE SAME

AMENDMENT

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated October 22, 2003, having a three-month shortened statutory period for response set to expire on January 22, 2004, reconsideration of the above-identified application is respectfully requested in view of the following remarks.

AMENDMENT TO THE CLAIMS

1-3. (Canceled)

4. (Original) A semiconductor integrated circuit device comprising:

a first circuit pattern having a first linear pattern and placed in a region in which a group of elements having a repetitive pattern are formed; and

a second circuit pattern having a second linear pattern and placed in a region in which components other than the group of elements are formed,

a dummy pattern being inserted in the region in which the second circuit pattern is placed such that a sum perimeter of the first linear pattern, the second linear pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first linear pattern per unit area.

5. (Original) The semiconductor integrated circuit device of claim 4, wherein the group of elements are memories.

6. (Original) The semiconductor integrated circuit device of claim 4, wherein a perimeter of the dummy pattern per unit area is 70% or more of the perimeter of the first linear pattern per unit area.

7-16. (Canceled)

17. (New) A semiconductor integrated circuit device comprising:

a first circuit pattern having a first gate electrode pattern and placed in a memory circuit region; and

a second circuit pattern having a second gate electrode pattern and placed in a logic circuit region,

a dummy pattern being inserted in the logic region in which the second circuit pattern is placed such that a sum perimeter of the first gate electrode pattern, the second gate electrode pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first gate electrode pattern per unit area.

18. (New) The semiconductor integrated circuit device of claim 17, wherein the dummy pattern has a rectangular like shape.

19. (New) The semiconductor integrated circuit device of claim 17, wherein the perimeter of the dummy pattern per unit area is 70% or more of the perimeter of the first gate electrode pattern per unit area.

REMARKS

As a preliminary matter, it is noted that the Examiner has not provided Applicants an initialed copy of the Information Disclosure Statement filed on September 28, 2001 nor the Information Disclosure Statement filed on October 21, 2003. Attached hereto are copies of the referenced IDS's with stamped-post cards showing receipt by the USPTO. It is respectfully requested that the Examiner provide initialed copies of the referenced IDS's indicating that each reference cited in each IDS has been considered and made formally of record.

The indication of allowable subject matter in claims 4-6 is acknowledged and appreciated. Accordingly, solely in order to expedite prosecution, claims 1-3 and non-elected claims 7-16 have been canceled without prejudice or disclaimer. New independent claim 17 (and its dependent claims) is submitted to be allowable for at least reasons generally similar to those rendering claim 4 allowable.

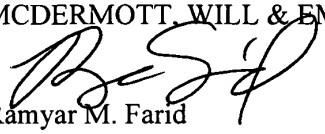
CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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US006709950B2

(12) **United States Patent**
Segawa et al.

(10) **Patent No.: US 6,709,950 B2**
(45) **Date of Patent: Mar. 23, 2004**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

(75) Inventors: **Mizuki Segawa**, Osaka (JP); **Isao Miyanaga**, Osaka (JP); **Toshiki Yabu**, Osaka (JP); **Takashi Nakabayashi**, Osaka (JP); **Takashi Uehara**, Osaka (JP); **Kyoji Yamashita**, Osaka (JP); **Takaaki Ukeda**, Osaka (JP); **Masatoshi Arai**, Osaka (JP); **Takayuki Yamada**, Osaka (JP); **Michikazu Matsumoto**, Osaka (JP)

(73) Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/902,157**

(22) Filed: **Jul. 11, 2001**

(65) **Prior Publication Data**

US 2001/0054741 A1 Dec. 27, 2001

Related U.S. Application Data

(62) Division of application No. 08/685,726, filed on Jul. 24, 1996, now Pat. No. 6,281,562.

(30) **Foreign Application Priority Data**

Jul. 27, 1995 (JP) 7-192181
Dec. 19, 1995 (JP) 7-330112

(51) **Int. Cl.**[7] **H01L 29/167**
(52) **U.S. Cl.** **438/424**; 438/359; 257/304; 257/510; 257/774
(58) **Field of Search** 438/359, 424, 438/425, 426; 257/304, 311, 382, 510, 774

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Primary Examiner—Amir Zarabian
Assistant Examiner—Jeff Vockrodt
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

An isolation which is higher in a stepwise manner than an active area of a silicon substrate is formed. On the active area, an FET including a gate oxide film, a gate electrode, a gate protection film, sidewalls and the like is formed. An insulating film is deposited on the entire top surface of the substrate, and a resist film for exposing an area stretching over the active area, a part of the isolation and the gate protection film is formed on the insulating film. There is no need to provide an alignment margin for avoiding interference with the isolation and the like to a region where a connection hole is formed. Since the isolation is higher in a stepwise manner than the active area, the isolation is prevented from being removed by over-etch in the formation of a connection hole to come in contact with a portion where an impurity concentration is low in the active area. In this manner, the integration of a semiconductor device can be improved and an area occupied by the semiconductor device can be decreased without causing degradation of junction voltage resistance and increase of a junction leakage current in the semiconductor device.

22 Claims, 21 Drawing Sheets

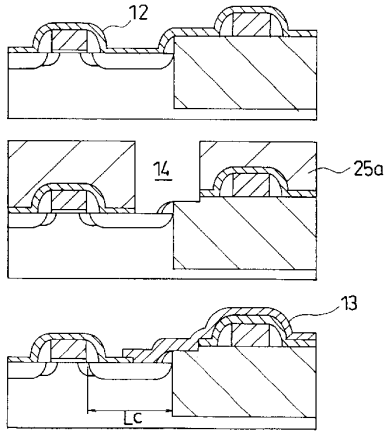

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FIG. 1(a)

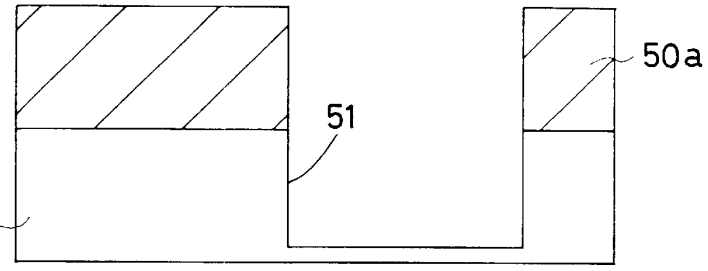


FIG. 1(b)

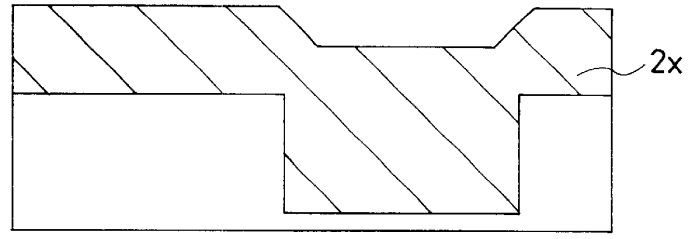


FIG. 1(c)

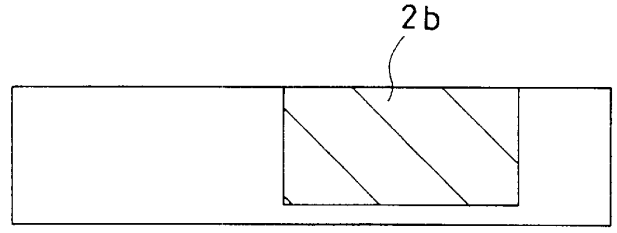


FIG. 1(d)

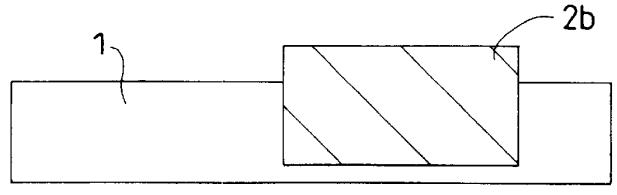


FIG. 2(a)

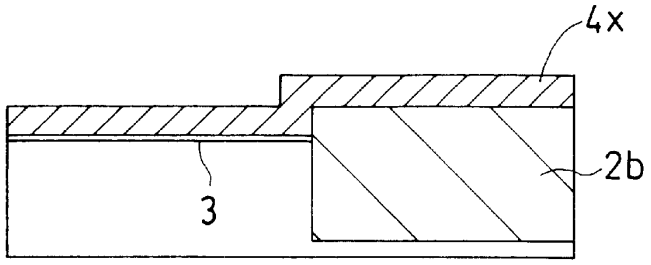


FIG. 2(b)

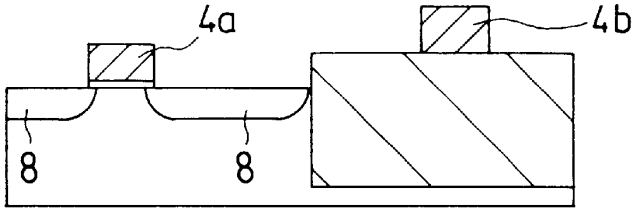


FIG. 2(c)

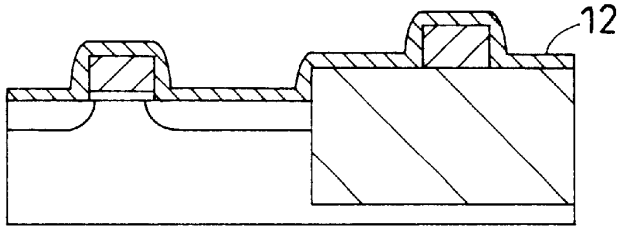


FIG. 2(d)

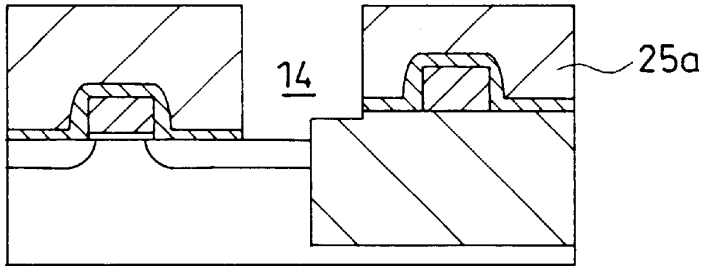


FIG. 2(e)

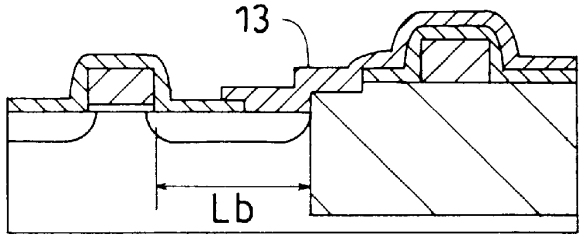


FIG. 3(a)

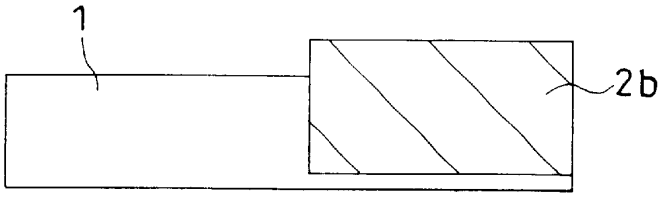


FIG. 3(b)

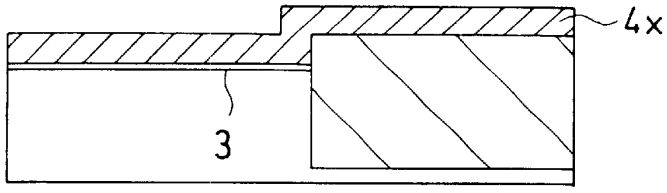


FIG. 3(c)

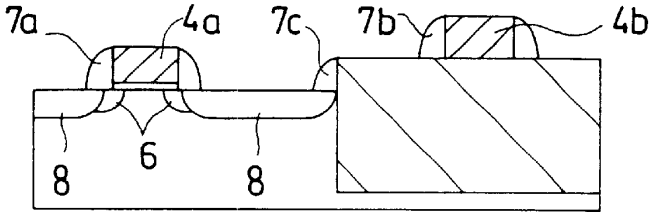


FIG. 3(d)

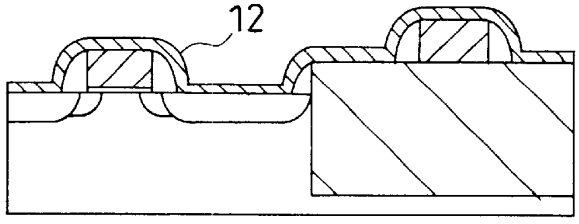


FIG. 3(e)

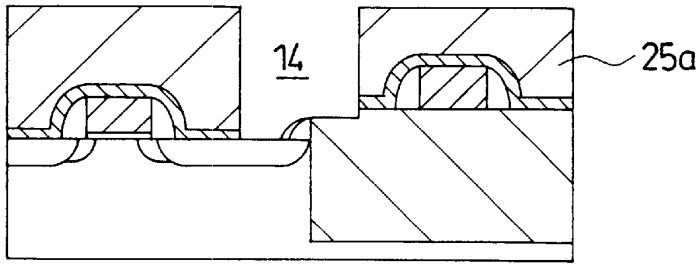


FIG. 3(f)

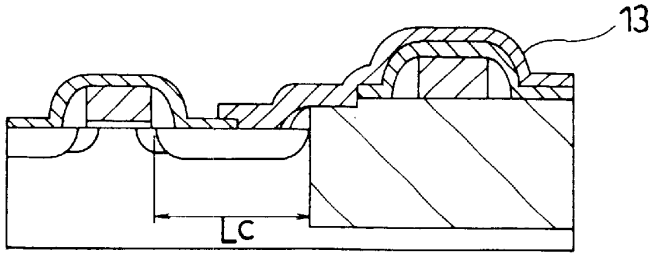


FIG. 4(a)

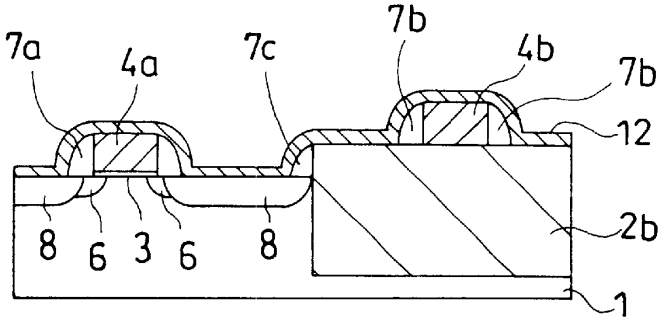


FIG. 4(b)

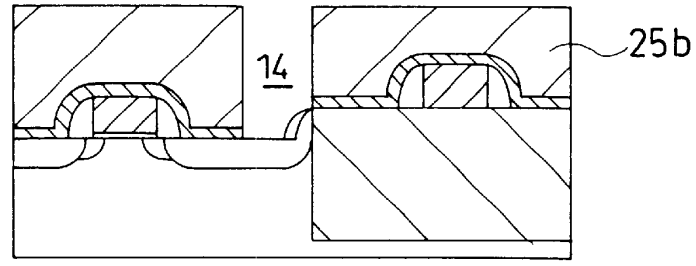


FIG. 4(c)

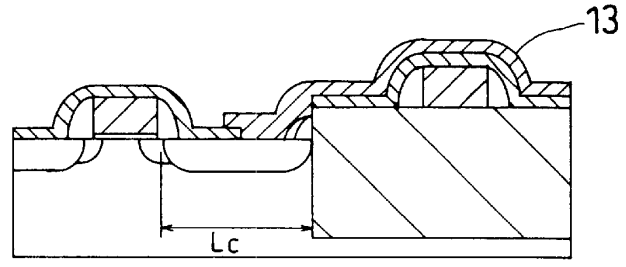


FIG. 5(a)

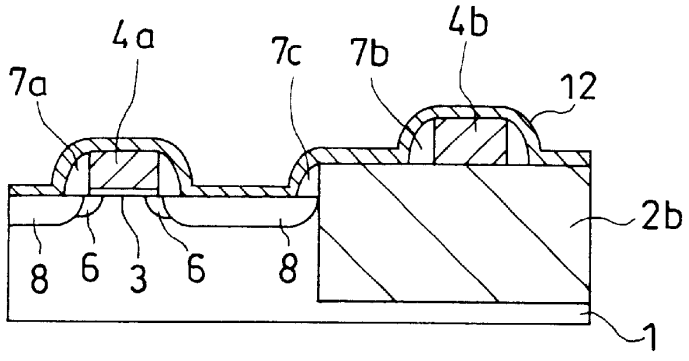
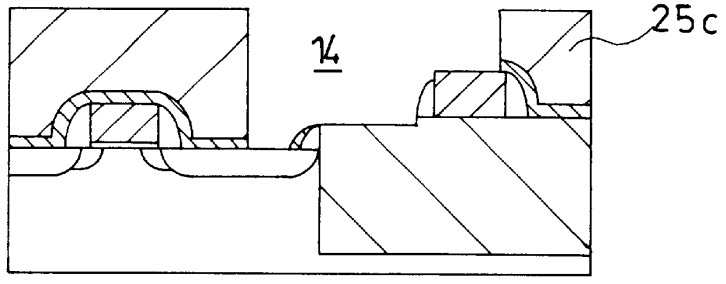


FIG. 5(b)



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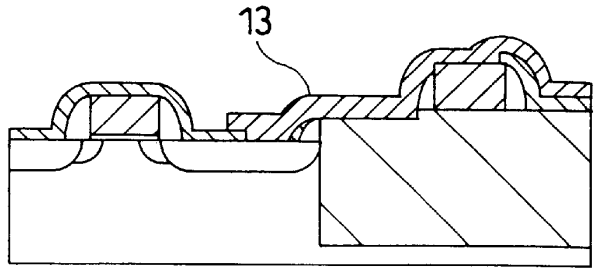


FIG. 6(a)

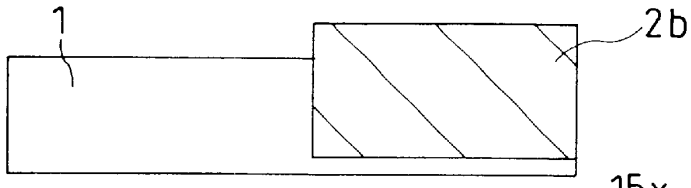


FIG. 6(b)

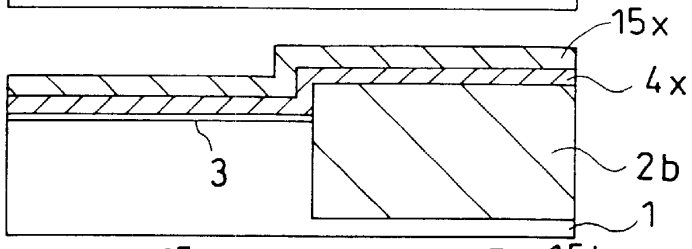


FIG. 6(c)

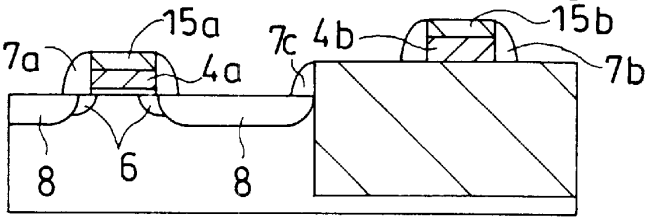


FIG. 6(d)

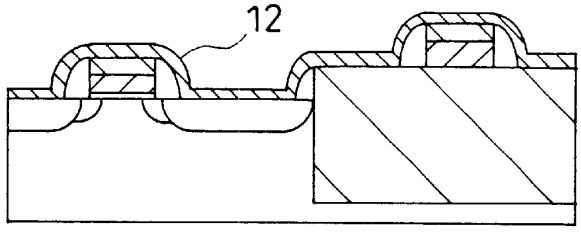


FIG. 6(e)

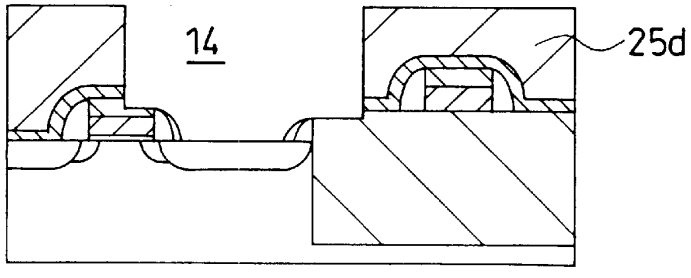


FIG. 6(F)

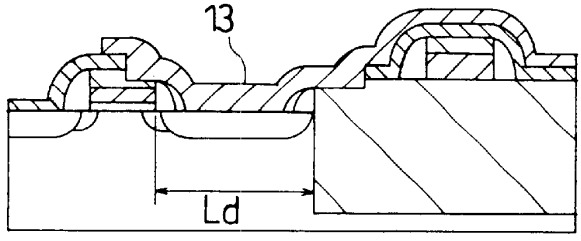


FIG. 7(a)

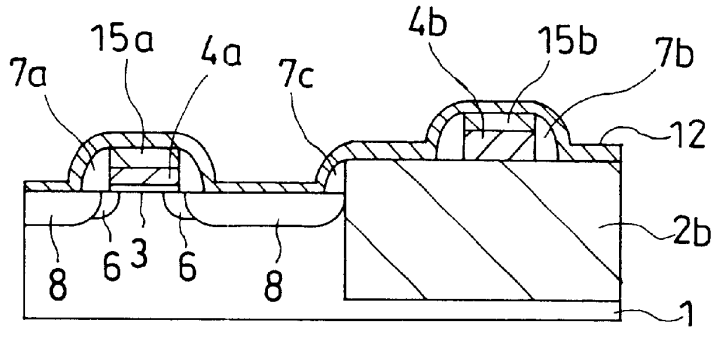


FIG. 7(b)

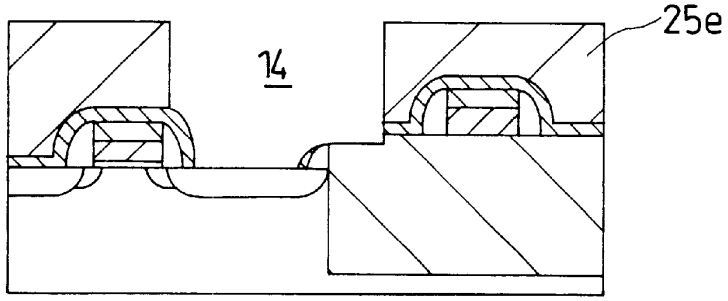


FIG. 7(c)

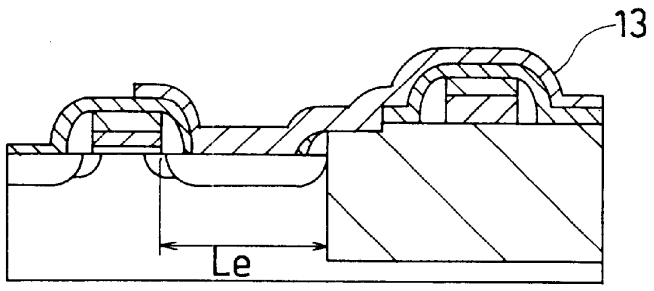


FIG. 8(a)

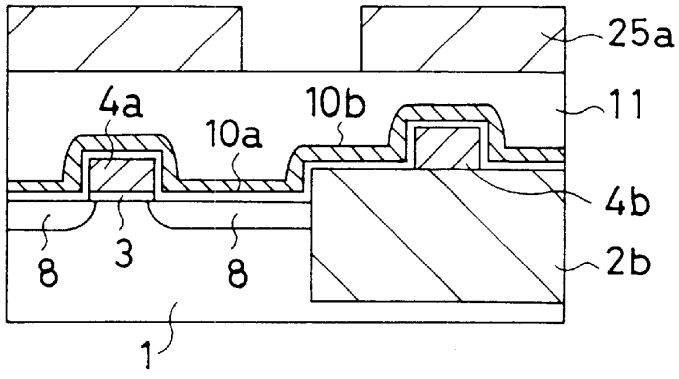


FIG. 8(b)

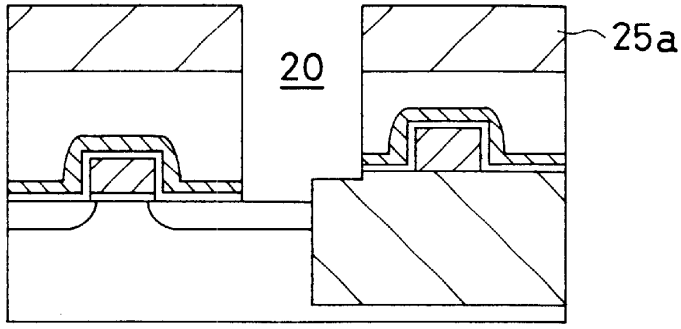


FIG. 8(c)

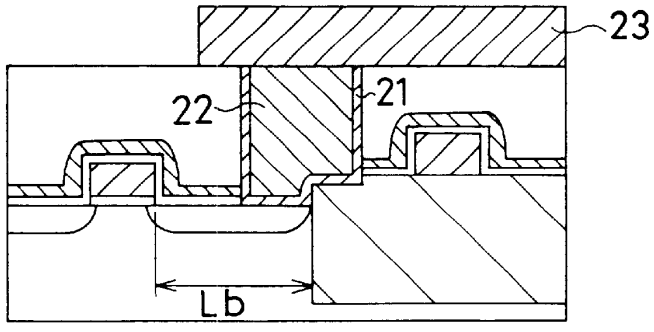


FIG. 9(a)

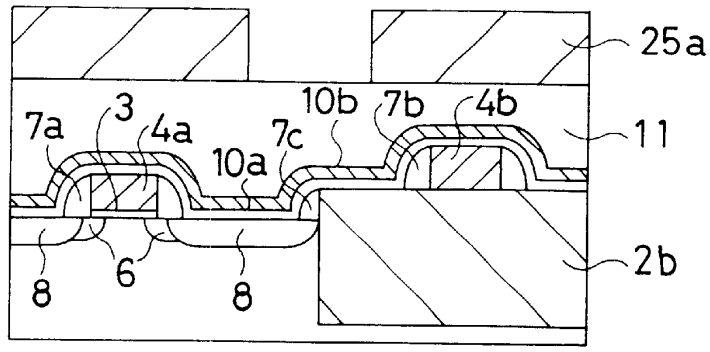


FIG. 9(b)

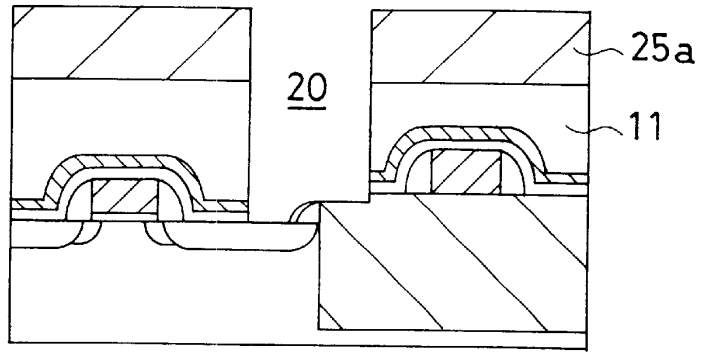


FIG. 9(c)

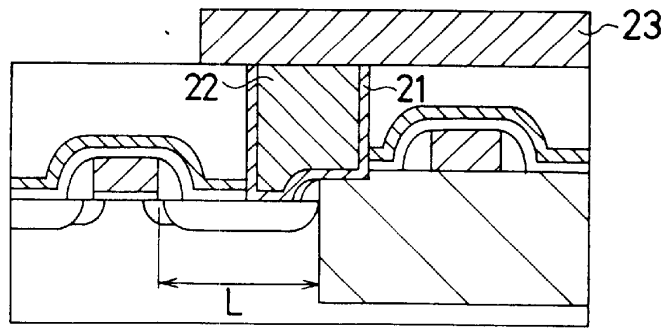


FIG. 10(a)

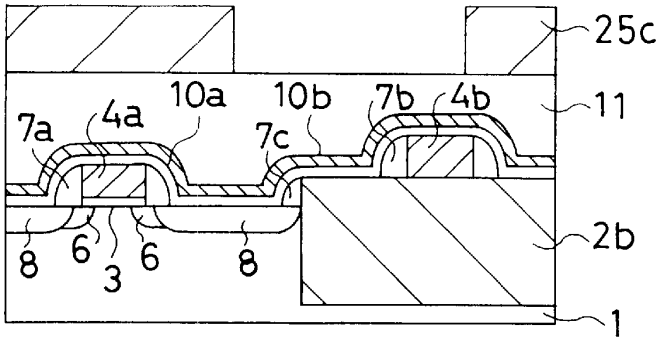


FIG. 10(b)

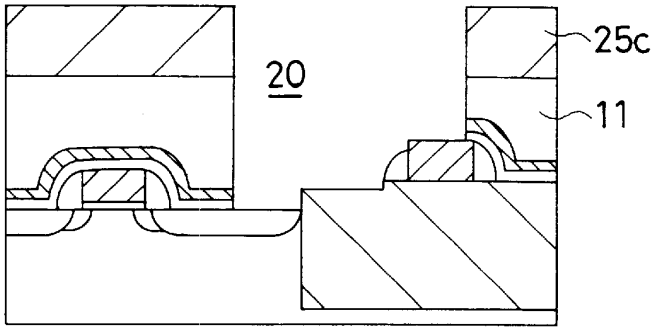


FIG. 10(c)

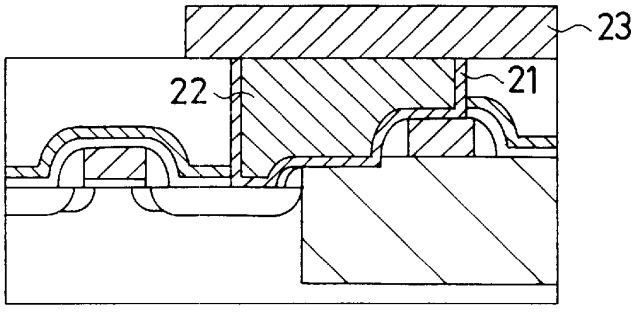


FIG. 11(a)

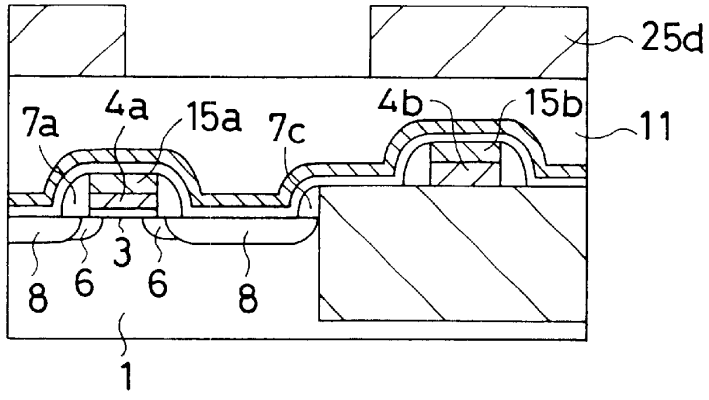


FIG. 11(b)

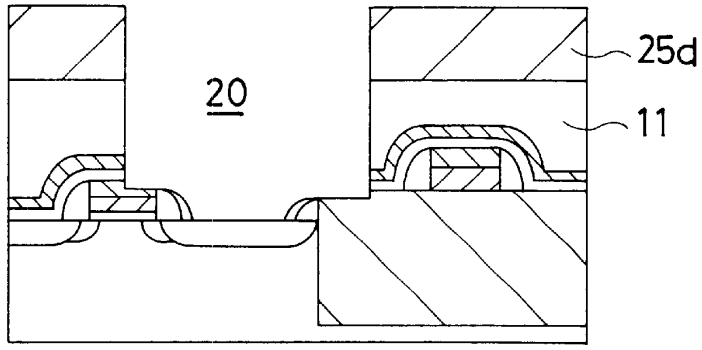


FIG. 11(c)

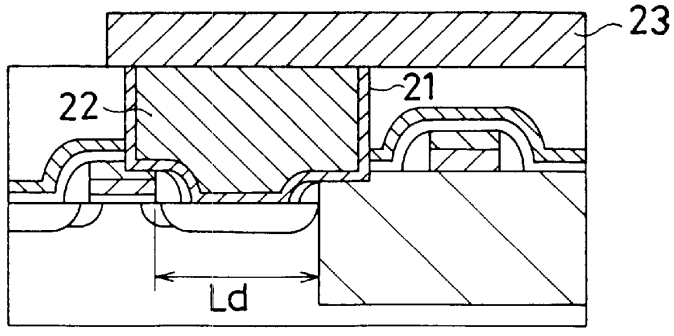


FIG. 12

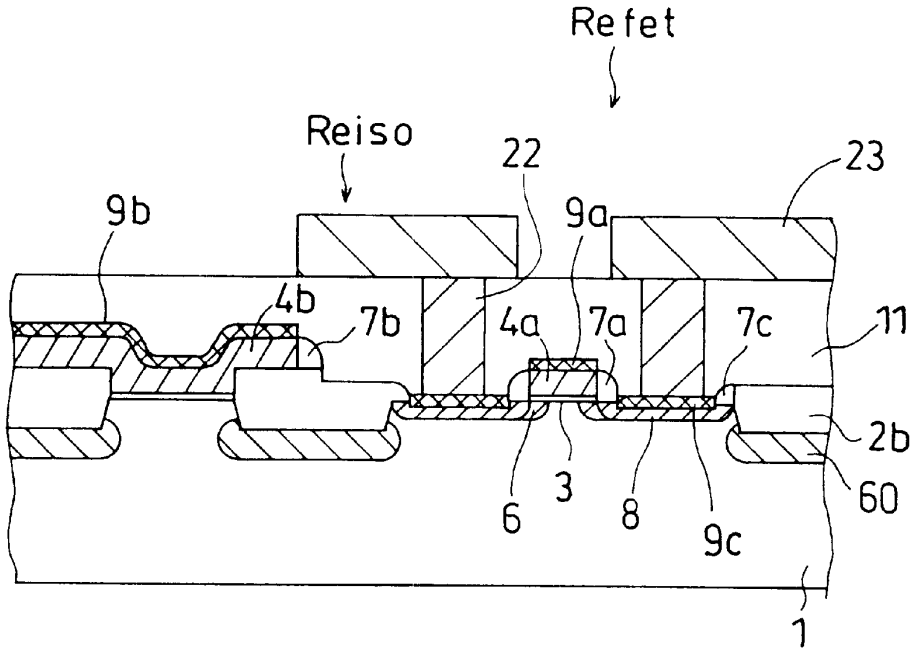


FIG. 13(a)

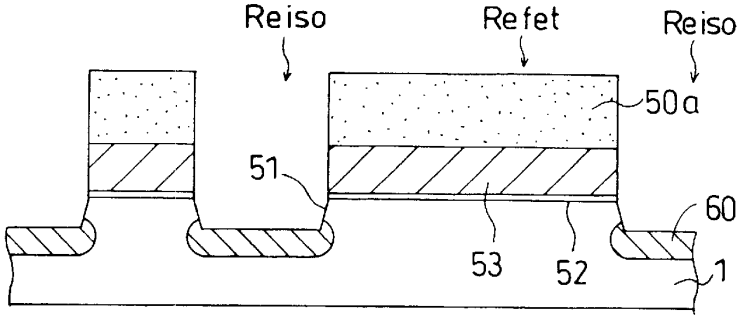


FIG. 13(b)

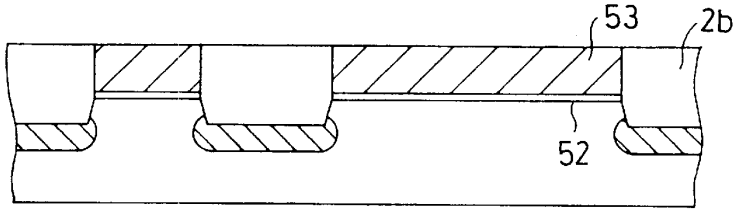


FIG. 13(c)

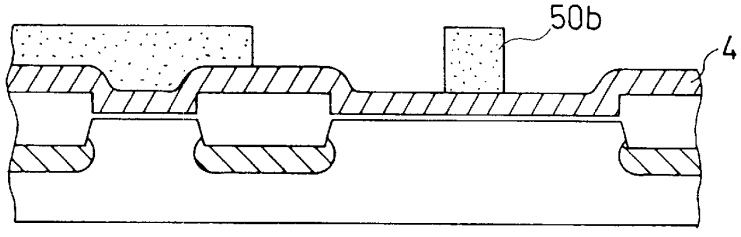


FIG. 13(d)

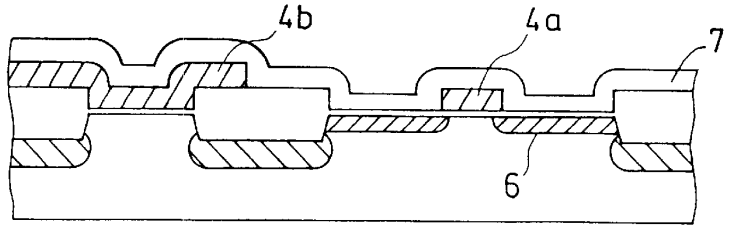


FIG. 13(e)

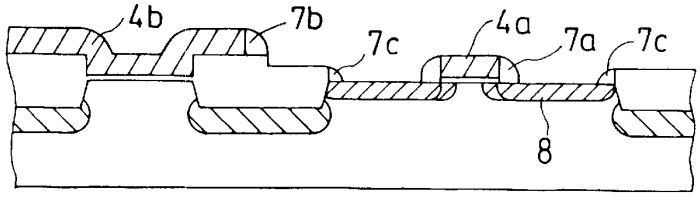


FIG. 14(a)

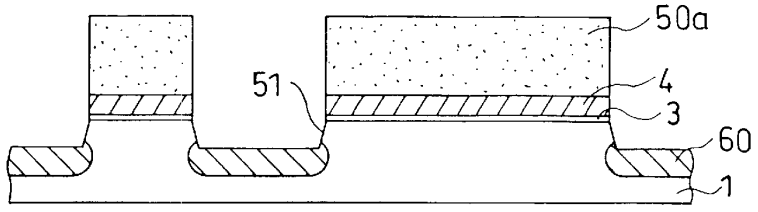


FIG. 14(b)

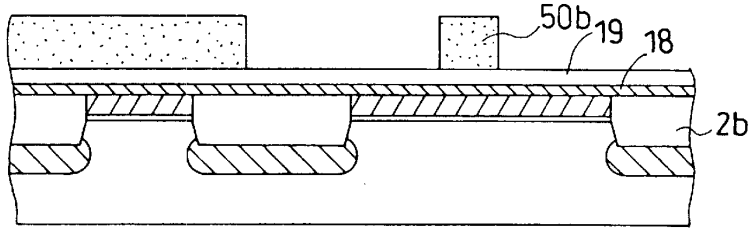


FIG. 14(c)

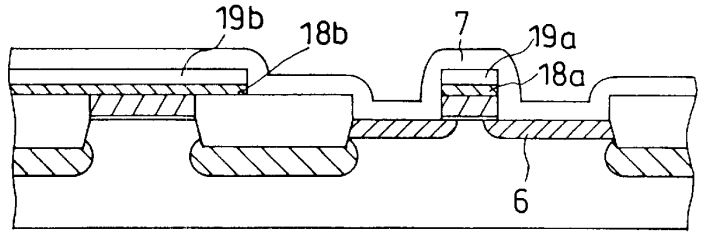


FIG. 14(d)

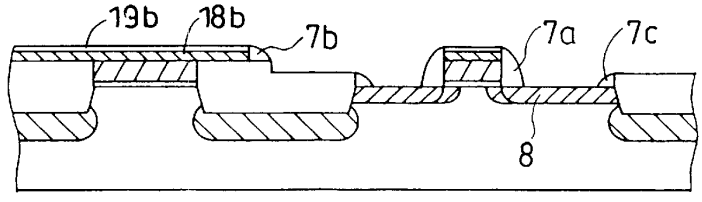


FIG. 14(e)

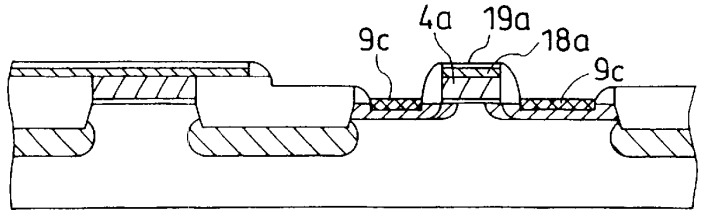


FIG. 15(a)

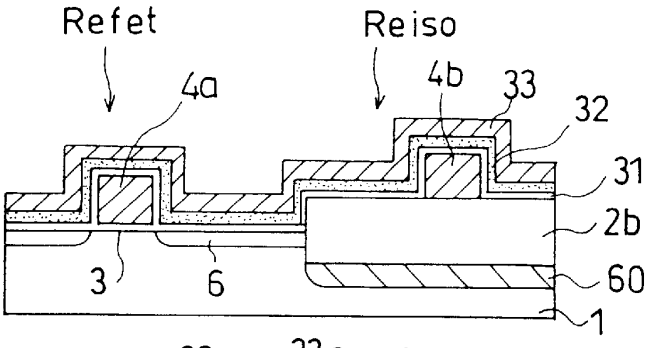


FIG. 15(b)

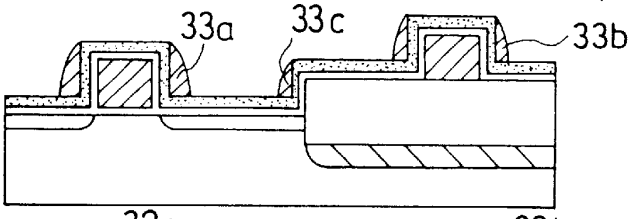


FIG. 15(c)

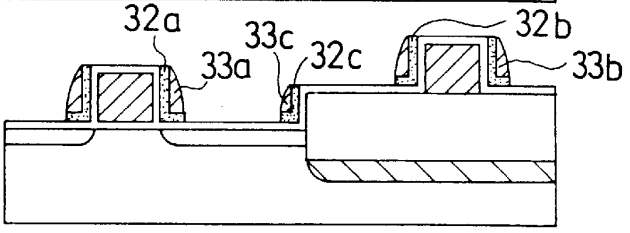


FIG. 15(d)

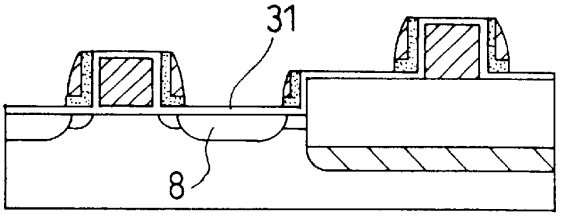


FIG. 15(e)

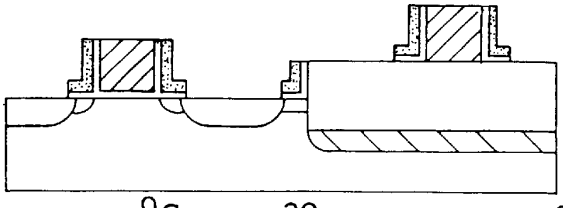


FIG. 15(f)

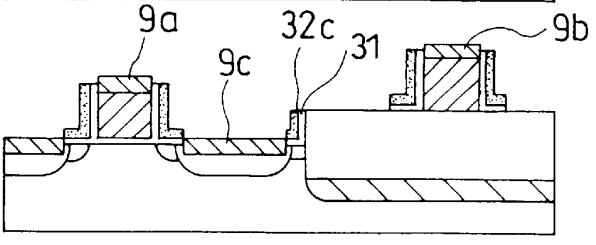


FIG. 16(a)

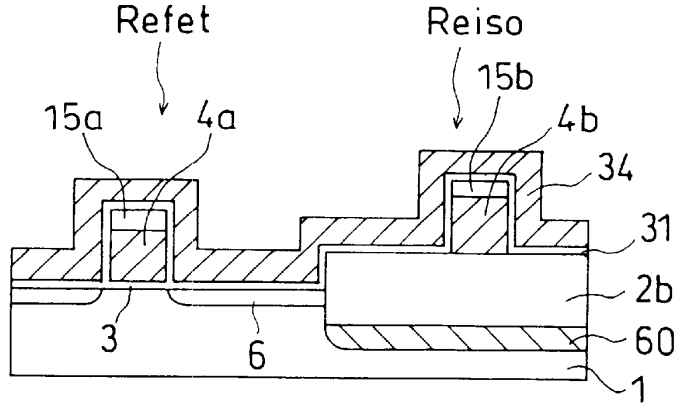


FIG. 16(b)

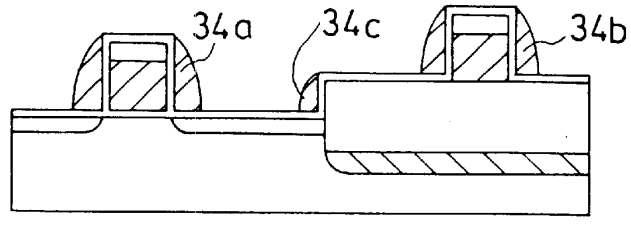


FIG. 16(c)

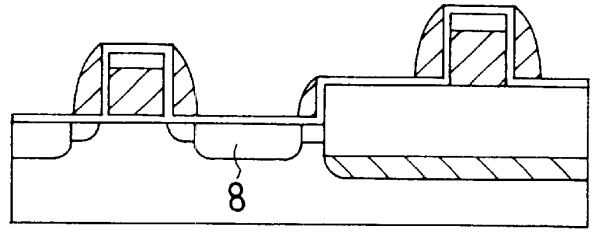


FIG. 16(d)

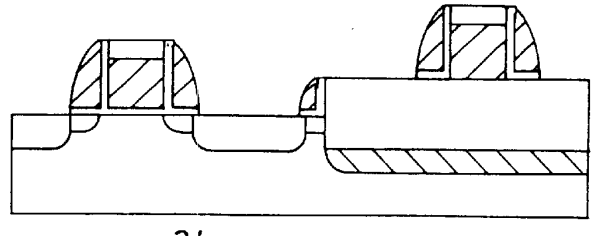


FIG. 16(e)

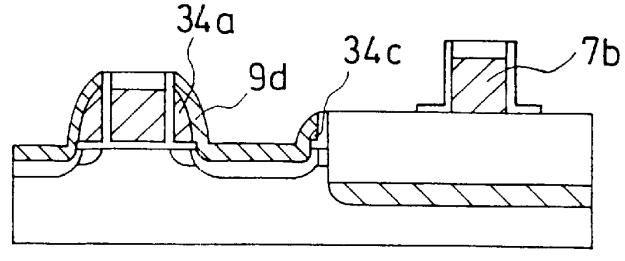


FIG. 17
PRIOR ART

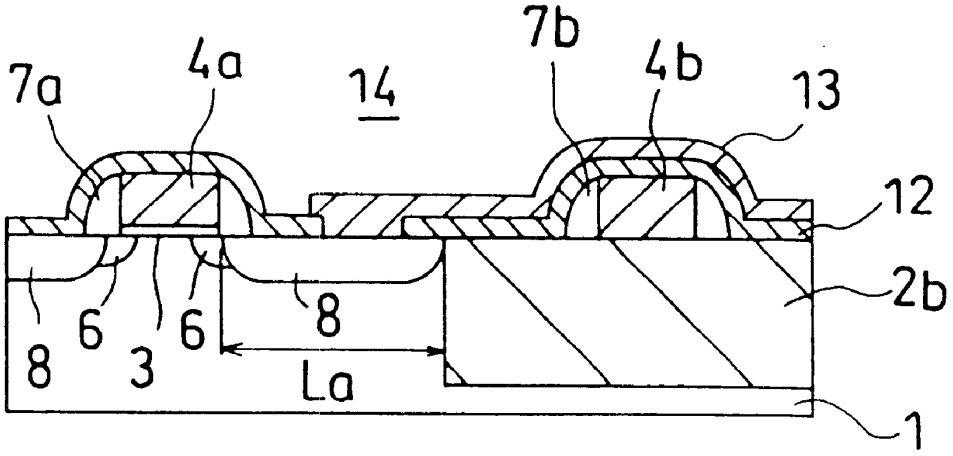


FIG. 18(a)
PRIOR ART

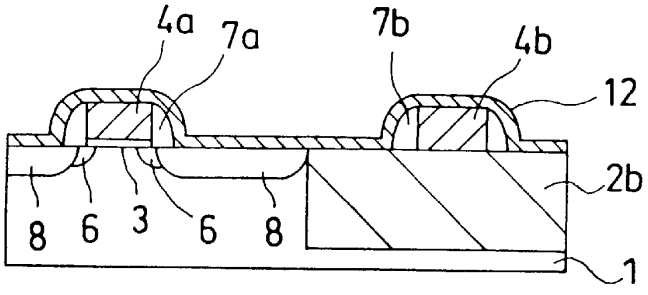


FIG. 18(b)
PRIOR ART

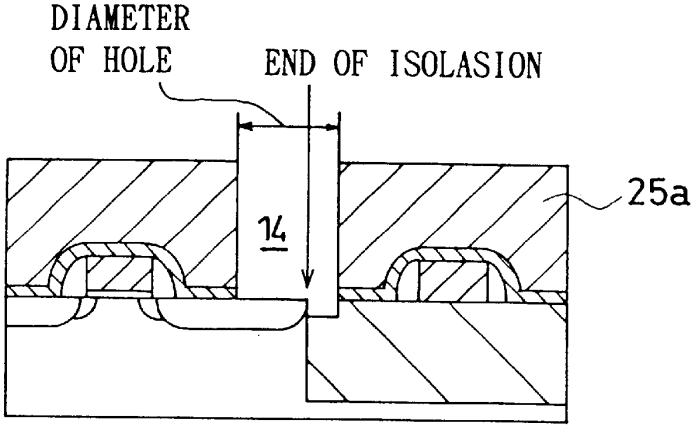


FIG. 18(c)
PRIOR ART

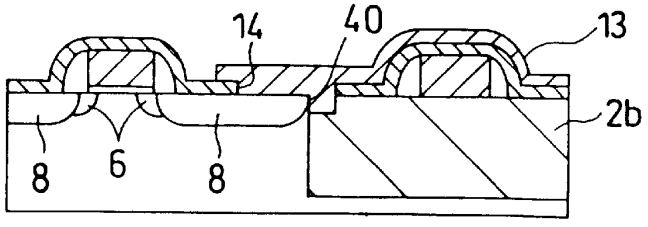
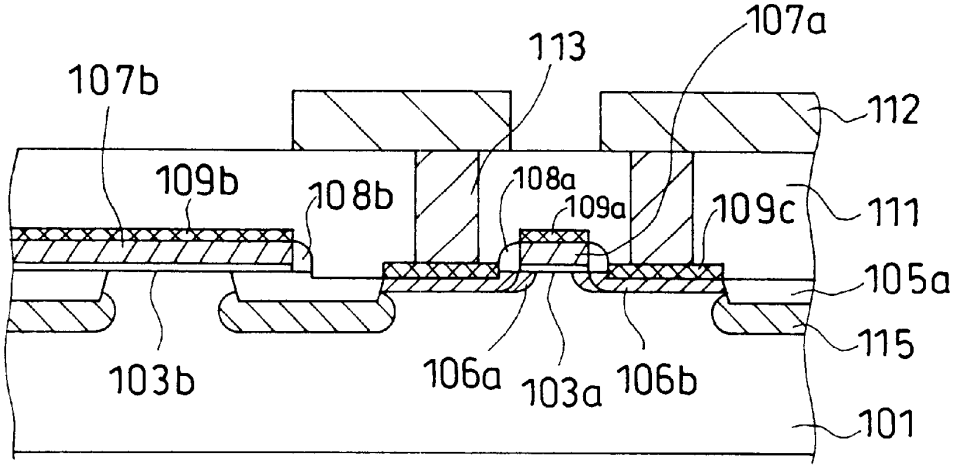


FIG. 19
PRIOR ART



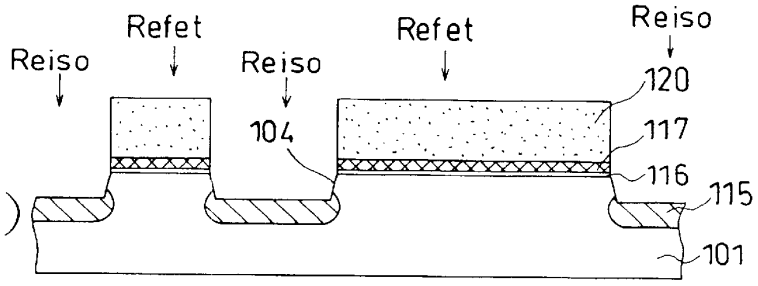


FIG. 20(a)
PRIOR ART

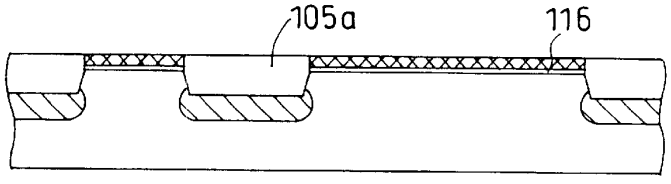


FIG. 20(b)
PRIOR ART

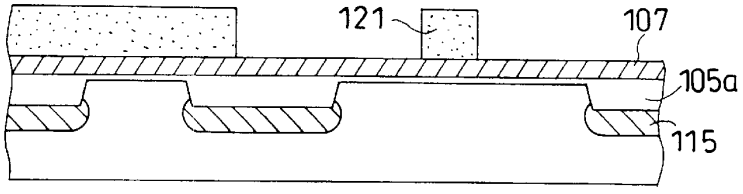


FIG. 20(c)
PRIOR ART

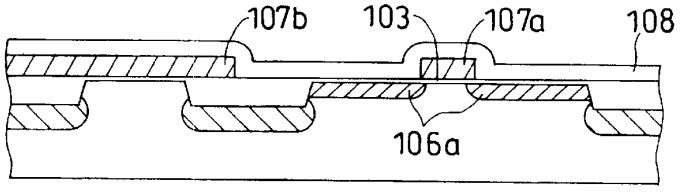


FIG. 20(d)
PRIOR ART

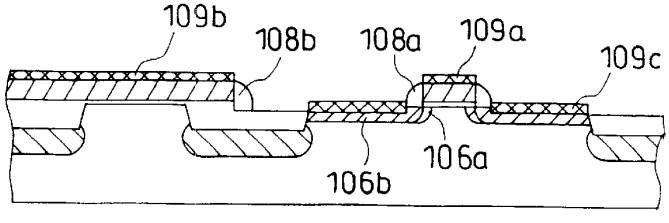


FIG. 20(e)
PRIOR ART

FIG. 21(a)
PRIOR ART

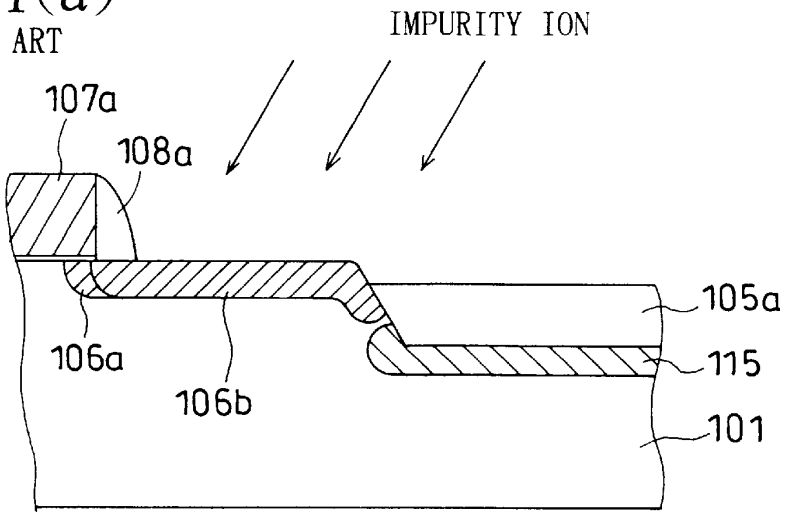
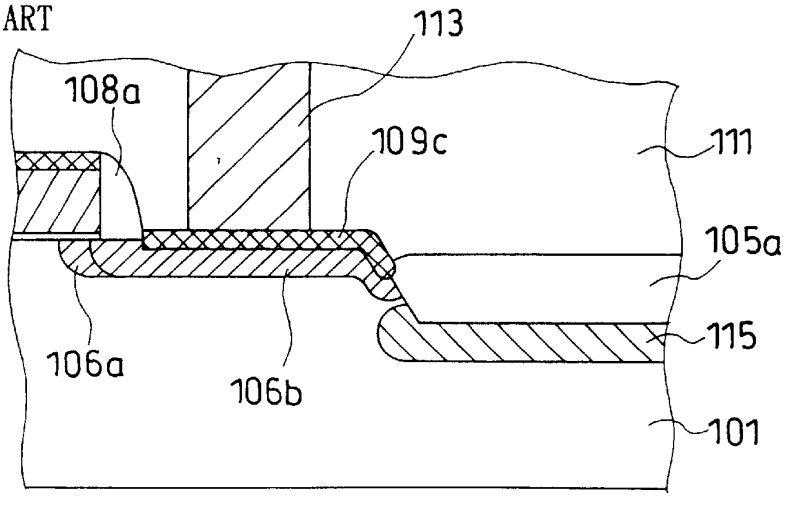


FIG. 21(b)
PRIOR ART



SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

This application is a divisional of application Ser. No. 08/685,726 filed Jul. 24, 1996, now U.S. Pat. No. 6,281,562.

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device including transistors and connection between the transistors for constituting an LSI with high integration and a decreased area.

With the recent development of a semiconductor device with high integration and high performance, there are increasing demands for more refinement of the semiconductor device. The improvement of the conventional techniques cannot follow these demands, and novel techniques are unavoidably introduced in some technical fields. For example, as a method of forming an isolation, the LOCOS isolation method is conventionally adopted in view of its simpleness and low cost. Recently, however, it is considered that a trench buried type isolation (hereinafter referred to as the trench isolation) is more advantageous for manufacturing a refined semiconductor device.

Specifically, in the LOCOS isolation method, since selective oxidation is conducted, the so-called bird's beak occurs in the boundary with a mask for preventing the oxidation. As a result, the dimension of a transistor is changed because an insulating film of the isolation invades a transistor region against the actually designed mask dimension. This dimensional change is unallowable in the refinement of a semiconductor device after the 0.5 μm generation. Therefore, even in the mass-production techniques, the isolation forming method has started to be changed to the trench isolation method in which the dimensional change is very small. For example, IBM corporation has introduced the trench isolation structure as a 0.5 μm CMOS process for the mass-production of an MPU (IBM Journal of Research and Development, VOL. 39, No. 1/2, 1995, pp. 33–42).

Furthermore, in a semiconductor device mounting elements such as a MOSFET in an active area surrounded with an isolation, an insulating film is deposited on the active area, the isolation and a gate electrode, and a contact hole is formed by partly exposing the insulating film for connection between the active area and an interconnection member on a layer above the insulating film. This structure is known as a very common structure for the semiconductor device.

FIG. **17** is a sectional view for showing the structure of a conventional semiconductor device. In FIG. **17**, a reference numeral **1** denotes a silicon substrate, a reference numeral **2***b* denotes an isolation with a trench isolation structure which is made of a silicon oxide film and whose top surface is flattened so as to be at the same level as the top surface of the silicon substrate **1**, a reference numeral **3** denotes a gate oxide film made of a silicon oxide film, a reference numeral **4***a* denotes a polysilicon electrode working as a gate electrode, a reference numeral **4***b* denotes a polysilicon interconnection formed simultaneously with the polysilicon electrode **4***a,* a reference numeral **6** denotes a low-concentration source/drain region formed by doping the silicon substrate with an n-type impurity at a low concentration, a reference numeral **7***a* denotes an electrode sidewall, a reference numeral **7***b* denotes an interconnection sidewall, a reference numeral **8** denotes a high-concentration source/drain region formed by doping the silicon substrate with an n-type impurity at a high concentration, a reference numeral **12** denotes an insulating film made of a silicon oxide film, and a reference numeral **13** denotes a local interconnection made of a polysilicon film formed on the insulating film **12**.

The local interconnection **13** is also filled within a connection hole **14** formed in a part of the insulating film **12**, so as to be contacted with the source/drain region in the active area through the connection hole **14**. In this case, the connection hole **14** is formed apart from the isolation **2***b* by a predetermined distance. In other words, in the conventional layout rule for such a semiconductor device, there is a rule that the edge of a connection hole is previously located away from the boundary between the active area and the isolation region so as to prevent a part of the connection hole **14** from stretching over the isolation **2***b* even when a mask alignment shift is caused in photolithography (this distance between the connection hole and the isolation is designated as an alignment margin).

However, in the structure of the semiconductor device as shown in FIG. **17**, there arise problems in the attempts to further improve the integration for the following reason:

A distance La between the polysilicon electrode **4***a* and the isolation **2***b* is estimated as an index of the integration. In order to prevent the connection hole **14** from interfering the isolation **2***b* as described above, the distance La is required to be 1.2 μm, namely, the sum of the diameter of the connection hole **14**, that is, 0.5 μm, the width of the electrode sidewall **7***a,* that is, 0.1 μm, the alignment margin from the polysilicon electrode **4***a,* that is, 0.3 μm, and the alignment margin from the isolation **2***b*, that is, 0.3 μm. A connection hole has attained a more and more refined diameter with the development of processing techniques, and also a gate length has been decreased as small as 0.3 μm or less. Still, the alignment margin in consideration of the mask alignment shift in the photolithography is required to be approximately 0.3 μm. Accordingly, as the gate length and the connection hole diameter are more refined, the proportion of the alignment margin is increased. This alignment margin has become an obstacle to the high integration.

Therefore, attempts have been made to form the connection hole **14** without considering the alignment margin in view of the alignment shift in the photolithography. Manufacturing procedures adopted in such a case will now be described by exemplifying an n-channel MOSFET referring to FIGS. **18**(*a*) through **18**(*c*).

First, as is shown in FIG. **18**(*a*), after forming an isolation **2***b* having the trench structure in a silicon substrate **1** doped with a p-type impurity (or p-type well), etch back or the like is conducted for flattening so as to place the surfaces of the isolation **2***b* and the silicon substrate **1** at the same level. In an active area surrounded with the isolation **2***b,* a gate oxide film **3**, a polysilicon electrode **4***a* serving as a gate electrode, an electrode sidewall **7***a,* a low-concentration source/drain region **6** and a high-concentration source/drain region **8** are formed. On the isolation **2***b* are disposed a polysilicon interconnection **4***b* formed simultaneously with the polysilicon electrode **4***a* and an interconnection sidewall **7***b.* At this point, the top surface of the high-concentration source/drain region **8** in the active area is placed at the same level as the top surface of the isolation **2***b.* Then, an insulating film **12** of a silicon oxide film is formed on the entire top surface of the substrate.

Next, as is shown in FIG. **18**(*b*), a resist film **25***a* used as a mask for forming a connection hole is formed on the insulating film **12**, and the connection hole **14** is formed by, for example, dry etching.

Then, as is shown in FIG. **18**(*c*), the resist film **25***a* is removed, and a polysilicon film is deposited on the insulat-

ing film **12** and within the connection hole **14**. The polysilicon film is then made into a desired pattern, thereby forming a local interconnection **13**.

At this point, in the case where the alignment margin in view of the mask alignment shift in the formation of the connection hole **14** is not considered in estimating the distance La between the polysilicon electrode **4***a* and the isolation **2***b*, a part of the isolation **2***b* is included in the connection hole **14** when the exposing area of the resist film **25***a* is shifted toward the isolation **2***b* due to the mask alignment shift in the photolithography. Through over-etch in conducting the dry etching of the insulating film **12**, although the high-concentration source/drain region **8** made of the silicon substrate is not largely etched because of its small etching rate, the part of the isolation **2***b* included in the connection hole **14** is selectively removed, resulting in forming a recess **40** in part of the connection hole **14**. When the recess **40** in the connection hole **14** has a depth exceeding a given proportion to the depth of the high-concentration source/drain region **8**, junction voltage resistance can be decreased and a junction leakage current can be increased because the concentration of the impurity in the high-concentration source/drain region **8** is low at that depth.

In order to prevent these phenomena, it is necessary to provide a predetermined alignment margin as is shown in the structure of FIG. **17** so as to prevent the connection hole **14** from interfering the isolation **2***b* even when the alignment shift is caused in the lithography. In this manner, in the conventional layout rule for a semiconductor device, an alignment margin in view of the mask alignment shift in the photolithography is unavoidably provided.

Furthermore, a distance between the polysilicon electrode **4***a* and the connection hole **14** is also required to be provided with an alignment margin. Otherwise, the connection hole **14** can interfere the polysilicon electrode **4***a* due to the fluctuation caused in the manufacturing procedures, resulting in causing electric short-circuit between an upper layer interconnection buried in the connection hole and the gate electrode.

As described above, it is necessary to provide the connection hole **14** with margins for preventing the interference with other elements around the connection hole, which has become a large obstacle to the high integration of an LSI.

Also in the case where a semiconductor device having the so-called salicide structure is manufactured, the following problems are caused due to a recess formed in the isolation:

FIG. **19** is a sectional view for showing an example of a semiconductor device including the conventional trench isolation and a MOSFET having the salicide structure. As is shown in FIG. **19**, a trench isolation **105***a* is formed in a silicon substrate **101**. In an active area surrounded with the isolation **105***a*, a gate insulating film **103***a*, a gate electrode **107***a*, and electrode sidewalls **108***a* on both side surfaces of the gate electrode **107***a* are formed. Also in the active area, a low-concentration source/drain region **106***a* and a high-concentration source/drain region **106***b* are formed on both sides of the gate electrode **107***a*. A channel stop region **115** is formed below the isolation **105***a*. Furthermore, in areas of the silicon substrate **101** excluding the isolation **105***a* and the active area, a gate interconnection **107***b* made of the same polysilicon film as that for the gate electrode **107***a* is formed with a gate insulating film **103***b* sandwiched, and the gate interconnection **107***b* is provided with interconnection sidewalls **108***b* on its both side surfaces. On the gate electrode **107***a*, the gate interconnection **107***b* and the high-concentration source/drain region **106***b*, an upper gate electrode **109***a*, an upper gate interconnection **109***b* and a source/drain electrode **109***c* each made of silicide are respectively formed. Furthermore, this semiconductor device includes an interlayer insulating film **111** made of a silicon oxide film, a metallic interconnection **112** formed on the interlayer insulating film **111**, and a contact member **113** (buried conductive layer) filled in a connection hole formed in the interlayer insulating film **111** for connecting the metallic interconnection **112** with the source/drain electrode **109***c*.

Now, the manufacturing procedures for the semiconductor device including the conventional trench isolation and the MOSFET with the salicide structure shown in FIG. **19** will be described referring to FIGS. **20**(*a*) through **20**(*e*).

First, as is shown in FIG. **20**(*a*), a silicon oxide film **116** and a silicon nitride film **117** are successively deposited on a silicon substrate **101**, and a resist film **120** for exposing an isolation region and masking a transistor region is formed on the silicon nitride film **117**. Then, by using the resist film **120** as a mask, etching is conducted, so as to selectively remove the silicon nitride film **116** and the silicon oxide film **117**, and further etch the silicon substrate **101**, thereby forming a trench **104**. Then, impurity ions are injected into the bottom of the trench **104**, thereby forming a channel stop region **115**.

Then, as is shown in FIG. **20**(*b*), a silicon oxide film (not shown) is deposited, and the entire top surface is flattened until the surface of the silicon nitride film **117** is exposed. Through this procedure, a trench isolation **105***a* made of the silicon oxide film filled in the trench **104** is formed in the isolation region Reiso.

Next, as is shown in FIG. **20**(*c*), after the silicon nitride film **117** and the silicon oxide film **116** are removed, a gate oxide film **103** is formed on the silicon substrate **101**, and a polysilicon film **107** is deposited thereon. Then, a photoresist film **121** for exposing areas excluding a region for forming a gate is formed on the polysilicon film **107**.

Then, as is shown in FIG. **20**(*d*), by using the photoresist film **121** as a mask, dry etching is conducted, thereby selectively removing the polysilicon film **107** and the gate oxide film **103**. Thus, a gate electrode **107***a* of the MOSFET in the transistor region Refet and a gate interconnection **107***b* stretching over the isolation **105***a* and the silicon substrate **101** are formed. After removing the photoresist film **121**, impurity ions are injected into the silicon substrate **101** by using the gate electrode **107***a* as a mask, thereby forming a low-concentration **382** source/drain region **106***a*. Then, a silicon oxide film **108** is deposited on the entire top surface of the substrate.

Next, as is shown in FIG. **20**(*e*), the silicon oxide film **108** is anisotropically dry-etched, thereby forming electrode sidewalls **108***a* and interconnection sidewalls **108***b* on both side surfaces of the gate electrode **107***a* and the gate interconnection **107***b*, respectively. At this point, the gate oxide film **103** below the silicon oxide film **108** is simultaneously removed, and the gate oxide film **103** below the gate electrode **107***a* alone remains. Then, impurity ions are diagonally injected by using the gate electrode **107***a* and the electrode sidewalls **108***a* as masks, thereby forming a high-concentration source/drain region **106***b*. Then, after a Ti film is deposited on the entire top surface, high temperature annealing is conducted, thereby causing a reaction between the Ti film and the components made of silicon directly in contact with the Ti film. Thus, an upper gate electrode **109***a*, an upper gate interconnection **109***b* and a source/drain electrode **109***c* made of silicide are formed.

The procedures to be conducted thereafter are omitted, but the semiconductor device including the MOSFET having the

structure as shown in FIG. **19** can be ultimately manufactured. In FIG. **19**, the metallic interconnection **112** is formed on the interlayer insulating film **111**, and the metallic interconnection **112** is connected with the source/drain electrode **109***c* through the contact member **113** including a W plug and the like filled in the contact hole.

When the aforementioned trench isolation structure is adopted, the dimensional change of the source/drain region can be suppressed because the bird's beak, that is, the oxide film invasion of an active area, which is caused in the LOCOS method where a thick silicon oxide film is formed by thermal oxidation, can be avoided. Furthermore, in the procedure shown in FIG. **20**(*c*), the surfaces of the isolation **105***a* and the silicon substrate **101** in the transistor region Refet are placed at the same level.

In such a semiconductor device having the trench type isolation, however, there arise the following problems:

When the procedures proceed from the state shown in FIG. **20**(*d*) to the state shown in FIG. **20**(*e*), the silicon oxide film **108** is anisotropically etched so as to form the sidewalls **108***a* and **108***b*. At this point, over-etch is required. Through this over-etch, the surface of the isolation **105***a* is removed by some depth.

FIGS. **21**(*a*) and **21**(*b*) are enlarged sectional views around the boundary between the high-concentration source/drain region **106***b* and the isolation **105***a* after this over-etch.

As is shown in FIG. **21**(*a*), between the procedures shown in FIGS. **20**(*d*) and **20**(*e*), the impurity ions are diagonally injected so as to form the high-concentration source/drain region **106***b*. Through this ion injection, the high-concentration source/drain region **106***b* is formed also below the edge of the isolation **105***a* because the isolation **105***a* is previously etched by some depth. Accordingly, the high-concentration source/drain region **106***b* is brought closer to the channel stop region **115**, resulting in causing the problems of degradation of the junction voltage resistance and increase of the junction leakage current.

In addition, as is shown in FIG. **21**(*b*), in the case where the Ti film or the like is deposited on the high-concentration source/drain region **106***b* so as to obtain the silicide layer through the reaction with the silicon below, the thus formed silicide layer can invade the interface between the silicon substrate **101** and the isolation **105***a* with ease. As a result, a short-circuit current can be caused between the source/drain electrode **109***c* made of silicide and the channel stop region **115**.

SUMMARY OF THE INVENTION

The object of the present invention is improving the structure of an isolation, so as to prevent the problems caused because the edge of the isolation is trenched in etching for the formation of a connection hole or sidewalls.

In order to achieve the object, the invention proposes first and second semiconductor devices and first through third methods of manufacturing a semiconductor device as described below.

The first semiconductor device of this invention in which a semiconductor element is disposed in each of plural active areas in a semiconductor substrate comprises an isolation for surrounding and isolating each active area, the isolation having a top surface at a higher level than a surface of the active area and having a step portion in a boundary with the active area; an insulating film formed so as to stretch over each active area and the isolation; plural holes each formed by removing a portion of the insulating film disposed at least on the active area; plural buried conductive layers filled in the respective holes; and plural interconnection members formed on the insulating film so as to be connected with the respective active areas through the respective buried conductive layers.

Owing to this structure, in the case where a part of or all the holes are formed so as to stretch over the active areas and the isolation due to mask alignment shift in photolithography, a part of the isolation is removed by over-etch for ensuring the formation of the holes. In such a case, even when the top surface of the isolation is trenched to be lower than the surface of the active area, the depth of the holes formed in the isolation is small in the boundary with the active area because of the level difference between the top surface of the isolation and the surface of the active area. Accordingly, degradation of the junction voltage resistance and increase of the junction leakage current can be suppressed. Therefore, there is no need to provide a portion of the active area where each hole is formed with an alignment margin for avoiding the interference with the isolation caused by the mask alignment shift in the lithography. Thus, the area of the active area can be decreased, resulting in improving the integration of the semiconductor device.

In the first semiconductor device, at least a part of the plural holes can be formed so as to stretch over the active area and the isolation due to fluctuation in manufacturing procedures.

In other words, even when no margin for the mask alignment in the lithography is provided, the problems caused in the formation of the holes can be avoided.

Furthermore, the angle between a side surface of the step portion and the surface of the active area is preferably 70 degrees or more.

As a result, when the hole interferes the isolation, the part of the isolation included in the hole is definitely prevented from being etched through over-etch in the formation of the holes down to a depth where the impurity concentration is low in the active area.

The isolation is preferably a trench isolation made of an insulating material filled in a trench formed by trenching the semiconductor substrate by a predetermined depth.

This is because no bird's beak is caused in the trench isolation differently from a LOCOS film as described above, and hence, the trench isolation is suitable particularly for the high integration and refinement of the semiconductor device.

In the first semiconductor device, when the semiconductor element is a MISFET including a gate insulating film and a gate electrode formed on the active area; and source/drain regions formed in the active area on both sides of the gate electrode, the following preferred embodiments can be adopted:

The semiconductor device can further comprise a gate interconnection made of the same material as that for the gate electrode and formed on the isolation, each of the holes can be formed on an area including the source/drain region, the isolation and the gate interconnection, and the plural interconnection members can be connected with the gate interconnection on the isolation.

Owing to this configuration, in the case where the interconnection members work as local interconnections for connecting a gate interconnection on the isolation with the active area, there is no need to separately form holes in the insulating film on the gate interconnection and the insulating

film on the active area. In addition, there is no need to provide the separate holes with alignment margins from the boundary between the active area and the isolation. Accordingly, the area of the isolation can also be decreased, resulting in largely improving the integration of the semiconductor device.

The semiconductor device can further comprise electrode sidewalls made of an insulating material and formed on both side surfaces of the gate electrode; and a step sidewall made of the same material as the insulating material for the electrode sidewalls and formed on the side surface of the step portion. In this semiconductor device, at least a part of the holes can be formed by also removing a portion of the insulating film disposed on the step sidewall.

Owing to this structure, the abrupt level difference between the surfaces of the isolation and the active area can be released by the step sidewall. Therefore, a residue is scarcely generated in patterning the interconnection members, and an upper interconnection is prevented from being disconnected and increasing in its resistance.

The semiconductor device can further comprise a gate protection film formed on the gate electrode, and at least a part of the holes can be formed so as to stretch over the source/drain region and at least a part of the gate protection film.

Owing to this structure, a part of the gate protection film included in the hole is removed by the over-etch in the formation of the holes. However, the gate electrode is protected by the gate protection film, and hence, electrical short circuit between the gate electrode and the interconnection member can be prevented. Accordingly, there is no need to provide an alignment margin from the gate electrode in the area where each hole is formed, resulting in further improving the integration.

The interconnection members can be first layer metallic interconnections, and the insulating film can be an interlayer insulating film disposed between the semiconductor substrate, and the first layer metallic interconnections. In this case, the semiconductor device preferably further comprises, between the interlayer insulating film and the semiconductor substrate an underlying film made of an insulating material having high etching selectivity against the interlayer insulating film.

The second semiconductor device of this invention in which a semiconductor element is disposed in each of plural active areas in a semiconductor substrate comprises a trench isolation for isolating and surrounding each active area, the trench isolation having a top surface at a higher level than a surface of the active area and having a step portion in a boundary with the active area; and a step sidewall formed on the side surface of the step portion of the trench isolation.

Owing to this structure, in the impurity ion injection for the formation of an impurity diffused layer of the semiconductor device, the step sidewall disposed at the edge of the trench isolation can prevent the impurity ions from being implanted below the edge of the isolation. Furthermore, also in adopting the structure including a source/drain electrode made of silicide, the step sidewall can prevent the silicide layer from being formed at a deep portion. Therefore, a short circuit current can be prevented from occurring between the source/drain electrode and a substrate region such as the channel stop region. In this manner, the function of the trench isolation to isolate each semiconductor element can be prevented from degrading.

In the second semiconductor device, the step sidewall is preferably made of an insulating material.

Also in the second semiconductor device, the semiconductor element can be a MISFET including a gate insulating film and a gate electrode formed on the active area; and source/drain regions formed in the active area on both sides of the gate electrode. This semiconductor device can be further provided with electrode sidewalls formed on both side surfaces of the gate electrode, and the step sidewall can be formed simultaneously with the electrode sidewalls.

Owing to this structure, the semiconductor elements can be a MISFET having the LDD structure suitable for the refinement. Because of this structure together with the trench isolation structure, the semiconductor device can attain a structure particularly suitable for the refinement and the high integration.

The first method of manufacturing a semiconductor device in which a semiconductor element is disposed in each of plural active areas in a semiconductor substrate comprises a first step of forming an isolation in a part of the semiconductor substrate, the isolation having a top surface at a higher level than a surface of the semiconductor substrate and having a step portion in a boundary with the surface of the semiconductor substrate; a second step of introducing an impurity at a high concentration into each active area of the semiconductor substrate surrounded by the isolation; a third step of forming an insulating film on the active area and the isolation; a fourth step of forming, on the insulating film, a masking member having an exposing area above an area at least including a portion of the active area where the impurity at the high concentration is introduced; a fifth step of conducting etching by using the masking member so as to selectively remove the insulating film and form holes; and a sixth step of forming a buried conductive layer by filling the holes with a conductive material and forming, on the insulating film, interconnection members to be connected with the buried conductive layer. In this method, in the fourth step, an alignment margin is not provided for preventing the exposing area of the masking member from including a portion above the isolation when mask shift is caused in photolithography.

In adopting this method, even when a part of the isolation is removed by over-etch in the fifth step so that the top surface of the isolation is etched to be lower than the surface of the active area, the depth of the holes formed in the isolation is small because of the level difference between the isolation and the active area. Accordingly, the decrease of the junction voltage resistance and the increase of the junction leakage current can be suppressed in the manufactured semiconductor device. In addition, the area of the active area can be decreased because no alignment margin from the isolation is provided, resulting in improving the integration of the manufactured semiconductor device.

In the first method of manufacturing a semiconductor device, the following preferred embodiments can be adopted:

The fifth step is preferably performed so as to satisfy the following inequality:

$$OE \times a \times (ER2/ER1) \leqq b + D \times (2/10)$$

wherein "a" indicates a thickness of the insulating film, "b" indicates a level difference between the surface of the active area and the top surface of the isolation, "ER1" indicates an etching rate of the insulating film, "ER2" indicates an etching rate of the isolation, "D" indicates a depth of an impurity diffused layer in the active area, and "OE" indicates an over-etch ratio of the insulating film.

In adopting this method, even when a part of the isolation included in the hole is removed by over-etch in the forma-

tion of the holes, the bottom of the etched portion does not reach a portion where the impurity concentration is low in the active area. In other words, the top surface of the isolation is never placed at a lower level than the surface of the active area. Accordingly, the degradation of the junction voltage resistance and the increase of the junction leakage current can be definitely prevented in the manufactured semiconductor device.

When the semiconductor element is a MISFET, the method can further include, before the second step, a step of forming a gate insulating film on the active area, a step of depositing a conductive film on the gate insulating film and a step of forming a gate electrode by patterning the conductive film, and in the second step, the impurity at the high concentration is introduced so as to form a source/drain region. In such a case, the following preferred embodiments can be adopted.

The method can further comprise, after the step of depositing the conductive film, a step of depositing a protection insulating film on the conductive film, and in the step of forming the gate electrode, the conductive film as well as the protection insulating film are patterned, so as to form a gate protection film on the gate electrode. The fifth step can be performed so as to satisfy the following inequality:

$$OE \times a \times (ER3/ER1) < c$$

wherein "a" indicates a thickness of the insulating film, "c" indicates a thickness of the gate protection film, "ER1" indicates an etching rate of the insulating film, "ER3" indicates an etching rate of the gate protection film and "OE" indicates an over-etch ratio of the insulating film.

When this method is adopted, while the area of the active area is decreased by not providing an alignment margin for avoiding the interference between the connection hole and the gate electrode, the hole is prevented from reaching the gate electrode below the gate protection film.

In the fourth step, the masking member can be formed to be positioned without providing a margin for preventing the exposing area thereof from including a portion above the gate protection film even when the mask shift is caused in the photolithography.

Alternatively, in the fourth step, the masking member can be formed to be positioned with the exposing area thereof including at least a part of a portion above the gate protection film when the mask shift is not caused in the photolithography.

In the third step, an interlayer insulating film can be formed as the insulating film, and in the sixth step, first layer metallic interconnections can be formed as the interconnection members. In such a case, it is preferred that the interlayer insulating film is formed in the third step after an underlying film made of an insulating material having high etching selectivity against the interlayer insulating film is formed below the interlayer insulating film.

The second method of manufacturing a semiconductor device of this invention comprises a first step of forming an underlying insulating film on a semiconductor substrate; a second step of depositing an etching stopper film on the underlying insulating film; a third step of forming a trench by exposing a portion of the etching stopper film and the underlying insulating film where an isolation is to be formed and etching the semiconductor substrate in the exposed portion; a fourth step of depositing an insulating film for isolation on an entire top surface of the substrate, flattening the substrate until at least a surface of the etching stopper film is exposed, and forming a trench isolation in the trench so as to surround a transistor region; a fifth step of removing, by etching, at least the etching stopper film and the underlying insulating film, so as to expose a step portion between the transistor region and the trench isolation; a sixth step of depositing a gate oxide film and a conductive film on the substrate and making the conductive film into a pattern of at least a gate electrode; a seventh step of depositing an insulating film for sidewalls on the entire top surface of the substrate and anisotropically etching the insulating film for the sidewalls, so as to form electrode sidewalls and a step sidewall on side surfaces of the gate electrode and the step portion, respectively; and an eighth step of introducing an impurity into the semiconductor substrate in the transistor region on both sides of the gate electrode, so as to form source/drain regions.

When this method is adopted, since the step sidewall is formed between the semiconductor substrate in the transistor region and the trench isolation after completing the fifth step, the impurity ions are prevented from being implanted below the edge of the trench isolation in the impurity ion injection in the eighth step. Furthermore, also when an area in the vicinity of the surface of the source/drain region is subsequently silicified, the step sidewall made of the insulating film can prevent the silicide layer from being formed at a deep portion. Accordingly, not only the degradation of the junction voltage resistance and the current leakage but also the occurrence of a short circuit current between the source/drain electrode and the substrate region such as the channel stop region can be prevented.

In the second method of manufacturing a semiconductor device, the following preferred embodiments can be adopted:

In the second step, the thickness of the etching stopper film is preferably determined in consideration of an amount of over-etch in the seventh step, so that the step portion having a level difference with a predetermined size or more is exposed in the fifth step.

The method can further comprise, after completing the eighth step, a step of silicifying at least an area in the vicinity of the surface of the source/drain region.

The third method of manufacturing a semiconductor device of this invention comprises a first step of forming a gate insulating film on a semiconductor substrate; a second step of depositing a first conductive film to be formed into a gate electrode on the gate insulating film; a third step of forming a trench by exposing a portion of the first conductive film where a trench isolation is to be formed and etching the semiconductor substrate in the exposed portion; a fourth step of depositing an insulating film for isolation on an entire top surface of the substrate, flattening the substrate at least until a surface of the first conductive film is exposed, and forming the trench isolation in the trench so as to surround a transistor region; a fifth step of depositing a second conductive film to be formed into at least an upper gate electrode on the entire top surface of the flattened substrate; a sixth step of making the first and second conductive films into a pattern at least of the gate electrode and exposing a step portion between the transistor region and the trench isolation; a seventh step of depositing an insulating film for sidewalls on the entire top surface of the substrate and anisotropically etching the insulating film for the sidewalls, so as to form electrode sidewalls and a step sidewall on side surfaces of the gate electrode and the step portion, respectively; and an eighth step of introducing an impurity into the semiconductor substrate in the transistor region on both sides of the gate electrode, so as to form source/drain regions.

When this method is adopted, the same effects as those attained by the second method of manufacturing a semicon-

ductor device can be attained. In addition, in the patterning process for the gate electrode, the top surface of the substrate is completely flat, and hence, the patterning accuracy for the gate electrode can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**(*a*) through **1**(*d*) are sectional views for showing manufacturing procedures of Embodiment 1 up to the formation of an isolation;

FIGS. **2**(*a*) through **2**(*e*) are sectional views for showing the manufacturing procedures of Embodiment 1 after the formation of the isolation;

FIGS. **3**(*a*) through **3**(*f*) are sectional views for showing manufacturing procedures of Embodiment 2 after the formation of an isolation;

FIGS. **4**(*a*) through **4**(*c*) are sectional views for showing manufacturing procedures of Embodiment 3;

FIGS. **5**(*a*) through **5**(*c*) are sectional views for showing manufacturing procedures of Embodiment 4;

FIGS. **6**(*a*) through **6**(*f*) are sectional views for showing manufacturing procedures of Embodiment 5;

FIGS. **7**(*a*) through **7**(*c*) are sectional views for showing manufacturing procedures of Embodiment 6;

FIGS. **8**(*a*) through **8**(*c*) are sectional views for showing manufacturing procedures of Embodiment 7 in which a comparatively thin insulating film of Embodiment 1 is replaced with a layered film and an interlayer insulating film;

FIGS. **9**(*a*) through **9**(*c*) are sectional views for showing the manufacturing procedures of Embodiment 7 in which a comparatively thin insulating film of Embodiment 2 is replaced with a layered film and an interlayer insulating film;

FIGS. **10**(*a*) through **10**(*c*) are sectional views for showing the manufacturing procedures of Embodiment 7 in which a comparatively thin insulating film of Embodiment 4 is replaced with a layered film and an interlayer insulating film;

FIGS. **11**(*a*) through **11**(*c*) are sectional views for showing the manufacturing procedures of Embodiment 7 in which a comparatively thin insulating film of Embodiment 5 is replaced with a layered film and an interlayer insulating film;

FIG. **12** is a sectional view for showing the structure of a semiconductor device of Embodiment 8;

FIGS. **13**(*a*) through **13**(*e*) are sectional views for showing manufacturing procedures for the semiconductor device of Embodiment 8;

FIGS. **14**(*a*) through **14**(*e*) are sectional views for showing manufacturing procedures for a semiconductor device of Embodiment 9;

FIGS. **15**(*a*) through **15**(*f*) are sectional views for showing manufacturing procedures for a semiconductor device of Embodiment 10;

FIGS. **16**(*a*) through **16**(*e*) are sectional views for showing manufacturing procedures for a semiconductor device of Embodiment 11;

FIG. **17** is a sectional view of a conventional semiconductor device in which the surfaces of an active area and a trench isolation are placed at the same level;

FIGS. **18**(*a*) through **18**(*c*) are sectional views for showing manufacturing procedures for the conventional semiconductor device of FIG. 17;

FIG. **19** is a sectional view of a conventional semiconductor device having a salicide structure and a trench isolation structure;

FIGS. **20**(*a*) through **20**(*e*) are sectional views for showing manufacturing procedures for the conventional semiconductor device of FIG. **19**; and

FIGS. **21**(*a*) and **21**(*b*) are partial sectional views for showing problems, in a conventional semiconductor device having a trench isolation, occurring in an impurity ion injection process and a silicifying process, respectively.

DETAILED DESCRIPTION OF THE INVENTION

(Embodiment 1)

Embodiment 1 of the invention will now be described referring to FIGS. **1**(*a*) through **1**(*d*) and **2**(*a*) through **2**(*e*). In the manufacturing procedures of this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is designed to stretch over an active area and an isolation when alignment shift is not caused in photolithography.

In this embodiment, the isolation is formed as a trench isolation. Furthermore, interconnection to be formed above is assumed to be local interconnection in which an insulating film can be comparatively thin, but the embodiment is applicable also to general global interconnection formed on a thick interlayer insulating film.

First, as is shown in FIG. **1**(*a*), a resist film **50***a* having a predetermined pattern is formed on a p-type silicon substrate **1** (or a p-type well). The silicon substrate **1** is dry-etched by using the resist film **50***a* as a mask, thereby forming a trench **51** with a depth of 1 μm.

Then, as is shown in FIG. **1**(*b*), the resist film **50***a* is removed, and then a silicon oxide film **2***x* is deposited on the entire top surface of the silicon substrate **1**. Through this procedure, the previously formed trench **51** is filled with the silicon oxide film **2***x*.

Next, as is shown in FIG. **1**(*c*), the silicon oxide film **2***x* on the silicon substrate **1** is removed by, for example, a CMP (chemical mechanical polishing) method or etch-back through dry etching using a resist film, and at the same time, a trench isolation **2***b* is formed. At this point, the top surface of the silicon substrate **1** and the top surface of the isolation **2***b* are flattened with no level difference therebetween.

Then, as is shown in FIG. **1**(*d*), dry etching with high etch selectivity is conducted so as to etch the silicon substrate **1** alone by a thickness of 0.2 μm. Thus, a step portion which is higher in a stepwise manner than the top surface of the silicon substrate **1** by 0.2 μm is formed in the isolation **2***b*. The level difference caused by the step portion is required to be sufficiently large in consideration of an amount of overetch in etching a subsequently formed insulating film **12**, and hence, the level difference is preferably equal to or larger than the thickness of the insulating film **12**.

It is noted that the method of causing the level difference between the top surface of the isolation **2***b* and the surface of the active area is not limited to that described above. For example, the level difference can be caused as follows: After an etching stopper film having a thickness corresponding to the level difference is previously deposited on the silicon substrate, a trench is formed and an insulating film for the trench isolation is deposited. Then, the entire top surface of the substrate is flattened by the CMP method or the like, and the etching stopper film is subsequently removed.

Next, As is shown in FIG. **2**(*a*), after forming a gate oxide film **3** on the silicon substrate **1**, a polysilicon film **4***x* is deposited on the entire top surface of the substrate.

Then, as is shown in FIG. **2**(*b*), after forming a resist film (not shown) having a predetermined pattern on the polysilicon film **4***x*, dry etching is conducted so as to form a

polysilicon electrode **4***a* on the active area and a polysilicon interconnection **4***b* on the isolation **2***b*. Then, by using the gate electrode **4***a* as a mask, n-type impurity ions are injected at a high concentration, thereby forming high-concentration source/drain regions **8** in the silicon substrate **1** on both sides of the polysilicon electrode **4***a*.

After this, as is shown in FIG. **2**(*c*), the insulating film **12** having a thickness of, for example, 0.15 μm is deposited, so that an interconnection subsequently formed above the insulating film (i.e., the local interconnection in this embodiment) can be electrically insulated from the polysilicon electrode, the polysilicon interconnection and the active area.

Next, as is shown in FIG. **2**(*d*), a resist film **25***a* having a pattern for forming a connection hole is formed on the insulating film **12**. At this point, the exposing area of the resist film **25***a* is positioned without an alignment margin for preventing interference with the isolation **2***b*. In this embodiment, after the resist film **25***a* is formed so that the exposing area stretches over the source/drain region **8**, that is, the active area of a transistor, and the isolation **2***b*, dry etching is conducted by using the resist film **25***a* as a mask, thereby forming a connection hole **14** by removing the insulating film **12** in the exposing area of the resist film **25***a*. At this point, when the insulating film **12** is, for example, 40% over-etched than its thickness of 0.15 μm in order to ensure the formation of the connection hole **14**, the isolation **2***b* in the exposing area of the resist film **25***a* is etched by a thickness of approximately 0.06 μm. However, in this embodiment, the step portion has a height of 0.2 μm, which is sufficiently larger than this etched amount, and hence, a recess where the top surface of the isolation **2***b* is lower than the top surface of the silicon substrate **1** is never formed in any part of the connection hole **14**.

Next, as is shown in FIG. **2**(*e*), a polysilicon film is deposited on the entire top surface and is patterned, thereby forming the local interconnection **13**. At this point, the local interconnection **13** is also formed within the connection hole **14**, so as to be electrically connected with the source/drain region **8** serving as the active area.

In a semiconductor device formed in the aforementioned procedures, the top surface of the isolation **2***b* is higher in a stepwise manner than the surface of the active area. Therefore, even when the isolation **2***b* is removed by some amount by the over-etch in dry etching the insulating film **12**, the isolation **2***b* is prevented from being etched by a thickness exceeding the level difference caused by the step portion. Accordingly, when mask alignment is shifted in the photolithography, a recess with a depth reaching a certain depth of the source/drain region **8** is prevented from being formed in the connection hole **14**. As a result, the conventional problems, that is, the degradation of the junction voltage resistance and the increase of the junction leakage current caused because of the low impurity concentration at a lower part of the active area of the silicon substrate corresponding to the sidewall of the recess, can be effectively prevented.

However, the level difference between the top surface of the isolation **2***b* and the surface of the active area is not necessarily required to be larger than the thickness of the insulating film **12**. The dimensions and materials of the respective components can be determined so as to satisfy the following inequality (1), wherein "a" denotes the thickness of the insulating film **12**; "b" denotes the level difference between the top surface of the isolation **2***b* and the surface of the active area; "ER**1**" denotes the etching rate of the insulating film **12**; "ER**2**" denotes the etching rate of the isolation **2***b*; "D" denotes the depth of an impurity diffused layer in the active area; and "OE" denotes the over-etch ratio of the insulating film **12** in the formation of the connection hole **14**.

$$OE\times a\times(\mathrm{ER}2/\mathrm{ER}1)\geqq b+D\times(2/10) \quad (1)$$

As far as the inequality (1) is satisfied, even when a part of the isolation **2***b* is removed to be at a lower level than the surface of the silicon substrate in the active area through the formation of the connection hole **14**, so that the recess **40** as is shown in FIG. **18**(*c*) is formed in a part of the connection hole **14**, the bottom of the recess **40** is prevented from reaching the depth where the impurity concentration is low.

Since the alignment margin in view of the mask shift in the photolithography can be omitted, the following effects can be attained: When a distance Lb between the polysilicon electrode **4***a* serving as the gate electrode and the isolation **2***b* is estimated as an index of the integration, the distance Lb is 0.8 μm, namely, the sum of the diameter of the connection hole, 0.5 μm, and the alignment margin from the gate electrode, 0.3 μm. Thus, the distance Lb can be decreased by 0.4 μm as compared with the conventional distance La of 1.2 μm (shown in FIG. **17**).

(Embodiment 2)

Embodiment 2 will now be described referring to FIGS. **3**(*a*) through **3**(*f*). In this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is formed so as to stretch over an active area and an isolation in the same manner as in Embodiment 1, and a step portion between the isolation and the active area is provided with a sidewall.

First, as is shown in FIGS. **3**(*a*) and **3**(*b*), an isolation **2***b* whose top surface is higher in a stepwise manner than the surface of an active area by a predetermined level difference and a gate oxide film **3** are formed on a silicon substrate **1** in the same manner as described in Embodiment 1. Then, a polysilicon film **4***x* is deposited on the entire top surface.

Next, the polysilicon film **4***x* is patterned, thereby forming a polysilicon electrode **4***a* and a polysilicon interconnection **4***b*. The procedures conducted so far are identical to those adopted in Embodiment 1. Then, a silicon oxide film is deposited on the entire top surface and is subjected to anisotropic etching, thereby forming electrode sidewalls **7***a* on both side surfaces of the polysilicon electrode **4***a* and interconnection sidewalls **7***b* on both side surfaces of the polysilicon interconnection **4***b*. At the same time, a step sidewall **7***c* is formed on the side surface of the step portion between the isolation **2***b* and the active area. Each of the sidewalls has a width of, for example, approximately 0.1 μm. After forming the polysilicon electrode **4***a*, an n-type impurity with a low concentration is ion-injected into the active area, so as to form a low-concentration source/drain region **6**. After forming the electrode sidewalls **7***a*, an n-type impurity with a high concentration is ion-injected into the active area, so as to form a high-concentration source/drain region **8**. This is a generally adopted method of manufacturing a MOSFET having the so-called LDD structure.

Then, as is shown in FIGS. **3**(*d*) through **3**(*f*), the procedures as described in Embodiment 1 referring to FIGS. **2**(*c*) through **2**(*e*) are conducted, thereby forming an insulating film **12** and a local interconnection **13** thereon.

This embodiment can achieve the effect to improve the integration similarly to Embodiment 1. In addition, owing to the step sidewall **7***c*, the abrupt level difference between the isolation **2***b* and the active area can be released. As a result, the amount of residue generated in the formation of the local interconnection **13** by patterning the polysilicon film can be

advantageously decreased, and disconnection of the local interconnection **13** and resistance increase thereof can also be prevented.

At this point, a distance Lc between the polysilicon electrode **4***a* serving as a gate electrode and the isolation **2***b* is estimated as an index of the integration. The distance Lc is 1.0 μm, namely, the sum of the diameter of the connection hole, 0.5 μm, the width of the electrode sidewall **7***a,* 0.1 μm, the alignment margin from the polysilicon electrode **4***a,* 0.3 μm, and the width of the step sidewall **7***c,* 0.1 μm. Thus, the distance Lc can be decreased by 0.2 μm as compared with the conventional distance La of 1.2 μm (shown in FIG. **17**).

(Embodiment 3)

Embodiment 3 will now be described referring to FIGS. **4**(*a*) through **4**(*c*).

In manufacturing procedures described in this embodiment, a connection hole is formed so as to stretch over an active area and an isolation only when mask alignment shift is caused in the photolithography.

FIG. **4**(*a*) shows a state where the procedures described in Embodiment 2 referring to FIGS. **3**(*a*) through **3**(*d*) have been completed. Specifically, as is shown in FIG. **4**(*a*), after an isolation **2***b* with a top surface higher in a stepwise manner than the surface of an active area, a step sidewall **7***c* on the side surface of the step portion of the isolation **2***b,* a gate oxide film **3**, a polysilicon electrode **4***a* serving as a gate electrode, electrode sidewalls **7***a* on both side surfaces of the polysilicon electrode **4***a,* a low-concentration source/drain region **6**, a high-concentration source/drain region **8**, a polysilicon interconnection **4***b* on the isolation **2***b,* and interconnection sidewalls **7***b* on both side surfaces of the polysilicon interconnection **4***b* are formed, an insulating film **12** with a thickness of approximately 0.15 μm is formed on the entire top surface.

Next, as is shown in FIG. **4**(*b*), a resist film **25***b* for forming a connection hole is formed. At this point, in this embodiment, the resist film **25***b* is formed so that the connection hole stretches over the active area (i.e., the high-concentration source/drain region **8**) and the step sidewall **7***c* when the mask alignment shift is not caused in the lithography. Then, the insulating film **12** is etched, thereby forming the connection hole **14** stretching over the active area and the step sidewall **7***c*.

Then, as is shown in FIG. **4**(*c*), a local interconnection **13** to be connected with the high-concentration source/drain region **8** is formed on the insulating film **12**.

In the state shown in FIG. **4**(*b*), the edge of the connection hole **14** can be shifted toward the isolation **2***b* by a maximum of 0.3 μm due to the mask alignment shift in the lithography. In such a case, the resultant structure becomes that described in Embodiment 2 (shown in FIG. **3**(*e*)). However, no recess is formed in the isolation **2***b* within the connection hole **14** as described in Embodiments 1 and 2 even in such a case. Alternatively, even if a recess is formed, the problems of the degradation of the junction voltage resistance and the increase of the junction leakage current can be avoided as far as the dimensions and the like of the respective components are determined so as to satisfy the inequality (1).

Also in this embodiment, a distance Lc between the polysilicon electrode **4***a* and the isolation **2***b* is estimated as an index of the integration. Similarly to Embodiment 2, the distance Lc is 1.0 μm, namely, the sum of the diameter of the connection hole, 0.5 μm, the width of the electrode sidewall **7***a,* 0.1 μm, the alignment margin from the polysilicon electrode **4***a,* 0.3 μm, and the width of the step sidewall **7***c,* 0.1 μm. Thus, the distance Lc can be decreased by 0.2 μm as compared with the conventional distance La of 1.2 μm.

(Embodiment 4)

Embodiment 4 will now be described referring to FIGS. **5**(*a*) through **5**(*c*). In manufacturing procedures described in this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is formed so as to stretch over an active area and a polysilicon interconnection on an isolation.

FIG. **5**(*a*) shows the state where the procedures described in Embodiment 2 referring to FIGS. **3**(*a*) through **3**(*d*) have been completed. Specifically, as is shown in FIG. **5**(*a*), after an isolation **2***b* with a top surface higher in a stepwise manner than the surface of the active area, a step sidewall **7***c* on the side surface of the step portion of the isolation **2***b,* a gate oxide film **3**, a polysilicon electrode **4***a* serving as a gate electrode, electrode sidewalls **7***a* on both side surfaces of the polysilicon electrode **4***a,* a low-concentration source/drain region **6**, a high-concentration source/drain region **8**, a polysilicon interconnection **4***b* on the isolation **2***b,* and interconnection sidewalls **7***b* on both side surfaces of the polysilicon interconnection **4***b* are formed, an insulating film **12** with a thickness of approximately 0.15 μm is formed on the entire top surface.

Next, as is shown in FIG. **5**(*b*), a resist film **25***c* for forming a connection hole is formed. In this embodiment, the resist film **25***c* is formed with its exposing area stretching over the active area (i.e., the high-concentration source/drain region **8**) and the polysilicon interconnection **4***b* on the isolation **2***b* when the mask alignment shift is not caused in the lithography. Then, the insulating film **12** is etched, thereby forming the connection hole **14** stretching over the high-concentration source/drain region **8**, the isolation **2***b* and the polysilicon interconnection **4***b*.

Then, as is shown in FIG. **5**(*c*), a local interconnection **13** to be connected with the high-concentration source/drain region **8** and the polysilicon interconnection **4***b* is formed on the insulating film **12**.

When the high-concentration source/drain region **8** is to be electrically connected with the polysilicon interconnection **4***b* serving as a gate interconnection formed on the isolation **2***b* in the conventional manufacturing procedures, a connection hole formed on the high-concentration source/drain region **8** and another connection hole formed on the polysilicon interconnection **4***b* are required to be positioned in consideration of alignment margins from the boundaries with the high-concentration source/drain region **8** and the isolation **2***b,* respectively. In contrast, in this embodiment, the interconnection member can be connected with the high-concentration source/drain region **8** and the polysilicon electrode **4***b* through one connection hole **14** without consideration of the alignment margins. In addition, as described in Embodiments 1 through 3, the problems of the degradation of the junction voltage resistance and the increase of the junction leakage current can be prevented from being caused through the over-etch in etching the insulating film **12**.

In this embodiment, the interconnection on the isolation **2***b* is made of a polysilicon film, but another conductive material or an interconnection on a layer different from the polysilicon electrode can be used instead.

(Embodiment 5)

Embodiment 5 will now be described referring to FIGS. **6**(*a*) through **6**(*f*). In manufacturing procedures described in this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is formed so as to stretch over an active area, a gate electrode and an isolation.

First, as is shown in FIG. **6**(*a*), an isolation **2***b* with a top surface higher in a stepwise manner than the surface of a p-type silicon substrate **1** is formed.

Next, as is shown in FIG. **6**(*b*), a polysilicon film **4***x* with a thickness of 0.2 μm is deposited on the entire top surface, and a silicon oxide film **15***x* for gate protection with a thickness of approximately 0.15 μm is deposited on the polysilicon film **4***x*. At this point, the thickness of the silicon oxide film **15***x* for gate protection is required to be sufficiently large in consideration of an amount of over-etch to be removed in etching a subsequently formed insulating film **12**. In this embodiment, the thickness of the silicon oxide film **15***x* is substantially the same as that of the insulating film **12**.

Then, as is shown in FIGS. **6**(*c*) and **6**(*d*), the procedures as described in Embodiment 2 referring to FIGS. **3**(*c*) and **3**(*d*) are conducted. Thus, after a polysilicon electrode **4***a* and a gate protection film **15***a* together serving as a gate electrode, electrode sidewalls **7***a* on both side surfaces of the polysilicon electrode **4***a* and the gate protection film **15***a,* a low-concentration source/drain region **6**, a high-concentration source/drain region **8**, a polysilicon interconnection **4***b* and an interconnection protection film **15***b* on the isolation **2***b,* interconnection sidewalls **7***b* on both side surfaces of the polysilicon interconnection **4***b* and the interconnection protection film **15***b* and a step sidewall **7***c* are formed, the insulating film **12** with a thickness of approximately 0.15 μm is formed on the entire top surface.

Next, as is shown in FIG. **6**(*e*), a resist film **25***d* for forming a connection hole is formed. At this point, in this embodiment, the resist film **25***d* is formed so that the connection hole stretches over the polysilicon electrode **4***a,* the high-concentration source/drain region **8** serving as the active area and the isolation **2***b* when the mask alignment shift is not caused in the lithography. Accordingly, when the alignment shift is not caused, the exposing area of the resist film **25***d* stretches also over a part of the polysilicon electrode **4***a*. Then, the insulating film **12** is patterned by dry etching. At this point, a part of the isolation **2***b* and the gate protection film **15***a* in the exposing area of the resist film **25***d* are also removed by some amount by the over-etch in the dry etching of the insulating film **12**. However, the connection hole **14** never reaches the polysilicon electrode **4***a*.

Then, as is shown in FIG. **6**(*f*), a polysilicon film is deposited on the entire top surface and then patterned, thereby forming a local interconnection **13** to be connected with the high-concentration source/drain region **8**.

In this embodiment, the problems of the degradation of the junction voltage resistance and the increase of the junction leakage current can be avoided as in the aforementioned embodiments even when the insulating film **12** is 40% over-etched than its thickness of 0.15 μm in order to form the connection hole **14**

In particular in this embodiment, the connection hole **14** stretches also over the polysilicon electrode **4***a* when the alignment shift is not caused in the lithography. Therefore, when the insulating film **12** is, for example, 40% over-etched than its thickness of 0.15 μm in the dry etching thereof, although a part of the gate protection film **15***a* is etched by a thickness of approximately 0.06 μm. However, the conventional problem of the electric short circuit with an interconnection on an upper layer through the connection hole can be avoided since the thickness of the gate protection film **15***a* is 0.15 μm, which is sufficiently larger than 0.06 μm.

It is noted that the thickness of the gate protection film **15***a* can be determined as follows: The dimensions and materials of the respective components are determined so as to satisfy the following inequality (2), wherein "a" denotes the thickness of the insulating film **12**; "c" denotes the thickness of the gate protection film **4***a,* "ER**1**" denotes the etching rate of the insulating film **12**; "ER**3**" denotes the etching rate of the gate protection film **4***a;* and "OE" denotes the over-etch ratio of the insulating film **12** in the formation of the connection hole **14**:

$$OE \times a \times (ER3/ER1) \leq c \quad (2)$$

At this point, a distance Ld between the polysilicon electrode **4***a* serving as the gate electrode and the isolation **2***b* is estimated as an index of the integration. The distance Ld is 0.7 μm, namely, the sum of the diameter of the connection hole, 0.5 μm, the width of the electrode sidewall **7***a,* 0.1 μm, and the width of the step sidewall **7***c,* 0.1 μm. Thus, the distance Ld can be decreased by 0.5 μm as compared with the conventional distance of 1.2 μm.

(Embodiment 6)

Embodiment 6 will now be described referring to FIGS. **7**(*a*) through **7**(*c*). In manufacturing procedures described in this embodiment, a connection hole for connecting an interconnection layer and a silicon substrate is formed so as to stretch over an active area, an electrode sidewall and an isolation when the alignment shift is not caused, and is formed so as to stretch also over a polysilicon electrode only when the alignment shift is caused.

FIG. **7**(*a*) shows the state where the procedures described in Embodiment 5 referring to FIGS. **6**(*a*) through **6**(*d*) have been completed. Specifically in FIG. **7**(*a*), after an isolation **2***b* having a top surface higher in a stepwise manner than the surface of the active area, a step sidewall **7***c* on the side surface of the step portion of the isolation **2***b,* a gate oxide film **3**, a polysilicon electrode **4***a* serving as a gate electrode, a gate protection film **15***a* on the polysilicon electrode **4***a,* electrode sidewalls **7***a* on both side surfaces of the polysilicon electrode **4***a* and the gate protection film **15***a,* a low-concentration source/drain region **6**, a high-concentration source/drain region **8**, a polysilicon interconnection **4***b* on the isolation **2***b,* an interconnection protection film **15***b* on the polysilicon interconnection **4***b,* and interconnection sidewalls **7***b* on both side surfaces of the polysilicon interconnection **4***b* and the interconnection protection film **15***b* are formed, an insulating film **12** having a thickness of approximately 0.15 μm is formed on the entire top surface.

Next, as is shown in FIG. **7**(*b*), a resist film **25***e* having a pattern for forming a connection hole is formed. At this point, in this embodiment, the resist film **25***e* is formed so that its exposing area can expose at least the step sidewall **7***c* and the high-concentration source/drain region **8** serving as the active area and stretches also over the electrode sidewall **7***a*.

Then, a polysilicon film is deposited on the entire top surface and patterned, thereby forming a local interconnection **13** to be connected with the high-concentration source/drain region **8**.

In the procedure shown in FIG. **7**(*b*) of this embodiment, when the exposing area of the resist film **25***e* is shifted by, for example, a maximum of 0.3 μm due to the alignment shift in the lithography, the connection hole **14** is formed so as to stretch also over a part of the polysilicon electrode **4***a*. When the exposing area of the resist film **25***e* is shifted in the reverse direction, the connection hole **14** is formed so as to stretch also over a part of the isolation **2***b*. However, in either case, the junction voltage at the edge of the isolation **2***b* is prevented from degrading and the junction leakage current is prevented from increasing as far as the dimensions and the like of the respective components are determined so as to satisfy the inequalities (1) and (2). In addition, an electrical short circuit between an interconnection member such as the local interconnection and the polysilicon electrode **4***a* can be avoided.

At this point, a distance Le between the polysilicon electrode **4***a* serving as the gate electrode and the isolation **2***b* is estimated as an index of the integration. Similarly to Embodiment 5, the distance Le is 0.7 μm, namely, the sum of the diameter of the connection hole, 0.5 μm, the width of the electrode sidewall **7***a,* 0.1 μm, and the width of the step sidewall **7***c,* 0.1 μm. Thus, the distance Le can be decreased by 0.5 μm as compared with the conventional distance of 1.2 μm.

In each of the aforementioned embodiments, the local interconnection is adopted as the interconnection member so as to make the insulating film **12** comparatively thin. However, each embodiment can be applied to an interconnection member using a general global interconnection formed with an interlayer insulating film sandwiched. When the global interconnection is adopted, the interlayer insulating film is comparatively thick. Therefore, the effects of the embodiments can be similarly attained by decreasing the over-etch ratio of the interlayer insulating film in the formation of the connection hole or by increasing the level difference between the top surface of the isolation and the surface of the active area. This will be described in more detail in Embodiment 7 below.

Furthermore, when the isolation **2***b* and the gate protection film **15***a* used in Embodiment 5 or 6 are made of a material having a smaller etching rate than the material for the insulating film **12** against the etching for forming the connection hole, the semiconductor device can be manufactured with more ease.

In addition, when the insulating film **12** in each of the aforementioned embodiments has a multilayered structure including at least one lower layer made of a material having a smaller etching rate against the etching for forming the connection hole, the semiconductor device can be manufactured with more ease.

(Embodiment 7)

Embodiment 7 will now be described in which an interconnection layer formed on a thick interlayer insulating film is connected with an active area of a semiconductor substrate through a contact hole formed on the interlayer insulating film.

FIGS. **8**(*a*) through **8**(*c*) are sectional views for showing procedures for forming a layered film **10** and an interlayer insulating film **11** instead of the comparatively thin insulating film **12** of Embodiment 1. As is shown in FIG. **8**(*a*), after conducting the procedures shown in FIGS. **1**(*a*) through **1**(*d*) and **2**(*a*) through **2**(*c*), a layered film **10** including a silicon oxide film **10***a* with a thickness of approximately 70 nm and a silicon nitride film **10***b* with a thickness of approximately 80 nm is formed on the entire top surface of the substrate. Then, an interlayer insulating film **11** of a silicon oxide film with a thickness of approximately 600 nm is deposited thereon. Next, a resist film **25***a* having a pattern for forming a contact hole is formed on the interlayer insulating film **11**. At this point, the exposing area of the resist film **25***a* is positioned without an alignment margin for avoiding interference with an isolation **2***b*. In FIG. **8**(*a*), the resist film **25***a* is formed so that the exposing area stretches over a source/drain region **8** serving as the active area of a transistor and the isolation **2***b*.

Next, as is shown in FIG. **8**(*b*), etching is conducted by using the resist film **25***a* as a mask, thereby selectively removing the interlayer insulating **25***a* and the layered film **10**. Thus, a contact hole **20** stretching over the isolation **2***b* and the active area is formed.

Then, as is shown in FIG. **8**(*c*), a plug underlying film **21** made of a TiN/Ti film and a W plug **22** are deposited within the contact hole **20** by selective CVD. Furthermore, an aluminum alloy film is deposited on the entire top surface of the substrate and the aluminum alloy film is patterned, thereby forming a first layer metallic interconnection **23**. At this point, the first layer metallic interconnection **23** is electrically connected with the source/drain region **8** serving as the active area through the W plug **22** and the plug underlying film **23** filled in the contact hole **20**.

FIGS. **9**(*a*) through **9**(*c*) are sectional views for showing procedures for forming a layered film **10** and an interlayer insulating film **11** instead of the comparatively thin insulating film **12** of Embodiment 2. In these manufacturing procedures, a procedure for forming sidewalls **7***a* through **7***c* is added to the manufacturing procedures shown in FIGS. **8**(*a*) through **8**(*c*), so as to manufacture a transistor having the LDD structure.

FIGS. **10**(*a*) through **10**(*c*) are sectional views for showing procedures for forming a layered film **10** and an interlayer insulating film **11** instead of the comparatively thin insulating film **12** of Embodiment 4. In the procedure shown in FIG. **10**(*a*), a resist film **25***c* having its exposing area stretching over the active area and the gate interconnection **4***b* is formed on the interlayer insulating film **11**. Thereafter, the same procedures as those shown in FIGS. **8**(*b*) and **8**(*c*) are conducted.

FIGS. **11**(*a*) through **11**(*c*) are sectional views for showing procedures for forming a layered film **10** and an interlayer insulating film **11** instead of the comparatively thin insulating film **12** of Embodiment 5. In the procedure shown in FIG. **11**(*a*), a gate protection silicon oxide film **15***a* is formed on a gate electrode **4***a,* and the layered film **10** and the interlayer insulating film **11** are formed thereon. Then, a resist film **25***d* having its exposing area stretching over the isolation, the active area and the gate electrode **4***a* is formed on the interlayer insulating film **11**. Thereafter, the same procedures as those shown in FIGS. **8**(*b*) and **8**(*c*) are conducted.

In each of the procedures shown in FIGS. **8**(*b*), **9**(*b*), **10**(*b*) and **11**(*b*), the silicon nitride film **10***b* having high etching selectivity against the silicon oxide film is formed below the interlayer insulating film **11**. Therefore, the silicon nitride film **10***b* is prevented from being completely removed by the over-etch in etching the interlayer insulating film **11**. When the silicon nitride film **10***b* is to be removed from the layered film **10**, the silicon oxide film **10***a* is prevented from being completely removed since the etching selectivity between the silicon nitride film **10***b* and the silicon oxide film **10***a* below is high. Furthermore, since the silicon oxide film **10***a* has a thickness of approximately 70 nm, which is smaller than the level difference of 0.2 μm between the isolation and the active area, the isolation **2***b* is prevented from being etched to be lower than the surface of the active area by the over-etch in etching the silicon oxide film **10***a*. In other words, a recess where the top surface of the isolation **2***b* is lower than the surface of the silicon substrate is never formed in any part of the contact hole **20**. Accordingly, in the formation of the contact hole for electrically connecting the interconnection layer formed on the interlayer insulating film and the active area of the semiconductor substrate, the same effects as those described in the aforementioned embodiments can be attained.

However, the underlying film below the interlayer insulating film can be omitted in this embodiment. Even when it is omitted, since the step portion is formed between the top surface of the isolation and the surface of the active area, the isolation cannot be etched to be lower than the surface of the active area in the formation of the contact hole. Thus, the

degradation of the junction voltage resistance the increase of the junction leakage current can be prevented as much as possible.

(Embodiment 8)

Embodiment 8 will now be described referring to FIGS. **12** and **13**(*a*) through **13**(*e*). FIG. **12** is a sectional view showing the structure of a semiconductor device of this embodiment, and FIGS. **13**(*a*) through **13**(*e*) are sectional views for showing manufacturing procedures for the semiconductor device having the structure shown in FIG. **12**.

As is shown in FIG. **12**, in a silicon substrate (or well) **1** of one conductivity type, a trench isolation **2***b* is formed in an isolation region Reiso for partitioning an area in the vicinity of the surface of the silicon substrate **1** into a plurality of transistor regions Refet. The top surface of the isolation **2***b* is sufficiently higher than the surface of the silicon substrate **1** in each transistor region Refet, and a step portion with a predetermined level difference is formed between the isolation **2***b* and the transistor region Refet. This isolation **2***b* is formed by filling a trench formed in the silicon substrate **1** with an insulating material as described below. Furthermore, a channel stop region **60** of the same conductivity type as that of the silicon substrate **1** is formed at least below the isolation **2***b*.

In each transistor region Refet partitioned by the isolation **2***b* is formed a MOS transistor including a gate electrode **4***a*, a gate oxide film **3**, electrode sidewalls **7***a*, a low-concentration source/drain region **6** and a high-concentration source/drain region **8**. Also, on the silicon substrate **1** excluding the transistor regions Refet and on the isolation **2***b*, a gate interconnection **4***b* formed simultaneously with the gate electrode **4***a* and interconnection sidewalls **7***b* are formed. Furthermore, an upper gate electrode **9***a*, an upper gate interconnection **9***b* and a source/drain electrode **9***c* each made of titanium silicide ($TiSi_2$) are formed on the gate electrode **4***a*, the gate interconnection **4***b* and the high-concentration source/drain region **8**, respectively.

This embodiment is characterized by a step sidewall **7***c* formed on the side surface of the step portion of the isolation **2***b* simultaneously with the electrode sidewalls **7***a* and the interconnection sidewalls **7***b*. A part of the step sidewall **7***c* is communicated with the electrode sidewalls **7***a* and the interconnection sidewalls **7***b*.

Furthermore, on the entire top surface of the substrate bearing the isolation **2***b*, the gate electrode **4***a* and the like, an interlayer insulating film **11** and a first layer metallic interconnection **23** are formed. The first layer metallic interconnection **23** is connected with the upper gate electrode **9***a* and the source/drain electrode **9***c* in the transistor region through a W plug **22**.

Now, the manufacturing procedures for realizing the structure shown in FIG. **12** will be described referring to FIGS. **13**(*a*) through **13**(*e*).

First, as is shown in FIG. **13**(*a*), a silicon oxide film **52** and a silicon nitride film **53** are deposited on a silicon substrate **1**. Then, a resist film **50***a* for exposing the isolation regions Reiso and masking the transistor regions Refet is formed on the silicon nitride film **53**. After this, etching is conducted by using the resist film **50***a* as a mask, so as to selectively remove the silicon nitride film **53** and the silicon oxide film **52** and further etch the silicon substrate **1**, thereby forming a trench **51**. At this point, differently from the conventional method of forming a trench, the silicon nitride film **53** has a thickness as large as approximately 150 through 200 nm. However, the silicon oxide film **52** has a thickness of 10 through 20 nm as in the conventional method. The depth of the trench **51** can be approximately 500 nm also as in the conventional method. Then, impurity ions of a conductivity type different from that of an impurity to be injected into a subsequently formed source/drain region are injected, thereby forming a channel stop region **60**.

Next, as is shown in FIG. **13**(*b*), after removing the resist film **50***a*, a silicon oxide film (not shown) is deposited so as to have a sufficient thickness larger than the sum of the depth of the trench **51** and the thickness of the remaining silicon nitride film **53**, namely, the height from the bottom of the trench **51** to the top surface of the silicon nitride film **53**. Then, the silicon oxide film is removed by the CMP method so as to expose the surface of the silicon nitride film **53**, thereby flattening the entire top surface of the substrate. Through this procedure, a trench isolation **2***b* made of the silicon oxide film is formed in the isolation region Reiso. The flattening method to be adopted is not limited to that described above but the surface can be flattened by etch-back using a resist film having a reverse pattern to the pattern of the transistor region Refet.

Then, the silicon nitride film **53** is removed by using a phosphoric acid boiling solution or the like and the silicon oxide film **52** is removed by using a hydrofluoric acid type wet etching solution or the like, so as to expose the surface of the silicon substrate **1** in the transistor region Refet, which procedures are not shown in the drawing. At this point, a step portion having a sufficient level difference between the surface of the silicon substrate **1** in the transistor region Refet and the top surface of the isolation **2***b* is exposed characteristically in this embodiment. The level difference is set at approximately 50 through 100 nm in consideration of the amount of over-etch in a procedure for forming sidewalls described below. However, in order to effectively achieve the effects of this embodiment, the thickness of an insulating film for the sidewall and the amount of over-etch are required to be appropriately determined in the subsequent procedure for forming the sidewalls.

Then, as is shown in FIG. **13**(*c*), a polysilicon film **4** is deposited on the silicon substrate **1** and the isolation **2***b*, and the resist film **50***b* for exposing an area excluding the areas for a gate electrode and a gate interconnection is formed thereon. Then, the dry etching is conducted by using the resist film **50***b* as a mask, thereby forming the gate electrode **4***a* and the gate interconnection **4***b*, which procedure is not shown in the drawing.

Next, as is shown in FIG. **13**(*d*), by using the gate electrode **4***a* as a mask, impurity ions at a low concentration are injected, thereby forming a low-concentration source/drain region **6**. Then, an insulating film **7** (a silicon oxide film) is deposited on the entire top surface of the substrate.

Then, as is shown in FIG. **13**(*e*), the insulating film **7** is anisotropically etched, thereby forming the electrode sidewalls **7***a* on the both side surfaces of the gate electrode **4***a* and interconnection sidewalls **7***b* on the both side surfaces of the gate interconnection **4***b*. At the same time, a step sidewall **7***c* is formed on the side surface of the step portion between the silicon substrate **1** in the transistor region Refet and the isolation **2***b*. After forming these sidewalls, impurity ions are injected, thereby forming the high-concentration source/drain region **8**. Also at this point, the step portion between the silicon substrate **1** in the transistor region Refet and the isolation **2***b* has the sufficient level difference.

Although the procedures thereafter are not shown in the drawing, an upper gate electrode **9***a*, an upper gate interconnection **9***b* and a source/drain electrode **9***c* are formed by a silicifying procedure, an interlayer insulating film **11** is

deposited and a contact hole is formed, and then the contact hole is filled with a metal, and a first layer metallic interconnection **12** is formed. In this manner, the MOS transistor having the trench isolation structure as shown in FIG. **12** is manufactured.

In the aforementioned procedures, the electrode sidewalls **7***a* and the like are formed in order to manufacture a transistor with the LDD structure. However, the electrode sidewalls **7***a* and the like can be formed in a transistor having the so-called pocket injection structure, in which a punch-through stopper is formed by injecting an impurity of a different conductivity type into an area between the source/drain region and the channel region. Therefore, this embodiment is applicable to such a transistor having the pocket injection structure.

In manufacturing a MOS transistor having a gate length of 1 μm or less as in this embodiment, it is necessary to form the electrode sidewalls **7***a* on the side surfaces of the gate electrode **4***a* in order to provide the transistor with the LDD structure or the pocket injection structure in which the short channel effect can be suppressed and the reliability of the transistor can be ensured. The thickness of the electrode sidewall **7***a* depends upon the characteristics of a device to be manufactured. Since the sidewall is formed by dry etching with high anisotropy, its thickness can be controlled substantially only by controlling the thickness of the film to be deposited. However, 10% through 30% over-etch is generally conducted in consideration of the fluctuation in the etching rate in the wafer and the fluctuation in the thickness of the deposited film. For example, when the electrode sidewall **7***a* is formed out of an insulating film with a thickness of 100 nm, the etching is conducted for a time period corresponding to time required for removing an insulating film with a thickness of 110 through 130 nm.

At this point, the isolation **2***b* made of an oxide film is etched at higher selectivity than the silicon substrate **1** in the transistor region Refet, and hence, the isolation **2***b* is removed by a thickness of, for example, 10 through 30 nm. Therefore, in the conventional structure, the surface of the isolation **105***a* becomes lower than the surface of the silicon substrate **101** as is shown in FIGS. **21**(*a*) and **21**(*b*), resulting in causing the aforementioned problems. In contrast, in the state of this embodiment shown in FIG. **13**(*d*), the isolation **2***b* has the step portion whose surface is higher than the surface of the silicon substrate in the transistor region Refet, resulting in effectively preventing the problems. In other words, even when the impurity ions are diagonally injected for the formation of the high-concentration source/drain region **8**, the impurity ions are prevented from being implanted below the edge of the isolation **2***b* because the step portion of the isolation **2***b* has a sufficient level difference. Accordingly, a distance between the high-concentration source/drain region **8** and the channel stop region **60** can be made substantially constant, thereby preventing the degradation of the junction voltage resistance and the increase of the junction leakage. Furthermore, in the formation of the source/drain electrode **9***c* of silicide on the high-concentration source/drain region **8**, the step sidewall **7***c* effectively prevents the silicide layer from being formed in the boundary between the silicon substrate **1** and the isolation **2***b*. Therefore, it is possible to effectively prevent a short circuit current from occurring between the source/drain electrode **9***c* and the channel stop region **60**.

In order to effectively achieve the aforementioned effects in this embodiment, however, the level difference caused by the step portion is-preferably larger than the amount of over-etch in the formation of the sidewalls, that is, 10 through 30 nm. Furthermore, in practical use, after the formation of the isolation **2***b,* other procedures are conducted in which the thickness of the silicon oxide film used as the isolation **2***b* is decreased, such as a procedure for removing the silicon oxide film **52**. Therefore, it is preferred that the step portion is previously formed so as to have a sufficiently large level difference also in consideration of the afterward decreased amount. Accordingly, the lower limit of the thickness of the silicon nitride film **53** deposited in the procedure shown in FIG. **13**(*a*) is determined on the basis of the amount of over-etch and the etched amount in the procedure for removing the silicon oxide film **52**.

In this embodiment, the silicon nitride film **53** is used as an etching mask for forming the trench **51**. This film can be made of any material which has large etching selectivity against the silicon oxide film, and can be, for example, a polysilicon film or the like.

This embodiment exemplifies the so-called salicide structure in which the upper gate electrode **9***a* and the source/drain electrode **9***c* are simultaneously silicified in a self-aligned manner for attaining low resistance. It goes without saying that the embodiment is applicable to a structure in which a gate electrode is previously formed as a polycide electrode and a source/drain electrode alone is silicified afterward.

(Embodiment 9)

Embodiment 9 will now be described referring to FIGS. **14**(*a*) through **14**(*e*). This embodiment is different from Embodiment 8 in that a gate oxide film and a polysilicon film serving as a gate electrode are deposited before forming a trench isolation.

First, as is shown in FIG. **14**(*a*), a gate oxide film **3** and a polysilicon film **4** serving as a gate electrode of a MOS transistor are successively deposited on a silicon substrate **1**. A resist film **50***a* for exposing an isolation region Reiso and masking a transistor region Refet is patterned. By using the resist film **50***a* as a mask, the polysilicon film **4** and the gate oxide film **3** are selectively removed, and further the silicon substrate **1** is etched, thereby forming a trench **51** serving as the isolation region. At this point, differently from the conventional method of forming a trench, the thickness of the polysilicon film **4** is set at 150 through 200 nm, that is, substantially the same thickness as that of the silicon nitride film used in Embodiment 8. The gate oxide film **3** has a thickness of 10 through 20 nm. The depth of the trench **51** is approximately 500 nm. Then, impurity ions of a different conductivity type from that of an impurity to be injected into a source/drain region formed afterward are injected, thereby forming a channel stop region **60**.

Then, after removing the resist film **50***a,* a silicon oxide film **2** (not shown) is deposited so as to have a sufficient thickness larger than the sum of the depth of the trench **51** and the thickness of the remaining polysilicon film **4**, namely, the height from the bottom of the trench **51** to the top surface of the polysilicon film **4**. The silicon oxide film **2** is removed by the CMP method until the surface of the polysilicon film **4** is exposed, thereby flattening the top surface of the substrate. Through this procedure, a trench isolation **2***b* made of the silicon oxide film is formed in the isolation region Reiso. The flattening method to be adopted is not limited to that described above but the surface can be flattened by etch-back using a resist film having a reverse pattern to the pattern of the transistor region Refet.

Next, as is shown in FIG. **14**(*b*), a conductive film **18** serving as a gate interconnection layer (which can be made of a conductive polysilicon film; a silicide film of WSi, TiSi or the like; or a metal with a high melting point such as W

with a sandwiched barrier metal such as TiN for achieving low resistance) and a protection film **19** made of an insulating film are deposited on the flattened substrate. Then, a resist film **50***b* for exposing an area excluding the areas for a gate electrode and a gate interconnection is formed. By using the resist film **50***b* as a mask, dry etching is conducted, thereby forming a gate electrode **4***a,* an upper gate electrode **18***a* and a protection film **19***a,* a gate interconnection **4***b,* an upper gate interconnection **18***b* and a protection film **19***b,* which procedures are not shown in the drawing. At this point, a step portion having a sufficient level difference between the surfaces of the silicon substrate **1** in the transistor region Refet and the isolation **2***b* is exposed characteristically in this embodiment. The level difference is approximately 50 through 100 nm in consideration of the amount of over-etch in the subsequent procedure for forming sidewalls and the like. However, in order to effectively achieve the effects of this embodiment, the thickness of an insulating film for the sidewall and the amount of over-etch are required to be appropriately determined in the subsequent procedure for forming the sidewalls.

Then, as is shown in FIG. **14**(*c*), similarly to Embodiment 8, after forming a low-concentration source/drain region **6** on either side of the gate electrode **4***a* in the active area, an insulating film **7** (silicon oxide film) is deposited on the entire top surface of the substrate.

Next, as is shown in FIG. **14**(*d*), the insulating film **7** is anisotropically etched, thereby forming electrode sidewalls **7***a* on both side surfaces of the gate electrode **4***a* and the like and interconnection sidewalls **7***b* on both side surfaces of the gate interconnection **4***b* and the like. At the same time, a step sidewall **7***c* is formed on the side surface of the step portion between the silicon substrate **1** in the transistor region Refet and the isolation **2***b*. After forming these sidewalls, impurity ions are injected, thereby forming a high-concentration source/drain region **8**. Also at this point, the step portion between the silicon substrate **1** in the transistor region Refet and the isolation **2***b* has a sufficient level difference.

Next, as is shown in FIG. **14**(*e*), a source/drain electrode **9***c* is formed out of silicide only on the high-concentration source/drain region **8**.

Although the procedures thereafter are not shown in the drawing, an interlayer insulating film **11** is deposited, a contact hole is formed, and the contact hole is filled with a metal (such as tungsten), and a first layer metallic interconnection **12** is formed. Thus, a MOS transistor having a trench isolation similar to that shown in FIG. **12** is manufactured. In this embodiment, however, on the gate electrode **4***a* and the gate interconnection **4***b* are formed the upper gate electrode **18***a* and the upper gate interconnection **18***b* made of conductive polysilicon, silicide or the like as well as the protection films **19***a* and **19***b* made of the insulating film, respectively. The source/drain electrode **9***c* of silicide is formed in the procedure different from that for forming the upper gate electrode **18***a* and the upper gate interconnection **18***b.*

In this manner, the step portion which is higher at the side closer to the isolation **2***b* is formed between the silicon substratel in the transistor region Refet and the isolation **2***b,* and the step portion is provided with the step sidewall **7***c* on its side surface in this embodiment. Therefore, the same effects as those of Embodiment 8 can be exhibited with a reduced number of manufacturing procedures.

In addition, the procedure for forming the gate electrode **4***a* and the gate interconnection **4***b* after the procedure shown in FIG. **14**(*b*) can be conducted on the completely flat top surface of the substrate without being affected by the step portion at the edge of the isolation **2***b* in this embodiment. Therefore, a refined pattern can be advantageously stably formed.

(Embodiment 10)

Embodiment 10 will now be described referring to FIGS. **15**(*a*) through **15**(*f*), which are sectional views for showing manufacturing procedures for a semiconductor device of this embodiment.

Before achieving the state shown in FIG. **15**(*a*), a trench isolation **2***b,* a channel stop region **60**, a low-concentration source/drain region **6**, a gate insulating film **3**, a gate electrode **4***a,* a gate interconnection **4***b* and the like are formed through the same procedures as those described in Embodiment 8. Then, a protection oxide film **31**, a silicon nitride film **32** for sidewalls and a polysilicon film **33** for a mask are deposited on the substrate by the CVD method. At this point, the thickness of a polysilicon film to be used as the gate electrode **4***a* and the gate interconnection **4***b* is 330 nm, and the minimum line width is 0.35 μm. The protection oxide film **31** has a thickness of approximately 20 nm, the silicon nitride film **32** has a thickness of approximately 30 nm, and the polysilicon film **33** has a thickness of approximately 100 nm.

Then, as is shown in FIG. **15**(*b*), the polysilicon film **33** is etched back by RIE (reactive ion etching), thereby forming electrode polysilicon masks **33***a*, interconnection polysilicon masks **33***b* and a step polysilicon mask **33***c* on side surfaces of the gate electrode **4***a,* the gate interconnection **4***b* and a step portion of the isolation **2***b,* respectively. At this point, the etching selectivity between the polysilicon film **33** and the silicon nitride film **32** is large.

Next, as is shown in FIG. **15**(*c*), by using the remaining polysilicon masks **33***a,* **33***b* and **33***c* as masks, wet etching using heated phosphoric acid (H_3PO_4) at 150° C. is conducted, so as to have portions of the silicon nitride film **32** covered with the polysilicon masks **33***a,* **33***b* and **33***c* remained and remove the other portions thereof. At this point, the etching selectivity between the silicon nitride film **32** and the polysilicon masks **33***a,* **33***b* and **33***c* can be approximately 30:1. Through this procedure, electrode sidewalls **32***a,* interconnection sidewalls **32***b* and a step sidewall **32***c* each having an L-shape remain on the sides of the gate electrode **4***a,* the gate interconnection **4***b* and the step portion, respectively.

Then, as is shown in FIG. **15**(*d*), by using the gate electrode **4***a,* the protection oxide film **31**, the electrode polysilicon mask **33***a,* the electrode sidewall **32***a,* the step polysilicon mask **33***c* and the step sidewall **32***c* as masks, impurity ions are injected at a high concentration into the active area of the silicon substrate **1**, thereby forming a high-concentration source/drain region **8**.

Then, as is shown in FIG. **15**(*e*), the polysilicon masks **33***a,* **33***b* and **33***c* are removed by dry or wet etching.

Next, as is shown in FIG. **15**(*f*), exposed portions of the protection oxide film **31** on the substrate are removed by using a HF type etching solution. Then, a titanium film is deposited and a first RTA treatment is conducted, thereby forming a silicide layer of a $TiSi_2$ film through the reaction between titanium and silicon. The titanium film is then removed, and a second RTA treatment is conducted, so that an upper electrode **9***a,* an upper interconnection **9***b* and a source/drain electrode **9***c* each of a silicide layer with a low resistance are formed on the gate electrode **4***a,* the gate interconnection **4***b* and the source/drain region **8**, respectively. Thereafter, an interlayer insulating film is deposited, the top surface of the substrate is flattened, a contact hole is formed, a metallic interconnection film is deposited, and a metallic interconnection is formed. Thus, an LSI is manufactured.

Since the protection oxide film **31** and the L-shaped step sidewall **32***c* are formed on the side surface of the step portion in the procedure shown in FIG. **15**(*f*) in this embodiment, the silicide layer is effectively prevented from being formed in the boundary between the active area of the silicon substrate **1** and the isolation **2***b*.

Furthermore, since the protection oxide film **31** is formed on the isolation **2***b* and the active area of the silicon substrate **1** in the procedures shown in FIGS. **15**(*c*) and **15**(*d*), the thickness of the isolation **2***b* is never decreased through the formation of the L-shaped sidewalls **32***a,* **32***b* and **32***c*. Accordingly, it is possible to decrease the level difference between the isolation **2***b* and the silicon substrate **1**, resulting in improving the patterning accuracy for the gate.

In the formation of the gate electrode, first and second conductive films can be used similarly to Embodiment 2. Also in this case, the same effects as those of this embodiment can be exhibited.

(Embodiment 11)

In each of the aforementioned embodiments, each sidewall is made of an insulating material such as a silicon oxide film and a silicon nitride film. The sidewall can be made of a conductive material such as a polysilicon film. FIGS. **16**(*a*) through **16**(*e*) are sectional views for showing manufacturing procedures for a semiconductor device including conductive sidewalls.

Before attaining the state shown in FIG. **16**(*a*), a trench isolation **2***b,* a channel stop region **60**, a low-concentration source/drain region **6**, a gate insulating film **3**, a gate electrode **4***a,* a gate interconnection **4***b* and the like are formed through the same procedures as those described in Embodiment 8. Then, a protection oxide film **31** and a polysilicon film **34** for sidewalls are deposited on the top surface by the CVD method. In this embodiment, on the gate electrode **4***a* and the gate interconnection **4***b* are formed protection silicon oxide films **15***a* and **15***b,* respectively. At this point, a polysilicon film to be used as the gate electrode **4***a* and the gate interconnection **4***b* has a thickness of 330 nm, and the minimum line width is 0.35 μm. The protection oxide film **31** has a thickness of approximately 20 nm and the polysilicon film **34** has a thickness of approximately 100 nm.

Next, as is shown in FIG. **16**(*b*), the polysilicon film **34** is etched back by the RIE, thereby forming electrode sidewalls **34***a,* interconnection sidewalls **34***b* and a step sidewall **34***c* each made of the polysilicon film on sides of the gate electrode **4***a,* the gate interconnection **4***b* and a step portion of the isolation **2***b,* respectively.

Next, as is shown in FIG. **16**(*c*), by using the gate electrode **4***a,* the protection oxide film **31**, the electrode sidewalls **34***a* and the step sidewall **34***c* as masks, impurity ions are injected at a high concentration into an active area of the silicon substrate **1**, thereby forming a high-concentration source/drain region **8**.

Then, as is shown in FIG. **16**(*d*), exposed portions of the protection oxide film **31** on the substrate are removed by using the HF type etching solution. Then, as is shown in FIG. **16**(*e*), a titanium film is deposited and a first RTA treatment is conducted, thereby forming a silicide layer made of a $TiSi_2$ film through the reaction between titanium and silicon. The titanium film is then removed and a second RTA treatment is conducted, thereby forming a source/drain electrode **9***d* made of a silicide layer stretching over the electrode sidewall **34***a,* the high-concentration source/drain region **8** and the step sidewall **34***c*. Since the silicide layer is formed also on the interconnection sidewall **34***b,* this silicide layer can be connected with the source/drain electrode. Therefore, in this embodiment, etching is conducted on the isolation **2***b* by using a resist film or the like, so as to selectively remove the interconnection sidewalls **34***b* on the sides of the gate interconnection **4***b* as well as the silicide layer thereon. Thus, the source/drain electrodes **9***d* in the respective active areas are prevented from being mutually connected. It is possible to selectively remove merely the interconnection sidewalls **34***b* on the sides of the gate interconnection **4***b* immediately after forming the sidewalls **34***a,* **34***b* and **34***c* of the polysilicon film.

Thereafter, an interlayer insulating film is deposited, the top surface of the substrate is flattened, a contact hole is formed, a metallic interconnection film is deposited, and a metallic interconnection is formed. Thus, an LSI is manufactured.

In this embodiment, the source/drain electrode **9***d* is ultimately formed so as to stretch over a large area including the electrode sidewall **34***a,* the high-concentration source/drain region **8** and the step sidewall **34***c*. Accordingly, the level difference between the transistor region Refet and the isolation **2***b* can effectively prevent the high-concentration source/drain region **8** from being brought close to the channel stop region **60** in the impurity ion injection. Furthermore, in the formation of the source/drain electrode **9***d* of silicide on the high-concentration source/drain region **8**, also the step sidewall **34***c* is silicified by a certain thickness. However, since the silicide layer is prevented from being formed in a further thickness, a short circuit current between the source/drain electrode **9***d* and the channel stop region **60** is effectively prevented from being caused by the formation of the silicide layer in the interface between the isolation and the silicon substrate. Moreover, since the large area stretching over the electrode sidewall **34***a,* the high-concentration source/drain region **8** and the step sidewall **34***c* is silicified in this embodiment, it is very easy to form a contact member to be connected with an upper first layer interconnection. As a result, the area of the transistor region Refet can be decreased, namely, the integration of the semiconductor device can be advantageously improved. Although the electrode sidewalls **34***a* and the interconnection sidewalls **34***b* are made of a conductive polysilicon film, there is no possibility of a short circuit between the sidewall and the gate because the respective sidewalls **34***a* and **34***b* are insulated from the gate electrode **4***a* and the gate interconnection **4***b* by the protection oxide film **31**.

In the formation of the gate electrode, first and second conductive films can be used similarly to Embodiment 9, and also in this case, the same effects as those of this embodiment can be attained.

The sidewalls are made of a polysilicon film in this embodiment, and the polysilicon film can be replaced with an amorphous silicon film. Furthermore, the sidewalls can be made not only of a silicon film but also of another conductive material such as a metal, and it is not necessarily required to silicify the sidewalls.

In each of the aforementioned embodiments, the description is made on the case where the semiconductor element formed in the active area is a field effect transistor. However, the invention is not limited to these embodiments, and is applicable when the semiconductor element is a bipolar transistor and the active area is an emitter diffused layer, a collector diffused layer or a base diffused layer of the bipolar transistor.

In each embodiment, setting of an angle of the side surface of the step portion to be equal to or more than 70° ensures a large level difference between the active area and the side surface of the step portion around the boundary of

the active area, thereby preventing formation of a deep recess on the isolation.

What is claimed is:

1. A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on a semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;

a third step of forming a gate electrode on the gate insulating film and forming an interconnection on the trench islation;

after the third step, a fourth step of forming an underlying film on the entire surface of the semiconductor substrate;

a fifth step of forming an interlayer insulating film on the underlying film;

a sixth step of forming a hole stretching over at least a part of the active area, at least a part of the interconnection and at least a part of the trench islation providided therebetween by selectively removing the interlayer insulating film and the underlying film; and

a seventh step of forming a buried conductive layer by filling the hole with a conductive material,

wherein the underlying film is made of an insulating material having high etching selectivity against the interlayer insulating film in a dry etching process.

2. The method of manufacturing a semiconductor device of claim **1**, wherein the underlying film has a silicon nitride film.

3. The method of manufacturing a semiconductor device of claim **1**, further comprising, after the third step and before the fourth step, a step of forming a source/drain region in the active area on both sides of the gate electrode,

wherein, in the sixth step, the hole are formed so as to reach the source/drain region.

4. The method of manufacturing a semiconductor device of claim **1**, wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

5. The method of manufacturing a semiconductor device of claim **4**, wherein the plug underlying film is made of a TiN/Ti film.

6. The method of manufacturing a semiconductor device of claim **1**, wherein in the sixth step, the trench isolation is not etched lower than the surface of the active area when forming of the hole.

7. The method of manufacturing a semiconductor device of claim **1** further comprising, after the third step and before the fourth step, a step of forming a source/drain region in the active area on both sides of the gate electrode, and a step of forming a silicide layer on the source/drain region.

8. The method of manufacturing a semiconductor device of claim **7** further comprising, after the third step, a step of forming sidewalls on both sides of the gate electrode before forming the source/drain region.

9. The method of manufacturing a semiconductor device of claim **1**, wherein the sixth step is performed so that the hole stretch over the entire part of the trench isolation provided between the active area and the interconnection.

10. A method of manufacturing a semiconductor device comprising:

a first step of forming an underlying insulating film on a semiconductor substrate;

a second step of depositing an etching stopper film on the underlying insulating film;

a third step of forming a trench by exposing a portion of the etching stopper film and the underlying insulating film where an isolation is to be formed and etching the semiconductor substrate in the exposed portion;

a fourth step of depositing an insulating film for isolation on an entire top surface of the substrate, flattening the substrate until at least a surface of the etching stopper film is exposed, and forming a trench isolation in the trench so as to surround a transistor region;

a fifth step of removing, by etching, at least the etching stopper film and the underlying insulating film, so as to expose a step portion between the transistor region and the trench isolation;

a sixth step of sequentially depositing a gate oxide film, a conductive film and a first protection insulating film on the substrate and forming a gate electrode and a gate insulating film by patterning the conductive film and the first protection insulating film;

after the sixth step, a seventh step of depositing a second protection insulating film on the entire top surface of the substrate;

after the seventh step, an eighth step of depositing an insulating film for sidewalls made of a silicon film on the entire top surface of the substrate and anisotropically etching the insulating film for the sidewalls, so as to form electrode sidewalls and a step sidewall on side surfaces of the gate electrode and the step portion, respectively;

a ninth step of introducing an impurity into the semiconductor substrate in the transistor region on both sides of the gate electrode, so as to form source/drain regions; and

after the ninth step, a tenth step of silicifying an area stretching over the electrode sidewall, the active area and the step sidewall.

11. The method of manufacturing a semiconductor device of claim **10**, wherein in the second step, a thickness of the etching stopper film is determined in consideration of an amount of over-etch in the eighth step, so that the step portion having a level difference with a predetermined size or more is exposed in the fifth step.

12. A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench islation on the semiconductor substrate;

a third step of forming a gate electrode on the gate insulating film;

after the third step, a fourth step of forming an insulating film on the substrate;

a fifth step of anisotropically etching the insulating film so as to form first sidewalls on both side surfaces of the gate electrode and form second sidewalls on a side surface of a step portion in the boundary between the trench isolation and the active area; and

after the fifth step, a sixth step of forming a laminated film made of a silicon oxide film and a silicon nitride film on the entire top surface of the substrate;

a seventh step of forming an interlayer insulating film on the silicon nitride film;

an eighth step of forming a hole by selectively removing the interlayer insulating film and the laminated film; and

a ninth step of forming a buried conductive layer by filling the hole with a conductive material.

13. The method of manufacturing a semiconductor device of claim **12** further comprising, after the fifth step and before the sixth step, a step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode,

wherein, in the eighth step, the hole are formed so as to reach the source/drain region.

14. The method of manufacturing a semiconductor device of claim **12**, wherein, in the eight step, the hole are formed over the active area, the sidewall and the trench isolation.

15. The method of manufacturing a semiconductor device of claim **12**, wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

16. The method of manufacturing a semiconductor device of claim **15**, wherein the plug underlying film is made of a TiN/Ti film.

17. A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate; a third step of forming a gate electrode on the gate insulating film;

after the third step, a fourth step of forming a laminated film made of a lower film and an upper film on the entire surface of the semiconductor substrate on which the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate is formed;

a fifth step of forming an interlayer insulating film on the upper film;

a sixth step of selectively removing the interlayer film and the laminated film and forming a hole; and

a seventh step of forming a buried conductive layer by filling the hole with a conductive material,

wherein the upper film is made of an insulating material having high etching selectivity against the interlayer insulating film in dry etching.

18. The method of manufacturing a semiconductor device of claim **17**, wherein the upper film is made of a silicon nitride film.

19. The method of manufacturing a semiconductor device of claim **17** further comprising, after the third step and before the fourth step, a step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode,

wherein in the sixth step, the hole are formed so as to reach the source/drain region.

20. The method of manufacturing a semiconductor device of claim **17**, wherein in the sixth step, the hole are formed over the active area, the sidewall and the trench isolation.

21. The method of manufacturing a semiconductor device of claim **17**, wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

22. The method of manufacturing a semiconductor device of claim **21**, wherein the plug underlying film is made of a TiN/Ti film.

* * * * *

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Appeal
1/21/03

ATTORNEY DOCKET NO. 60188-1076
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Mizuki Segawa et al.

Group Art Unit: 2822

Serial No.: 09/902,157
(DIV of SN: 08/685,726)

Examiner: J. VOCKROD

Filed: July 11, 2001

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

AMENDMENT UNDER 37 C.F.R. § 1.111

Hon. Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated October 15, 2002, having a shortened statutory period for response set to expire on January 15, 2003, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 18-30 and 35-38, without prejudice, and add new claims 39-51 as follows:

39. A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;

a third step of forming a gate electrode on the gate insulating film;

after the third step, a fourth step of forming an insulating film on the substrate; and

a fifth step of anisotropically etching the insulating film so as to form first sidewalls on both side surfaces of the gate electrode and form second sidewalls on a side surface of a step portion in the boundary between the trench isolation and the active area.

40. The method of manufacturing a semiconductor device of Claim ~~39~~ further comprising, after the fifth step, a sixth step of forming a laminated film made of a silicon oxide film and a silicon nitride film on the entire top surface of the substrate;

a seventh step of forming an interlayer insulating film on the silicon nitride film;

an eighth step of selectively removing the interlayer insulating film and the laminated film and forming holes; and

a ninth step of forming a buried conductive layer by filling the holes with a conductive material.

41. The method of manufacturing a semiconductor device of Claim 40 further comprising, after the fifth step and before the sixth step, a step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode,

wherein, in the eighth step, the holes are formed so as to reach the source/drain region.

42. The method of manufacturing a semiconductor device of Claim 40,

wherein, in the eighth step, the holes are formed over the active area, the sidewall and the trench isolation.

43. The method of manufacturing a semiconductor device of Claim 40,

wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

44. The method of manufacturing a semiconductor device of Claim 43,

wherein the plug underlying film is made of a TiN/Ti film.

45. The method of manufacturing a semiconductor device of Claim 39 further comprising, after the fifth step, a sixth step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode;

after the sixth step, a seventh step of forming an insulating film on the entire top surface of the substrate,

an eighth step of removing the insulating film and forming holes so as to reach the source/drain region; and

a ninth step of forming an interconnection connected to the source/drain region through the holes on the insulating film.

46. A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;

a third step of forming a gate electrode on the gate insulating film;

after the third step, a fourth step of forming a laminated film made of a lower film and an upper film on the entire surface of the semiconductor substrate on which the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate is formed;

a fifth step of forming an interlayer insulating film on the upper film;

a sixth step of selectively removing the interlayer insulating film and the laminated film and forming holes; and

a seventh step of forming a buried conductive layer by filling the holes with a conductive material,

wherein the upper film is made of an insulating material having high etching selectivity against the interlayer insulating film in dry etching.

47. The method of manufacturing a semiconductor device of Claim 46, wherein the upper film is made of a silicon nitride film.

48. The method of manufacturing a semiconductor device of Claim 46 further comprising, after the third step and before the fourth step, a step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode,

wherein in the sixth step, the holes are formed so as to reach the source/drain region.

49. The method of manufacturing a semiconductor device of Claim 46, wherein in the sixth step, the holes are formed over the active area, the sidewall and the trench isolation.

50. The method of manufacturing a semiconductor device of Claim 46, wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

51. The method of manufacturing a semiconductor device of Claim 50, wherein the plug underlying film is made of a TiN/Ti film.

REMARKS

I. Introduction

In response to the pending rejection, Applicants have cancelled claims 18-30 and 35-38, without prejudice, and added new claims 39-51. More specifically, new claims 39-45 are supported, for example, by Figs. 3-7, 9-11, and the corresponding portions of the specification, and claims 46-51 are supported, for example, by Fig. 8. No new matter has been added.

Applicants note with appreciation the Examiner's early indication of allowance of claims 31-34.

For the reasons set forth below, Applicants respectfully submit that the newly submitted claims are patentable over the cited prior art.

II. Claim 39 Is Patentable Over The Cited Prior Art

As recited by claim 39, the present invention relates to a method of manufacturing a semiconductor device, which comprises the steps of:

> *a) a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;*
> *b) a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;*
> *c) a third step of forming a gate electrode on the gate insulating film;*
> *d) after the third step, a fourth step of forming an insulating film on the substrate; and*
> *e) a fifth step of anisotropically etching the insulating film so as to form first sidewalls on both side surfaces of the gate electrode and form second sidewalls on a side surface of a step portion in the boundary between the trench isolation and the active area.*

According to the foregoing method (referring for example to Figs. 3a-3f), the gate insulating film 3 and the gate electrode 4a are sequentially formed on the active area

surrounded by the trench isolation 2b, and then the first sidewalls 7a are formed on both sides surfaces of the gate electrode and the second sidewalls 7c are formed on a side surface of the step portion in the boundary between the trench isolation and the active area. As a result of the formation of the second sidewalls, the abrupt level difference between the surface of the isolation and the active area can be released by the step sidewall. Therefore, a residue is substantially eliminated in patterning of the interconnection members, and an upper interconnection is prevented from being disconnected or exhibiting an increase in its resistance.

Moreover, in the case where holes are formed on the interlayer insulating film, even when the holes are formed over the active area, the sidewall and the trench isolation, which is caused by the alignment shift in the lithography, degradation of the junction voltage resistance and an increase of the junction leakage current at the ends of the trench isolation is advantageously suppressed.

It is further noted that new claim 39 includes the step recited in allowed claim 31 (*see*, step 7 in claim 31, and step e of claim 39) that was indicated in the Office Action as being one of the reasons for allowance of claim 31.

Turning to the cited prior art, as shown in Fig. 1B thereof, Josquin (EP 0 243 988) discloses a field insulation 6 to be utilized as an isolation, which is formed by the LOCOS method. It is respectfully submitted that the field insulation 6 of Josquin is clearly different from the trench isolation of the present invention, and therefore Josquin fails to disclose the claimed trench isolation.

More importantly, as already noted by the Examiner, as shown in Fig. 3B of Josquin, although sidewalls 43 are formed on the side surfaces of the gate electrode 35,

no sidewall is found on the step portion in the boundary between the field insulation 6 and the active area. ***In other words, Josquin fails to disclose or suggest that the first sidewalls are formed on both side surfaces of the gate electrode and second sidewalls are formed on a side surface of a step portion in the boundary between the trench isolation and the active area as is recited by new claim 39.***

Turning to Mandelman (USP No. 5,521,422), as shown in Fig. 5 thereof, a spacer (sidewall) 22 is formed on the step portion in the boundary between the trench isolation 18 and a silicon substrate 10, and then a gate insulating film 38 and a gate electrode 40 are formed. As a result of the structure, it is technically impossible to form the spacer (sidewall) 22 on the step portion in the boundary between the trench isolation 18 and the silicon substrate 10 and form the sidewall on the side surface of the gate electrode 40 during the same etching step. Thus, Mandelman also fails to disclose or suggest new claim 39.

For at least the foregoing reasons, as neither Josquin nor Mandelman disclose or suggest the foregoing steps recited by the method of new claim 39, it is respectfully submitted that new claim 39 and the claims dependent thereon, are patentable over the cited prior art references.

III. Claim 46 Is Patentable Over The Cited Prior Art

New claim 46, which corresponds to original claim 30, recites a method of manufacturing a semiconductor device, comprising the steps of:

> *a) a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;*

b) a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;

c) a third step of forming a gate electrode on the gate insulating film;

d) after the third step, a fourth step of forming a laminated film made of a lower film and an upper film on the entire surface of the semiconductor substrate on which the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate is formed;

e) a fifth step of forming an interlayer insulating film on the upper film;

f) a sixth step of selectively removing the interlayer insulating film and the laminated film and forming holes; and

g) a seventh step of forming a buried conductive layer by filling the holes with a conductive material,

***wherein the upper film is made of an insulating material having high* etching selectivity against the interlayer insulating film <u>in dry etching</u>.**

By utilizing the foregoing process, which includes forming an upper film having high etching selectivity on the active area and the trench isolation prior to formation of the interlayer insulating film, even when etching the interlayer insulating film utilizing a dry etching process, the trench isolation having a top surface at a higher level than a surface of the active area is not etched or reduced in height during the etching of the interlayer insulating film.

More specifically, when forming the holes in the thick interlayer insulating film (used to form the buried conductive layers), it is necessary to increase the over-etch ratio. However, as a result of the process of present invention, the surfaces of the active area and the trench isolation are not etched because they are protected by the laminated film including an upper film having high etching selectivity. Thus, when selectively etching the laminated film having a thin thickness, a small over-etch ratio is sufficient, and the initial step portion in the boundary is not degraded during the etching process.

Turning to the cited prior art applied against claim 30, it is noted that the Examiner acknowledges that Josquin and Mandelman do not disclose the use of the

laminated film comprising a lower film and an upper film, where **the upper film is made of an insulating material having high etching selectivity against the interlayer insulating film in dry etching**. Hsia (USP No. 5,393,708) is relied upon as curing this defect in the combination of Josquin and Mandelman. Applicants respectfully submit that this conclusion is in error for at least the following reasons.

First, as recited by the pending claim, a laminated film having an upper film and a lower film is formed over the entire substrate including the upper surface of the trench. Then, the interlayer insulating film is formed on the upper film of the laminated layer. However, as noted by the Examiner, Hsia only discloses a thin silicon dioxide layer 16 and a thick BPSG layer 18 formed on the gate electrode. Accordingly, even assuming *arguendo* that the BPSG layer 18 of Hsia corresponds to the claimed interlayer insulating film, Hsia has no component corresponding to the claimed laminated film having an upper film and a lower film. Indeed, Hsia would only disclose a single layer disposed between the gate electrode and the interlayer insulating film.

Moreover, while it is asserted in the pending rejection that Hsia discloses depositing TEOS oxide over the gate electrode followed by a BPSG layer, Hsia merely discloses that layer 16 is silicon oxide (*see*, col. 2, lines 36-39). However, even assuming it was a TEOS layer, the TEOS layer would still fail to satisfy the selectivity to etching requirement of the upper layer of the laminated film as recited by claim 30. Specifically, while it is known that TEOS oxide films exhibit high etching selectivity against BPSG films in a wet etching process, TEOS oxide films do not exhibit high etching selectivity against BPSG films in a dry etching process. Indeed, in a dry etching process, the TEOS oxide film and the BPSG film are etched at substantially the same

rate when utilizing an etching gas for an oxide film system. Thus, in the dry etching process, the TEOS oxide film does not exhibit a high etching selectivity against the BPSG film as is required by new claim 46.

Accordingly, even assuming *arguendo* that the combination of Josquin, Mandelman and Hsia is proper, the combination still fails to disclose or suggest at least the two foregoing limitations recited by claim 46. As such, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 (*see*, M.P.E.P. § 2143.03), and the cited combination does not do so, it is respectfully submitted that claim 46 and the claims dependent thereon are patentable over Josquin, Mandelman and Hsia.

Furthermore, it is also submitted that there is no motivation to combine the references in the manner suggested in the pending rejection. The alleged basis for combining the references was to achieve the planarization effects taught by Hsia. However, it is noted that the planarization techniques disclosed by Hsia relate to modifying layers disposed on top of the metal layer 20. Hsia does not appear to disclose or suggest any modification of the layers disposed on the gate electrode and the substrate. Thus, even if Hsia and the other references were combined, the combination would not result in the modification proposed in the pending rejection. For this additional reason, it is submitted that the pending rejection is in error.

IV. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: 1/15/03

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APPENDIX

Claims 18-30 and 35-38 has been canceled and new claims 39-51 have been added as follows:

39. A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;

a third step of forming a gate electrode on the gate insulating film;

after the third step, a fourth step of forming an insulating film on the substrate; and

a fifth step of anisotropically etching the insulating film so as to form first sidewalls on both side surfaces of the gate electrode and form second sidewalls on a side surface of a step portion in the boundary between the trench isolation and the active area.

40. The method of manufacturing a semiconductor device of Claim 39 further comprising, after the fifth step, a sixth step of forming a laminated film made of a silicon oxide film and a silicon nitride film on the entire top surface of the substrate;

a seventh step of forming an interlayer insulating film on the silicon nitride film;

an eighth step of selectively removing the interlayer insulating film and the laminated film and forming holes; and

a ninth step of forming a buried conductive layer by filling the holes with a conductive material.

41. The method of manufacturing a semiconductor device of Claim 40 further comprising, after the fifth step and before the sixth step, a step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode,

wherein, in the eighth step, the holes are formed so as to reach the source/drain region.

42. The method of manufacturing a semiconductor device of Claim 40,

wherein, in the eighth step, the holes are formed over the active area, the sidewall and the trench isolation.

43. The method of manufacturing a semiconductor device of Claim 40,

wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

44. The method of manufacturing a semiconductor device of Claim 43,

wherein the plug underlying film is made of a TiN/Ti film.

45. The method of manufacturing a semiconductor device of Claim 39 further comprising, after the fifth step, a sixth step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode;

after the sixth step, a seventh step of forming an insulating film on the entire top surface of the substrate,

an eighth step of removing the insulating film and forming holes so as to reach the source/drain region; and

a ninth step of forming an interconnection connected to the source/drain region through the holes on the insulating film.

46. A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;

a third step of forming a gate electrode on the gate insulating film;

after the third step, a fourth step of forming a laminated film made of a lower film and an upper film on the entire surface of the semiconductor substrate on which the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate is formed;

a fifth step of forming an interlayer insulating film on the upper film;

a sixth step of selectively removing the interlayer insulating film and the laminated film and forming holes; and

a seventh step of forming a buried conductive layer by filling the holes with a conductive material,

wherein the upper film is made of an insulating material having high etching selectivity against the interlayer insulating film in dry etching.

47. The method of manufacturing a semiconductor device of Claim 46,

wherein the upper film is made of a silicon nitride film.

48. The method of manufacturing a semiconductor device of Claim 46 further comprising, after the third step and before the fourth step, a step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode,

wherein in the sixth step, the holes are formed so as to reach the source/drain region.

49. The method of manufacturing a semiconductor device of Claim 46,

wherein in the sixth step, the holes are formed over the active area, the sidewall and the trench isolation.

50. The method of manufacturing a semiconductor device of Claim 46, wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

51. The method of manufacturing a semiconductor device of Claim 50, wherein the plug underlying film is made of a TiN/Ti film.

Docket No.: 60188-076 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Mizuki SEGAWA, et al. :

Serial No.: 09/902,157 : Group Art Unit: 2822

Filed: July 11, 2001 : Examiner: J. VOCKRODT

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

THE COMMISSIONER FOR PATENTS AND TRADEMARKS
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

☒ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	17	21	0	$18.00 =	$0.00
Independent Claims	3	3	0	$84.00 =	$0.00
		Multiple claims newly presented			$0.00
		Fee for extension of time			$0.00
					$0.00
				Total of Above Calculations	$0.00

☐ Please charge my Deposit Account No. 500417 in the amount of $0.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 MEF:men
Facsimile: (202) 756-8087
Date: January 15, 2003

Docket No.: 60188-076

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Mizuki SEGAWA, et al.	:	Confirmation Number: 8789
Serial No.: 09/902,157	:	Group Art Unit: 2822
Filed: July 11, 2001	:	Examiner: Jeff B. Vockrodt

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

AMENDMENT

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated June 27, 2003, having a three-month shortened statutory period for response set to expire on September 27, 2003, a petition for a one month extension of time up to and including October 27, 2004 being filed concurrently herewith, reconsideration of the above-identified application is respectfully requested in view of the following amendment and remarks.

AMENDMENT TO THE CLAIMS

1-30. (Canceled)

31. (Currently amended) A method of manufacturing a semiconductor device comprising:

a first step of forming an underlying insulating film on a semiconductor substrate;

a second step of depositing an etching stopper film on the underlying insulating film;

a third step of forming a trench by exposing a portion of the etching stopper film and the underlying insulating film where an isolation is to be formed and etching the semiconductor substrate in the exposed portion;

a fourth step of depositing an insulating film for isolation on an entire top surface of the substrate, flattening the substrate until at least a surface of the etching stopper film is exposed, and forming a trench isolation in the trench so as to surround a transistor region;

a fifth step of removing, by etching, at least the etching stopper film and the underlying insulating film, so as to expose a step portion between the transistor region and the trench isolation;

a sixth step of sequentially depositing a gate oxide film ~~and~~, a conductive film and a first protection insulating film on the substrate and forming a gate electrode and a gate insulating film by patterning ~~making~~ the conductive film and the first protection insulating film ~~into a pattern of at least a gate electrode~~;

after the sixth step, a seventh step of depositing a second protection insulating film on the entire top surface of the substrate;

after the ~~a~~ seventh step, an eighth step of depositing an insulating film for sidewalls made of a silicon film on the entire top surface of the substrate and anisotropically etching the insulating film for the sidewalls, so as to form electrode sidewalls and a step sidewall on side surfaces of the gate electrode and the step portion, respectively; ~~and~~

~~an eighth~~ a ninth step of introducing an impurity into the semiconductor substrate in the transistor region on both sides of the gate electrode, so as to form source/drain regions; and

after the ninth step, a tenth step of silicifying an area stretching over the electrode sidewall, the active area and the step sidewall.

D1

11. (Currently amended) The method of manufacturing a semiconductor device of claim 10, wherein, in the second step, a thickness of the etching stopper film is determined in consideration of an amount of over-etch in the ~~seventh~~ eighth step, so that the step portion having a level difference with a predetermined size or more is exposed in the fifth step.

33-38. (Canceled)

12. (Currently amended) A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;

a third step of forming a gate electrode on the gate insulating film;

after the third step, a fourth step of forming an insulating film on the substrate;

~~and~~

a fifth step of anisotropically etching the insulating film so as to form first sidewalls on both side surfaces of the gate electrode and form second sidewalls on a side surface of a step portion in the boundary between the trench isolation and the active area; and

after the fifth step, a sixth step of forming a laminated film made of a silicon oxide film and a silicon nitride film on the entire top surface of the substrate;

a seventh step of forming an interlayer insulating film on the silicon nitride film;

an eighth step of forming a hole by selectively removing the interlayer insulating film and the laminated film; and

a ninth step of forming a buried conductive layer by filling the hole with a conductive material.

40. (Canceled)

~~41~~ 13. (Currently amended) The method of manufacturing a semiconductor device of Claim ~~40~~ ~~39~~ 12 further comprising, after the fifth step and before the sixth step, a step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode,

wherein, in the eighth step, the hole ~~holes~~ are formed so as to reach the source/drain region.

14
~~42~~. (Currently amended) The method of manufacturing a semiconductor device of Claim ~~40~~ 12, wherein, in the eighth step, the hole ~~holes~~ are formed over the active area, the sidewall and the trench isolation.

15
~~43~~. (Currently amended) The method of manufacturing a semiconductor device of Claim ~~40~~ 12, wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

16
~~44~~. (Previously presented) The method of manufacturing a semiconductor device of Claim ~~43~~ 15, wherein the plug underlying film is made of a TiN/Ti film.

45. (Canceled)

17
~~46~~. (Currently amended) A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on the semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;

a third step of forming a gate electrode on the gate insulating film;

after the third step, a fourth step of forming a laminated film made of a lower film and an upper film on the entire surface of the semiconductor substrate on which the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate is formed;

a fifth step of forming an interlayer insulating film on the upper film;

a sixth step of selectively removing the interlayer insulating film and the laminated film and forming a hole; and

a seventh step of forming a buried conductive layer by filling the hole ~~holes~~ with a conductive material,

wherein the upper film is made of an insulating material having high etching selectivity against the interlayer insulating film in dry etching.

P'

18

47. (Previously presented) The method of manufacturing a semiconductor device of Claim 46, wherein the upper film is made of a silicon nitride film.

19

48. (Currently amended) The method of manufacturing a semiconductor device of Claim 46 further comprising, after the third step and before the fourth step, a step of forming a source/drain region in the semiconductor substrate in the active area on both sides of the gate electrode,

wherein in the sixth step, the hole ~~holes~~ are formed so as to reach the source/drain region.

~~49~~ 20. (Currently amended) The method of manufacturing a semiconductor device of Claim ~~46~~ 17, wherein in the sixth step, the hole ~~holes~~ are formed over the active area, the sidewall and the trench isolation.

~~50~~ 21. (Previously presented) The method of manufacturing a semiconductor device of Claim ~~46~~ 17, wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

~~51~~ 22. (Previously presented) The method of manufacturing a semiconductor device of Claim ~~50~~ 21, wherein the plug underlying film is made of a TiN/Ti film.

P'

~~52~~ 1. (Currently amended) A method of manufacturing a semiconductor device comprising:

a first step of forming a trench isolation on ~~the~~ a semiconductor substrate, the trench isolation having a top surface at a higher level than a surface of the semiconductor substrate;

a second step of forming a gate insulating film on an active area surrounded by the trench isolation on the semiconductor substrate;

a third step of forming a gate electrode on the gate insulating film and forming an interconnection on the trench isolation;

after the third step, a fourth step of forming an underlying film on the entire surface of the semiconductor substrate;

a fifth step of forming an interlayer insulating film on the underlying film;

a sixth step of forming a hole stretching over at least a part of the active area, at least a part of the interconnection and at least a part of the trench isolation provided therebetween by selectively removing the interlayer insulating film and the underlying film ~~and forming holes~~; and

a seventh step of forming a buried conductive layer by filling the hole ~~holes~~ with a conductive material,

wherein the underlying film is made of an insulating material having high etching selectivity against the interlayer insulating film in a dry etching process.

~~53~~ 2. (Previously presented) The method of manufacturing a semiconductor device of Claim ~~52~~ 1, wherein the underlying film has a silicon nitride film.

~~54~~ 3. (Currently amended) The method of manufacturing a semiconductor device of Claim ~~52~~ 1 further comprising, after the third step and before the fourth step, a step of forming a source/drain region in the active area on both sides of the gate electrode,

wherein in the sixth step, the hole ~~holes~~ are formed so as to reach the source/drain region.

55. (Canceled)

~~56~~ 4. (Previously presented) The method of manufacturing a semiconductor device of Claim ~~52~~ 1, wherein the buried conductive layer is composed of a plug underlying film and a tungsten plug.

57. (Previously presented) The method of manufacturing a semiconductor device of Claim 56, wherein the plug underlying film is made of a TiN/Ti film.

58. (Currently amended) The method of manufacturing a semiconductor device of Claim 56, wherein in the sixth step, the trench isolation is not etched lower than the surface of the active area when forming of the hole ~~holes~~.

59. (Previously presented) The method of manufacturing a semiconductor device of Claim 52 further comprising, after the third step and before the fourth step, a step of forming a source/drain region in the active area on both sides of the gate electrode, and a step of forming a silicide layer on the source/drain region.

60. (Previously presented) The method of manufacturing a semiconductor device of Claim 59 further comprising, after the third step, a step of forming sidewalls on both sides of the gate electrode before forming the source/drain region.

61. (New) The method of manufacturing a semiconductor device of Claim 52, wherein the sixth step is performed so that the hole stretch over the entire part of the trench isolation provided between the active area and the interconnection.

REMARKS

The indication of allowable subject matter in claims 34, 40-44 and 46-51 is acknowledged and appreciated. In order to expedite prosecution, independent claims 31 and 39 have been amended to include what is believed to be the allowable subject matter of claims 34 and 40, respectively, thereby obviating the pending rejections against claims 31 and 39, and their dependent claims.

Claims 52-55 and 58-60 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hirobumi in view of Barber, and claims 56-57 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hirobumi in view of Barber and Dixit. Claim 52 is independent. These rejections are respectfully traversed for the following reasons.

Claim 52 recites in pertinent part, "a third step of forming a gate electrode on the gate insulating film ***and forming an interconnection on the trench isolation***; ... a sixth step of forming holes stretching over at least a part of the active area, at least a part of the interconnection and at least a part of the trench isolation provided therebetween ... " (emphasis added). Support for these features can be found, for example, in Figures 10a-10c of Applicants' drawings and page 49, lines 8-16 of Applicants' specification.

Hirobumi does not disclose or suggest forming an interconnection on the alleged trench isolation 25, and the contact holes are formed over only the alleged active regions 32,33. Barber does not disclose or suggest forming holes over any part of the trench isolation 14 located between the alleged active area 12 and the polysilicon line 16. Accordingly, neither Hirobumi nor Barber, alone or in combination, disclose or suggest the novel combination of features recited in claim 52. Further, neither Hirobumi nor Barber

disclose or suggest the ***combination*** of a gate electrode on an active area and an interconnection on a trench isolation, nor provide any motivation or rationale for doing so.

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 52 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 52 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on all the foregoing, it is submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102 and 103 be withdrawn.

CONCLUSION

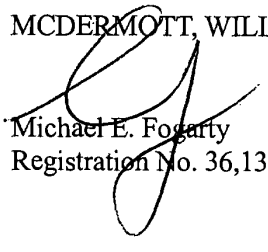
Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully

solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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Facsimile: (202) 756-8087
Date: October 24, 2003

Notice of Allowability	Application No.	Applicant(s)	
	09/902,157	SEGAWA ET AL.	
	Examiner	Art Unit	
	Jeff Vockrodt	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 10-24-03*.
2. ☒ The allowed claim(s) is/are *31-32, 39, 41-44, 46-54, 56-61*.
3. ☒ The drawings filed on *11 July 2001* are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *08/685,726*.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☐ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☐ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (PTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____.
5☐ Information Disclosure Statements (PTO-1449), Paper No. ____.
6☒ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other

ABAIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

16/E

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In claim 58, replace "55" with --52--.

The following is an examiner's statement of reasons for allowance: Claim 58 has been changed to depend from claim 52 instead of cancelled claim 55. The examiner's statement of reasons for allowance mailed on May 22, 2003 is incorporated by reference. With regard to claims 52-54 and 56-61, the examiner agrees with applicant's remarks submitted October 24, 2003 as to why those claims are allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The official fax number for this group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

November 6, 2003
J. Vockrodt

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

US006538324B1

(12) **United States Patent**
Tagami et al.

(10) **Patent No.: US 6,538,324 B1**
(45) **Date of Patent: Mar. 25, 2003**

(54) **MULTI-LAYERED WIRING LAYER AND METHOD OF FABRICATING THE SAME**

(75) Inventors: **Masayoshi Tagami**, Tokyo (JP); **Yoshihiro Hayashi**, Tokyo (JP)

(73) Assignee: **NEC Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/596,415**

(22) Filed: **Jun. 19, 2000**

(30) **Foreign Application Priority Data**

Jun. 24, 1999 (JP) 11-214110

(51) **Int. Cl.**[7] **H01L 23/48**; H01L 23/52
(52) **U.S. Cl.** **257/751**; 257/762
(58) **Field of Search** 257/751, 752, 257/753, 758, 762, 773; 438/626, 627, 628, 643, 644, 645

(56) **References Cited**

U.S. PATENT DOCUMENTS

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JP	9-293690	* 11/1997
JP	10-256256	9/1998

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M. T. Wang, et al., "Barrier Properties of Very Thin Ta and TaN Layers Against Copper Diffusion", Journal Electrochemical Society, Jul. 1998, pp. 2538–2545.

D. Denning, et al., An Inlaid CVD Cu Based Integration for Sub 0.25μm Technology, 1998 Symposium on VLSI Technology Digest of Technical Papers, 1998, pp. 22–23.

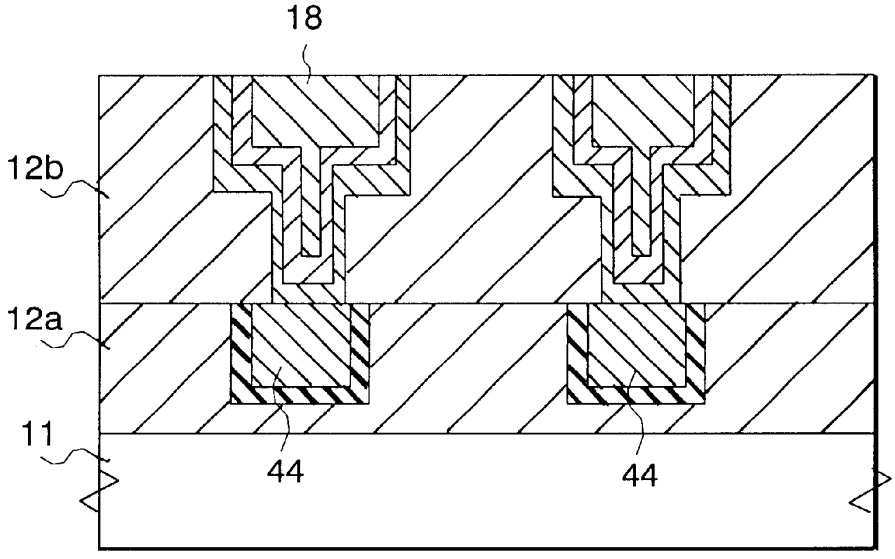
* cited by examiner

Primary Examiner—Tom Thomas
Assistant Examiner—Hung Kim Vu
(74) *Attorney, Agent, or Firm*—Scully, Scott, Murphy & Presser

(57) **ABSTRACT**

There is provided a barrier film preventing diffusion of copper from a copper wiring layer formed on a semiconductor substrate. The barrier film has a multi-layered structure of first and second films wherein the first film is composed of crystalline metal containing nitrogen therein, and the second film is composed of amorphous metal nitride. The barrier film is constituted of common metal atomic species. The barrier film prevents copper diffusion from a copper wiring layer into a semiconductor device, and has sufficient adhesion characteristic to both a copper film and an interlayer insulating film.

10 Claims, 20 Drawing Sheets



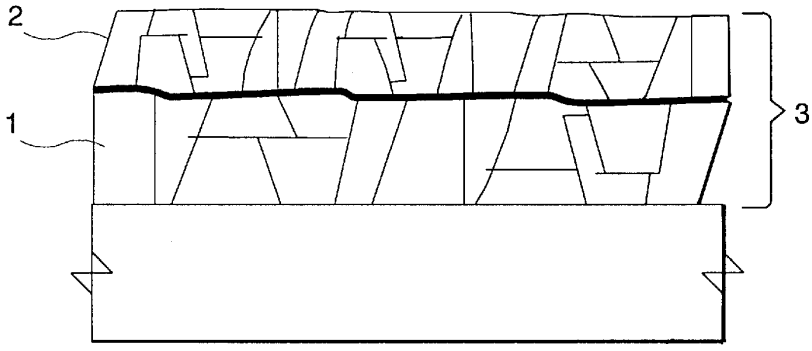


FIG. 1
(Prior Art)

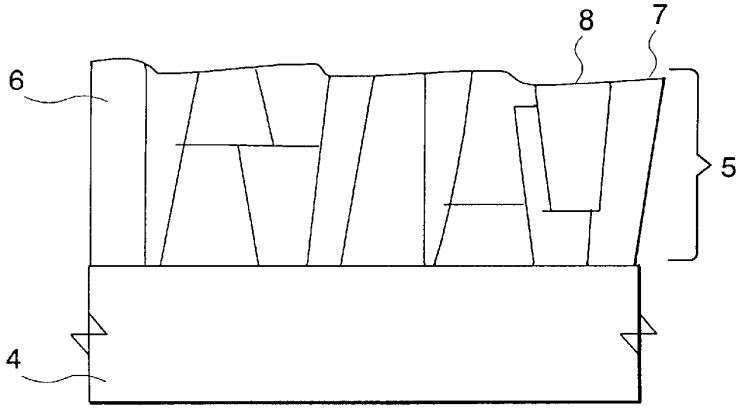


FIG. 2
(Prior Art)

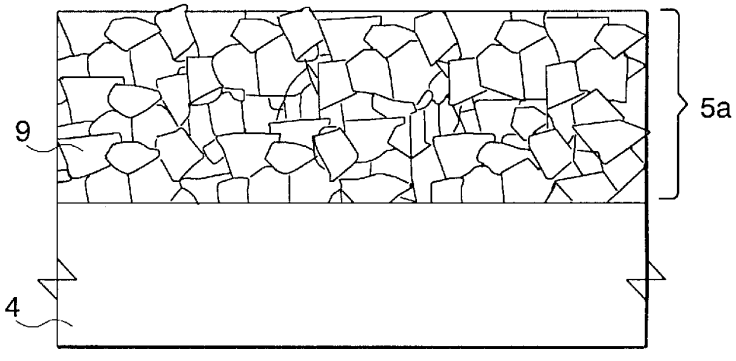


FIG. 3
(Prior Art)

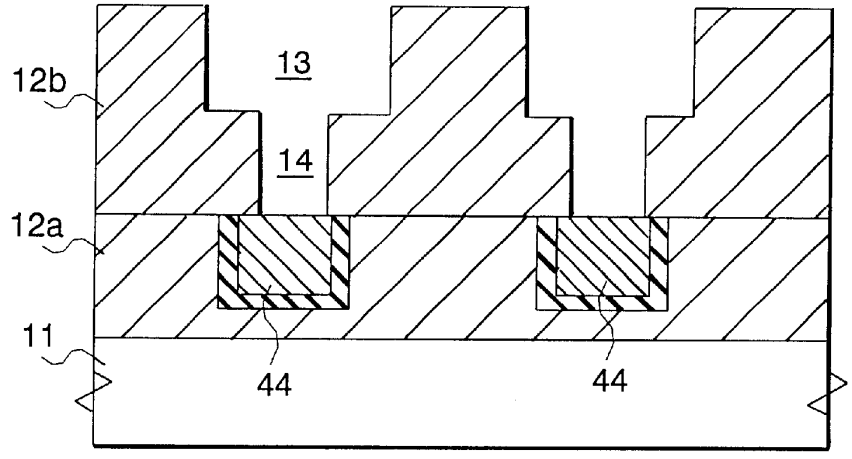


FIG. 4A

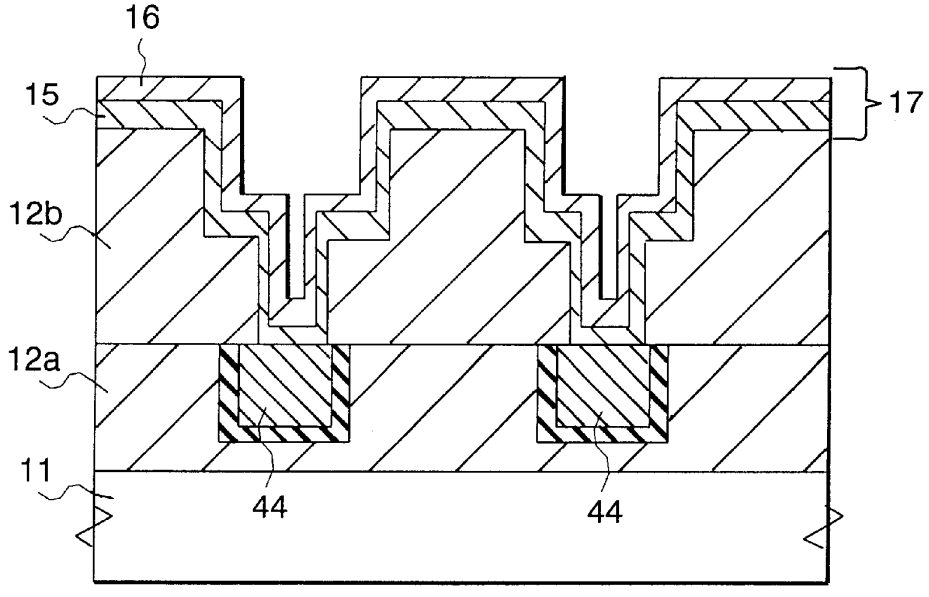


FIG. 4B

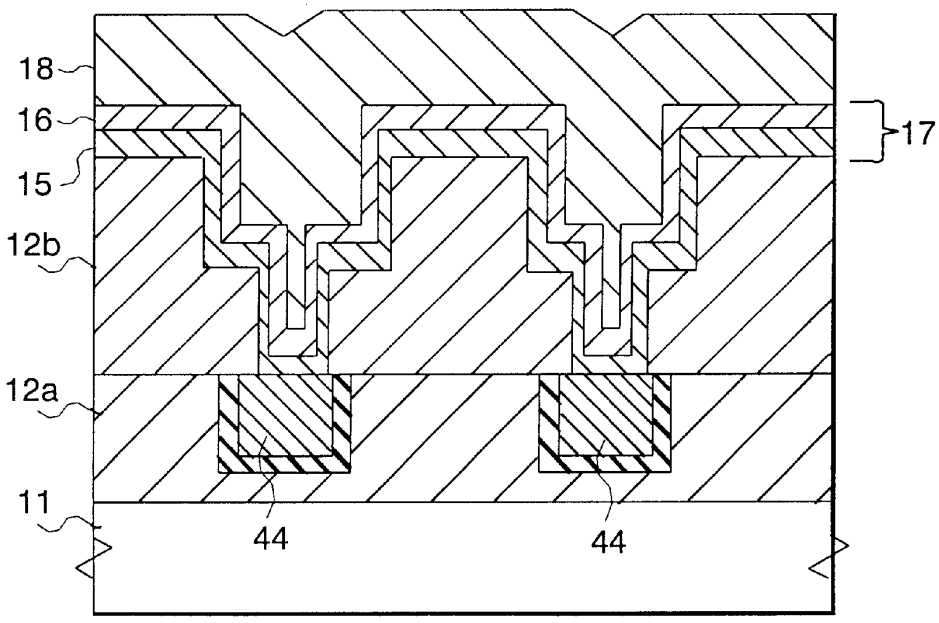


FIG. 4C

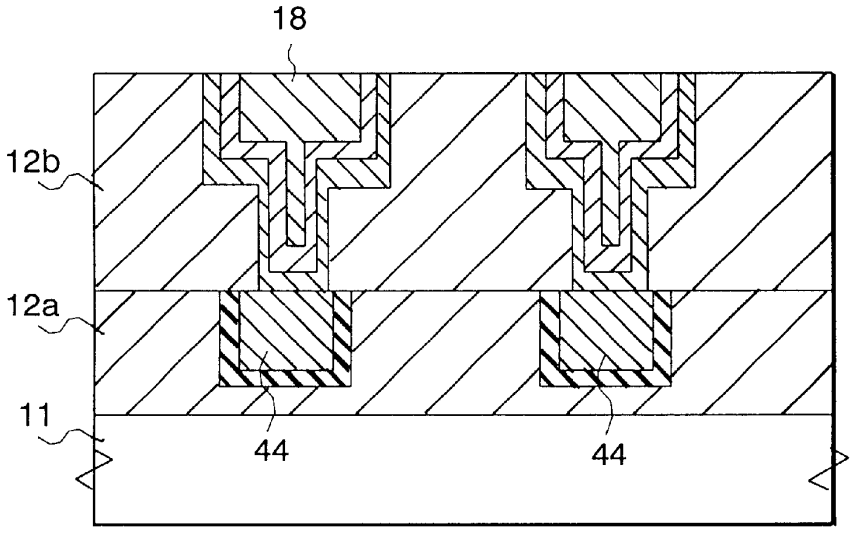


FIG. 4D

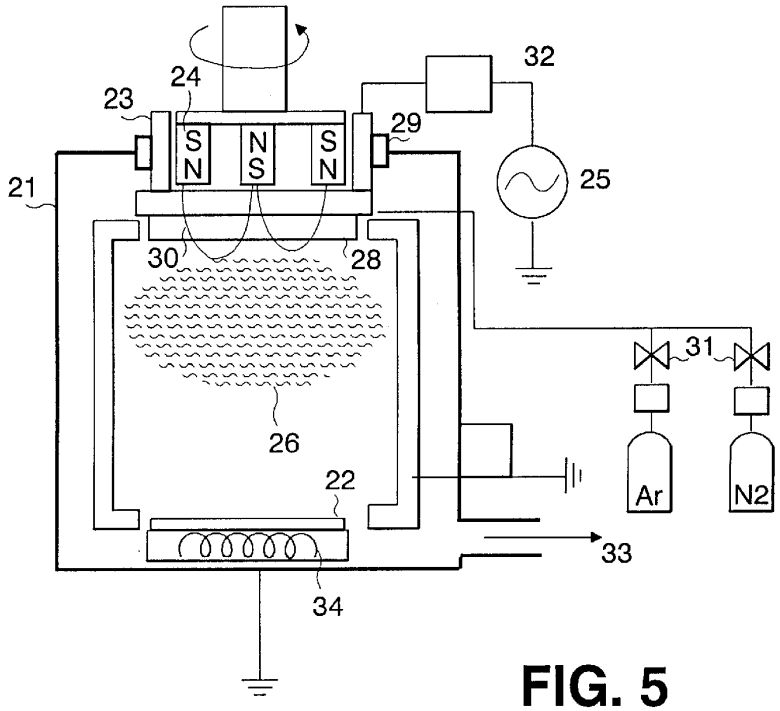

32
24
23
29
S
N
N
S
S
N
25
21
30
28
31
26
22
Ar
N2
33
34

FIG. 5

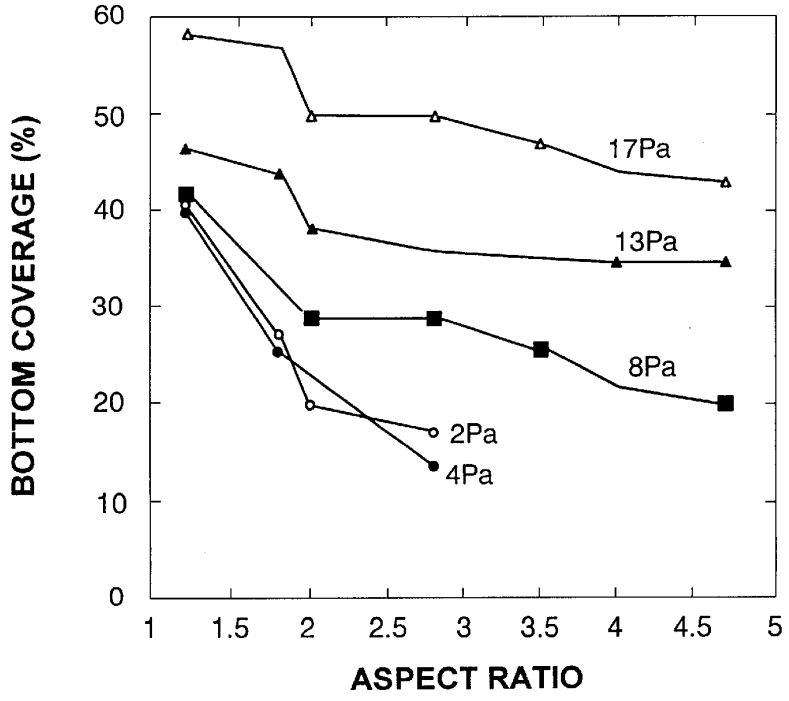

BOTTOM COVERAGE (%)
60
50
40
30
20
10
0
1
1.5
2
2.5
3
3.5
4
4.5
5
ASPECT RATIO
17Pa
13Pa
8Pa
2Pa
4Pa

FIG. 6

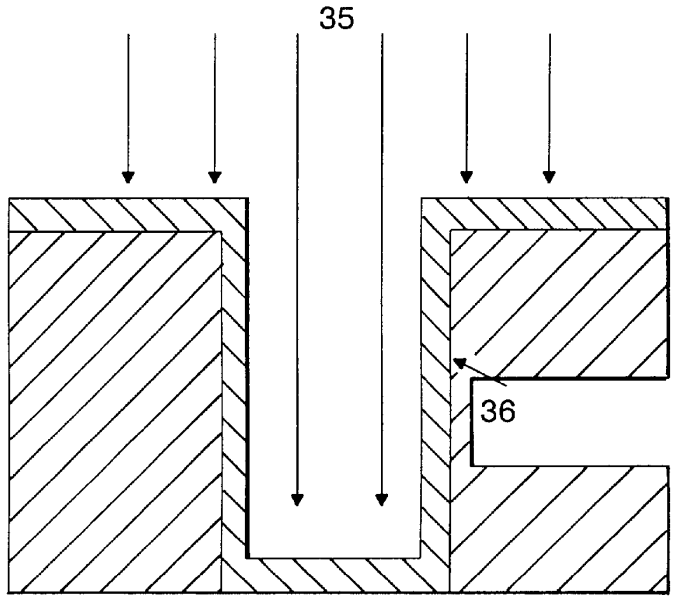


FIG. 7

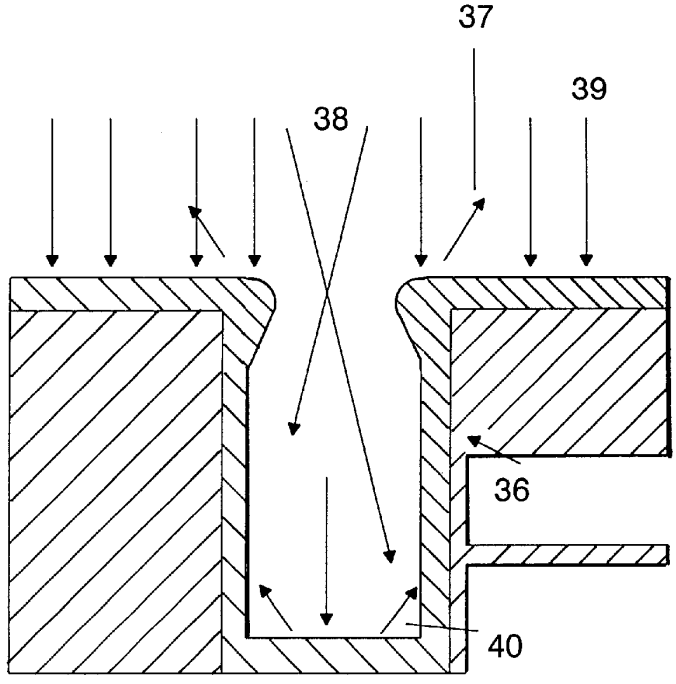


FIG. 8

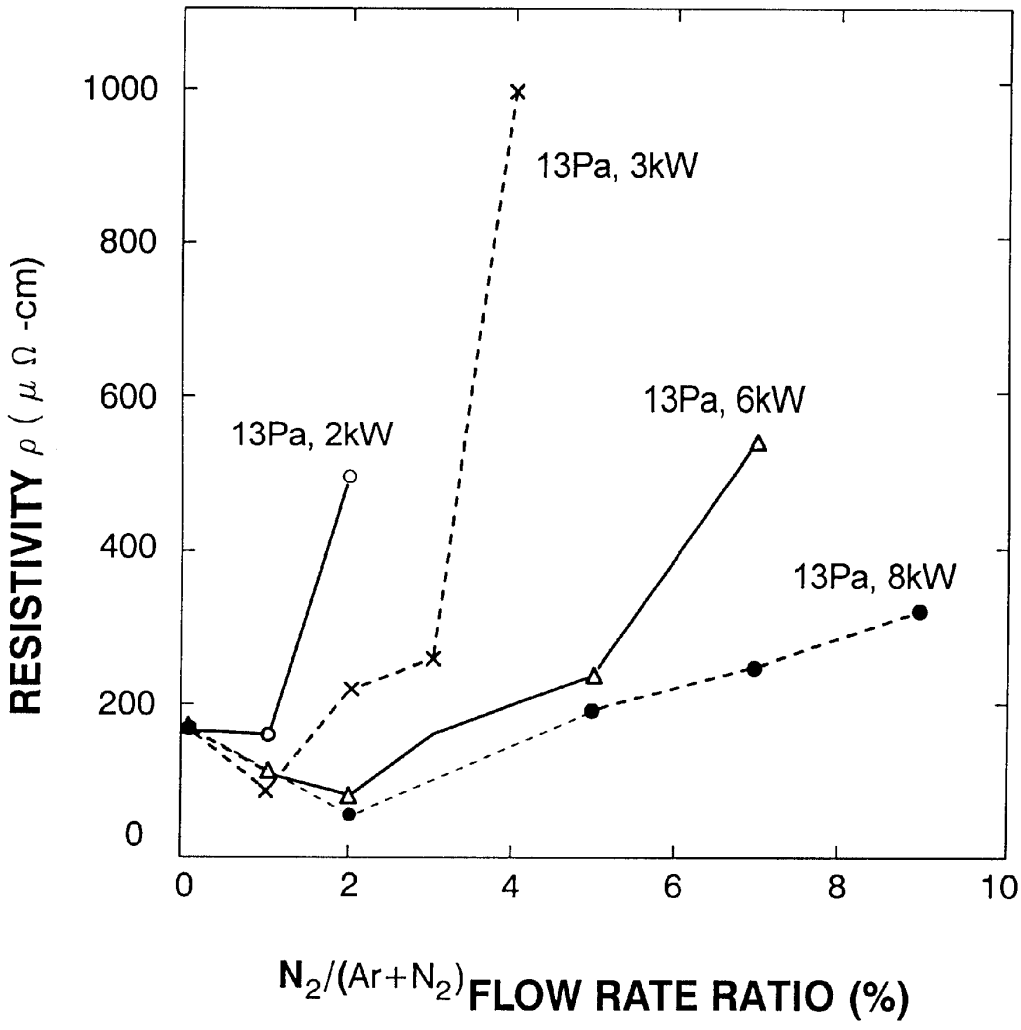

1000
800
600
400
200
0
RESISTIVITY ρ (μ Ω -cm)
13Pa, 3kW
13Pa, 2kW
13Pa, 6kW
13Pa, 8kW
0
2
4
6
8
10
N2/(Ar+N2) FLOW RATE RATIO (%)

FIG. 9

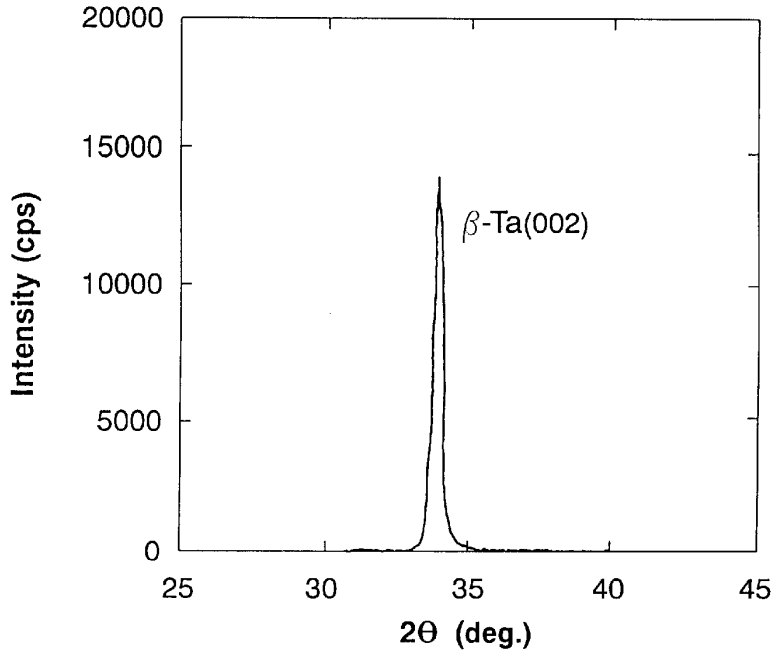

20000
15000
10000
5000
0
Intensity (cps)
β-Ta(002)
25
30
35
40
45
2θ (deg.)

FIG. 10

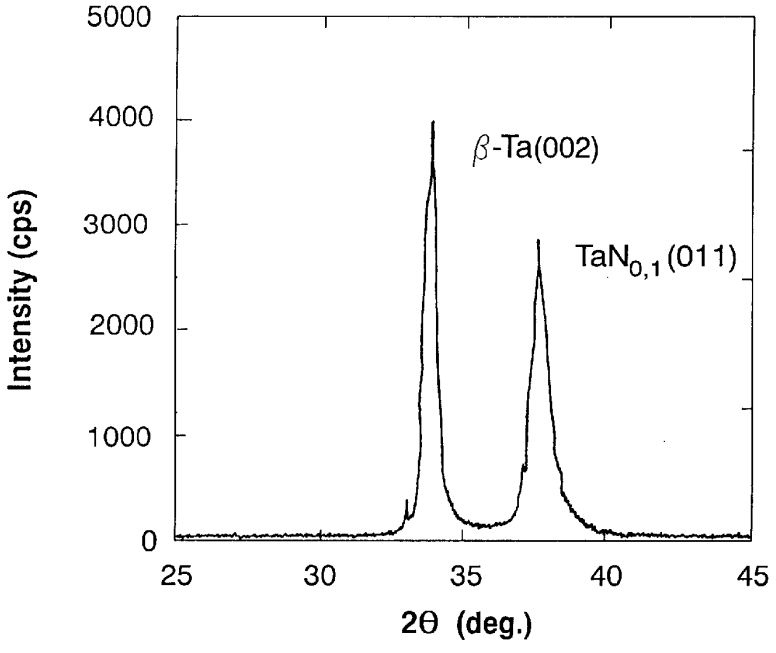

5000
4000
3000
2000
1000
0
Intensity (cps)
β-Ta(002)
TaN0,1 (011)
25
30
35
40
45
2θ (deg.)

FIG. 11

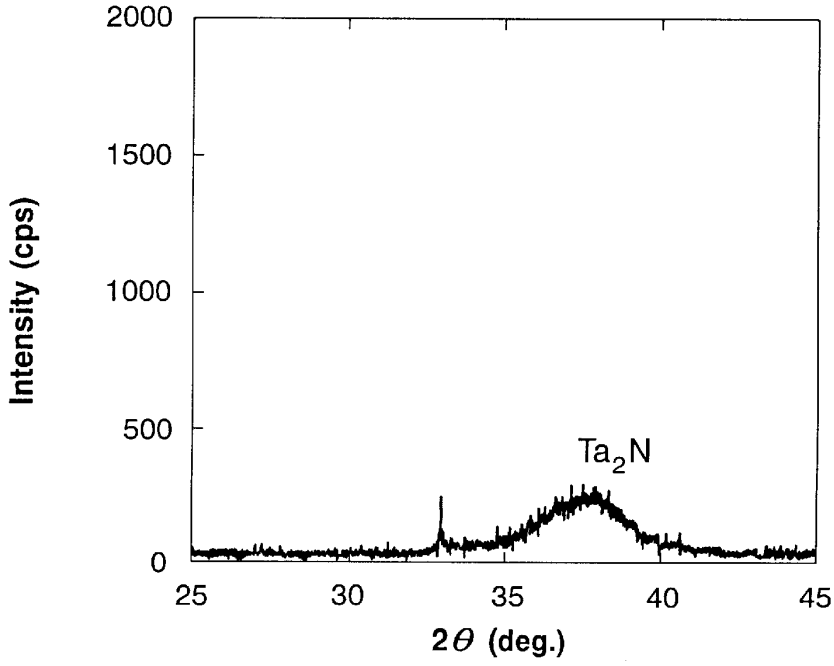

2000
1500
1000
500
0
Intensity (cps)
Ta_2N
25
30
35
40
45
2θ (deg.)

FIG. 12

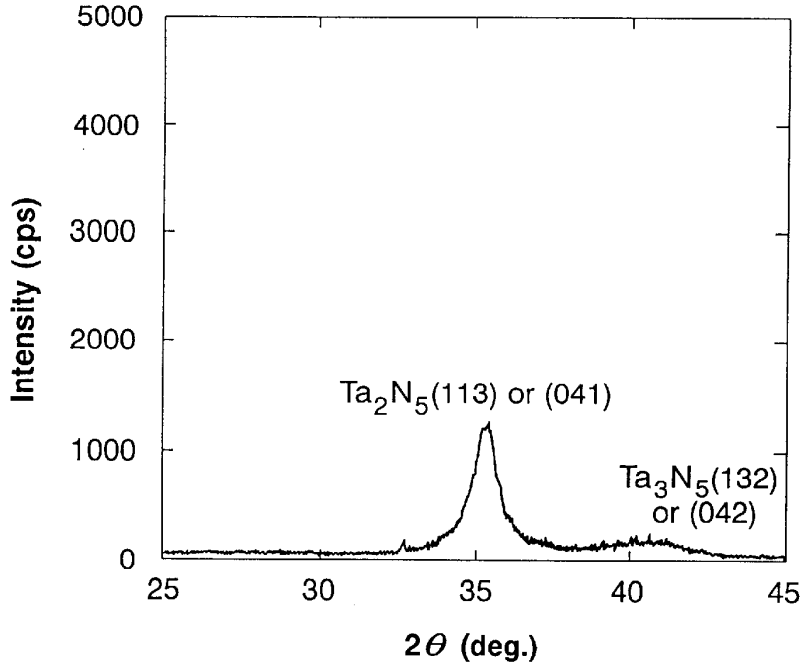

5000
4000
3000
2000
1000
0
Intensity (cps)
Ta_2N_5(113) or (041)
Ta_3N_5(132) or (042)
25
30
35
40
45
2θ (deg.)

FIG. 13

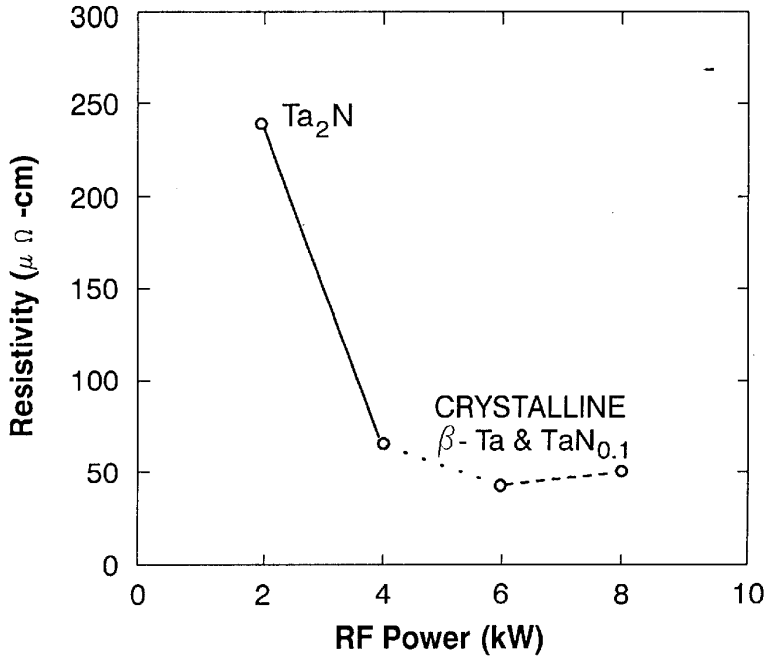

300
250
200
150
100
50
0
Resistivity (μ Ω -cm)
Ta2N
CRYSTALLINE
β- Ta & TaN0.1
0
2
4
6
8
10
RF Power (kW)

FIG. 14

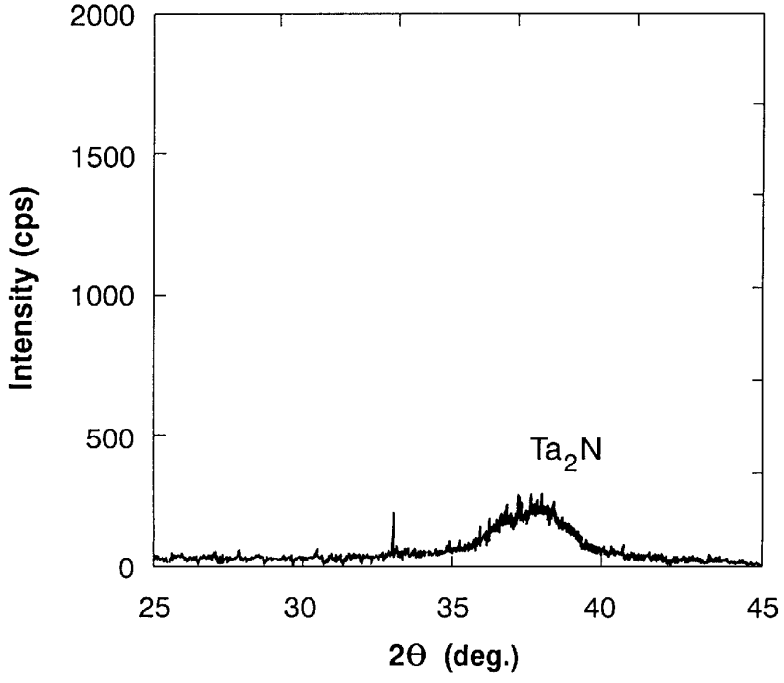

2000
1500
1000
500
0
Intensity (cps)
Ta2N
25
30
35
40
45
2θ (deg.)

FIG. 15

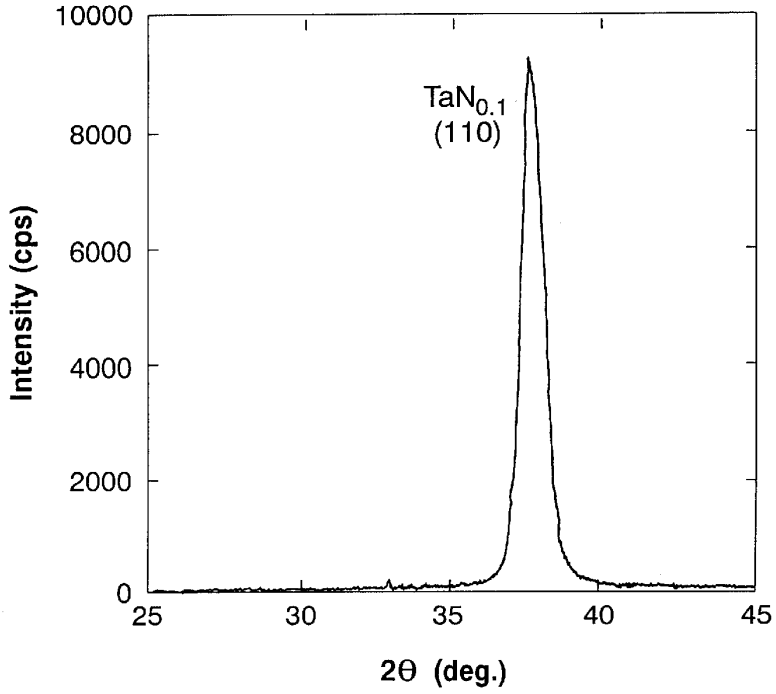

10000
8000
6000
4000
2000
0
Intensity (cps)
$TaN_{0.1}$
(110)
25
30
35
40
45
2θ (deg.)

FIG. 16

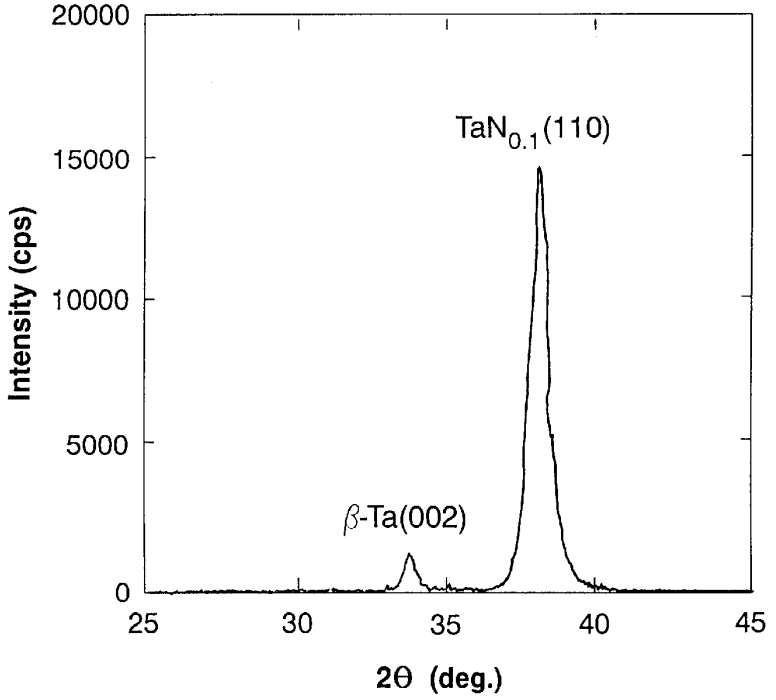

20000
15000
10000
5000
0
Intensity (cps)
$TaN_{0.1}$(110)
β-Ta(002)
25
30
35
40
45
2θ (deg.)

FIG. 17

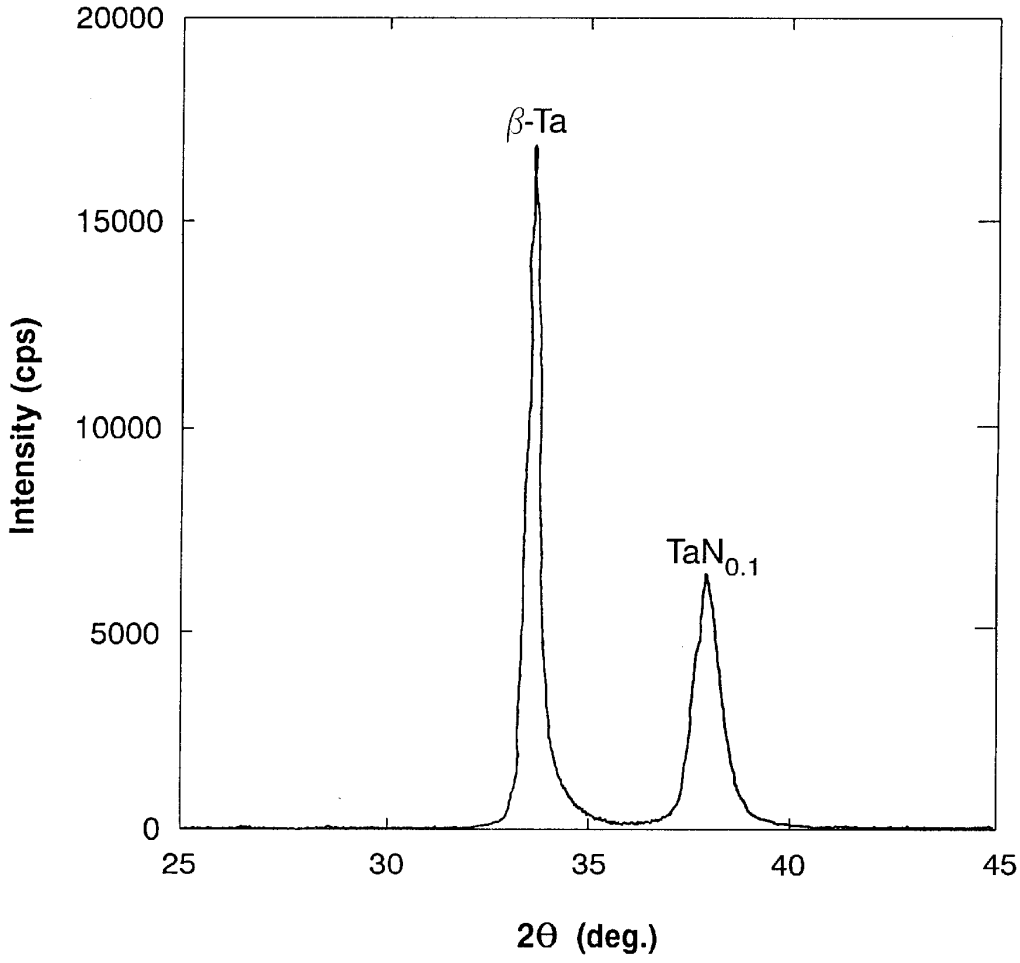

20000
15000
10000
5000
0
Intensity (cps)
β-Ta
TaN0.1
25
30
35
40
45
2θ (deg.)

FIG. 18

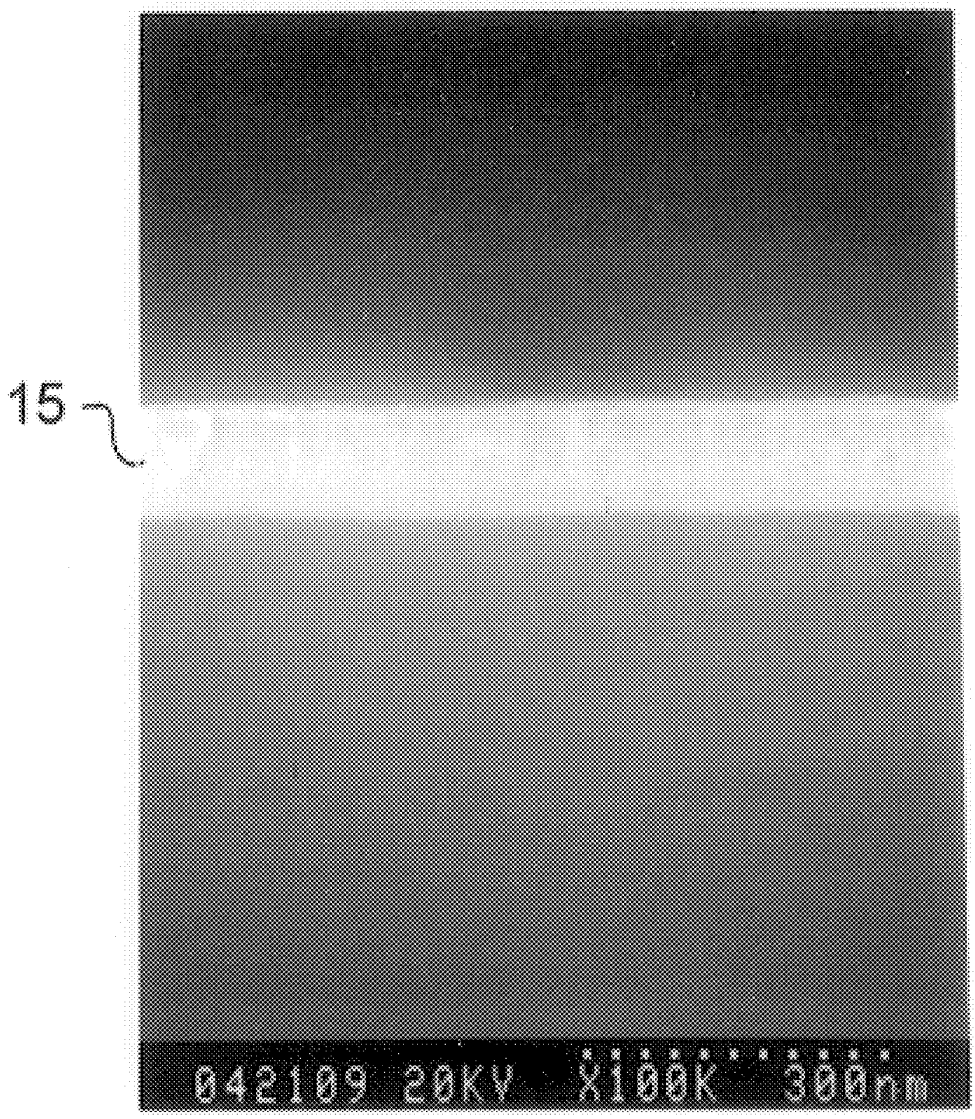


FIG. 19

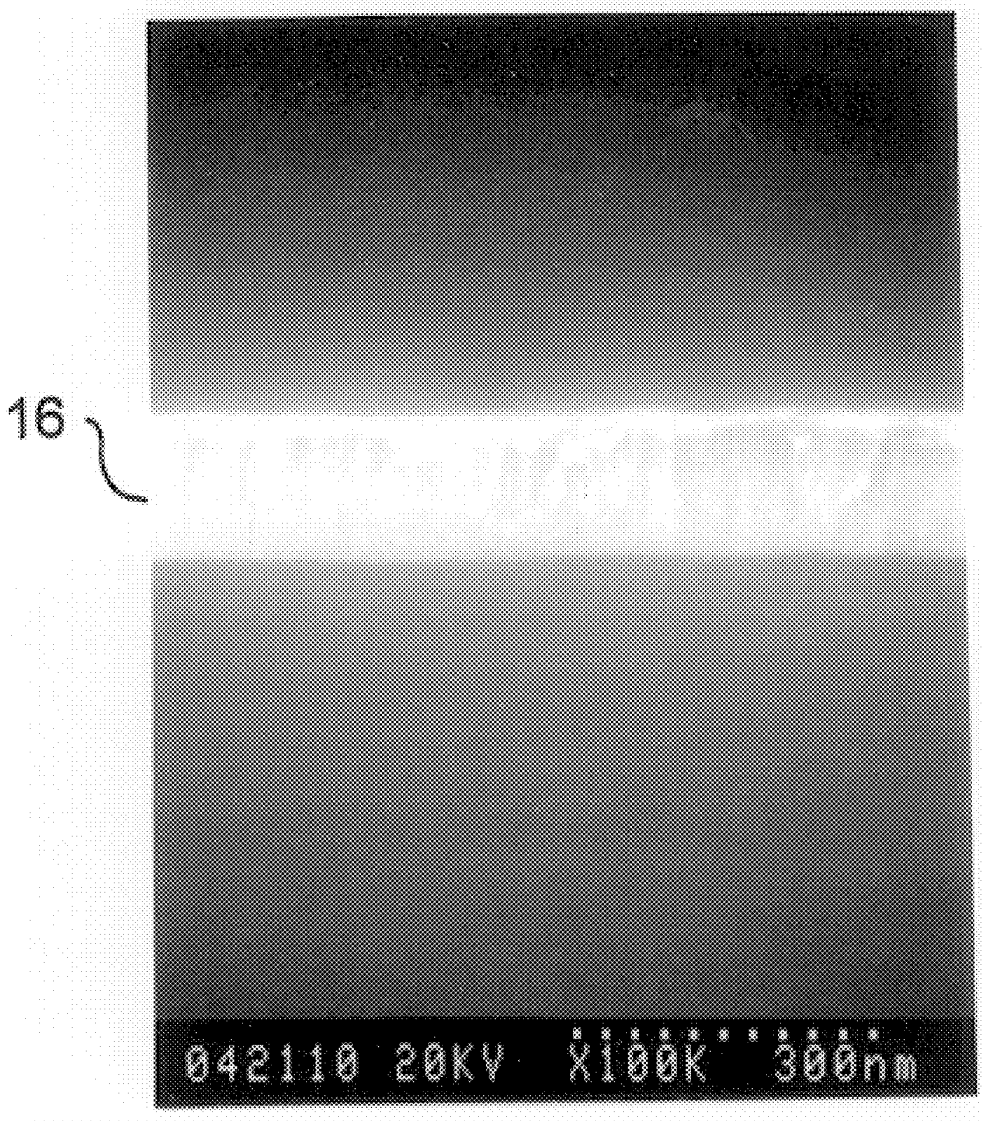


FIG. 20

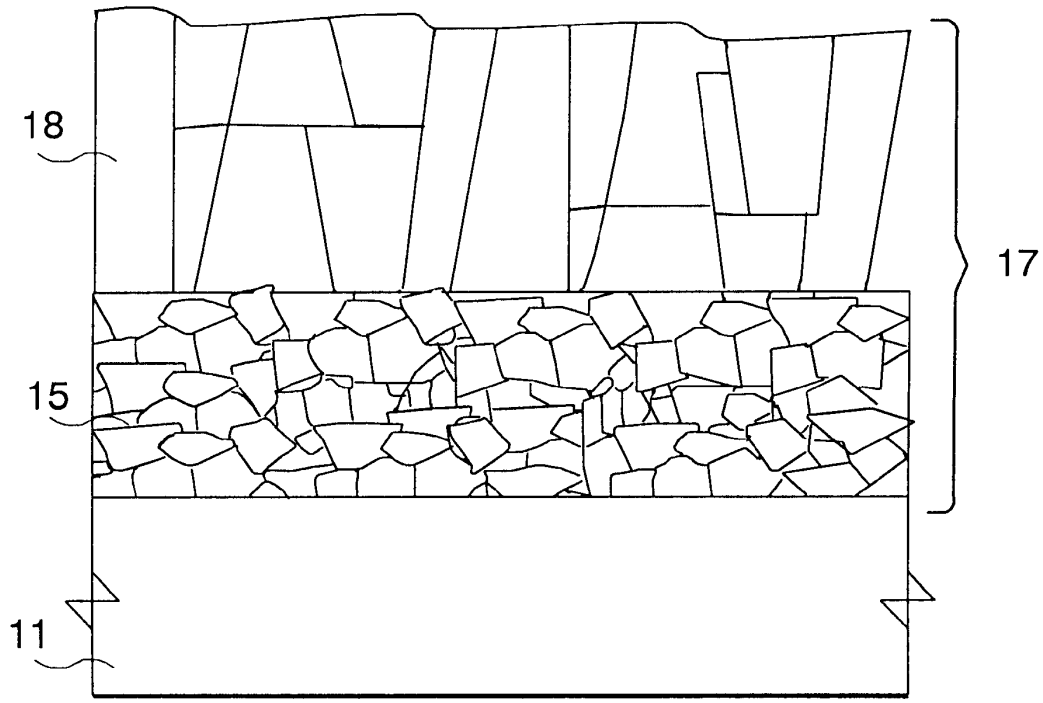


FIG. 21

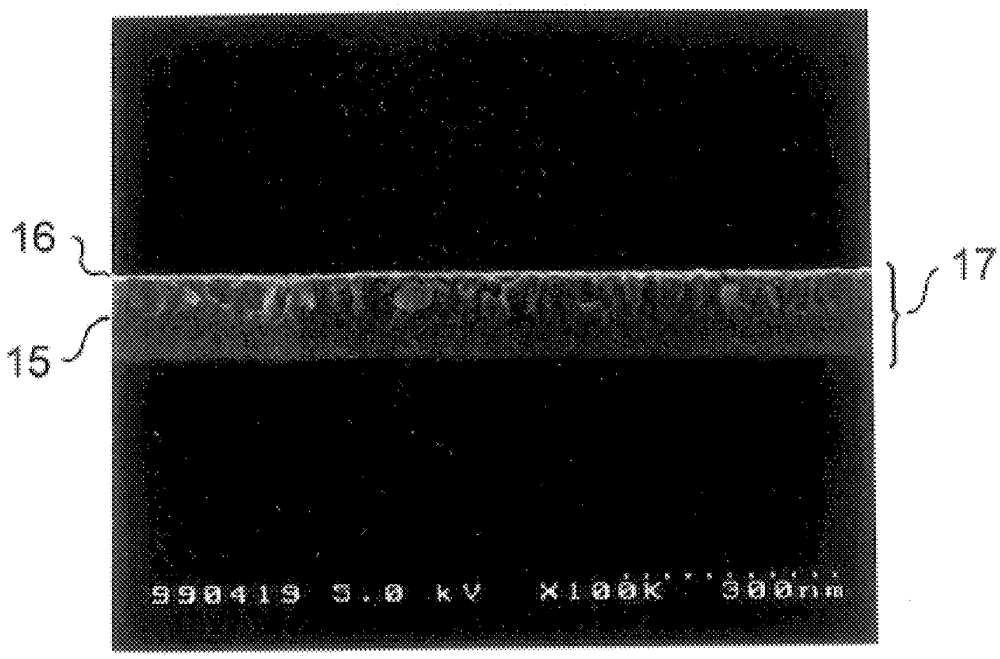


FIG. 22

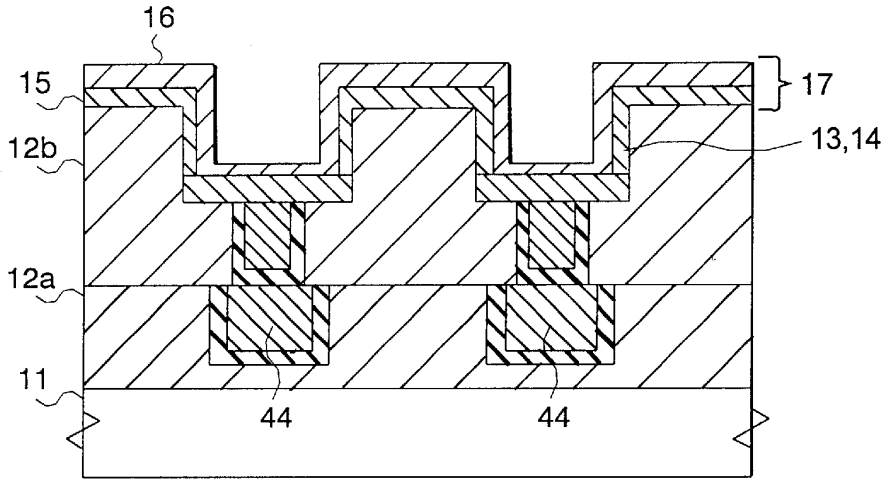

16
15
17
12b
13,14
12a
11
44
44

FIG. 23

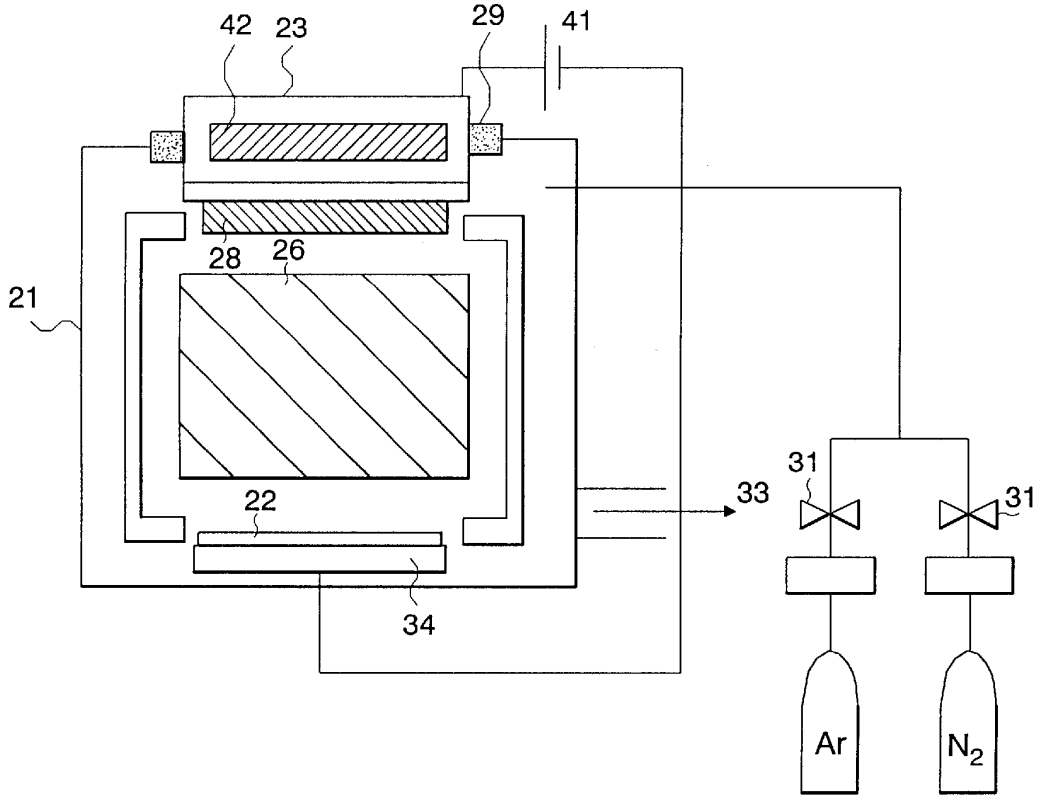

42
23
29
41
28
26
21
22
34
33
31
31
Ar
N_2

FIG. 24

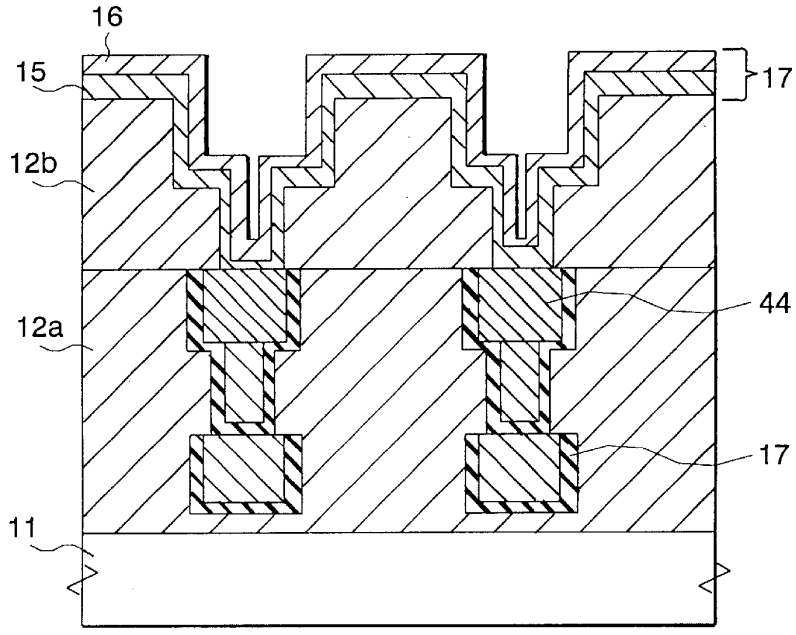


FIG. 25

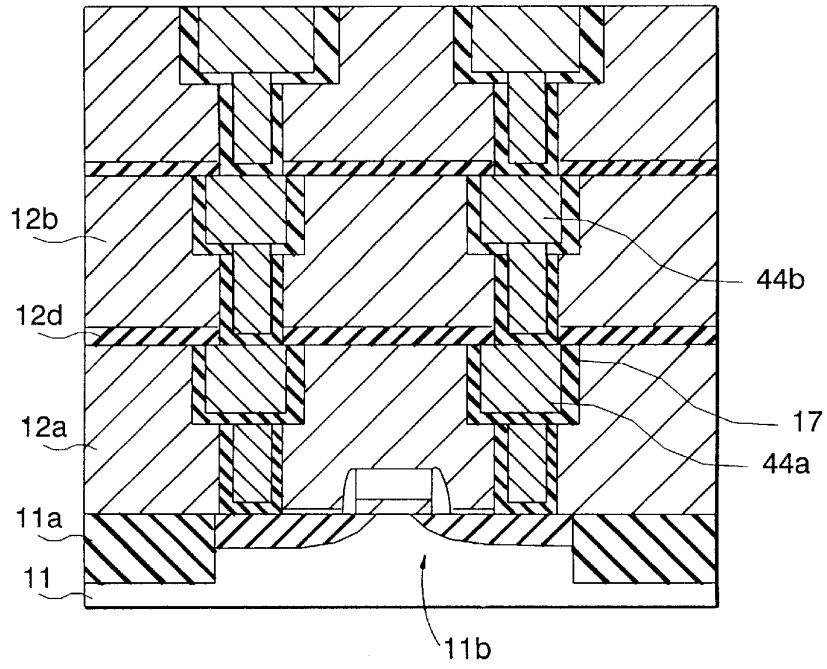


FIG. 26

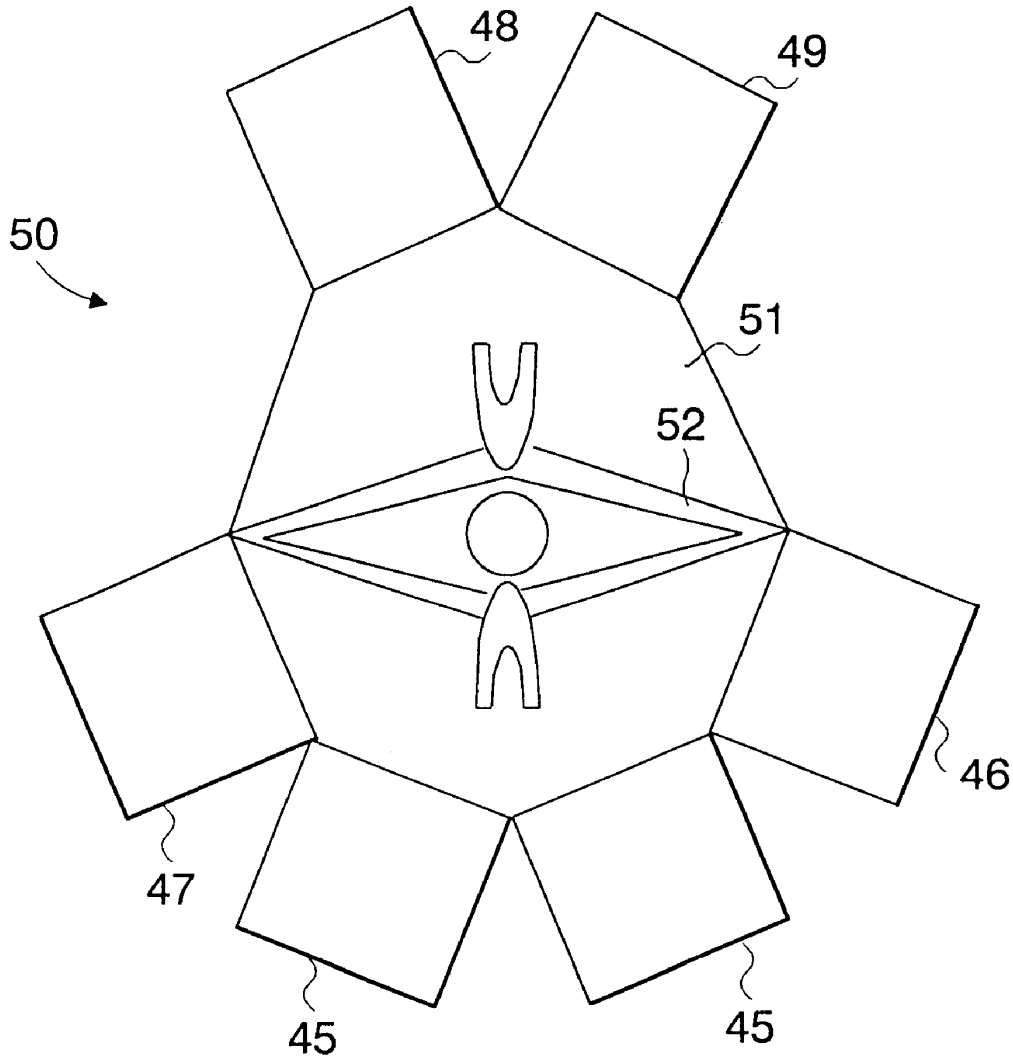


FIG. 27

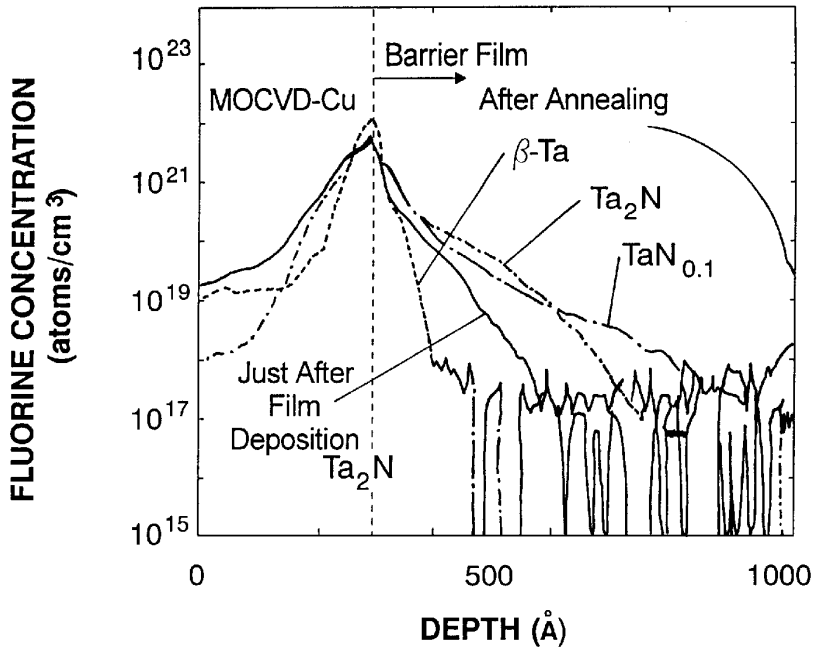

FLUORINE CONCENTRATION (atoms/cm 3)
10^{23}
10^{21}
10^{19}
10^{17}
10^{15}
Barrier Film
MOCVD-Cu
After Annealing
β-Ta
Ta_2N
$TaN_{0.1}$
Just After Film Deposition Ta_2N
0
500
1000
DEPTH (Å)

FIG. 28

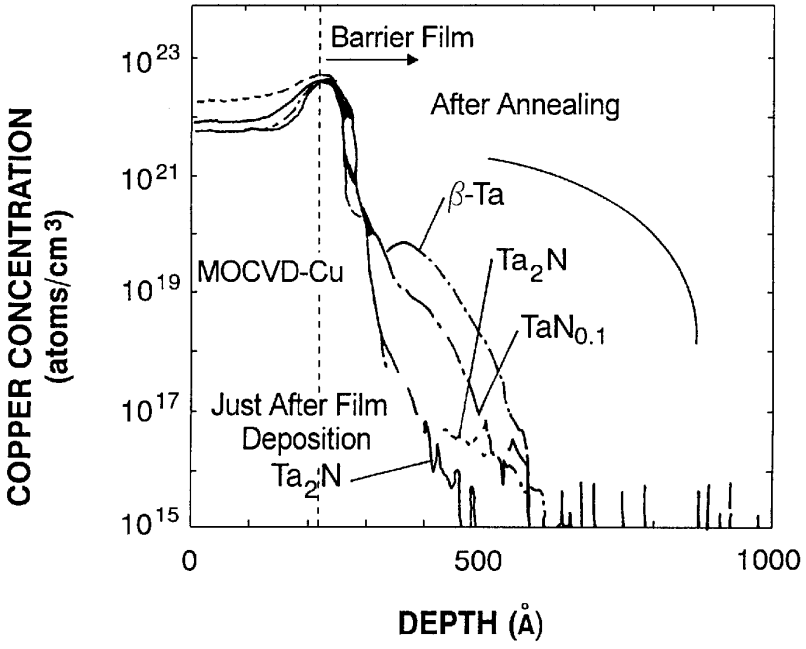

COPPER CONCENTRATION (atoms/cm 3)
10^{23}
10^{21}
10^{19}
10^{17}
10^{15}
Barrier Film
After Annealing
β-Ta
Ta_2N
$TaN_{0.1}$
MOCVD-Cu
Just After Film Deposition Ta_2N
0
500
1000
DEPTH (Å)

FIG. 29

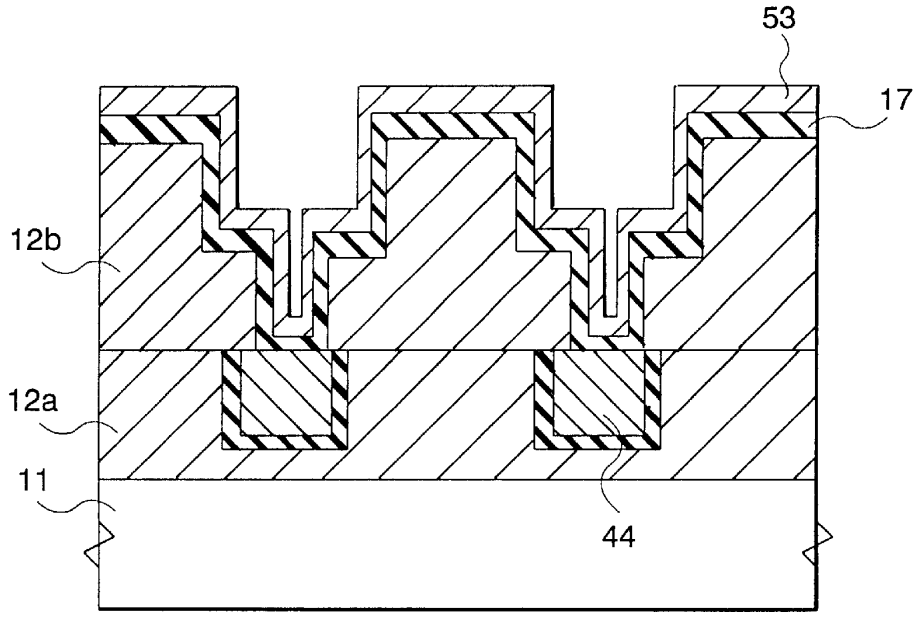


FIG. 30

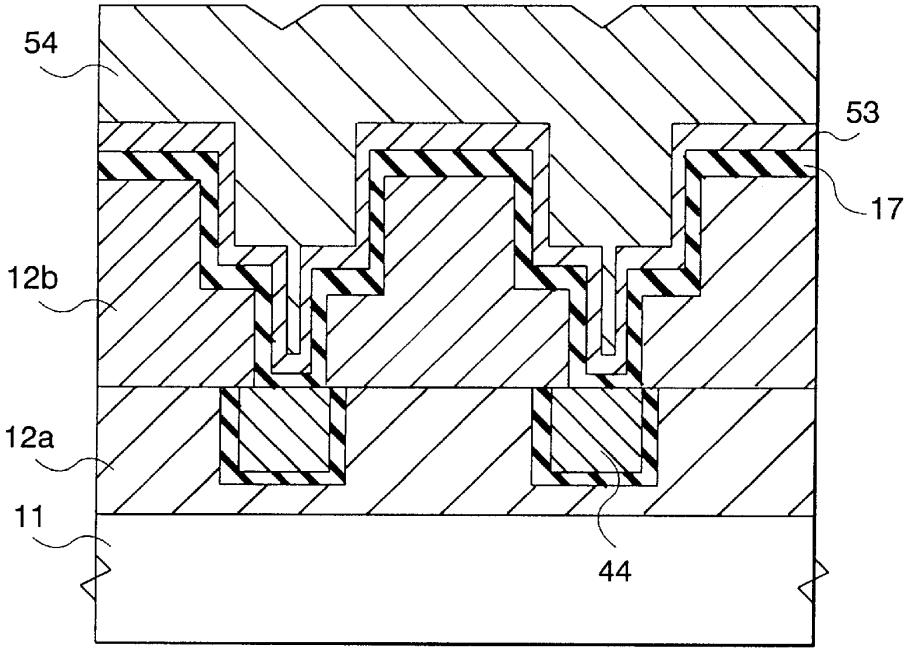


FIG. 31

MULTI-LAYERED WIRING LAYER AND METHOD OF FABRICATING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a semiconductor integrated circuit including a copper wiring layer, and more particularly to a barrier film which prevents copper diffusion from such a copper wiring layer.

2. Description of the Related Art

As a semiconductor device has been designed to be smaller and smaller in size, wiring delay exerts greater influence on a silicon ULSI device. As a result, though a wiring layer has been composed of aluminum, it is necessary to compose a wiring layer of copper in place of aluminum.

Resistivity of copper is equal to about 70% of resistivity of aluminum. However, since copper does not form passive state composed of an oxide film, at a surface thereof, unlike aluminum, copper is more corrosive than aluminum.

In addition, since copper has a high diffusion rate in both silicon (Si) and silicon dioxide (SiO_2), if copper enters MOSFET formed on a silicon substrate, copper would induce reduction in carrier lifetime.

Hence, it is absolutely necessary for a semiconductor device having a copper wiring layer to have a diffusion-barrier film for preventing diffusion of copper into an interlayer insulating film formed between copper wiring layers. In addition, since such a diffusion-barrier film has to have high adhesion characteristic to both an interlayer insulating film and a copper wiring layer in order to keep reliability in wiring.

Thus, there have been made many suggestions about a structure of a barrier metal layer and a method of fabricating the same, in order to prevent copper diffusion form a copper wiring layer.

For instance, a structure of a barrier metal layer is suggested in the following articles:

(a) Semiconductor World, Nobuyoshi Awaya, February 1998, pp. 91–96 (hereinafter, referred to as Prior Art 1);

(b) Advanced Metallization and Interconnect Systems for ULSI Applications in 1997, Kee-Won Kwon et al., 1998, pp. 711–716 (hereinafter, referred to Prior Art 2);

(c) Journal Electrochemical Society, M. T. Wang et al., July 1998, pp. 2538–2545 (hereinafter, referred to as Prior Art 3); and

(d) 1998 Symposium on VLSI Technology Digest of Technical Papers, D. Denning et al., 1998, pp. 22–23.

In addition, a structure of a barrier metal layer and a method of fabricating the same both for preventing copper diffusion is suggested also in Japanese Unexamined Patent Publications 8-139092, 8-274098, 9-64044 and 10-256256, and Japanese Patent Application No. 10-330938. Herein, Japanese Patent Application No. 10-330938 is not published yet, and hence does not constitute prior art to the present invention. However, it is explained in the specification only for better understanding of the present invention. The applicant does not admit that Japanese Patent Application No. 10-330938 constitutes prior art to the present invention.

It is quite difficult to dry-etch copper, and hence, a copper wiring layer is formed generally by chemical mechanical polishing (CMP).

Specifically, a copper wiring layer is formed as follows.

An insulating film is formed on an underlying copper wiring layer. Then, the insulating film is formed with a recess and a through-hole reaching the underlying copper wiring layer. Then, a thin diffusion-barrier film is formed on surfaces of the recess and the through-hole therewith such that the recess and the through-hole is completely covered at surfaces thereof with the diffusion-barrier film in order to prevent copper diffusion from uncovered region.

Thereafter, a copper film is deposited filling the recess and the through-hole therewith by CVD or sputtering. Then, the copper film and the diffusion-barrier film are removed in selected regions by CMP. Thus, a copper wiring layer is completed.

As will be obvious to those skilled in the art, the diffusion-barrier film is required to have high coverage as well as capability of preventing copper diffusion and adhesion to copper.

The diffusion-barrier film is composed, for instance, of refractive metal such as tungsten (W), tantalum (Ta) or titanium (Ti), or nitride of such refractive metal such as tungsten nitride (WN), titanium nitride (TiN) or tantalum nitride (TaN).

As explained in Prior Art 2, for instance, a tantalum (Ta) barrier film has high adhesion with a copper film formed on the tantalum barrier film by sputtering, ensuring improvement in crystallinity of the copper film. However, since copper is diffused into the tantalum film, it would be necessary for the tantalum barrier film formed below the copper film, to have a thickness of 50 nm or greater.

Prior Art 4 reports that if a copper film is formed on a tantalum film by CVD, fluorine (F) segregates at an interface between the copper film and TaN, resulting in degradation in adhesion therebetween.

Prior Art 3 reports that a crystalline TaN barrier film oriented in directions of (200) and (111) can prevent copper diffusion more highly than a crystalline Ta barrier film.

As an solution to enhance a characteristic of preventing copper diffusion and adhesion to copper, a multi-layered structure of a metal film and a metal nitride film has been suggested.

For instance, the above-mentioned Japanese Patent Application No. 10-330938 has suggested a method of fabricating a multi-layered barrier film including a titanium film and formed by sputtering.

As illustrated in FIG. **1**, in accordance with the suggested method, only an argon gas is introduced into a sputter chamber to thereby form a titanium film **1**. Then, a nitrogen gas is introduced into the sputter chamber, and a thin titanium nitride film **2** is formed on the titanium film **1** auxiliarily making use of reaction between titanium and nitrogen. Thus, there is formed a multi-layered barrier structure **3** comprised of the titanium film **1** and the thin titanium nitride film **2**.

In the method, a metal oxide film formed on an underlying wiring film is removed by argon plasma prior to carrying out sputtering.

However, the conventional barrier film for preventing copper diffusion is accompanied with the following problems.

The first problem is that it is quite difficult to make a diffusion-barrier film have both a characteristic of preventing copper diffusion and a sufficient adhesive force with copper.

As illustrated in FIG. **2**, it is now assumed to form a metal film **5** having a crystallized pillar structure, on a semiconductor substrate **4**. In the metal film **5**, a lot of grains each comprised of individual crystals, and grain boundaries **7** each defining an interface between the grains **6** exist throughout the metal film **5**, that is, from an upper surface to

a bottom of the metal film **5**. The grain boundaries **7** define paths **8** through which copper is diffused. As a result, the metal film **5** has low barrier characteristic of preventing copper diffusion.

As illustrated in FIG. **3**, it is now assumed to form a metal film **5***a* on a semiconductor substrate **4**. If the metal film **5***a* is composed of metals having small resistivity, such as tungsten (W), titanium (Ti) or tantalum (Ta), the metal film **5** would have a polycrystal structure. As a result, the metal film **5***a* would have a pillar-like structure similarly to the metal film **5** illustrated in FIG. **2**, and accordingly, the metal film **5***a* would have small barrier characteristic of preventing copper diffusion.

However, it should be noted that if a copper film is formed on a crystalline metal film, such as a β-Ta (002) film as obtained in sputtering of a tantalum film, by sputtering, the copper film would have high adhesion and rich crystal orientation, though a barrier characteristic of preventing copper diffusion would be deteriorated. As a result, the copper film would enhance reliability in copper wiring.

In contrast, the metal film **5***a* illustrated in FIG. **3**, which is composed of particles **9** such as amorphous TaN and formed on the semiconductor substrate **4**, has small resistivity, specifically in the range of about 200 to 250 μΩcm, and does not have the paths through which copper is diffused unlike the crystalline metal film **5** illustrated in FIG. **2**. As a result, the metal film **5***a* would have high barrier characteristic of preventing copper diffusion.

However, since a surface of the metal film **5***a* is amorphous and hence crystal lattice is not uniformly arranged, if a copper film s formed on the amorphous metal film **5***a* by CVD or sputtering, copper crystallinity and adhesion to copper are degraded.

As mentioned so far, it is quite difficult to form a diffusion-barrier film having a single-layered structure comprised only of a crystalline metal film or an amorphous metal nitride film, and further having high barrier characteristic of preventing copper diffusion and high adhesion to copper.

The second problem is caused when a diffusion-barrier film is designed to have a multi-layered structure in order to avoid the above-mentioned problem of the single-layered diffusion-barrier film.

For instance, if a diffusion-barrier film is designed to have a multi-layered structure comprised of a crystalline metal film having high adhesion to copper and an amorphous metal nitride film having high barrier characteristic, such as TaN, there would be obtained a diffusion-barrier film having high barrier characteristic of preventing copper diffusion and high adhesion to copper.

However, since it was not possible in a conventional method to successively form a crystalline metal film and an amorphous metal nitride film by sputtering, the crystalline metal film and the amorphous metal nitride film had to be separately formed in the same sputtering chamber or be formed in separate sputtering chambers.

For instance, the above-mentioned Japanese Patent Application No. 10-330938 has suggested a method including the steps of introducing an argon gas into a sputtering chamber to thereby form a titanium film, and introducing a nitrogen gas into the sputtering chamber to thereby form a titanium nitride film on the titanium film.

However, in accordance with this method, the titanium nitride film cannot be formed until partial pressures of argon and nitrogen become stable by varying a mixture ratio of argon and nitrogen. Hence, it is impossible to enhance a fabrication yield of fabricating a diffusion-barrier film having a multi-layered structure.

The third problem relates to coverage of a film formed by sputtering.

In general, when a metal film or a metal nitride film is formed by sputtering, a metal target is sputtered by argon plasma generated by virtue of rotational magnetic field and application of DC bias, and resultingly, a metal film or a metal nitride film is deposited on a substrate located in facing relation to the metal target.

In sputtering, a pressure at which a metal target is sputtered is low, specifically, equal to 1 Pa or smaller. Since metal particles sputtered by argon plasma are radiated randomly to a surface of a substrate, for instance, if the substrate is formed at a surface thereof with a deep recess or hole, it would almost impossible to deposit a metal film such that such a recess or hole is completely covered with the metal film.

In addition, since a sputtering pressure is low, argon plasma could have a low plasma density, and hence, there cannot be expected re-sputtering effect in which a metal film deposited onto a surface of a substrate is sputtered by argon plasma.

In order to enhance coverage of a metal film, there has been suggested collimate sputtering in which a metal plate formed with a lot of through-holes is located between a sputtering target and a substrate, and metal particles are caused to pass through the through-holes to thereby uniform direction of metal particles. In accordance with the collimate sputtering, it is possible to deposit a metal film on a bottom of a recess formed at a surface of a substrate, but it is not possible to deposit a metal film onto an inner sidewall of the recess.

The fourth problem is that a crystalline metal film having high adhesion with a copper film tends to react with atmosphere to thereby a reaction layer at a surface thereof.

Such a reaction layer would much deteriorate adhesion of a metal film with a copper film.

The fifth problem is a copper oxide film is adhered again to a recess or hole.

An oxide film formed on a surface of an underlying wiring metal film is removed by argon plasma prior to deposition of a diffusion-barrier film by sputtering. When an underlying wiring layer is composed of copper, a copper oxide film is scattered by argon sputtering, and as a result, the thus scattered copper oxide is adhered again to a recess or hole formed at a surface of an insulating film.

The sixth problem is that when a copper film is formed on a tantalum film and an amorphous TaN film by CVD, adhesion between the copper film and a diffusion-barrier film is deteriorated.

SUMMARY OF THE INVENTION

In view of the above-mentioned problems in a conventional diffusion-barrier film, it is an object of the present invention to provide a diffusion-barrier film having both a diffusion-barrier characteristic of preventing copper from being diffused into a semiconductor device and high adhesion between a copper film and an interlayer insulating film.

It is also an object of the present invention to provide a multi-layered wiring structure including the above-mentioned diffusion-barrier film.

Another object of the present invention is to provide a method of fabricating such the above-mentioned diffusion-barrier film.

A further object of the present invention is to provide a method of fabricating a multi-layered copper wiring layer in which copper is buried above the above-mentioned diffusion-barrier film.

In one aspect of the present invention, there is provided a barrier film preventing diffusion of copper from a copper wiring layer formed on a semiconductor substrate, including a multi-layered structure of first and second films, the first film being composed of crystalline metal containing nitrogen therein, the second film being composed of amorphous metal nitride, the barrier film being constituted of common metal atomic species.

It is preferable that the first film is formed on the second film.

It is preferable that the second film has a thickness in the range of 80 angstroms to 150 angstroms both inclusive.

It is preferable that the first film has a thickness in the range of 60 angstroms to 300 angstroms both inclusive.

In another aspect of the present invention, there is provided a multi-layered wiring structure including a barrier film which prevents diffusion of copper from a copper wiring layer formed on a semiconductor substrate, the barrier film having a multi-layered structure of first and second films, the first film being composed of crystalline metal containing nitrogen therein, the second film being composed of amorphous metal nitride, the barrier film being constituted of common metal atomic species.

It is preferable that the barrier film covers a recess and a hole formed throughout an insulating film formed on an underlying wiring layer.

It is preferable that the multi-layered wiring structure further includes a copper film formed on the first film.

In still another aspect of the present invention, there is provided a method of forming a diffusion-barrier film by sputtering, including the steps of (a) preparing gas containing nitrogen therein, and (b) varying only power of an electric power source for generating plasma to thereby successively form a diffusion-barrier film having a multi-layered structure of first and second films, the first film being composed of crystalline metal containing nitrogen therein, the second film being composed of amorphous metal nitride, the barrier film being constituted of metal atomic species of sputter target.

It is preferable that the gas containing nitrogen therein has a pressure equal to or greater than 5 Pa.

It is preferable that the gas contains nitrogen at 10 volume % or smaller.

It is preferable that the metal atomic species of sputter target is one of tantalum, tungsten, titanium, molybdenum and niobium alone or in combination.

It is preferable that the second film has a thickness in the range of 80 angstroms to 150 angstroms both inclusive.

It is preferable that the first film has a thickness in the range of 60 angstroms to 300 angstroms both inclusive.

There is further provided a method of forming a diffusion-barrier film by RF magnetron sputtering making use of rotational magnetic field and RF power, including the steps of (a) preparing gas containing nitrogen therein, and (b) varying the RF power to thereby successively form a diffusion-barrier film having a multi-layered structure of first and second films, the first film being composed of crystalline metal containing nitrogen therein, the second film being composed of amorphous metal nitride, the barrier film being constituted of metal atomic species of sputter target.

There is still further provided a method of forming a diffusion-barrier film by RF magnetron sputtering, including the steps of (a) setting an electric power source for generation plasma to generate power having a first value, to thereby a first film, with a concentration of nitrogen in plasma gas being kept at a constant, and (b) setting the electric power source to generate power having a second value greater than the first value at the moment when the first film is formed by a predetermined thickness, to thereby form a second film on the first film.

It is preferable that the first film is composed of amorphous metal nitride, and the second film is composed of crystalline metal containing nitrogen therein.

There is yet further provided a method of forming a copper wiring film, including the steps of (a) radiating plasma of argon containing hydrogen therein, to a recess or hole formed at an insulating film formed on a semiconductor substrate, (b) forming a diffusion-barrier film to cover the recess or hole therewith without exposing to atmosphere, the diffusion-barrier film having a multi-layered structure of first and second films, the first film being composed of crystalline metal containing nitrogen therein, the second film being composed of amorphous metal nitride, and (c) forming a copper film on the diffusion-barrier film without exposing to atmosphere.

It is preferable that the diffusion-barrier film is formed by sputtering.

It is preferable that the copper film is formed in vacuum.

It is preferable that the copper film is formed by thermal chemical vapor deposition in which thermal dismutation in a complex of organic metal is utilized.

It is preferable that the copper film is formed by sputtering in which copper target is used.

The advantages obtained by the aforementioned present invention will be described hereinbelow.

In the diffusion-barrier film in accordance with the present invention, a copper film makes direct contact with a crystalline metal film containing nitrogen therein, ensuring high adhesion therebetween and high crystallinity of a copper film.

In addition, since the metal film contains nitrogen therein, copper diffusion into a semiconductor device can be prevented more effectively than a metal film having pure crystals.

In the diffusion-barrier film in accordance with the present invention, an amorphous metal film containing nitrogen therein lies under a crystalline metal film containing nitrogen therein. Hence, it is possible to effectively prevent copper diffusion, and to ensure high adhesion with an underlying insulating film such as a silicon dioxide film. That is, by forming a copper wiring layer on the diffusion-barrier film in accordance with the present invention, it is possible to not only ensure high crystallinity and high adhesion of a copper wiring layer, but also to prevent copper diffusion.

The method in accordance with the present invention makes it possible to successively form a diffusion-barrier film having a multi-layered structure of first and second films, by varying only power of an electric power source for generating plasma in sputtering in which gas containing nitrogen therein is employed. Herein, the first film is composed of crystalline metal containing nitrogen therein, and the second film is composed of amorphous metal nitride. The barrier film is constituted of metal atomic species of sputter target.

Specifically, an electric power source for generating plasma is first set to generate relatively low power with a concentration of nitrogen in plasma gas being kept constant. A film is formed in such a condition. Target metal makes sufficient reaction with nitrogen, and resultingly, an amor-

phous metal nitride film is formed. Immediately after the formation of the amorphous metal nitride film, the electric power source is set to generate relatively high power to thereby form a film without allowing sufficient time for reaction between nitrogen and target metal. As a result, there is obtained a crystalline metal film containing nitrogen therein.

Thus, it is possible to successively form a diffusion-barrier film in the same chamber, wherein the diffusion-barrier film has a multi-layered structure including a crystalline metal film containing nitrogen therein and an amorphous metal nitride film.

The method of fabricating a diffusion-barrier film employs RF magnetron sputtering in which rotational magnetic field and RF power are utilized. Since the method makes it possible to carry out sputtering where a nitrogen-containing gas has a pressure equal to or greater than 5 Pa, plasma density of argon which is a main constituent of sputtering gas can be enhanced, and thus, there can be obtained coverage for entirely covering a recess or hole formed at a surface of a substrate, with the diffusion-barrier film.

The method of fabricating a diffusion-barrier film, in accordance with the present invention, includes the step of radiating plasma of argon containing hydrogen therein, to a recess or hole formed at an insulating film formed on a semiconductor substrate. This step reduces a copper oxide film formed on a surface of an underlying copper wiring layer, to thereby turn copper oxide back to copper, ensuring remarkable reduction in re-sputtering of a copper oxide film to a surface of a recess or hole formed at a surface of an insulating film.

Then, a diffusion-barrier film is formed to cover the recess or hole therewith without exposing to atmosphere, wherein the diffusion-barrier film has a multi-layered structure of first and second films, the first film being composed of crystalline metal containing nitrogen therein, the second film being composed of amorphous metal nitride. Then, a thin copper film is formed on the diffusion-barrier film in vacuum. As a result, there is obtained a multi-layered structure comprised of the diffusion-barrier film and the copper wiring film without a metal oxide layer being sandwiched therebetween.

The above and other objects and advantageous features of the present invention will be made apparent from the following description made with reference to the accompanying drawings, in which like reference characters designate the same or similar parts throughout the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of a conventional copper wiring structure.

FIG. **2** is a cross-sectional view of another conventional copper wiring structure.

FIG. **3** is a cross-sectional view of still another conventional copper wiring structure.

FIG. **4**A is a cross-sectional view of a diffusion-barrier film in accordance with the first embodiment of the present invention, illustrating the first step of a method of fabricating the same.

FIG. **4**B is a cross-sectional view of a diffusion-barrier film in accordance with the first embodiment of the present invention, illustrating the second step of a method of fabricating the same.

FIG. **4**C is a cross-sectional view of a diffusion-barrier film in accordance with the first embodiment of the present invention, illustrating the third step of a method of fabricating the same.

FIG. **4**D is a cross-sectional view of a diffusion-barrier film in accordance with the first embodiment of the present invention, illustrating the fourth step of a method of fabricating the same.

FIG. **5** illustrates a high-pressure RF magnetron sputtering apparatus used in the first embodiment.

FIG. **6** is a graph showing coverage characteristic of a tantalum film in high-pressure RF magnetron sputtering.

FIGS. **7** and **8** are cross-sectional views of a recess covered with a tantalum film in high-pressure RF magnetron sputtering.

FIG. **9** is a graph showing a relation among a ratio of a nitrogen gas in a mixture gas introduced into a chamber, RF power, and resistivity of a film formed by sputtering.

FIGS. **10** to **18** are graphs each showing film quality and characteristics of TaN and Ta films in high-pressure RF magnetron sputtering.

FIGS. **19** and **20** are photographs of a film formed by high-pressure RF magnetron sputtering which photograph is taken by means of a scanning electron microscopy (SEM).

FIG. **21** is a cross-sectional view of a diffusion-barrier film formed by high-pressure RF magnetron sputtering which barrier-diffusion film is comprised of a crystalline Ta film containing nitrogen in solid solution and an amorphous metal TaN film.

FIG. **22** is a photograph of a film formed by high-pressure RF magnetron sputtering which photograph is taken by means of a scanning electron microscopy (SEM).

FIG. **23** is a cross-sectional view of a diffusion-barrier film covering a recess therewith.

FIG. **24** illustrates a DC magnetron sputtering apparatus used in the fourth embodiment.

FIG. **25** is a cross-sectional view of a diffusion-barrier film covering a recess formed at a surface of an insulating film formed above a lower wiring layer.

FIG. **26** is a cross-sectional view of a diffusion-barrier film covering a recess formed at a surface of an insulating film formed above lower wiring layers.

FIG. **27** is a plan view of a cluster apparatus used for forming a copper wiring layer.

FIG. **28** is a graph showing a diffusion profile of fluorine into a diffusion-barrier film.

FIG. **29** is a graph showing a diffusion profile of copper into a diffusion-barrier film.

FIG. **30** is a cross-sectional view of a copper wiring structure in accordance with the seventh embodiment.

FIG. **31** is a cross-sectional view of a copper wiring structure in accordance with the seventh embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments in accordance with the present invention will be explained hereinbelow with reference to drawings.

A method of fabricating a diffusion-barrier film in accordance with the preferred embodiment is explained hereinbelow with reference to FIGS. **4**A to **4**D.

As illustrated in FIG. **4**A, a first insulating film **12***a* is formed on a semiconductor substrate **11**, and a second insulating film **12***b* is formed on the first insulating film **12***a*. A copper wiring layer **44** is buried in the first insulating film

12*a*. The second insulating film **12***b* is formed at a surface thereof with recesses **13** in each of which a wiring is to be formed. Holes **14** reach the first insulating film **12***a* from a bottom of each of the recesses **13**.

First, the semiconductor substrate **11** is exposed to argon plasma containing hydrogen therein, in a first chamber.

Then, the semiconductor substrate **11** is transferred in vacuum to a second chamber, and a film is formed on the semiconductor substrate **11** in a nitrogen-containing gas by sputtering in which a sputtering target is composed of refractive metal.

First, an electric power source for generating plasma is set to generate relatively low power with a concentration of nitrogen in plasma gas being kept constant. As a result, the target metal makes sufficient reaction with nitrogen, and an amorphous metal nitride film **15** is deposited over a surface of the second insulating film **12***b*, as illustrated in FIG. **4**B.

Then, immediately after the formation of the amorphous metal nitride film **15**, the electric power source is set to generate relatively high power to thereby form a film without allowing sufficient time for reaction between nitrogen and the target metal. As a result, a crystalline metal film **16** containing nitrogen therein is formed on the amorphous metal nitride film **15**.

Thus, as illustrated in FIG. **4**B, it is possible to successively and effectively fabricate the diffusion-barrier film **17** having a multi-layered structure, on both an inner sidewall and a bottom of the recesses **13** and the holes **14** in the same chamber. By setting a sputtering pressure sufficiently high while deposition of the diffusion-barrier film **17** by sputtering, it would be possible to enhance coverage of the diffusion-barrier film **17**.

Thereafter, the semiconductor substrate **11** is transferred into a third chamber in vacuum. Then, a copper film **18** is deposited over the diffusion-barrier film **17** in vacuum in the third chamber to thereby completely fill the recesses **13** and the holes **14** with the copper film **18**, as illustrated in FIG. **4**C. Since the crystal metal film **16** containing nitrogen therein is exposed outside and the semiconductor substrate **11** is transferred in vacuum, an oxide film is not formed at a surface of the crystal metal film **16**.

Then, as illustrated in FIG. **4**D, the diffusion-barrier film **17** and the copper film **18** are removed by CMP until the second insulating film **12***b* appears. Thus, there is obtained a copper wiring structure having high reliability.

The reason of enhancement in barrier characteristic of preventing copper diffusion is to introduce nitrogen into the metal film **16**. In addition, the metal film **16** containing nitrogen ensures high adhesion with copper. The amorphous metal nitride film **15** also has a characteristic of preventing copper diffusion, and further enhances adhesion with the second insulating film **12***b*. Thus, it is possible to ensure high adhesion between the copper film **18** and the diffusion-barrier film **17**, and to prevent copper from being diffused from the copper film **18** into the second insulating film **12***b*.

Hereinbelow are explained detailed examples of the above-mentioned embodiment.

FIRST EXAMPLE

In the first example, hereinbelow is explained sputtering for fabricating a multi-layered structure comprised of a crystalline metal film containing nitrogen therein and an amorphous metal nitride film.

The sputtering in the first example is carried out in a RF magnetron sputtering apparatus illustrated in FIG. **5**.

In the illustrated RF magnetron sputtering apparatus, a chamber **21** is kept to be in vacuum, specifically, to have an internal pressure of about 1×10^{-7} Pa to about 1×10−6 Pa by means of a pump **33** such as a dry pump, a cryosorption pump or a turbo pump. In the chamber **21** is placed a heater **34** which can heat a semiconductor substrate **22** introduced into the chamber **21**, up to about 20 to 300 degrees centigrade. A metal target **28** or the semiconductor substrate **22** is designed to be able to raise or lower, and hence, a distance between the metal target **28** and the semiconductor substrate **22** can be varied in the range of 102 mm to 134 mm.

Argon and nitrogen gases are adjusted with respect to a flow rate by means of mass flow controllers **31**, and then, introduced into the chamber **21**. When the argon and nitrogen gases are introduced into the chamber **21**, the chamber **21** has an internal pressure of about 2 Pa to about 17 Pa.

The metal target **28** has a diameter, for instance, in the range of about 300 mm to about 320 mm. The metal target **28** is fixed to the chamber **21** through a target holder **27**, a cathode **23** and insulators **29**. In the cathodes **23** are rotatably arranged a plurality of permanent magnets **24**. By rotating the permanent magnets **24**, magnetic field **30** in the chamber **21** is uniformized, and erosion at a surface of the metal target **28** is also uniformized. As a result, it is possible to enhance uniformity of a film to be formed on the semiconductor substrate **22**.

A RF electric power source **25** for introducing RF power into the chamber **21** is in electrical connection with the cathode **23** through a matching box **32** carrying out impedance matching. The RF electric power source **25** applies radio frequency (RF) having a frequency of 13.56 MHz to the metal target **28** having a diameter of 300 mm, at 0 to 10 kW.

Turning the RF electric power source **25** on to thereby introduce RF into the chamber **21**, there is generated argon plasma containing nitrogen therein. The target metal **28** is sputtered by argon ions generated in the argon plasma **26**. As a result, metal particles of the target metal **28** fly into the semiconductor substrate **22**, and thus, the crystalline metal film **16** containing nitrogen therein or the amorphous metal nitride film **15** is formed.

The inventor actually formed a tantalum film covering therewith the hole **14** (see FIG. **4**A) formed through the second insulating film **12***b* by means of the above-mentioned RF magnetron sputtering apparatus. The coverage characteristic of the tantalum film is shown in FIG. **6**.

The hole **14** had a diameter in the range of 0.3 μm to 1.5 μm. The second insulating film **12***b* had a thickness of about 1.5 μm where the hole **14** was formed.

As is obvious in view of FIG. **6**, as a sputtering pressure is increased from 2 Pa to 17 Pa, bottom coverage is enhanced. Herein, bottom coverage is defined as a ratio of a thickness of the tantalum film at a bottom of the hole **14** to a thickness of the tantalum film at a surface of the second insulating film **12***b*. Specifically, when a sputtering pressure is over 5 Pa, sufficient coverage can be obtained to a hole having a great aspect ratio.

A thickness of the tantalum film at an inner sidewall of the hole **14** is equal to about a half of a thickness of the tantalum film at a bottom of the hole **14**. As a sputtering pressure is increased, the tantalum film covers an inner sidewall of the hole **14** therewith to a greater degree.

The reason of this phenomenon is considered as follows.

The first reason is an increase in the number of Ta ions in plasma gas, as illustrated in FIG. **7**.

As a sputtering pressure is increased, tantalum atomics increasingly make collision with excited argon atomics, resulting in that argon atomics are facilitated to be ionized. The resultant tantalum ions are attracted to negative self-bias generated at the semiconductor substrate **22**. As a result, an incident angle at which tantalum ion flux **35** is radiated to the semiconductor substrate **22** becomes nearly 90 degrees. Thus, overhanging which occurs in the vicinity of an edge of recess or hole in conventional sputtering is suppressed, ensuring tantalum atomics to reach a bottom of the hole **14** or recess **13**. As a result, a tantalum film **36** entirely covers an inner sidewall of the hole **14**.

The second reason is that the deposited tantalum film **36** is re-sputtered by argon ions **39**, as illustrated in FIG. **8**.

The argon ions **39** which are primary constituents of plasma gas are accelerated by electric field and reach not only a target but also the semiconductor substrate **22** which is in a condition of negative self-bias. This means that the tantalum film **36** having been deposited onto the semiconductor substrate **22** is re-sputtered. Since the tantalum film deposited in the vicinity of an edge of the hole **14** or recess **13** and causing overhanging is re-sputtered by the argon ions **39**, as indicated with an arrow **37**, tantalum atomics **38** directing to a bottom of the hole **14** or recess **13** are not interfered at the edge of the hole **14** or recess **13**. Accordingly, it is ensured that a tantalum film is deposited on a bottom and an inner sidewall of the hole **14** or recess **13**.

In addition, since the tantalum film **36** deposited on a bottom of the hole **14** or recess **13** is re-sputtered by the argon ions **39**, tantalum atomics generated by re-sputtering are deposited again on an inner sidewall **40** of the hole **14** or recess **13**, ensuring enhancement in coverage at the sidewall **40** of the hole **14** or recess **13**.

It is not possible to determine which is a main reason for enhancement in coverage among the above-mentioned first and second reasons. However, since mean free path of plasma ion is just a few millimeters under a pressure over 5 Pa, it is considered that almost 90 degrees of an incident angle of the tantalum ion flux **35** does not contribute to enhancement in coverage so much. The main reason why the coverage is enhanced is considered that argon ions are generated in a sufficient density by virtue of a high pressure, and a tantalum film having been deposited are re-sputtered by the argon ions.

In accordance with the experiments the inventor had conducted, it was confirmed that coverage was enhanced in sputtering of a tantalum nitride film, carried out under a high pressure over 5 Pa.

As mentioned so far, it is preferable that a sputtering pressure is set equal to or greater than 5 Pa in RF magnetron sputtering.

SECOND EXAMPLE

FIG. **9** shows a relation between a flow rate ratio and resistivity of a film formed by high-pressure RF magnetron sputtering having been explained in the first example, for various RF powers. Herein, the flow rate ratio is defined as a ratio of a volume of argon gas to be introduced into the chamber **21** to a volume of nitrogen gas to be introduced into the chamber **21** ($N_2/(Ar+N_2)$).

The relation shown in FIG. **9** was observed when the chamber **21** had a pressure of 13 Pa, the semiconductor substrate **22** was heated at 200 degrees centigrade, the permanent magnets **24** were rotated at 10 r.p.m., and the distance between the metal target **28** and the semiconductor substrate **22** was 134 mm.

As a ratio of N_2 gas in the flow rate ratio $N_2/(Ar+N_2)$ is increased, the resistivity is once reduced, and thereafter, increased again, regardless the RF power. However, an increase rate of the N_2 gas ratio is dependent on the RF power. The resistivity increases at a lower rate at the greater RF power.

FIGS. **10** to **13** show how X-ray diffraction (XRD) patterns vary as the N_2 gas ratio is varied when RF power of 6 kW (8.5 W/cm^2) is applied to the tantalum target having a diameter of 300 mm.

Specifically, FIGS. **10** to **13** shows XRD patterns when the N_2 gas ratio is equal to 0%, 1%, 5%, and 7% respectively. Hereinbelow are explained FIGS. **10** to **13** in comparison with FIG. **9**.

When the N_2 gas ratio is equal to 0%, there is obtained a β-Ta(002)-oriented crystalline tantalum film which has resistivity in the range of about 160 to 200 μΩ-cm, as illustrated in FIG. **10**.

When the N_2 gas ratio is equal to 1%, there is obtained a crystalline metal film (herein, a tantalum film) containing nitrogen therein, which includes β-Ta and $TaN_{0.1}$ in mixture and which has resistivity in the range of about 100 μΩ-cm, as illustrated in FIG. **11**.

When the N_2 gas ratio is equal to 5%, it is understood in view of FIG. **12** that XRD pattern strength is reduced, and hence, there is formed an amorphous metal nitride film, which has resistivity in the range of about 200 to 250 μΩ-cm.

When the N_2 gas ratio is equal to 7%, a crystalline metal nitride film (Ta_3N_5) is formed, and resistivity is further increased, as illustrated in FIG. **13**.

As mentioned above, when the tantalum target is selected, a crystalline structure, composition and resistivity of a film to be formed by sputtering vary in dependence on both a concentration of nitrogen gas in sputtering gas and RF power. Conversely speaking, this means that it is possible to control characteristics of a film to be formed by sputtering, by controlling both a concentration of nitrogen gas in sputtering gas and RF power. The present invention is based on this discovery.

However, it is difficult to vary a flow rate of sputtering gas (that is, a pressure of sputtering gas) and N_2 composition ratio in sputtering. Accordingly, it is necessary in practical use to keep both a flow rate of sputtering gas (that is, a pressure of sputtering gas) and N_2 composition ratio constant, and to vary only RF power, to thereby control a crystalline structure, composition and resistivity of a film to be formed by sputtering.

FIG. **14** shows how resistivity varies when only RF power is varied while a N_2 gas ratio is kept fixed at 2%. As is obvious in view of FIG. **14**, it is understood that it is possible to control film quality and resistivity of a film to be formed by sputtering, even when only RF power is varied. In FIG. **14**, resistivity is varied when a gas pressure is equal to 10 Pa, the permanent magnets are rotated at 10 r.p.m., and the substrate was heated at 200 degrees centigrade.

FIGS. **15** to **18** show XRD characteristics relative to RF power. FIGS. **15** to **18** show XRD characteristics observed when RF power is equal to 2 kW, 3 kW, 6 kW and 8 kW, respectively.

Specifically, when RF power is equal to 2 kW, there is obtained amorphous Ta_2N, as illustrated in FIG. **15**. By increasing RF power, there is obtained crystalline $TaN_{0.1}$. When RF power is equal to 8 kW, there is obtained a crystalline metal film containing nitrogen therein, which includes a β-Ta film and $TaN_{0.1}$ in mixture.

FIGS. **19** and **20** are SEM (Scanning Electron Microscopy) photographs of films obtained when RF power is set equal to 2 kW and 8 kW, respectively.

When RF power is set equal to 2 kW, as is obvious in view of XRD illustrated in FIG. **15**, there is not observed grain boundary, because a deposited film has an amorphous structure. In contrast, when RF power is set equal to 8 kW, as is obvious in view of XRD illustrated in FIG. **18**, there is obtained a crystalline film including a β-Ta film and $TaN_{0.1}$ in mixture, and having a pillar-like structure.

That is, if Ta_2N, which is an amorphous metal nitride film, is deposited at 2 kW of RF power, and RF power is increased up to 8 kW immediately when the film has acquired a desired thickness, the film is turned into a crystalline metal film containing nitrogen therein. As a result, as illustrated in FIG. **21**, a diffusion-barrier film **17** is formed on a semiconductor substrate **11** where the diffusion-barrier film **17** has a multi-layered structure comprised of an amorphous metal nitride film **15** and a crystalline metal film **16** containing nitrogen therein. Specifically, the amorphous metal nitride film **15** is an amorphous Ta_2N film, and the crystalline metal film **16** is composed of crystalline β-Ta and crystalline $TaN_{0.1}$ in mixture.

FIG. **22** is a SEM photograph of a cross-section of the diffusion-barrier film **17** which is formed by changing sputtering power from 2 kW to 8 kW while a TaN film is being deposited, to thereby successively deposit the crystalline metal film **16** and the amorphous metal nitride film **15** each by a thickness of about 500 angstroms. It is confirmed in FIG. **22** that the amorphous Ta_2N film **15** and the crystalline metal film **16** containing nitrogen therein form a multi-layered structure.

The reason of this phenomenon is considered as follows.

When sputtering power is set equal to 2 kW, since a sputtering rate caused by argon ions is relatively low, there is sufficient time for a tantalum target to be nitrided by N_2 at a surface thereof. Hence, the tantalum target is nitrided at a surface thereof, and turned into Ta_2N. Since the thus produced Ta_2N is sputtered by argon ions, a Ta_2N film is deposited. However, when sputtering power is set equal to 8 kW, the tantalum target is sputtered by argon ions before a surface of the tantalum target is sufficiently nitrided. As a result, there is obtained a tantalum film slightly containing nitrogen.

By utilizing the above-mentioned phenomenon, it is possible to form the diffusion-barrier film **17** having a multi-layered structure and covering therewith the recess **13** or the hole **14** formed at the second insulating film **12***b* formed on the semiconductor substrate **11**, as illustrated in FIG. **23**.

The lower film or amorphous metal nitride (Ta_2N) film **15** is required to have such a thickness that barrier characteristic of preventing copper diffusion is ensured and adhesion with the underlying insulating film **12***b* is also ensured. A desired thickness of the amorphous metal nitride (Ta_2N) film **15** is in the range of about 80 angstroms to about 150 angstroms.

On the other hand, the crystalline nitrogen-containing metal film **16** composed of crystalline β-Ta and crystalline $TaN_{0.1}$ in mixture is required to have such a thickness that barrier characteristic of preventing copper diffusion is ensured and adhesion with copper is also ensured. A desired thickness of the crystalline metal film **16** is in the range of about 60 angstroms to about 300 angstroms.

THIRD EXAMPLE

The RF magnetron sputtering having been explained in the first example makes it possible to enhance coverage characteristic of a deposited film for covering a recess or hole therewith, by introducing a gas having a higher pressure than usual, specifically, a pressure equal to or greater than 5 Pa, into a chamber. That is, it is possible to form the multi-layered barrier film **17** under desired coverage characteristic by switching RF power with a sputtering pressure being kept equal to or greater than 5 Pa, even when there is carried out dual-damassin process in which the recess **13** and the hole **14** formed at a surface of the second insulating film **12***b* formed on the semiconductor substrate **11** are concurrently filled with the diffusion-barrier film **17**.

FOURTH EXAMPLE

In the above-mentioned first and second examples, the process in which a multi-layered barrier film is successively formed by switching RF power while the film is being formed is applied to RF magnetron sputtering. This process may be applied to DC magnetron sputtering, as illustrated in FIG. **24**, though a N_2 gas ratio and RF power are different from those in the first and second examples.

FIG. **24** illustrates a DC magnetron sputtering apparatus. The apparatus is comprised of a chamber **21**, a heater **34** fixed on a bottom of the chamber **21** for heating a semiconductor substrate **22**, a target metal **28** fixed to a top of the chamber **21** by means of insulators **29** and a cathode **23**, a pump **33** for exhausting air from the chamber **21** such that a pressure in the chamber **21** is in the range of about 1×10^{-7} Pa to about 1×10^{-6} Pa, a magnet **42** positioned above the target metal **28**, mass flow controllers **31** for adjusting flow rates of argon gas and nitrogen gas, and allowing the gases to enter the chamber **21**, and a DC electric power source **41** for applying a DC voltage to both the cathode **23** and the heater **34**.

Turning the DC electric power source **41** on, argon plasma containing nitrogen therein is generated in the chamber **21**.

FIFTH EXAMPLE

In the first and second examples, there is formed only one via-hole and wiring. However, it should be noted that the present invention may be applied to a copper wiring structure including two or more via-holes and wirings.

In the fifth example, as illustrated in FIG. **25**, a first insulating film **12***a* is formed on a semiconductor substrate **11**. The first insulating film **12***a* is formed with via-holes which is filled with a copper wiring layer **44** with a diffusion-barrier film **17** being sandwiched between an inner surface of each of the via-holes and the copper wiring layer **44**. A second insulating film **12***b* is formed on the first insulating film **12***a*. The second insulating film **12***b* is also formed with recesses and via-holes which is filled with a copper wiring (not illustrated) with a diffusion-barrier film **17** being sandwiched between inner surfaces of the recesses and the via-holes, and the copper wiring.

Thus, recesses and/or holes formed throughout each of multi-layered insulating films are covered with the diffusion-barrier film **17**, and then, the recesses and/or holes may be filled with a copper wiring layer.

An example of the multi-layered structure is illustrated in FIG. **26**. The illustrated multi-layered structure is comprised of three insulating layers. Each of the insulating layers is formed with recesses and via-holes, which are covered at their surfaces with a diffusion-barrier layer **17**, and filled with copper wiring layers **44***a* and **44***b*.

Hereinbelow is explained a method of fabricating the multi-layered structure illustrated in FIG. **26**.

A semiconductor substrate **11** is formed at a surface thereof with oxide layers **11***a*. A semiconductor device **11***b* is formed on the semiconductor substrate **11** between the oxide layers **11***a*.

A first insulating film **12***a* is formed on the semiconductor substrate **11**. The first insulating film **12***a* is comprised of, for instance, a silicon dioxide film. The first insulating film **12***a* is formed with recess and holes reaching the semiconductor device **11***b*. The recesses and holes are covered at their inner surfaces with the diffusion-barrier film **17**. The diffusion-barrier film **17** has a multi-layered structure comprised of a crystalline nitrogen-containing metal film and an amorphous metal nitride film, and has sufficient coverage to cover recesses and holes therewith. The diffusion-barrier film **17** may be formed by such high-pressure RF magnetron sputtering as mentioned in the first example.

Then, the recesses and holes are filled with copper in vacuum. Then, the copper film and the diffusion-barrier film **17** are removed by CMP until the first insulating film **12***a* appears. Thus, there is fabricated the copper wiring layer **44***a*.

Since copper does not form passive state at a surface, the copper wiring layer **44***a* may be oxidized. In order to prevent oxidation of the copper wiring layer **44***a*, a silicon nitride film **12***d* is formed over the first insulating film **12***a*.

Then, a second insulating film **12***b* is formed on the first insulating film **12***a*. The second insulating film **12***b* is formed with recesses and holes reaching the copper wiring layer **44***a* formed in the first insulating film **12***a*. Then, the recesses and holes formed in the second insulating film **12***b* are covered with the diffusion-barrier film **17**, and the recesses and holes are filled with the copper wiring layer **44***b*. By repeating the above-mentioned steps by the desired number, there can be fabricated a semiconductor device having such a multi-layered copper wiring structure as illustrated in FIG. **26**.

SIXTH EXAMPLE

The sixth example relates to an apparatus and a method of successively forming both a diffusion-barrier film having a multi-layered structure and copper wiring layer.

FIG. **27** is a top plan view of an apparatus of forming a copper wiring layer, in accordance with the sixth example.

The apparatus includes a cluster chamber **51** including a separation chamber **51** at a center. The separation chamber **51** is equipped therein with a robot **52** for transferring a semiconductor substrate.

The cluster chamber **51** is comprised further of two lord lock chambers **45**, a chamber **46** used for heating a semiconductor substrate, an etching chamber **47** used for cleaning recesses and holes, a sputter chamber **48** used for fabricating a diffusion-barrier film, and a chamber **49** used for forming a copper wiring layer, arranged around the separation chamber **51**.

It is possible to form a copper wiring layer without exposure of a semiconductor substrate to atmosphere through the use of the cluster chamber **50**.

Hereinbelow are explained steps of fabricating a copper wiring layer.

First, a semiconductor substrate is introduced into one of the lord lock chambers **45**. An insulating film is formed in advance on the semiconductor substrate, and the insulating film is formed in advance with a recess and/or hole.

Then, the lord lock chamber **45** is evacuated of air by means of a dry pump and a turbo pump for about five minutes. As a result, the lord lock chamber **45** has a vacuum degree of 7×10^{-3} Pa to 8×10^{-3} Pa.

Then, a gate valve between the lord lock chamber **45** and the separation chamber **51** is made open. The separation chamber **51** is in advance kept in a vacuum degree of about 5×10^{-5} Pa to 1×10^{-5} Pa by means of a dry pump and a turbo pump. Hence, the semiconductor substrate is transferred into the separation chamber **52** by the robot **52** without being exposed to atmosphere.

Then, the semiconductor substrate is transferred into the chamber **46** which is in advance kept in a vacuum degree of about $6\times10^{31\ 5}$ Pa by means of a dry pump and a turbo pump. The semiconductor substrate is heated at about 50 to about 200 degrees centigrade in the chamber **46** to thereby remove moisture existing at a surface of the semiconductor substrate and clean a surface of the semiconductor substrate.

Then, the semiconductor substrate is transferred into the etching chamber **47** from the chamber **46** through the separation chamber **51**. The etching chamber **47** is kept in a vacuum degree of about 5×10^{-6} Pa by means of a cryosorption pump, dry pump and a turbo pump.

After introducing the semiconductor substrate into the etching chamber **47**, the semiconductor substrate is plasma-etched in argon gas or argon gas diluted with hydrogen gas (H_2/Ar=3%). By carrying out plasma-etching, a surface of the semiconductor substrate and inner surfaces of a recess and a hole are reduced and cleaned.

The plasma-etching has an advantage that edges of a recess and a hole are ground by the plasma-etching, and accordingly, an opening area of the recess and hole is broadened, ensuring enhancement in coverage characteristic.

Then, the semiconductor substrate is transferred into the sputter chamber **48** from the etching chamber **47** by means of the robot **52**. The sputter chamber **48** is kept in a vacuum degree of about 4×10^{-6} Pa by means of a cryosorption pump, dry pump and a turbo pump. The high-pressure RF magnetron sputtering as having been explained in the first example is carried out in the sputter chamber **48**.

In the sputter chamber **48**, a crystalline nitrogen-containing metal film (a film composed of crystalline β-Ta and crystalline $TaN_{0.1}$ in mixture) and an amorphous metal nitride film (a Ta_2N film) are deposited on the semiconductor substrate by the method having been explained in the first and second examples, wherein RF power is instantaneously switched. In this example, a gas pressure is kept at 10 Pa, a substrate temperature is kept at 200 degrees centigrade, a N_2 gas ratio is kept at 2%, and RF power is switched from 2 kW to 8 kW. As a result, there is obtained a diffusion-barrier film having a multi-layered structure and also having enhanced coverage characteristic under the characteristics illustrated in FIG. **6**.

Then, the semiconductor substrate is transferred in vacuum to the chamber **49** from the sputter chamber **48**. The chamber **49** is kept in a vacuum degree of about 4×10^{-4} Pa by means of a dry pump and a turbo pump. Since the semiconductor substrate is transferred in vacuum, the crystalline nitrogen-containing metal film in the diffusion-barrier film is kept clean at a surface thereof. A copper film is deposited on the crystalline nitrogen-containing metal film by chemical vapor deposition (CVD) such that the recess and hole is filled with copper, as follows.

The semiconductor substrate is kept at about 170 to about 200 degrees centigrade. A source including Cu (hfac) tmvs (trimethylvinylsilyl hexafluoroacetylacetonate copper (I)) as a main constituent is introduced into a carburetor at 1 to 2

grams per minute through a liquid transfer system. The source gasified in the carburetor is introduced into the chamber **49** together with nitrogen carrier gas, resulting in that the chamber **49** is kept at about 1 kPa.

The gas introduced into the chamber **49** makes chemical reaction on the semiconductor substrate, and is turned into copper, and then, deposited on the semiconductor substrate. Herein, copper is deposited by such a thickness that a recess and/or hole is sufficiently filled with copper, for instance, a thickness in the range of about 8000 angstroms to about 15000 angstroms.

In particular, when a copper film is formed by CVD, segregation of fluorine at a surface of the diffusion-barrier film, diffusion of fluorine into the diffusion-barrier film, and diffusion of copper into the diffusion-barrier film exert a great influence on the adhesion, which fluorine is contained in Cu (hfac) tmvs which is a source for carrying out CVD.

FIGS. **28** and **29** illustrate diffusion profiles of fluorine and copper into the diffusion-barrier film, respectively, which profiles were measured by SIMS (secondary ion mass spectroscopy).

In a β-Ta film obtained by sputtering carried out in argon atmosphere, since fluorine segregates at an interface between copper and tantalum, the β-Ta film would have poor adhesion. With respect to a Ta_2N film, though fluorine is diffused into the Ta_2N film, copper is scarcely diffused in the Ta_2N film. As a result, atomics are coupled with each other with a poor force, and hence, the Ta_2N film would have poor adhesion. In contrast, with respect to a $TaN_{0.1}$ film, since copper and fluorine are allowed to be diffused into the $TaN_{0.1}$ film, atomics are coupled with each other with a strong force, and as a result, the $TaN_{0.1}$ film would high adhesion.

Thus, it is understood that if copper is deposited by CVD, the diffusion-barrier film having a multi-layered structure comprised of a crystalline $TaN_{0.1}$ film and an amorphous Ta_2N film would have enhanced adhesion and barrier characteristic of preventing copper diffusion.

In accordance with the sixth example, a copper wiring layer can be formed on a semiconductor substrate without the semiconductor substrate being exposed to atmosphere. Accordingly, the diffusion-barrier film is kept clean at a surface, and hence, film quality of a copper film formed by CVD is likely to be reflected to a crystalline structure of a tantalum film of the diffusion-barrier film. Thus, it is possible to enhance crystal orientation of copper and adhesion between copper and a diffusion-barrier film.

SEVENTH EXAMPLE

The seventh example relates to the cluster chamber **50** illustrated in FIG. **27**. In the seventh example, the sputter chamber **48** is positioned in a region where a copper wiring layer is to be formed, which region corresponds to the chamber **49** in which a copper wiring layer is formed. Since the diffusion-barrier film includes a $TaN_{0.1}$ film containing crystalline β-Ta therein, at a surface, adhesion between the diffusion-barrier film and a copper film formed by sputtering is kept the same as adhesion between the diffusion-barrier film and a copper film formed by CVD.

EIGHTH EXAMPLE

In the eighth example, the semiconductor substrate is taken out of the cluster chamber **50** illustrated in FIG. **27**. The semiconductor substrate has such a copper wiring structure as illustrated in FIG. **30**. Specifically, recesses and holes formed in the second insulating film **12***b* are covered with the diffusion-barrier film **17**, and a copper film **53** is formed covering the diffusion-barrier film **17** therewith.

A second copper film **54** is deposited over the copper film **53** by plating such that the recesses and holes are filled with the second copper film **54**. As a result, as illustrated in FIG. **31**, it is possible to fabricate a structure comprised of the multi-layered barrier layer **17**, the copper film **53** formed by CVD or sputtering, and the second copper film **54** formed by plating. Thereafter, as illustrated in FIG. **4**D, for instance, the second copper film **54**, the copper film **53** and the diffusion-barrier film **17** are removed by CMP. Thus, there is obtained a copper wiring structure.

While the present invention has been described in connection with the preferred embodiments, the present invention provides the following advantages.

The first advantage is that it is possible to have a diffusion-barrier film having sufficient barrier characteristic of preventing copper diffusion and high adhesion with a copper film. This is because the diffusion-barrier film is designed to have a multi-layered structure comprised of an amorphous metal nitride film having a high barrier characteristic of preventing copper diffusion and a crystalline nitrogen-containing metal film having high adhesion with copper.

The second advantage is that it is possible to successively fabricate the diffusion-barrier film in a common chamber. This ensures reduction in apparatus cost and reduction in time for fabricating the diffusion-barrier film.

This is because that it is possible to successively form an amorphous metal nitride film and a crystalline nitrogen-containing metal film by instantaneously changing only RF power with a volume ratio of a nitrogen gas to a process gas introduced into a chamber, being kept constant. In accordance with this method, an upper metal film in the diffusion-barrier film inevitably contains nitrogen therein.

The third advantage is that a copper film can be formed with a surface of the diffusion-barrier film being kept clean, through the use of an apparatus of transferring a semiconductor substrate in vacuum. As a result, reliability in a copper wiring layer can be enhanced.

While the present invention has been described in connection with certain preferred embodiments, it is to be understood that the subject matter encompassed by way of the present invention is not to be limited to those specific embodiments. On the contrary, it is intended for the subject matter of the invention to include all alternatives, modifications and equivalents as can be included within the spirit and scope of the following claims.

The entire disclosure of Japanese Patent Application No. 11-214110 filed on Jun. 24, 1999 including specification, claims, drawings and summary is incorporated herein by reference in its entirety.

What is claimed is:

1. A barrier film preventing diffusion of copper from a copper wiring layer formed on a semiconductor substrate, comprising a multi-layered structure of first and second films,

said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film in direct contact with said second film,

said first film containing nitrogen in a smaller content than that of said second film.

2. The barrier film as set forth in claim **1**, wherein said second film has a thickness in the range of 80 angstroms to 150 angstroms both inclusive.

3. The barrier film as set forth in claim **1**, wherein said first film has a thickness in the range of 60 angstroms to 300 angstroms both inclusive.

4. The barrier film as set forth in claim **1**, wherein said first film is composed of β-Ta and $TaN_{0.1}$, and said second film is composed of Ta_2N.

5. A multi-layered wiring structure comprising a barrier film which prevents diffusion of copper from a copper wiring layer formed on a semiconductor substrate,

said barrier film having a multi-layered structure of first and second films,

said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film in direct contact with said second film,

said first film containing nitrogen in a smaller content than that of said second film.

6. The multi-layered wiring structure as set forth in claim **5**, wherein said second film has a thickness in the range of 80 angstroms to 150 angstroms both inclusive.

7. The multi-layered wiring structure as set forth in claim **5**, wherein said first film has a thickness in the range of 60 angstroms to 300 angstroms both inclusive.

8. The multi-layered wiring structure as set forth in claim **5**, wherein said barrier film covers a recess and a hole formed throughout an insulating film formed on an underlying wiring layer.

9. The multi-layered wiring structure as set forth in claim **5**, further comprising a copper film formed on said first film.

10. The multi-layered wiring structure as set forth in claim **5**, wherein said first film is composed of β-Ta and $TaN_{0.1}$, and said second film is composed of Ta_2N.

* * * * *

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Masayoshi Tagami, et al.	**Examiner:**	H. Vu
Serial No:	09/596,415	**Art Unit:**	2811
Filed:	June 19, 2000	**Docket:**	13715
For:	MULTI-LAYERED WIRING LAYER AND METHOD OF FABRICATING THE SAME	**Dated:**	December 20, 2001

#7/9 2-2-02 Payton

Assistant Commissioner for Patents
United States Patent and Trademark Office
Washington, D.C. 20231

RESPONSE UNDER 37 C.F.R. § 1.111

Sir:

In response to the official Office Action dated September 25, 2001, the applicant respectfully presents the following Amendment and Remarks as set forth herein below.

IN THE CLAIMS:

Please cancel claims 2 and 6.

Subt B1

Please amend claim 1 to read as follows:

a1

1. (Amended) A barrier film preventing diffusion of copper from a copper wiring layer formed on a semiconductor substrate, comprising a multi-layered structure of first and second films,

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on December 20, 2001.

Dated: December 20, 2001

Mishelle Mustafa

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said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film containing nitrogen in a smaller content than that of said second film.

Please amend claim 5 to read as follows:

5. (Amended) A multi-layered wiring structure comprising a barrier film which prevents diffusion of copper from a copper wiring layer formed on a semiconductor substrate,

said barrier film having a multi-layered structure of first and second films,

said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film containing nitrogen in a smaller content than that of said second film.

Please add the following new claims 37 and 38.

~~37~~ 4. (New) The barrier film as set forth in claim 1, wherein said first film is composed of β -Ta and $TaN_{0.1}$, and said second film is composed of Ta_2N.

~~38~~ 10. (New) The multi-layered wiring structure as set forth in claim 5, wherein said first film is composed of β -Ta and $TaN_{0.1}$, and said second film is composed of Ta_2N.

REMARKS

Reconsideration of this application based on the foregoing Amendment and the following Remarks is respectfully requested.

The Examiner has acknowledged the applicant's election of Group I, claims 1-10, in the applicant's Response to a Requirement for Restriction of July 5, 2001. Claims 11-36 are withdrawn from consideration pursuant to 37 C.F.R. § 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. The Examiner has treated the election as an election without traverse, in that the election was made without traverse in the applicant's July 5, 2001 response.

Claims 1-3, 5-7 and 10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Vitkavage et al. (U.S. 5,858,873) and claims 4, 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Vitkavage et al.

In response, the applicants have amended claims 1 and 5 to recite that the first film is formed on the second film, the first film containing nitrogen in a smaller content than that of the second film. The applicants have added new claims 37 and 38 which recite that the first film is composed of β –Ta and $TaN_{0.1}$ and the second film is composed of Ta_2N. Support for the amendment to claims 1 and 5 and the addition of new claims 37 and 38 is provided in the specification on page 23, line 20, to page 30, line 1, of the application. No new matter has been added.

Vitkavage et al. discloses in column 4, lines 1-12, that the first layer 14 is comprised of a refractory material such as refractory nitride, carbide or boronide. For instance, the first layer 14 is comprised of TiN, TiC or TiB. The adhesion or second layer 12 is comprised of a metal such as Ti, Ta, Zr, Hf or W. The first layer 14 is formed on the

second layer 12. In a typical case in the cited reference, the first layer 14 is composed of TiN is formed on the second layer 12 composed of Ti. Herein, the first layer 14 contains nitrogen in a *higher* content than that of the second layer 12.

In contrast, in the present invention, claims 1 and 5, as amended, and the corresponding new dependent claims 37 and 38, recite that the first film 16 in the present invention is comprised of a crystalline metal film containing nitrogen therein. For instance, the first film 16 is composed of $TaN_{0.1}$ which is called nitrogen-containing α -Ta, or a combination of $TaN_{0.1}$ and β -Ta. The second film 15 in the present invention is comprised of an amorphous metal nitride film. For instance, the second film 15 is composed of Ta_2N. That is, the first film 16 is composed of crystalline metal containing nitrogen at 10% or smaller, and the second film 15 is composed of amorphous metal nitride containing nitrogen at about 30%. The first layer 16 contains nitrogen in a *smaller content* than that of the second film 15, which is structurally different from the cited reference.

In addition, in the present invention of amended claims 1 and 5, the copper film 18 makes contact with the first film 16 beneath which the second film 16 is formed. As illustrated in Fig. 9, the first film 16 composed of nitrogen-containing crystalline metal has a smaller resistivity that that of a Ta film containing no nitrogen. Hence, the first film is formed of not a pure-metal film, but a nitrogen-containing crystalline metal film.

Therefore, the applicants respectfully maintain that the present invention of amended claims 1 and 5, and new claims 37 and 38 patentably distinguish over Vitkavage et al and that the claims are not anticipated by Vitkavage et al. under 35 U.S.C. § 102(b). Claim 3 stands together with claim 1 and claims 7 and 10 stand together with claim 5.

With regard to the rejections of claims 4, 8 and 9 under 35 U.S.C. § 103(a), the applicants respectfully maintain that claim 4 stands together with claim 1, as amended, and claims 8 and 9 stand together with claim 5, as amended.

The foregoing Amendment and Remarks establish the patentable nature of all of the claims under consideration in the application, i.e., claims 1, 3-5, and 7-10. Claims 2 and 6 have been cancelled. No new matter has been added, wherefore, early and favorable reconsideration of the present application and issuance of a Notice of Allowability are respectfully requested.

Respectfully submitted,

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Encl. (Version with Markings to Show Changes Made)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 2 and 6 have been cancelled.

Claim 1 has been amended as follows:

1. (Amended) A barrier film preventing diffusion of copper from a copper wiring layer formed on a semiconductor substrate, comprising a multi-layered structure of first and second films,

said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film containing nitrogen in a smaller content than that of said second film.

Claim 5 has been amended as follows:

5. (Amended) A multi-layered wiring structure comprising a barrier film which prevents diffusion of copper from a copper wiring layer formed on a semiconductor substrate,

said barrier film having a multi-layered structure of first and second films,

said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film containing nitrogen in a smaller content than that of said second film.

New claims 37 and 38 have been added as follows:

37. (New) The barrier film as set forth in claim 1, wherein said first film is composed of β -Ta and $TaN_{0.1}$, and said second film is composed of Ta_2N.

38. (New) The multi-layered wiring structure as set forth in claim 5, wherein said first film is composed of β -Ta and $TaN_{0.1}$, and said second film is composed of Ta_2N.

#9/response 6-25-02 JD

RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2811

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Masayoshi Tagami, et al.	**Examiner:**	H. Vu
Serial No.:	09/596,415	**Art Unit:**	2811
Filed:	June 19, 2000	**Docket:**	13715
For:	MULTI-LAYERED WIRING LAYER AND METHOD OF FABRICATING THE SAME	**Dated:**	June 4, 2002

Assistant Commissioner for Patents
United States Patent and Trademark Office
Washington, D.C. 20231

RESPONSE AFTER FINAL REJECTION UNDER 37 C.F.R. § 1.116

Sir:

In response to the Final Office Action dated April 4, 2002, the applicant respectfully requests consideration of the following Remarks in the above-identified case:

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on June 4, 2002.

Dated: June 4, 2002

Mishelle Mustafa

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REMARKS

This response is submitted in response to the Final Office Action dated April 4, 2002 and respectfully requests that the Examiner reconsider the rejection of the claims as set forth therein.

The Examiner objects to claims 37 and 38 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Examiner has considered the applicants' arguments with respect to claims 1 and 5 but the Examiner considers the arguments moot in view of new grounds of rejection.

The Examiner has rejected claims 1, 3-5 and 7-10 under 35 U.S.C. 102(b) as being anticipated by Hong et al. (U.S. 5,668,411 – filed July 23, 1996 – issued September 16, 1997).

Hong et al is a new reference cited by the Examiner. In the first Office Action, the Examiner cited Vitkavage et al. (U.S. 5,858,873 – filed March 12, 1997 – issued January 12, 1999). The Examiner now asserts that FIGS. 7-10 and Table 1 of Hong et al disclose the limitations of claim 1 of a barrier film preventing diffusion of copper from a copper wiring structure comprising a barrier film which prevents diffusion of copper from a copper wiring layer formed on a semiconductor substrate.

In response, the applicants respectfully maintain with respect to claims 1 and 5 that Hong et al does not disclose the first film being formed on the second film, as recited by claims 1 and 5. Instead, Hong et al, FIGS. 7 and 10 discloses

that there is a seed layer 46 of the diffusion barrier film positioned between the top layer 48 and the bottom layer 44.

Furthermore, the top layer 48 of Hong et al, which corresponds to the first film of the present invention, contains TiN or TiWN. The bottom layer 44 of Hong et al, which corresponds to the second film of the present invention, contains TiN, TiAlN, or TiSiN. Therefore, contrary to the Examiner's assertion, Hong et al does not disclose that the first film contains nitrogen in a smaller content than that of the second film. Instead, in Hong et al, preferably, both the first and second films can be TiN, or both can be TiWN.

Although tungsten has an atomic weight of 183.84 which is greater than the atomic weight of either aluminum or silicon, and the compound TiWN suggested by Hong et al for the top layer or first film does contain nitrogen in a smaller content than that of the bottom layer or second film, Hong et al does not specify that the first layer must contain nitrogen in a smaller content than that of the second layer, as recited by claims 1 and 5.

Therefore, claims 1 and 5, by reciting that the first film is formed on the second film, patentably distinguish over Hong et al. Furthermore, in the best mode described by Hong et al, the nitrogen content of the first and second films are equivalent, being comprised of TiN. Furthermore, Hong et al does not teach or suggest any particular advantage of the first film being comprised of TiWN while the second film is comprised of TiN or TiAlN.

With regard to claims 3-4 and 7-10, in view of the applicants' arguments in favor of claims 1 and 5 as patentably distinguishing over Hong et al, the applicants

respectfully maintain that claims 3-4 and 7-10 also patentably distinguish over Hong et al.

The applicant respectfully requests that the Examiner consider the foregoing Remarks. The foregoing Remarks establish the patentable nature of all of the claims currently in the application, i.e. claims 1, 3-5, and 7-10. Claims 2 and 6 were previously cancelled. Claims 37 and 38 are objected to as being dependent upon a rejection base claim but would be allowable if rewritten in independent form to include all of the limitations of the base claims and any intervening claims. No new issues have been raised, wherefore, early and favorable reconsideration and issuance of a Notice of Allowance are respectfully solicited.

Respectfully submitted,

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09/577,702

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Masayoshi Tagami, et al.	**Examiner:**	H. Vu
Serial No.:	09/596,415	**Art Unit:**	2811
Filed:	June 19, 2000	**Docket:**	13715
For:	MULTI-LAYERED WIRING LAYER AND METHOD OF FABRICATING THE SAME	**Dated:**	August 5, 2002

13/B
FJONES
8-20-02

Assistant Commissioner for Patents
United States Patent and Trademark Office
Washington, D.C. 20231

PRELIMINARY AMENDMENT UNDER 37 C.F.R. § 1.115

Sir:

In response to the Final Office Action dated April 4, 2002, and the Advisory Action of July 2, 2002 issued in response to the applicants' Response After Final Rejection Under 37 CFR 1.116 of June 4, 2002 and the telephonic interview with the applicants' representative, Anthony N. Fresco, on July 29, 2002, the applicants respectfully submit the following Preliminary Amendment in conjunction with the concurrently-filed request for continued examination (RCE):

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on August 5, 2002.

Dated: August 5, 2002

Mishelle Mustafa

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IN THE CLAIMS:

Please amend claim 1 to read as follows:

1. (Twice Amended) A barrier film preventing diffusion of copper from a copper wiring layer formed on a semiconductor substrate, comprising a multi-layered structure of first and second films,

said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film in direct contact with said second film,

said first film containing nitrogen in a smaller content than that of said second film.

Please amend claim 5 to read as follows:

5. (Twice Amended) A multi-layered wiring structure comprising a barrier film which prevents diffusion of copper from a copper wiring layer formed on a semiconductor substrate,

said barrier film having a multi-layered structure of first and second films,

said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

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said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film in direct contact with said second film,

said first film containing nitrogen in a smaller content than that of said second film.

REMARKS

This Preliminary Amendment and the concurrently filed RCE are submitted in response to the Final Office Action dated April 4, 2002 and respectfully requests that the Examiner reconsider the rejection of the claims as set forth therein.

The Examiner objects to claims 37 and 38 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Examiner has considered the applicants' arguments with respect to claims 1 and 5 but the Examiner considers the arguments moot in view of new grounds of rejection.

The Examiner has rejected claims 1, 3-5 and 7-10 under 35 U.S.C. 102(b) as being anticipated by Hong et al. (U.S. 5,668,411 – filed July 23, 1996 – issued September 16, 1997).

Hong et al is a new reference cited by the Examiner. In the first Office Action, the Examiner cited Vitkavage et al. (U.S. 5,858,873 – filed March 12, 1997 – issued January 12, 1999). The Examiner now asserts that FIGS. 7-10 and Table 1

of Hong et al disclose the limitations of claim 1 of a barrier film preventing diffusion of copper from a copper wiring structure comprising a barrier film which prevents diffusion of copper from a copper wiring layer formed on a semiconductor substrate.

In the applicants' June 4, 2002 Response After Final Rejection Under 37 CFR 1.116, the applicants respectfully maintained with respect to claims 1 and 5 that Hong et al does not disclose the first film being formed on the second film, as recited by claims 1 and 5. Instead, Hong et al, FIGS. 7 and 10 discloses that there is a seed layer 46 of the diffusion barrier film positioned between the top layer 48 and the bottom layer 44.

Furthermore, the applicants also argued that the top layer 48 of Hong et al, which corresponds to the first film of the present invention, contains TiN or TiWN. The bottom layer 44 of Hong et al, which corresponds to the second film of the present invention, contains TiN, TiAlN, or TiSiN. Therefore, contrary to the Examiner's assertion, Hong et al does not disclose that the first film contains nitrogen in a smaller content than that of the second film. Instead, in Hong et al, preferably, both the first and second films can be TiN, or both can be TiWN.

Although tungsten has an atomic weight of 183.84 which is greater than the atomic weight of either aluminum or silicon, and the compound TiWN suggested by Hong et al for the top layer or first film does contain nitrogen in a smaller content than that of the bottom layer or second film, Hong et al does not specify that the first layer must contain nitrogen in a smaller content than that of the second layer, as recited by claims 1 and 5.

The applicants argued that, therefore, claims 1 and 5, by reciting that the first film is formed on the second film, patentably distinguish over Hong et al. Furthermore, in the best mode described by Hong et al, the nitrogen content of the first and second films are equivalent, being comprised of TiN. Furthermore, Hong et al does not teach or suggest any particular advantage of the first film being comprised of TiWN while the second film is comprised of TiN or TiAlN.

In the Advisory Action of July 2, 2002, the Examiner rejected the foregoing arguments, asserting that Hong et al discloses forming a first film (48) containing nitrogen (TiWN, TiAlN, TiSiN or TaSiN) in a smaller content than that of the second film (44) which is TiN or TaN. The Examiner's position further is that Hong et al also discloses forming the first film (48) on the second film (44). The Examiner noted however that the claimed language does not state whether the first film is formed on and in direct contact with the second film.

In response, in a facsimile sent on July 25, 2002 to the Examiner, the applicants proposed amendments to claims 1 and 5 to recite "said first film in direct contact with said second film,".

In a telephonic interview with the Examiner on July 29, 2002, based on the proposed amendments to claims 1 and 5 sent by facsimile, the Examiner indicated to the applicants' representative, Anthony N. Fresco, that the proposed amendment to claims 1 and 5 requires further search and consideration, and that a RCE would be required. Therefore, the applicants are herein submitting this Preliminary Amendment Under 37 CFR 1.115 in conjunction with the

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 1 has been amended as follows:

1. (Twice Amended) A barrier film preventing diffusion of copper from a copper wiring layer formed on a semiconductor substrate, comprising a multi-layered structure of first and second films,

said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film in direct contact with said second film,

said first film containing nitrogen in a smaller content than that of said second film.

Claim 5 has been amended as follows:

5. (Twice Amended) A multi-layered wiring structure comprising a barrier film which prevents diffusion of copper from a copper wiring layer formed on a semiconductor substrate,

said barrier film having a multi-layered structure of first and second films,

said first film being composed of crystalline metal containing nitrogen therein,

said second film being composed of amorphous metal nitride,

concurrently filed RCE to enter the amendments to claims 1 and 5 to recite "said first film in direct contact with said second film,". No new matter has been added.

With regard to claims 3-4 and 7-10, in view of the applicants' amendments to claims 1 and 5, which the applicants respectfully maintain establish claims 1 and 5 as patentably distinguishing over Hong et al, the applicants maintain that claims 3-4 and 7-10 also patentably distinguish over Hong et al.

The foregoing Remarks establish the patentable nature of all of the claims currently in the application, i.e. claims 1, 3-5, and 7-10 and 37-38. Claims 2 and 6 were previously cancelled. Claims 37 and 38 are objected to as being dependent upon a rejection base claim but would be allowable if rewritten in independent form to include all of the limitations of the base claims and any intervening claims. No matter has been added and no new issues have been raised, wherefore, early and favorable reconsideration and issuance of a Notice of Allowance are respectfully solicited.

Respectfully submitted,

Anthony N. Fresco

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Registration No.: 45,784

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ANF:yd

Enclosure: Version with Markings to Show Changes Made

said barrier film being constituted of common metal atomic species,

said first film being formed on said second film,

said first film in direct contact with said second film,

said first film containing nitrogen in a smaller content than that of said second film.

Notice of Allowability	Application No.	Applicant(s)	
	09/596,415	TAGAMI ET AL.	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/5/02*.
2. ☒ The allowed claim(s) is/are *1,3-5,7-10,37 and 38*.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☒ CORRECTED DRAWINGS must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☒ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☒ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (PTO-152)
3☒ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____.
5☐ Information Disclosure Statements (PTO-1449), Paper No. ____.
6☒ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other _____

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Examiner's Amendment

1. This application is in condition for allowance except for the presence of claims 11-39 to invention non-elected without traverse. Accordingly, claims 11-36 have been cancelled.

Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance:

Applicants' claims 1, 3-5,7-10 and 37-38 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed invention such as the barrier film preventing diffusion of copper from a copper wiring layer formed on a semiconductor substrate comprising, a multi-layered structure of first and second films, the first film being composed of crystalline metal containing nitrogen therein the second film being composed of amorphous metal nitride, the barrier film being constituted of common metal atomic species, the first film being formed on the second film, the first film in direct contact with the second film, the first film containing nitrogen in a smaller content than that of the second film.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Papers related to this application may be submitted to Technology Center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to ***Hung Vu*** whose telephone number is **(703) 308-4079**. The Examiner is in the Office generally between the hours of 7:00 AM to 5:30 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ***Tom Thomas***, can be reached on **(703) 308-2772**.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **(703) 308-0956**.

Vu

September 6, 2002

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

ANSI/IEEE Std 100-1988

IEEE Standard Dictionary of Electrical and Electronics Terms