
EXHIBIT H

(12) **United States Patent**
Ikoma et al.

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(45) **Date of Patent:** **Oct. 9, 2007**

(54) **SEMICONDUCTOR DEVICE**

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(73) Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 270 days.

* cited by examiner

Primary Examiner—Phat X. Cao

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(21) Appl. No.: **11/148,208**

(22) Filed: **Jun. 9, 2005**

(57) **ABSTRACT**

(65) **Prior Publication Data**

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A semiconductor device includes a semiconductor substrate; a diffusion region which is formed in the semiconductor substrate and serves as a region for the formation of a MIS transistor; an element isolation region surrounding the diffusion region; at least one gate conductor film which is formed across the diffusion region and the element isolation region, includes a gate electrode part located on the diffusion region and a gate interconnect part located on the element isolation region, and has a constant dimension in the gate length direction; and an interlayer insulating film covering the gate electrode. The semiconductor device further includes a gate contact which passes through the interlayer insulating film, is connected to the gate interconnect part, and has the dimension in the gate length direction larger than the gate interconnect part.

(30) **Foreign Application Priority Data**

Jul. 22, 2004 (JP) 2004-213903

(51) **Int. Cl.**

H01L 27/10 (2006.01)

(52) **U.S. Cl.** **257/204**; 257/206; 257/369; 257/E27.064

(58) **Field of Classification Search** 257/204, 257/206, 202, 369, E27.064

See application file for complete search history.

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11 Claims, 7 Drawing Sheets

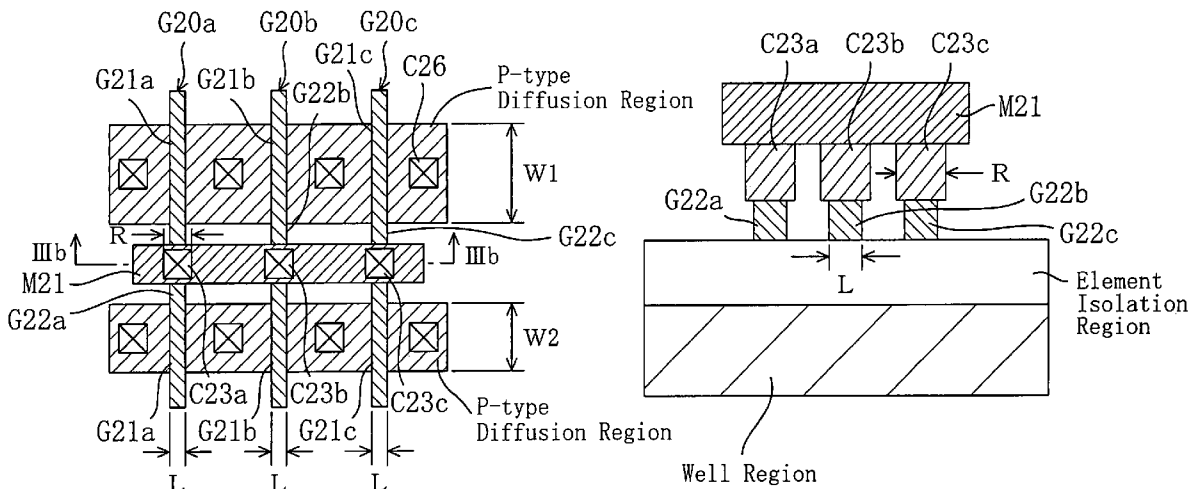


FIG. 1B

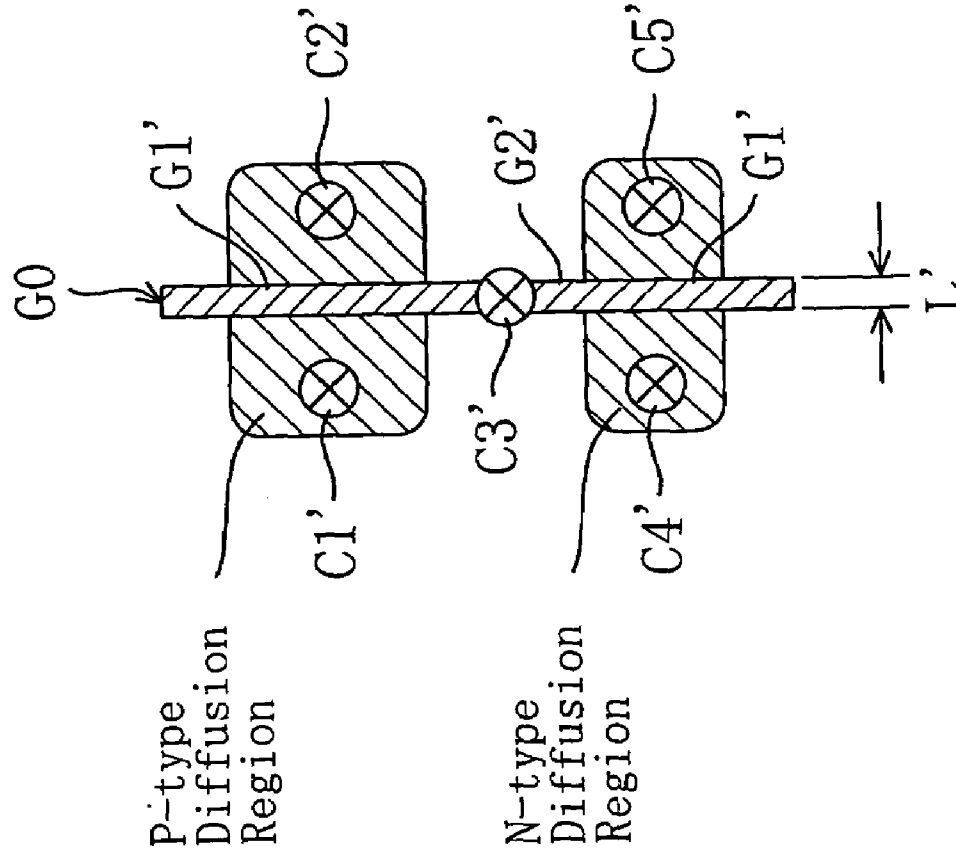
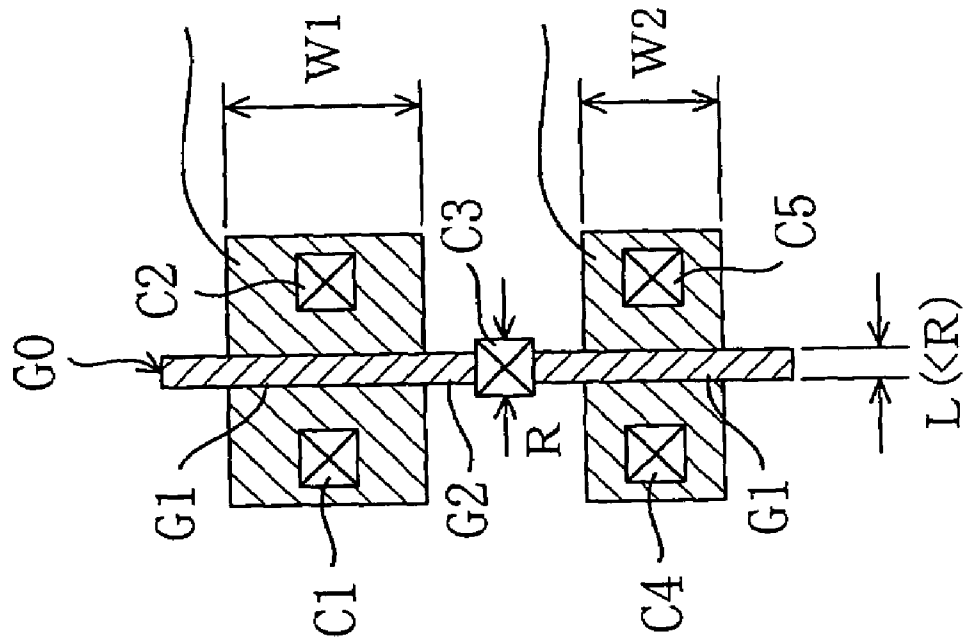


FIG. 1A



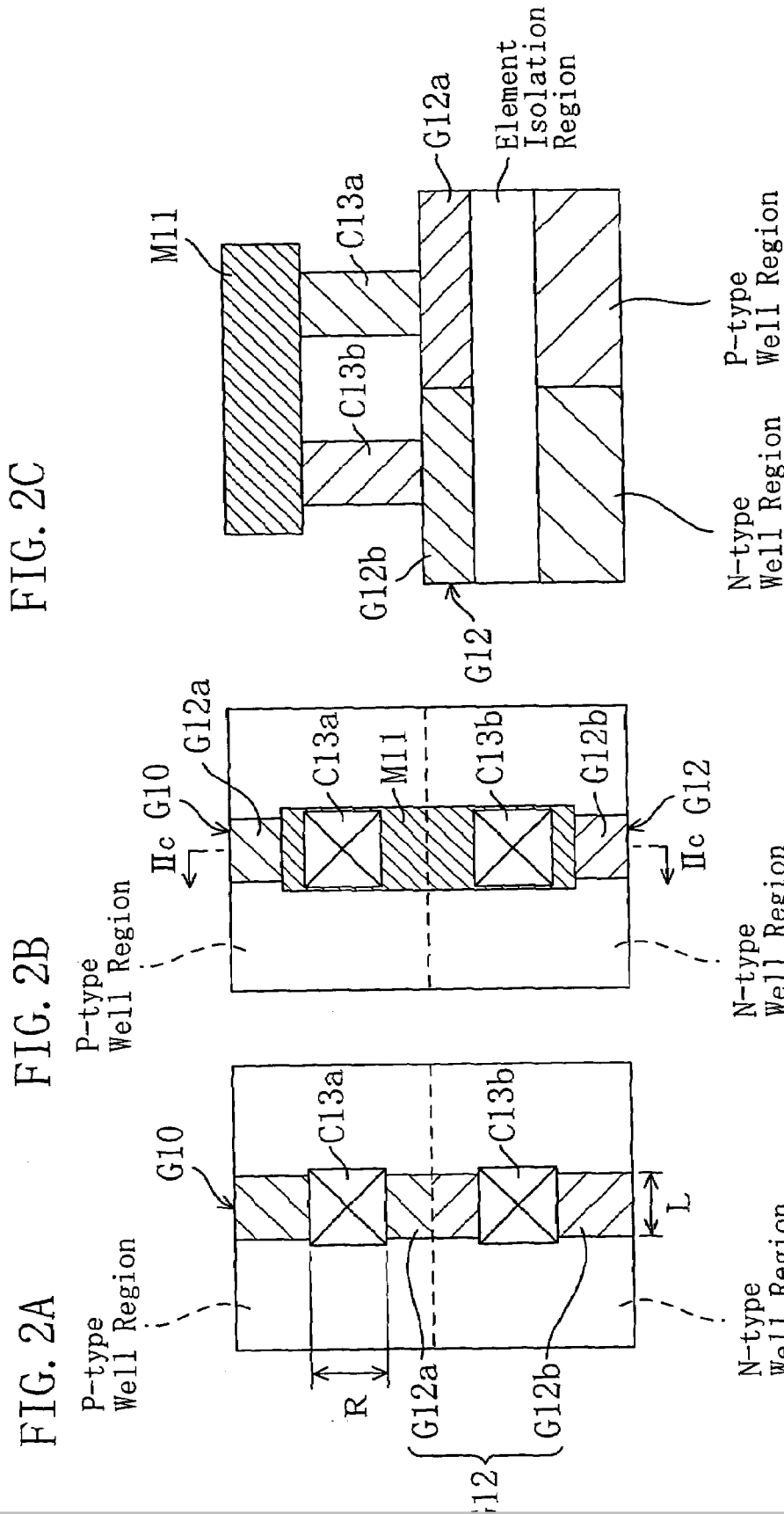


FIG. 3B

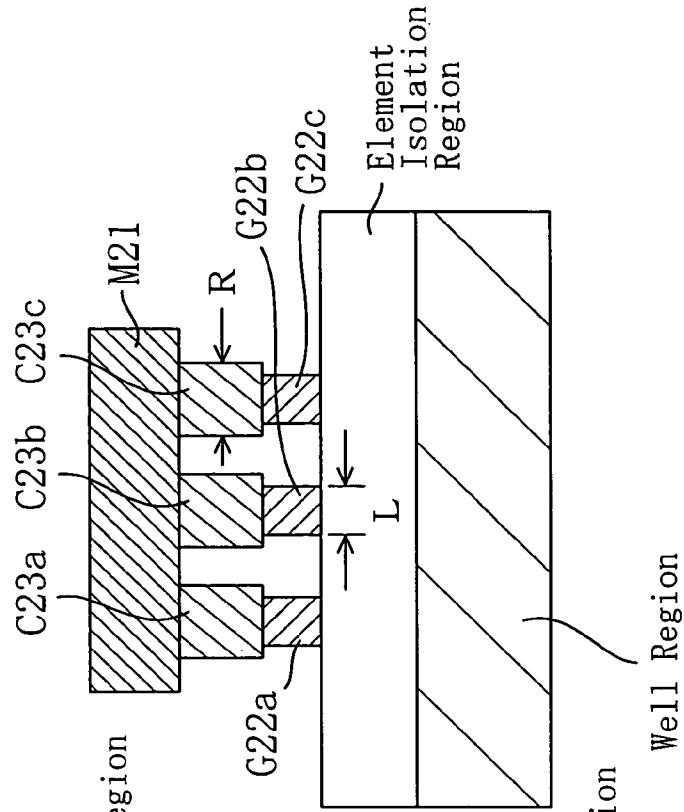
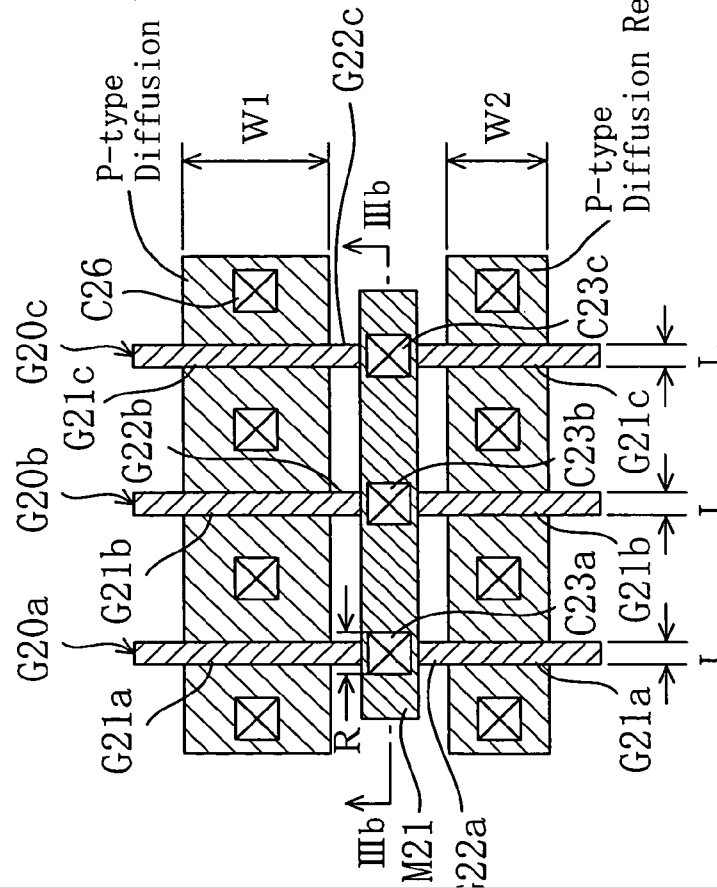


FIG. 3A



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