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**EXHIBIT B**

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US006794677B2

(12) **United States Patent**  
**Tamaki et al.**

(10) **Patent No.:** **US 6,794,677 B2**  
 (45) **Date of Patent:** **Sep. 21, 2004**

(54) **SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD FOR FABRICATING THE SAME**

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(73) Assignee: **Matsushita Electric Industrial Co., Ltd., Osaka (JP)**

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 168 days.

(21) Appl. No.: **09/964,868**

(22) Filed: **Sep. 28, 2001**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

Oct. 2, 2000 (JP) ..... 2000-302277

(51) Int. Cl.<sup>7</sup> ..... **H01L 29/06; H01L 31/0352**

(52) U.S. Cl. .... **257/41; 257/2; 257/390; 257/401**

(58) Field of Search ..... **257/41, 2, 202-211, 257/390, 401**

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(57) **ABSTRACT**

Variations in the size of a linear pattern resulting from difference in mask pattern layout are prevented by setting the perimeter of the linear pattern per unit area in a specified range irrespective of the type of a semiconductor integrated circuit device or by adjusting a process condition in accordance with type-to-type difference in the perimeter of the linear pattern per unit area.

**6 Claims, 9 Drawing Sheets**

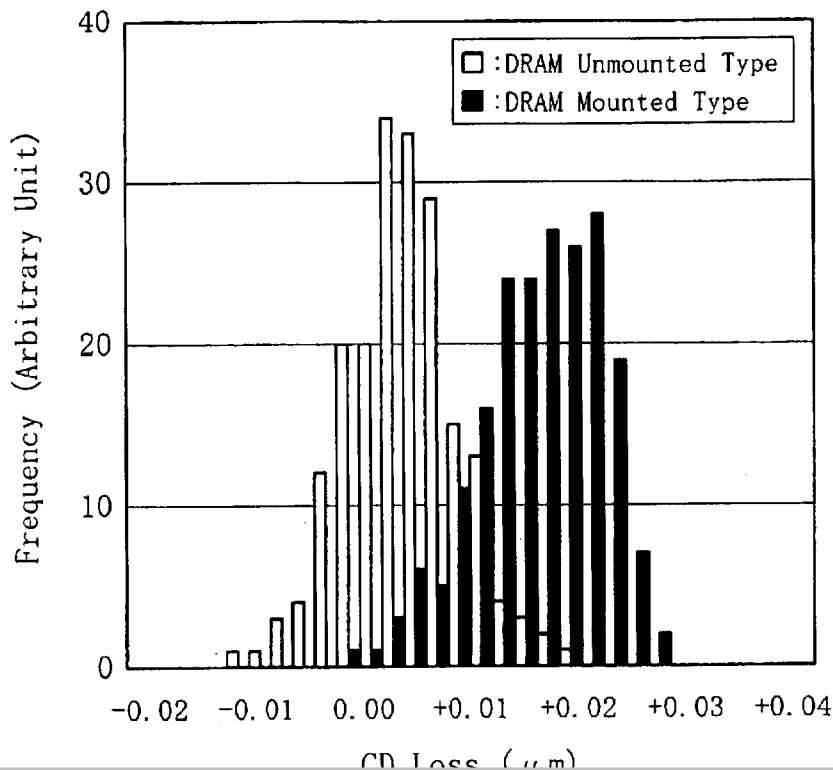


FIG. 1

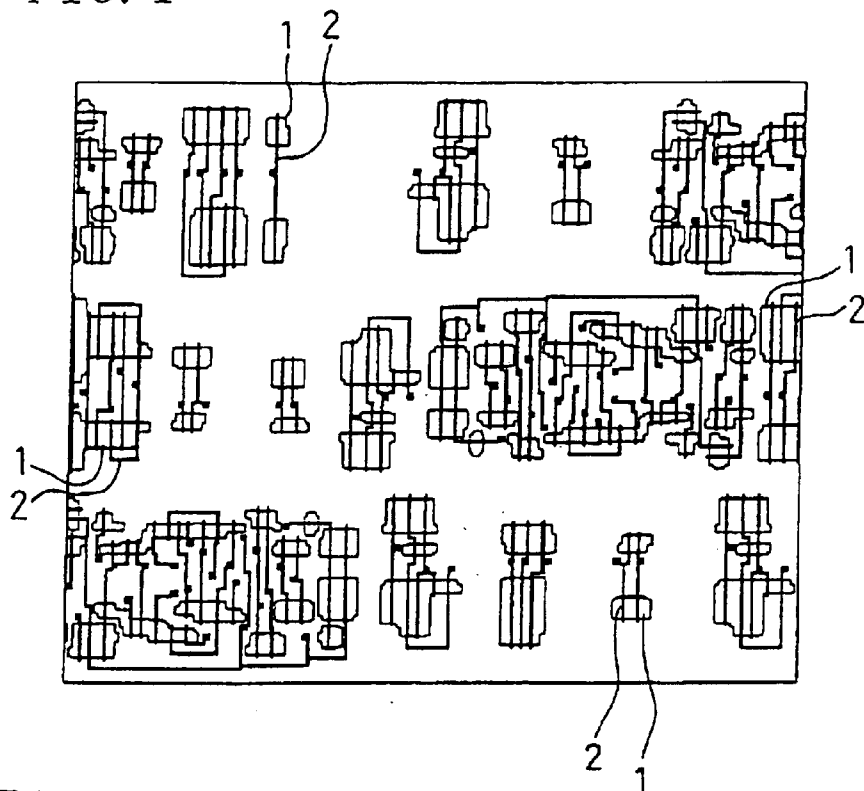


FIG. 2

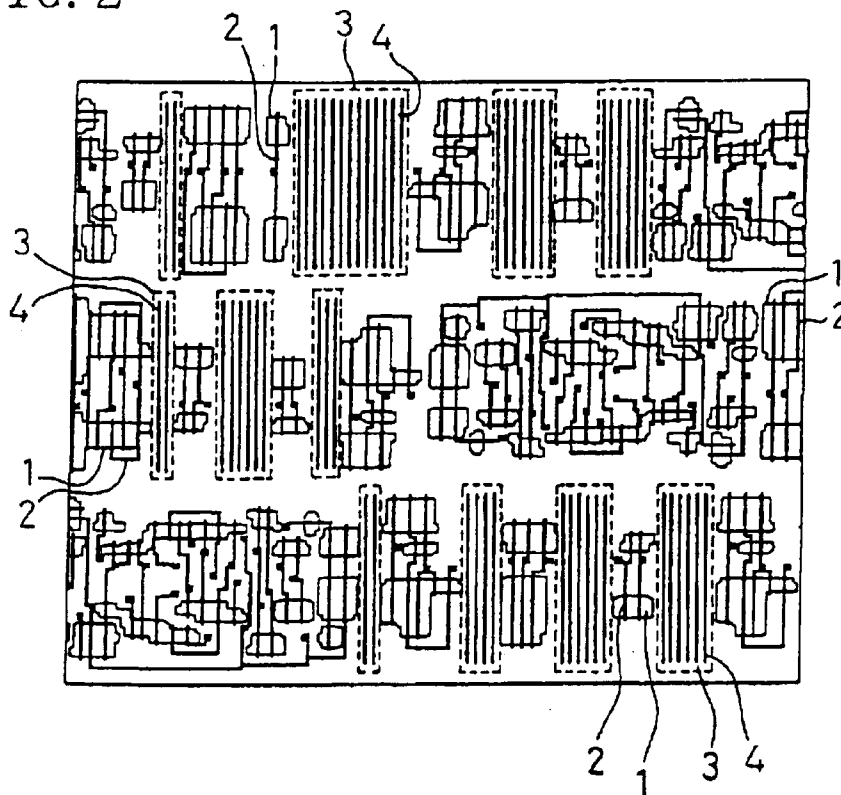


FIG. 3A

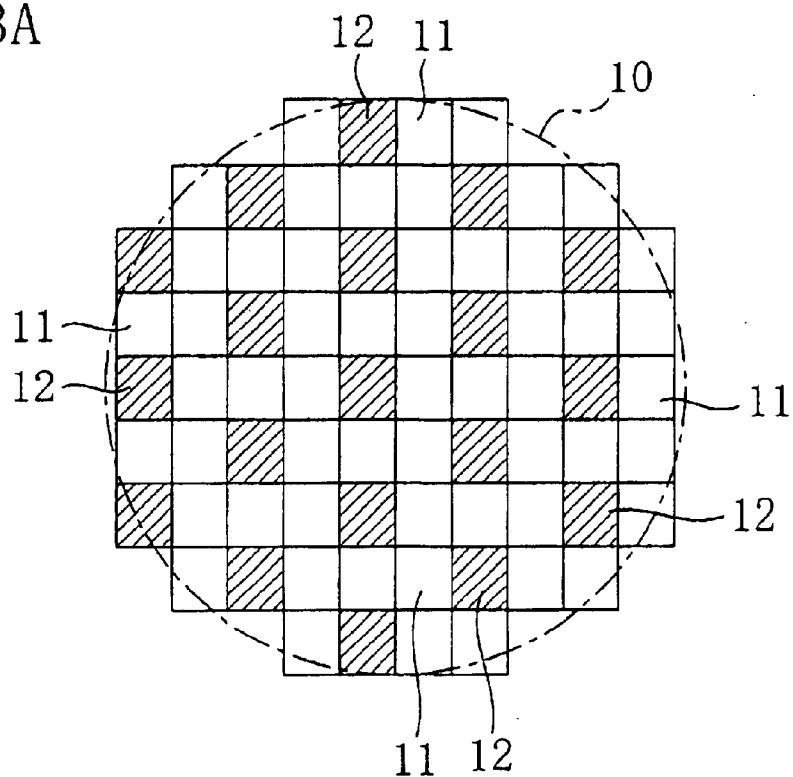


FIG. 3B

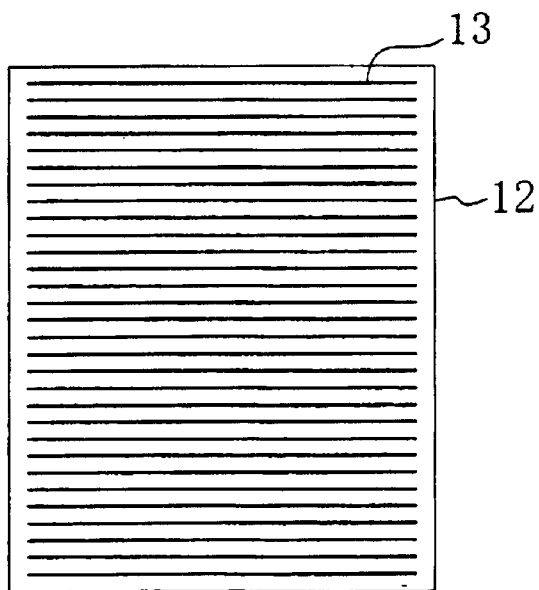
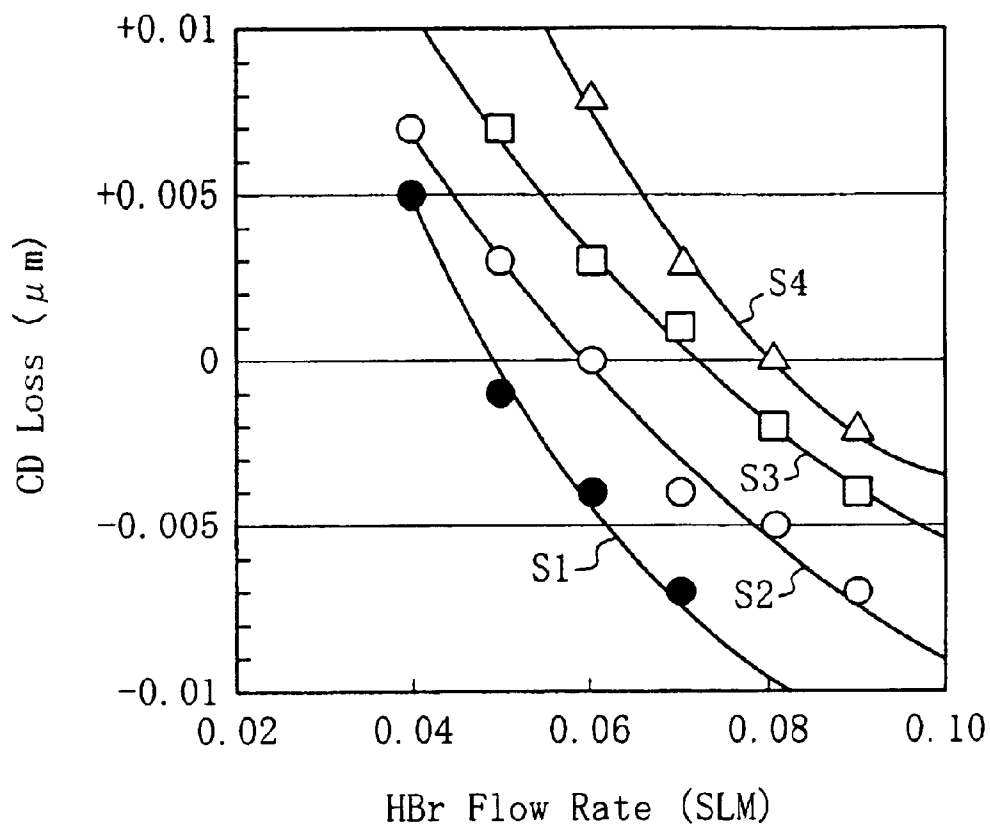


FIG. 4



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