EXHIBIT P

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- 1. A solid state imaging apparatus comprising:
- (A) a plurality of photodiodes arranged in an array;
- (B) a plurality of floating diffusion sections each being connected to ones of the photodiodes via each of
- (C) a plurality of transfer transistors;
- (D) a plurality of read-out lines each being selectively connected to at least two of the transfer transistors;
- (E) a plurality of reset transistors each being connected to one of the plurality of floating diffusion sections;
- (X) a plurality of reset pulse lines each being connected to at least one of the plurality of reset transistors; and
- (F) a plurality of pixel amplifier transistors each detecting and outputting the potential of each said floating diffusion wherein (A) the plurality of photodiodes includes (a1) a first photodiode, (a2) a second photodiode and (a3) a third
- (a1) the first photodiode is in row n, where n is a positive integer,
- (a2) the second photodiode is in row n+1,
- (a3) the third photodiode is in row n+2,
- (D) the plurality of read-out lines includes (d1) a first read-out line and (d2) a second read-out line,
- (d1) the first read-out line and (d2) the second read-out line are disposed between the row n and the row n+1,
- (x1) one of the (X) plurality of reset pulse lines is disposed between the row n+1 and the row n+2,
- (f1) one of the (F) plurality of pixel amplifier transistors is disposed between the row n+1 and the row n+2.



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Pixel Circuit Diagram

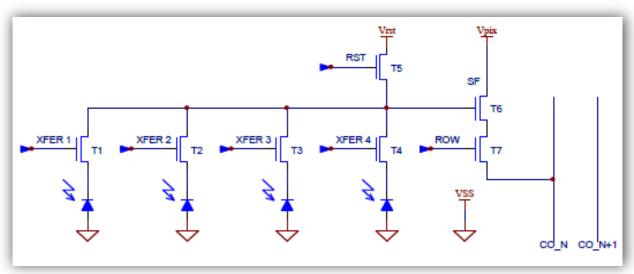
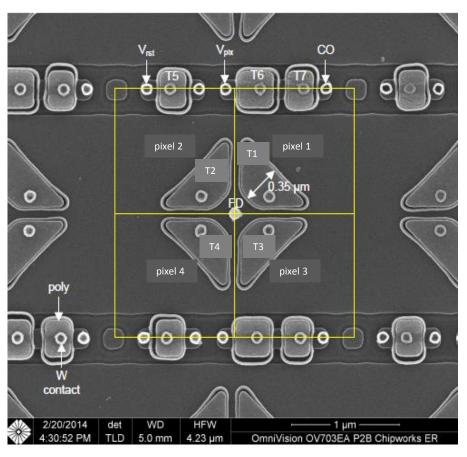


Figure 4.1.1 Shared Pixel Schematic

The shared pixel schematic for the four-shared pixel architecture is shown in Figure 4.1.1. I four photodiodes output through the transfer transistors (T1 – T4) to a common floating diffu (FD).



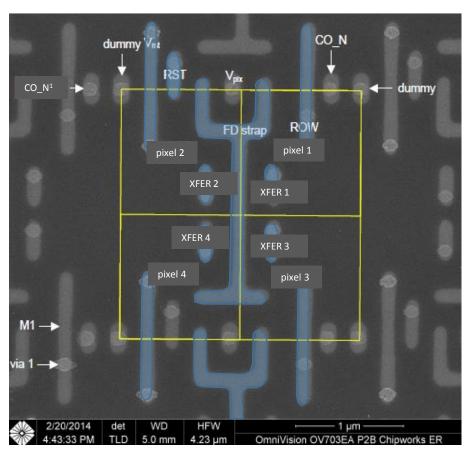
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Shared Pixels at Contact/Poly - SEM



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