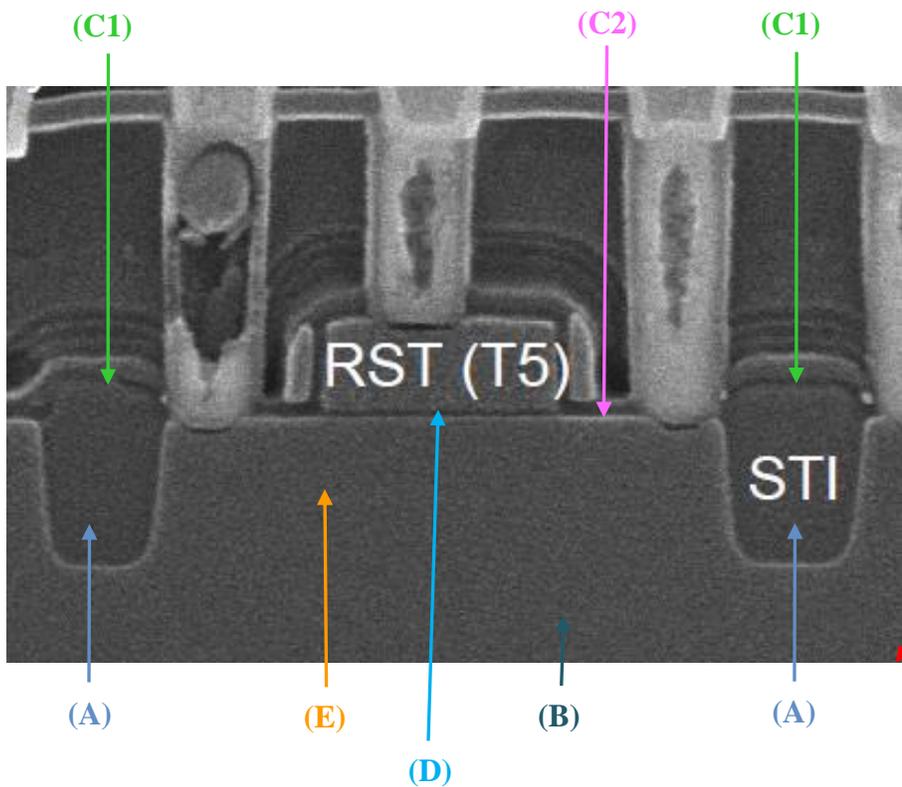

EXHIBIT M

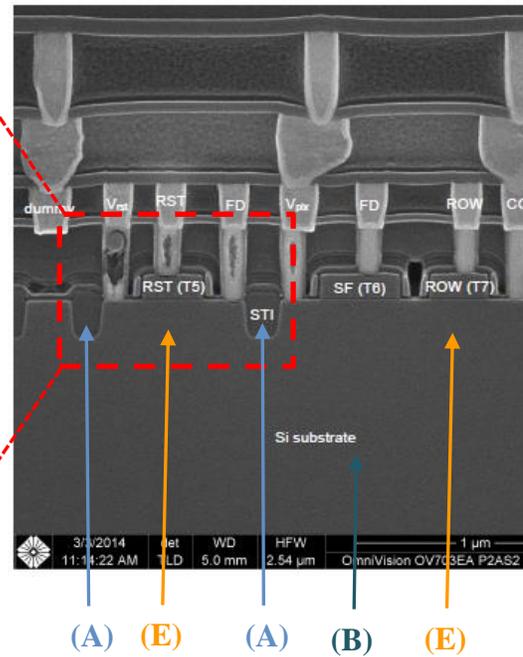
12. A method of manufacturing a semiconductor device comprising:
a first step of forming **(A) a trench isolation** on **(B) [a] semiconductor substrate**, the trench isolation having **(C1) a top surface** higher level than **(C2) a surface** of the semiconductor substrate;
a second step of forming **(D) a gate insulating film** on **(E) an active area** surrounded by the trench isolation on the semiconductor substrate;
a third step of forming **(F) a gate electrode** on the gate insulating film;
after the third step, a fourth step of forming **(X) an insulating film** on the substrate;
a fifth step of anisotropically etching the insulating film so as to form **(X1) first sidewalls** on both side surfaces of the gate electrode and form **(X2) second sidewalls** on a side surface of a step portion in the boundary between the trench isolation and the gate electrode;
after the fifth step, a sixth step of forming **(G) a laminated film** made of **(G1) a silicon oxide film** and **(G2) a silicon nitride film** on the entire top surface of the substrate;
a seventh step of forming **(H) an interlayer insulating film** on the silicon nitride film;
an eighth step of forming **(I) a hole** by selectively removing the interlayer insulating film and the laminated film; and
a ninth step of forming **(J) a buried conductive layer** by filling the hole with a conductive material.

Claim 12

A method of manufacturing a semiconductor device comprising: a first step of forming (A) a trench isolation on (B) a semiconductor substrate, the trench isolation having (C1) a top surface at a higher level than (C2) a surface of the semiconductor substrate; a second step of forming (D) a gate insulating film on (E) an active area surrounded by the trench isolation on the semiconductor substrate;

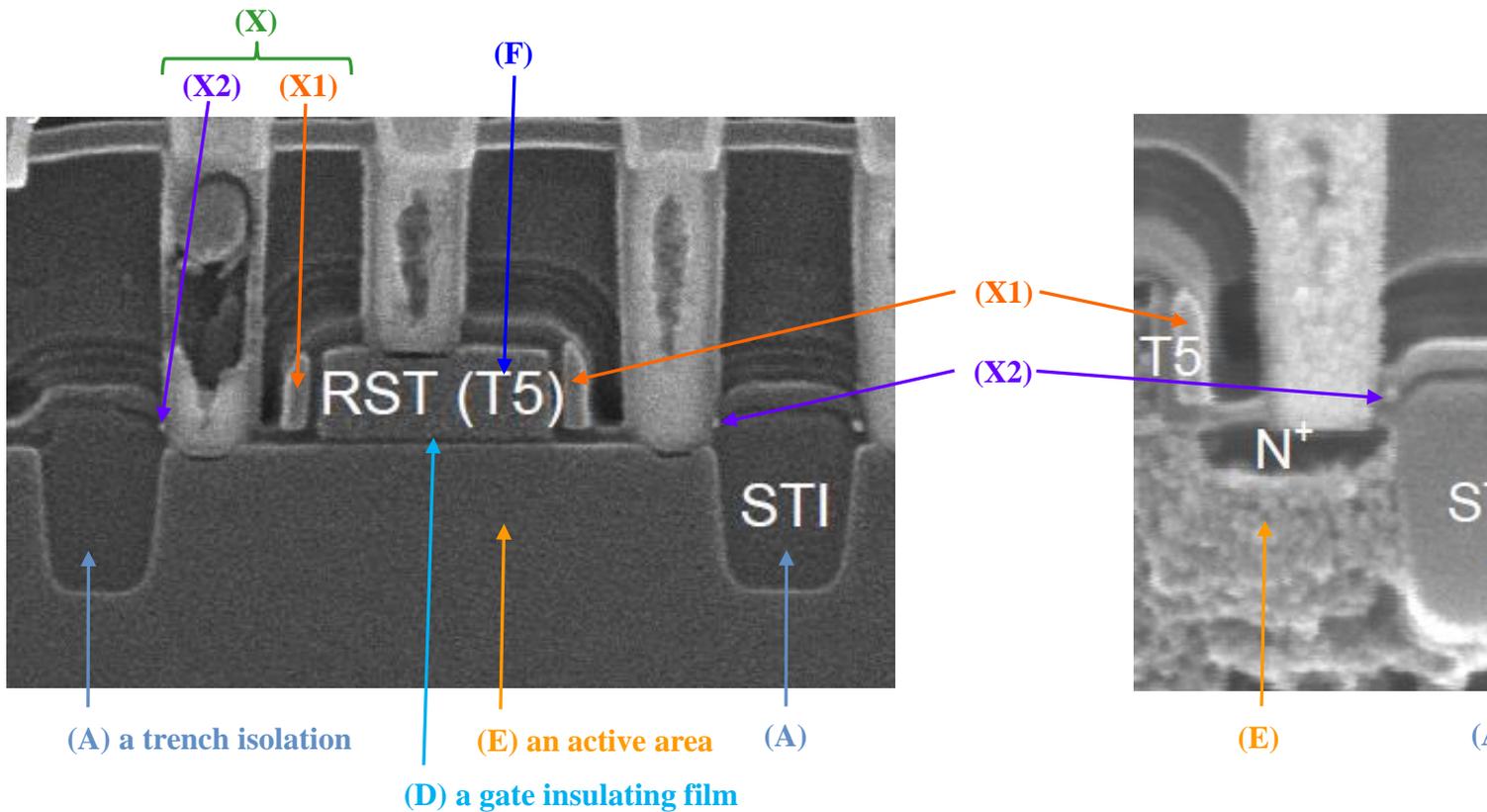


(Cross section: gate length direction)



Claim 12

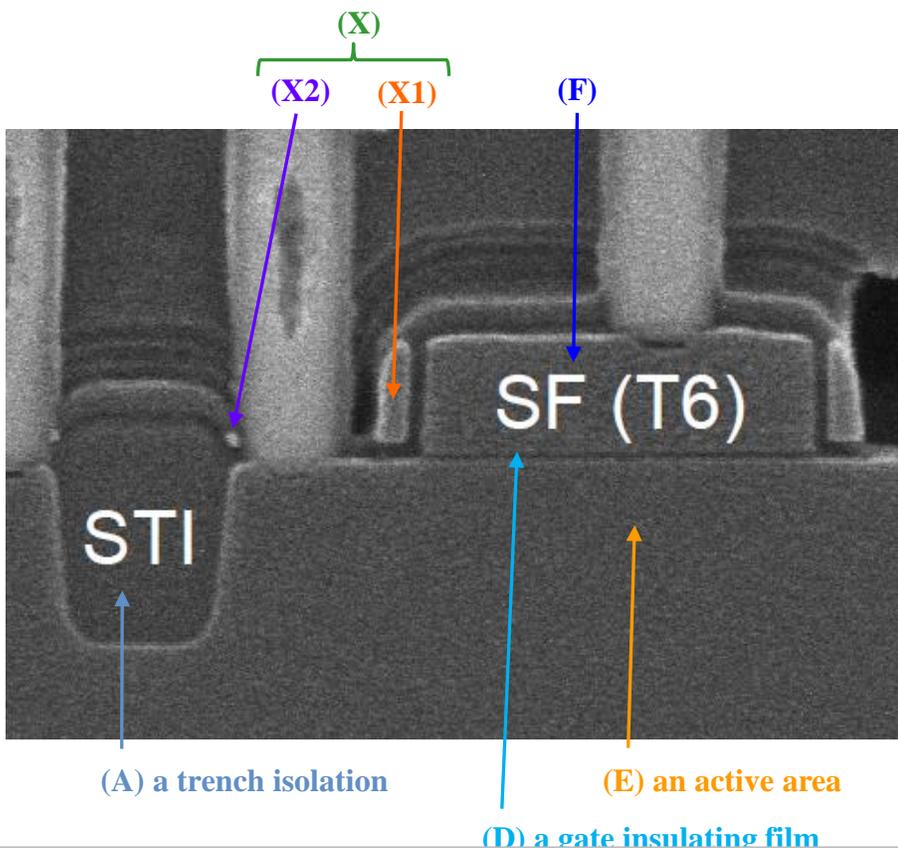
a third step of forming **(F) a gate electrode** on the gate insulating film; after the third step, a fourth step of forming **(X) film** on the substrate; a fifth step of anisotropically etching the insulating film so as to form **(X1) first sidewalls** on both of the gate electrode and form **(X2) second sidewalls** on a side surface of a step portion in the boundary between the trench and the active area; and



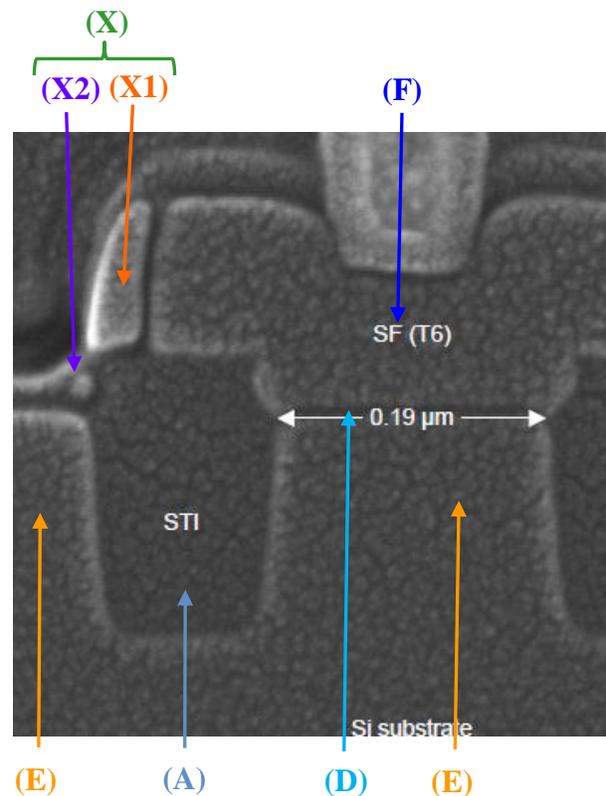
Claim 12

a third step of forming **(F) a gate electrode** on the gate insulating film; after the third step, a fourth step of forming **(X) film** on the substrate; a fifth step of anisotropically etching the insulating film so as to form **(X1) first sidewalls** on both of the gate electrode and form **(X2) second sidewalls** on a side surface of a step portion in the boundary between the trench and the active area; and

(source follower (T6): gate length direction)



(source follower (T6): gate width direction)



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