EXHIBIT 1

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(12) **United States Patent**
Leedy

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(54) **THREE DIMENSIONAL STRUCTURE MEMORY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**

H01L 23/48	(2006.01)
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H01L 25/065	(2006.01)
H01L 27/06	(2006.01)
H01L 21/768	(2006.01)
H01L 23/522	(2006.01)
H01L 27/108	(2006.01)
G11C 5/06	(2006.01)

(52) **U.S. Cl.**

CPC ***G11C 5/02*** (2013.01); *H01L 2224/8083* (2013.01); ***H01L 25/0657*** (2013.01); ***H01L 27/0688*** (2013.01); ***H01L 21/76898*** (2013.01); *Y10S 438/977* (2013.01); *H01L 2924/01079* (2013.01); ***H01L 23/5226*** (2013.01); ***H01L 27/10897*** (2013.01); ***H01L 23/481*** (2013.01); ***G11C 5/06*** (2013.01)

USPC **257/777**; 257/778; 257/685; 438/977

(58) **Field of Classification Search**

USPC 257/777–778, 685–686; 365/63, 51, 365/230.06; 438/455, 977, 107, 108

See application file for complete search history.

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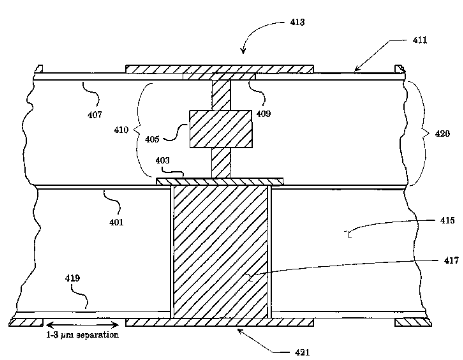
(57) **ABSTRACT**

A Three-Dimensional Structure (3DS) Memory allows for physical separation of the memory circuits and the control logic circuit onto different layers such that each layer may be separately optimized. One control logic circuit suffices for several memory circuits, reducing cost. Fabrication of 3DS memory involves thinning of the memory circuit to less than 50 microns in thickness and bonding the circuit to a circuit stack while still in wafer substrate form. Fine-grain high density inter-layer vertical bus connections are used. The 3DS memory manufacturing method enables several performance and physical size efficiencies, and is implemented with established semiconductor processing techniques.

165 Claims, 9 Drawing Sheets



or a conventional die), or a pattern for conventional insertion interconnect, DCA (Direct Chip Attach) or FCA (Flip-Chip Attach). If another circuit layer is to be bonded to the 3DScircuit stack, steps 1 through 4 are repeated.

6. Perform step 5A or 5B of Method A.

3DS Memory Device Yield Enhancement Methods

The 3DS circuit may be considered a vertically assembled MCM (Multi-Chip Module) and as with an MCM the final yield is the product of the yield probabilities of each component circuit (layer) in the completed 3DS circuit. The 3DS circuit uses several yield enhancement methods that are synergistic in their combined usage within a single memory IC. The yield enhancement methods used in the 3DS memory circuit include small memory array block size, memory array block electrical isolation through physically unique or separate vertical bus interconnections, intra memory array block gate-line sparing, memory array layer sparing (inter-block gate-line sparing), controller sparing and ECC (Error Correcting Codes). The term sparing is used to mean substitution by a redundant element.

The selected size of the memory array block is the first component in the yield equation for the 3DS memory circuit. Each memory array block is individually (uniquely) accessed and powered by the controller circuit and is physically independent of each and every other memory array block including those on the same memory array layer in addition to those on a different memory array layer. The size of the memory array block is typically less than 5 mm^2 and preferably less than 3 mm^2, but is not limited to a specific size. The size of memory array block, the simplicity of its NMOS or PMOS fabrication process and its physical independence from each of the other memory array blocks, for nearly all production IC processes, provides a conservatively stated nominal yield of greater than 99.5%. This yield assumes that most point defects in the memory array block such as open or shorted interconnect lines or failed memory cells can be spared (replaced) from the intra-block or inter-block set of redundant gate-lines. Major defects in a memory array block which render the complete memory array block unusable result in the complete sparing of the block from a redundant memory array layer or the rejection of the 3DS circuit.

In the example of a 3DS DRAM circuit the yield of a stack of memory array blocks is calculated from the yield equation $Ys=((1-(1-PY)2)n)b$, where n is the number DRAM array layers, b is the number of blocks per DRAM array and Py is the effective yield (probability) of a DRAM array block less than 3 mm2 in area. Assuming a DRAM array block redundancy of 4% for gate-lines in the DRAM array block lines and one redundant DRAM array layer, and assuming further that the number of blocks per layer is 64, the number of memory array layers in the stack is 17 and the effective value for Py is 0.995, then the stack yield Ys for the complete memory array (including all memory array block stacks) is 97.47%.

The Ys memory array stack yield is then multiplied by the yield of the controller Yc. Assuming a die size of less than 50 mm^2, a reasonable Yc for a controller fabricated from a 0.5 micron BiCMOS or mixed signal process would be between 65% and 85%, giving a net 3DS memory circuit yield of between 63.4% and 82.8%. If a redundant controller circuit layer is added to the 3DS memory stack, the yield probabilities would be between 85.7% and 95.2%.

The effective yield of a memory array block can be further increased by the optional use of ECC logic. ECC logic corrects data bit errors for some group size of data bits. The syndrome bits necessary for the operation of ECC logic

necessary, in order to accommodate the storage of ECC syndrome bits, additional memory array layers could be added to the circuit.

Advantageous 3DS Memory Device Controller Capabilities

As compared to a conventional memory circuit, the 3DS memory controller circuit can have various advantageous capabilities due the additional area available for controller circuitry and the availability of various mixed signal process fabrication technologies. Some of these capabilities are self-test of memory cells with dynamic gate-line address assignment, virtual address translation, programmable address windowing or mapping, ECC, data compression and multi-level storage.

Dynamic gate-line address assignment is the use of programmable gates to enable the layer and gate-line for a read/write operation. This allows the physical order of memory storage to be separate or different from the logical order of stored memory.

The testing of each generation of memory devices has resulted in significantly increased test costs. The 3DS memory controller reduces the cost of testing by incorporating sufficient control logic to perform an internal test (self-test) of the various memory array blocks. Circuit testing in the conventional ATE manner is required only for verification of controller circuit functions. The scope of the internal test is further extended to the programmable (dynamic) assignment of unique addresses corresponding to the various gate-lines of each memory array block on each layer. Self-test capability of the 3DS controller circuit can be used anytime during the life of the 3DS memory circuit as a diagnostic tool and as a means to increase circuit reliability by reconfiguring (sparing) the addresses of gate-lines that fail after the 3DS memory circuit is in use in a product.

ECC is a circuit capability that, if included in the controller circuit, can be enabled or disabled by a programming signal or made a dedicated function.

Data compression logic will allow the total amount of data that can be stored in the 3DS memory array to be increased. There are various generally known data compression methods available for this purpose.

Larger sense amps allow greater dynamic performance and enable higher speed read operations from the memory cells. Larger sense amps are expected to provide the capability to store more than one bit (multi-level storage) of information in each memory cell; this capability has already been demonstrated in non-volatile memory circuits such as flash EPROM. Multi-level storage has also been proposed for use in the 4 Gbit DRAM generation circuits.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.

The invention claimed is:

1. A thin and substantially flexible structure comprising:

a thin, substantially flexible monocrystalline semiconductor layer of one piece; and

a silicon-based dielectric layer formed on the thin semi-

2. The thin and substantially flexible structure of claim **1**, further comprising:

a vertical interconnect conductor extending vertically through the thin semiconductor layer; and

a vertical silicon-based dielectric insulator extending vertically through the thin semiconductor layer and around the interconnect conductor and having a stress of less than 5×10^8 dynes/cm^2 tensile.

3. The thin and substantially flexible structure of claim **2**, wherein:

the thin semiconductor layer comprises vertical holes etched therethrough; and

the vertical interconnect conductor and the vertical silicon-based dielectric insulator are formed in one of the vertical holes of the thin semiconductor layer.

4. The thin and substantially flexible structure of claim **2**, wherein the thin semiconductor layer is formed from a semiconductor wafer.

5. The thin and substantially flexible structure of claim **2**, wherein the thin semiconductor layer has a thickness of 50 microns or less.

6. The thin and substantially flexible structure of claim **4**, wherein the semiconductor wafer comprises monocrystalline silicon, and the thin semiconductor layer comprises monocrystalline silicon formed from the semiconductor wafer.

7. The thin and substantially flexible structure of claim **2**, wherein the thin semiconductor layer is unitary.

8. The thin and substantially flexible structure of claim **2**, wherein the thin semiconductor layer extends from edge to edge of the dielectric layer.

9. The thin and substantially flexible structure of claim **8**, wherein the dielectric layer extends from edge to edge of the thin semiconductor layer.

10. The thin and substantially flexible structure of claim **1**, wherein the thin semiconductor layer comprises a polished surface formed by removing semiconductor material during thinning of the thin semiconductor layer to expose a surface thereof and then polishing the exposed surface, wherein the thin semiconductor layer is substantially flexible based on being thinned and having the polished surface.

11. The thin and substantially flexible structure of claim **2**, further comprising:

a bottomside surface and a topside surface;

a contact formed on the bottomside surface and electrically connected to the vertical interconnect conductor; and

an interconnect, contact or circuit formed on or near the topside surface and electrically connected to the vertical interconnect conductor;

wherein the interconnect, contact or circuit is electrically connected to the contact on the bottomside surface via the vertical interconnect.

12. A thin and substantially flexible circuit comprising:

a thin monocrystalline semiconductor layer of one piece;

a silicon-based dielectric layer formed on the thin semiconductor layer and having a stress of less than 5×10^8 dynes/cm^2 tensile; and

circuitry supported by the thin semiconductor layer and the dielectric layer defining an integrated circuit die having an area, wherein the thin semiconductor layer extends throughout a substantial portion of the area of the integrated circuit die.

13. The thin and substantially flexible circuit of claim **12**, comprising:

a vertical interconnect conductor extending vertically

a vertical silicon-based dielectric insulator extending vertically through the thin semiconductor layer and around the interconnect conductor and having a stress of less than 5×10^8 dynes/cm^2 tensile.

14. The thin and substantially flexible circuit of claim **13**, wherein the thin semiconductor layer is formed from a semiconductor wafer.

15. The thin and substantially flexible circuit of claim **13**, wherein the thin semiconductor layer has a thickness of 50 microns or less.

16. The thin and substantially flexible circuit of claim **14**, wherein the semiconductor wafer comprises monocrystalline silicon, and the thin semiconductor layer comprises monocrystalline silicon formed from the semiconductor wafer.

17. The thin and substantially flexible circuit of claim **13**, wherein the thin semiconductor layer is unitary.

18. The thin and substantially flexible circuit of claim **13**, wherein the thin semiconductor layer extends from edge to edge of the dielectric layer.

19. The thin and substantially flexible circuit of claim **18**, wherein the dielectric layer extends from edge to edge of the thin semiconductor layer.

20. The thin and substantially flexible circuit of claim **12**, wherein the thin semiconductor layer comprises a polished surface formed by removing semiconductor material during thinning of the thin semiconductor layer to expose a surface thereof and then polishing the exposed surface, wherein the thin semiconductor layer is substantially flexible based on being thinned and having the polished surface.

21. The thin and substantially flexible circuit of claim **13**, further comprising:

a bottomside surface and a topside surface;

a contact formed on the bottomside surface and electrically connected to the vertical interconnect conductor; and

an interconnect, contact or circuit formed on or near the topside surface and electrically connected to the vertical interconnect conductor;

wherein the interconnect, contact or circuit is electrically connected to the contact on the bottomside surface via the vertical interconnect.

22. A structure comprising:

a monocrystalline semiconductor layer of one piece; and

a silicon-based dielectric layer formed on the semiconductor layer and having a stress of less than 5×10^8 dynes/cm^2 tensile;

wherein the semiconductor layer is capable of being thinned to obtain a thin and substantially flexible substrate.

23. The structure of claim **22**, comprising:

a vertical interconnect conductor extending vertically through the thin semiconductor layer and coupled to said circuitry; and

a vertical silicon-based dielectric insulator extending vertically through the thin semiconductor layer and around the interconnect conductor and having a stress of less than 5×10^8 dynes/cm^2 tensile.

24. A thin and substantially flexible integrated circuit comprising:

a thin, substantially flexible monocrystalline semiconductor layer of one piece comprising integrated circuit devices; and

a silicon-based dielectric layer formed on the thin semiconductor layer and having a stress of less than 5×10^8 dynes/cm^2 tensile.

25. The structure of claim **23**, wherein:

EXHIBIT 2

DOCKET ALARM

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