Exhibit 6

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US008653672B2

(12) **United States Patent**
Leedy

(10) **Patent No.: US 8,653,672 B2**
(45) **Date of Patent: *Feb. 18, 2014**

(54) **THREE DIMENSIONAL STRUCTURE MEMORY**

(76) Inventor: **Glenn J Leedy**, Parkland, FL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 96 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/788,618**

(22) Filed: **May 27, 2010**

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Related U.S. Application Data

(60) Continuation of application No. 10/143,200, filed on May 13, 2002, which is a continuation of application No. 09/607,363, filed on Jun. 30, 2000, now Pat. No. 6,632,706, which is a continuation of application No. 08/971,565, filed on Nov. 17, 1997, now Pat. No. 6,133,640, which is a division of application No. 08/835,190, filed on Apr. 4, 1997, now Pat. No. 5,915,167.

(51) **Int. Cl.**
H01L 23/48 (2006.01)

(52) **U.S. Cl.**
USPC **257/777**; 257/686

(58) **Field of Classification Search**
USPC 365/200, 201, 230.06; 257/777–778, 257/685–686; 438/455, 977, 107–108
See application file for complete search history.

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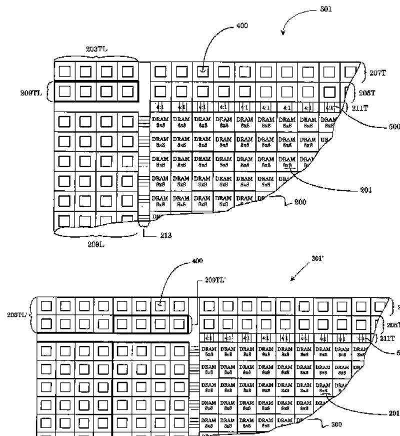
(74) *Attorney, Agent, or Firm* — Useful Arts IP

(57) **ABSTRACT**

A Three-Dimensional Structure (3DS) Memory allows for physical separation of the memory circuits and the control logic circuit onto different layers such that each layer may be separately optimized. One control logic circuit suffices for several memory circuits, reducing cost. Fabrication of 3DS memory involves thinning of the memory circuit to less than 50 μm in thickness and bonding the circuit to a circuit stack while still in wafer substrate form. Fine-grain high density inter-layer vertical bus connections are used. The 3DS memory manufacturing method enables several performance and physical size efficiencies, and is implemented with established semiconductor processing techniques.

169 Claims, 9 Drawing Sheets



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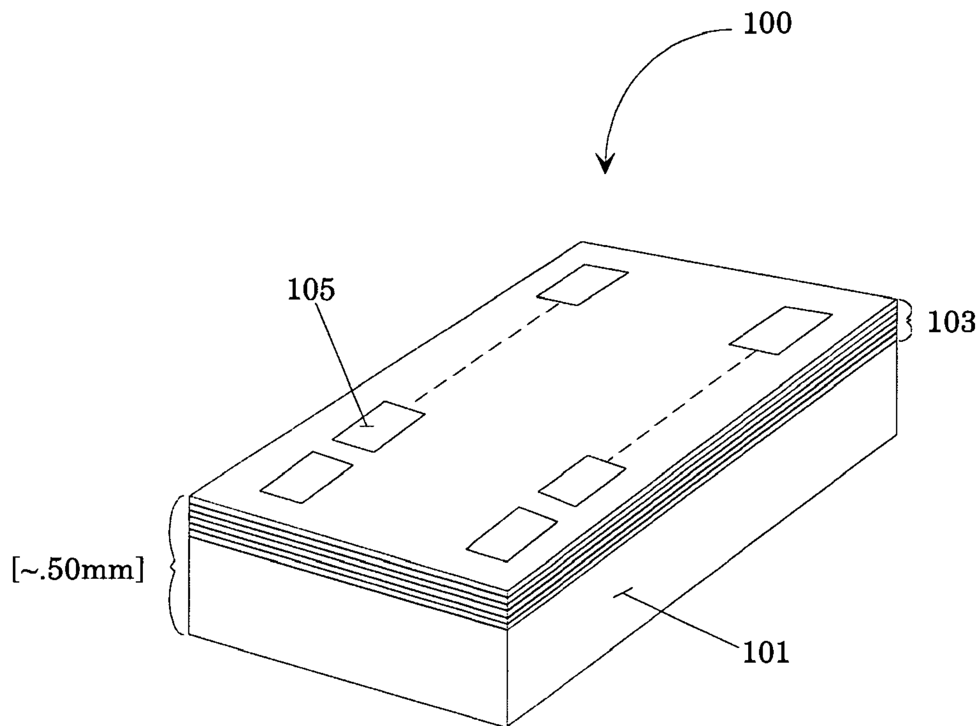

Figure 1a

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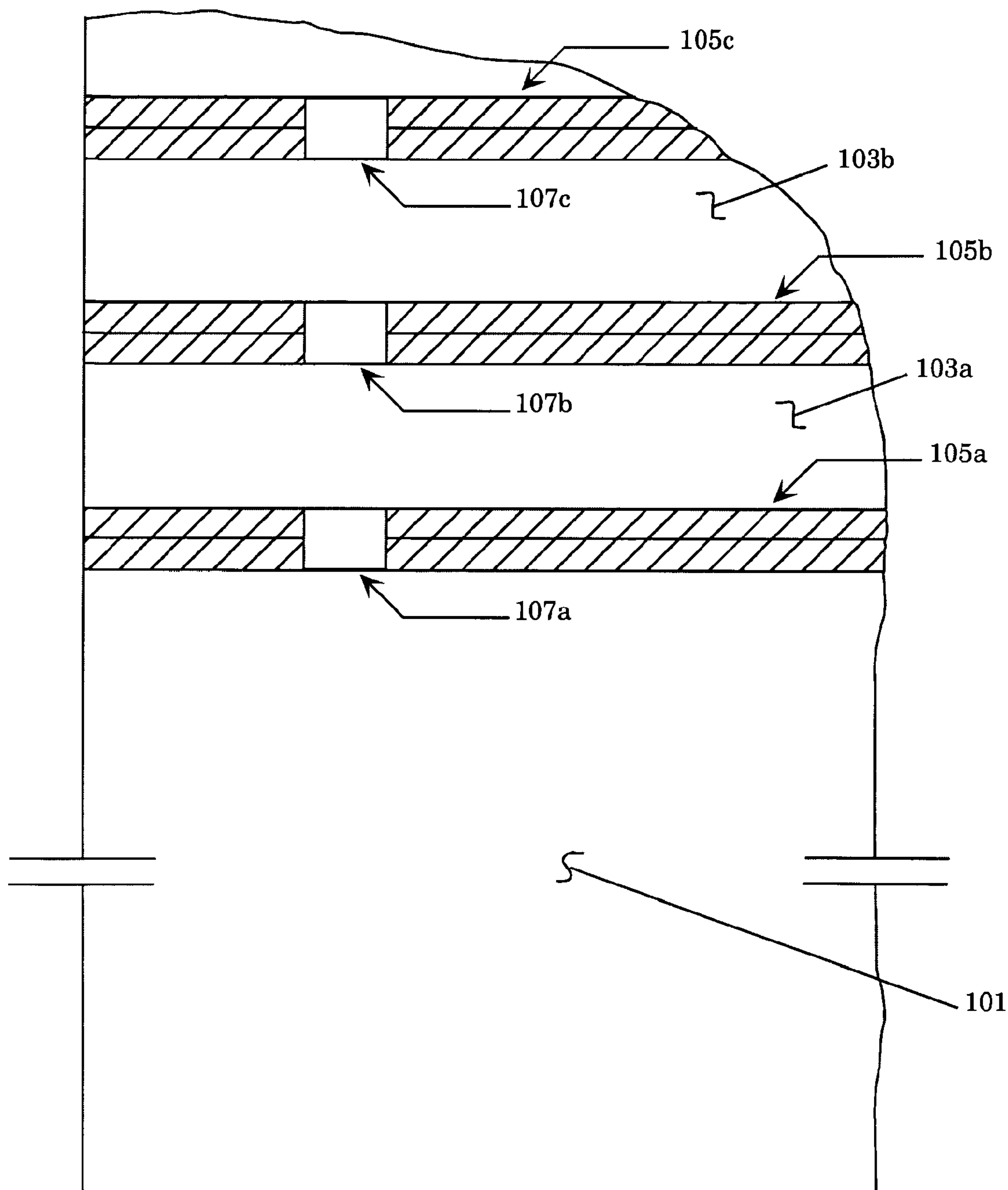

Figure 1b

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