

Exhibit 5

(12) **United States Patent**
Leedy

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(54) **THREE DIMENSIONAL STRUCTURE MEMORY**

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 (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(60) Division of application No. 10/222,816, filed on Aug. 19, 2002, now Pat. No. 7,504,732, which is a division of application No. 09/776,885, filed on Feb. 6, 2001, now Pat. No. 6,551,857, which is a continuation of application No. 09/607,363, filed on Jun. 30, 2000, now Pat. No. 6,632,706, which is a continuation of application No. 08/971,565, filed on Nov. 17, 1997, now Pat. No. 6,133,640, which is a division of application No. 08/835,190, filed on Apr. 4, 1997, now Pat. No. 5,915,167.

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H01L 21/768 (2006.01)
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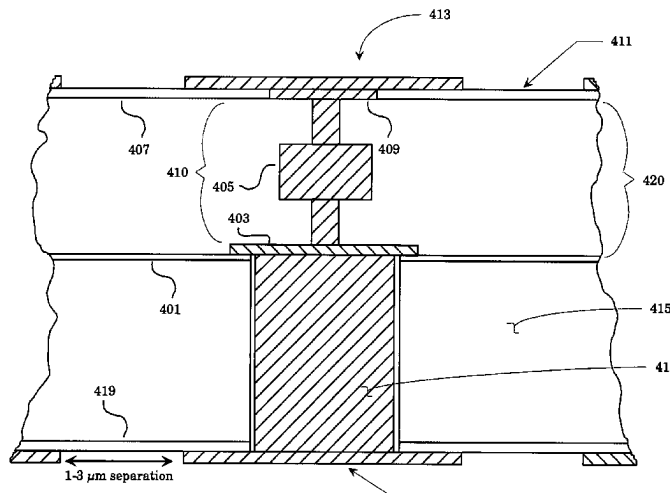
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(52) **U.S. Cl.**
 USPC **257/686**; 257/E21.597; 257/E27.026;
 257/E27.081; 257/E27.097; 257/777; 438/108;
 438/107; 438/455; 438/598

(57) **ABSTRACT**
 A Three-Dimensional Structure (3DS) Memory allows for physical separation of the memory circuits and the control logic circuit onto different layers such that each layer may be separately optimized. One control logic circuit suffices for several memory circuits, reducing cost. Fabrication of 3DS memory involves thinning of the memory circuit to less than 50 μm in thickness and bonding the circuit to a circuit stack while still in wafer substrate form. Fine-grain high density inter-layer vertical bus connections are used. The 3DS memory manufacturing method enables several performance and physical size efficiencies, and is implemented with established semiconductor processing techniques.

(58) **Field of Classification Search**
 USPC 257/777, 778, E21.597; 438/455, 598
 See application file for complete search history.

49 Claims, 9 Drawing Sheets



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