Exhibit 22

Three dimensional structure integrated circuit

US 7193239 B2

ABSTRACT

A Three-Dimensional Structure (3DS) Memory allows for physical separation of the memory circuits and the control logic circuit onto different layers such that each layer may be separately optimized. One control logic circuit suffices for several memory circuits, reducing cost. Fabrication of 3DS memory involves thinning of the memory circuit to less than 50 μm in thickness and bonding the circuit to a circuit stack while still in wafer substrate form. Fine-grain high density inter-layer vertical bus connections are used. The 3DS memory manufacturing method enables several performance and physical size efficiencies, and is implemented with established semiconductor processing techniques.

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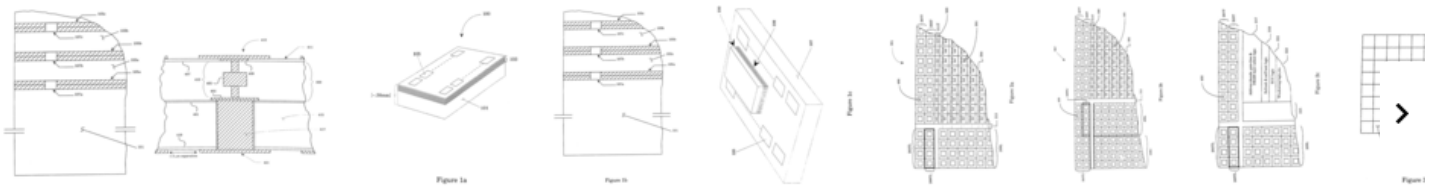

DESCRIPTION

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of, commonly assigned U.S. patent application Ser. No. 09/607,363, filed Jun. 30, 2000 now U.S. Pat. No. 6,632,706, which is a continuation of U.S. patent application Ser. No. 08/971,565, filed Nov. 17, 1997, now U.S. Pat. No. 6,133,640, which is a division of U.S. patent application Ser. No. 08/835,190, filed Apr. 4, 1997, now U.S. Pat. No. 5,915,167, all of which are incorporated by reference herein in their entireties.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relate s to stacked integrated circuit memory.

2. State of the Art

Manufacturing methods for increasing the performance and decreasing the cost of electronic circuits, nearly without exception, are methods that increase the integration of the circuit and decrease its physical size per equivalent number of circuit devices such as transistors or capacitors. These methods have produced as of 1996 microprocessors capable of over 100 million operations per second that cost less than $1,000 and 64 Mbit DRAM circuits that access data in less than 50 ns and cost less than $50. The physical size of such circuits is less than 2 cm^2. Such manufacturing methods support to a large degree the economic standard of living in the major industrialized countries and will most certainly

CLAIMS (79)

1. Circuitry comprising:

a plurality of monolithic substrates having integrated circuits formed thereon and stacked in layers such that each layer comprises only one of the substrates, wherein at least one of the plurality of substrates is a substantially flexible substrate, and wherein a major portion of the monolithic substrate is removed; and

between adjacent substrates, a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof.

2. The apparatus of claim 1, further comprising vertical interconnects having vertical interconnect segments formed of a first metal contact on a first substrate bonded to a second aligned metal contact on a second adjacent substrate.

3. The apparatus of claim 2, wherein the plurality of aligned vertical interconnect segments are joined to form a vertical interconnect between non-adjacent substrates.

4. The apparatus of claim 1, wherein at least one of said substrates is a substantially rigid substrate having a first thickness.

5. The apparatus of claim 4, wherein a plurality of substrates have a reduced second thickness substantially less than said first thickness

Circuit manufacturing methods take two primary forms: process integration and assembly integration. Historically the line between these two manufacturing disciplines has been clear, but recently with the rise in the use of MCMs (Multi-Chip Modules) and flip-chip die attach, this clear separation may soon disappear. (The predominate use of the term Integrated Circuit (IC) herein is in reference to an Integrated Circuit in singulated die form as sawed from a circuit substrate such as s semiconductor wafer versus, for example, an Integrated Circuit in packaged form.) The majority of ICs when in initial die form are presently individually packaged, however, there is an increasing use of MCMs. Die in an MCM are normally attached to a circuit substrate in a planar fashion with conventional IC die I/O interconnect bonding methods such as wire bonding, DCA (Direct Chip Attach) or FCA (Flip-Chip Attach).

Integrated circuit memory such as DRAM, SRAM, flash EPROM, EEPROM, Ferroelectric, GMR (Giant MagnetoResistance), etc. have the common architectural or structural characteristic of being monolithic with the control circuitry integrated on the same die with the memory array circuitry. This established (standard or conventional) architecture or circuit layout structure creates a design trade-off constraint between control circuitry and memory array circuitry for large memory circuits. Reductions in the fabrication geometries of memory cell circuitry has resulted in denser and denser memory ICs, however, these higher memory densities have resulted in more sophisticated control circuitry at the expense of increased area of the IC. Increased IC area means at least higher fabrication costs per IC (fewer ICs per wafer) and lower IC yields (fewer working ICs per wafer), and in the worst case, an IC design that cannot be manufactured due to its non-competitive cost or unreliable operation.

As memory density increases and the individual memory cell size decreases more control circuitry is required. The control circuitry of a memory IC as a percentage of IC area in some cases such as DRAMs approaches or exceeds 40%. One portion of the control circuitry is the sense amp which senses the state, potential or charge of a memory cell in the memory array circuitry during a read operation. The sense amp circuitry is a significant portion of the control circuitry and it is a constant challenge to the IC memory designer to improve sense amp sensitivity in order to sense ever smaller memory cells while preventing the area used by the sense amp from becoming too large.

If this design constraint or trade-off between control and memory circuits did not exist, the control circuitry could be made to perform numerous additional functions, such as sensing multiple storage states per memory cell, faster memory access through larger more sensitive sense amps, caching, refresh, address translation, etc. But this trade-off is the physical and economic reality for memory ICs as they are presently made by all manufacturers.

The capacity of DRAM circuits increase by a factor of four from one generation to the next; e.g. 1 Mbit, 4 Mbit, 16 Mbit and 64 Mbit DRAMs. This four times increase in circuit memory capacity per generation has resulted in larger and larger DRAM circuit areas. Upon introduction of a new DRAM generation the circuit yields are too low and, therefore, not cost effective for high volume manufacture. It is normally several years between the date prototype samples of a new DRAM generation are shown and the date such circuits are in volume production.

Assembling die in a stacked or three dimensional (3D) manner is disclosed in U.S. Pat. No. 5,354,695 of the present inventor, incorporated herein by reference. Furthermore, assembling die in a 3D manner has been attempted with regard to memory. Texas Instruments of Dallas Tex., Irvine Sensors of Costa Mesa Calif. and Cubic Memory Corporation of Scotts Valley Calif., have all attempted to produce stacked or 3D DRAM products. In all three cases, conventional DRAM circuits in die form were stacked and the interconnect between each DRAM in the stack was formed along the outside surface of the

said second thickness is approximately 10:1.

7. The apparatus of claim 5, wherein a ratio of said first thickness to said second thickness is at least 10:1.

8. The apparatus of claim 1, further comprising vertical interconnects formed between the adjacent bonded substrates to interconnect the integrated circuits in subsequent processing steps.

9. The apparatus of claim 1, further comprising vertical interconnects formed between the adjacent bonded substrates to interconnect the integrated circuits in subsequent processing steps.

10. The apparatus of claim 1, wherein the circuitry is formed with a low stress dielectric.

11. The apparatus of claim 10, wherein the low stress dielectric is at least one of a silicon dioxide dielectric, an oxide of silicon dielectric, and caused to have stress of about 5×10^8 dynes/cm^2 or less.

12. The apparatus of claim 11, wherein the stress of the low stress dielectric is tensile.

13. An integrated circuit structure comprising:

a first substrate having a first surface; and

a second substrate bonded to the first surface of the first substrate to form conductive paths between the first substrate and the second substrate wherein the second substrate is a substantially flexible monolithic monocrystalline semiconductor substrate having active circuitry formed thereon, wherein no other substrates are bonded to the first surface, and wherein a major portion of the second substantially flexible monolithic monocrystalline semiconductor substrate is removed.

14. The apparatus of claim 13, wherein the first substrate having polycrystalline active circuitry formed thereon.

15. The apparatus of claim 13, wherein the first substrate having active circuitry formed thereon.

16. The apparatus of claim 13, wherein at least one of the first and second substrates having passive circuitry formed thereon.

17. The apparatus of claim 13, wherein at least one of the first substrate and the second substrate is a thinned substantially flexible substrate.

18. The apparatus of claim 13, further comprising a low stress dielectric layer overlying at least one of the first substrate and the second substrate.

19. The apparatus of claim 18, wherein the low stress dielectric layer is at least one of a silicon dioxide dielectric, an oxide of silicon dielectric, and caused to have a stress of about 5×10^8 dynes cm^2 or less.

20. The apparatus of claim 19, wherein the stress of the low stress dielectric is tensile.

21. The apparatus of claim 13, wherein at least one substrate of the first and second substrates has memory circuitry formed thereon and at least one of the first and second substrates has logic circuitry formed thereon, wherein the at least one substrate that has logic circuitry formed thereon performs programmable gate line address assignment with respect to the at least one substrate that has memory circuitry formed thereon.

some use in space and military applications due to their small physical size or footprint.

The DRAM circuit type is referred to and often used as an example in this specification, however, this invention is clearly not limited to the DRAM type of circuit Undoubtedly memory cell types such as EEPROMs (Electrically Erasable Programmable Read Only Memories), flash EPROM, Ferroelectric, or combinations (intra or inter) of such memory cells can also be used with the present Three Dimensional Structure (3DS) methods to form 3DS memory devices.

The present invention furthers, among others, the following objectives:

1. Several-fold lower fabrication cost per megabyte of memory than circuits conventionally made solely with monolithic circuit integration methods.

2. Several-fold higher performance than conventionally made memory circuits.

3. Many-fold higher memory density per IC than conventionally made memory circuits.

4. Greater designer control of circuit area size, and therefore, cost.

5. Circuit dynamic and static self-test of memory cells by an internal controller.

6. Dynamic error recovery and reconfiguration.

7. Multi-level storage per memory cell.

8. Virtual address translation, address windowing, various address functions such as indirect addressing or content addressing, analog circuit functions and various graphics acceleration and microprocessor functions.

SUMMARY OF THE INVENTION

The present 3DS memory technology is a stacked or 3D circuit assembly technology. Features include:

1. Physical separation of the memory circuits and the control logic circuit onto different layers;

2. The use of one control logic circuit for several memory circuits;

3. Thinning of the memory circuit to less than about 50 μm in thickness forming a substantially flexible substrate with planar processed bond surfaces and bonding the circuit to the circuit stack while still in wafer substrate form; and

4. The use of fine-grain high density inter layer vertical bus connections.

The 3DS memory manufacturing method enables several performance and physical size efficiencies, and is implemented with established semiconductor processing techniques. Using the DRAM circuit as an example, a 64 Mbit DRAM made with a 0.25 μm process could have a die size of 84 mm^2, a memory area to die size ratio of 40% and a access time of about 50 ns for 8 Mbytes of storage; a 3DS DRAM IC made with the same 0.25 μm process would have a die size of 18.6 mm^2, use 17 DRAM array circuit layers, a memory area to die size ratio of 94.4% and an expected access time of less than 10 ns for 64 Mbytes of storage. The 3DS DRAM IC manufacturing method represents a scalable, many-fold reduction in the cost per megabyte versus that of conventional DRAM IC manufacturing methods. In other words, the 3DS memory manufacturing method represents, at the infrastructure level, a fundamental cost savings that is independent of the process fabrication technology used.

BRIEF DESCRIPTION OF THE DRAWING

performed on data routed between the first and second substrates.

23. The apparatus of claim 13, wherein at least one substrate of the first and second substrates has logic circuitry formed thereon for performing at least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

24. A stacked integrated circuit comprising:

a plurality of integrated circuit substrates having formed on corresponding surfaces thereof complementary patterns of a material bondable using thermal diffusion bonding, wherein at least one of the plurality of substrates is a substantially flexible monolithic integrated circuit substrate, and wherein a major portion of the at least one substantially flexible monolithic integrated circuit substrate is removed; and

a thermal diffusion bonded region between the complementary patterns.

25. The apparatus of claim 24, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has memory circuitry formed thereon, the memory circuitry having a plurality of memory locations including at least one memory location used for sparing, wherein data from the at least one memory location on the at least one integrated circuit substrate that has memory circuitry formed thereon is used instead of data from a defective memory location on the at least one integrated circuit substrate that has memory circuitry formed thereon.

26. The apparatus of claim 24, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has memory circuitry formed thereon and at least one integrated circuit substrate of the plurality of integrated circuit substrates has logic circuitry formed thereon, wherein the at least one integrated circuit substrate that has logic circuitry formed thereon performs programmable gate line address assignment with respect to the at least one integrated circuit substrate that has memory circuitry formed thereon.

27. The apparatus of claim 24, wherein information processing is performed on data routed between circuitry of at least two of the plurality of integrated circuit substrates.

28. The apparatus of claim 24, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has reconfiguration circuitry.

29. The apparatus of claim 24, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has logic circuitry formed thereon for performing at least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

30. The apparatus of claim 24, further comprising:

a memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores a data value and has circuitry for coupling that

FIG. 1 a is a pictorial view of a 3DS DRAM IC manufactured with Method A or Method B and demonstrating the same physical appearance of I/O bond pads as a conventional IC die;

FIG. 1 b is a cross-sectional view of a 3DS memory IC showing the metal bonding interconnect between several thinned circuit layers;

FIG. 1 c is a pictorial view of a 3DS DRAM IC stack bonded and interconnected face-down onto a larger conventional IC or another 3DS IC;

FIG. 2 a is a diagram showing the physical layout of a 3DS DRAM array circuit block with one data-line set of bus lines, i.e one port;

FIG. 2 b is a diagram showing the physical layout of a 3DS DRAM array circuit block with two sets of data-line bus lines, i.e. two ports;

FIG. 2 c is a diagram showing the physical layout of a portion of an exemplary memory controller circuit;

FIG. 3 is a diagram showing the physical layout of a 3DS DRAM array circuit showing partitions for sixty-four (64) 3DS DRAM array blocks;

FIG. 4 is a cross-sectional view of a generic 3DS vertical interconnection or feed-through in a thinned substrate;

FIG. 5 is a diagram showing the layout of a 3DS memory multiplexer for down-selecting gate-line read or write selection.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1 a and FIG. 1 b, the 3DS (Three Dimensional Structure) memory device 100 is a stack of integrated circuit layers with fine-grain vertical interconnect between all circuit layers. The term fine-grain inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 μm and more typically less than 10 μm, but not limited to a pitch of less than 2 μm, as best seen in FIG. 2 a and FIG. 2 b. The fine-grain inter-layer vertical interconnect also functions to bond together the various circuit layers. As shown in FIG. 1 b, although the bond and interconnect layers 105 a, 105 b, etc., are preferably metal, other material may also be used as described more fully hereinafter.

The pattern 107 a, 107 b, etc. in the bond and interconnect layers 105 a, 105 b, etc. defines the vertical interconnect contacts between the integrated circuit layers and serves to electrically isolate these contacts from each other and the remaining bond material; this pattern takes the form of either voids or dielectric filled spaces in the bond layers.

The 3DS memory stack is typically organized as a controller circuit 101 and some number of memory array circuit layers 103, typically between nine (9) and thirty-two (32), but there is no particular limit to the number of layers. The controller circuit is of nominal circuit thickness (typically 0.5 mm or greater), but each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness. Conventional I/O bond pads are formed on a final memory array circuit layer for use with conventional packaging methods. Other metal patterns may be used such as insertion interconnection (disclosed in U.S. Pat. Nos. 5,323,035 and 5,453,404 of the present inventor), DCA (Direct Chip Attach) or FCA (Flip-Chip Attach) methods.

Further, the fine grain inter-layer vertical interconnect can be used for direct singulated die bonding between a 3DS memory die and a conventional die (wherein the conventional die could be the controller circuit as shown in FIG. 1 c) or a 3DS memory die and another 3DS memory die; it should be assumed that

lines;

circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and

a controller that determines if one of the plurality of memory cells is defective and alters the mapping to eliminate references to the one of the plurality of memory cells that is defective.

31. The apparatus of claim 24, further comprising:

at least one controller substrate having logic circuitry formed thereon;

at least one memory substrate having memory circuitry formed thereon;

a plurality of data lines and a plurality of gate lines on each memory substrate;

an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting of one of the plurality of gate lines;

a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and

controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

32. The apparatus of claim 31, wherein said controller substrate logic:

tests the array of memory cells periodically to determine if one of said memory cells is defective; and

removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

33. The apparatus of claim 31, further comprising programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

34. The apparatus of claim 31, wherein the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order, wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

35. The apparatus of claim 31, wherein:

the logic circuitry of the at least one controller substrate is tested by an external means; and

the array of memory cells of the at least one memory substrate are tested by the logic circuitry of the at least one controller substrate

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