Exhibit 13

designlines PROTOTYPING

Blog

Moore's Lag Shifts Paradigm of Semi Industry

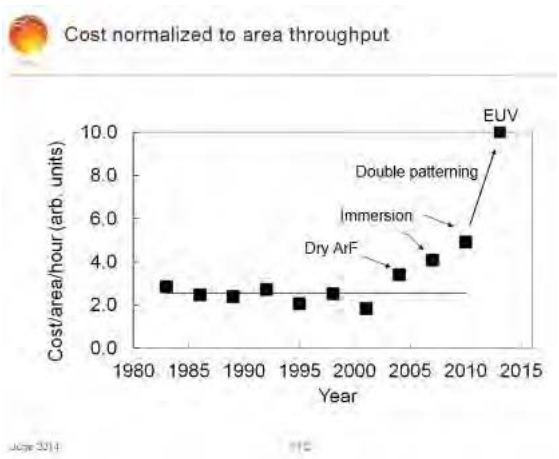
Moore's Law lagging may be a good thing

Zvi Or-Bach, MonolithIC 3D Inc.
9/3/2014 04:30 PM EDT
15 comments post a comment

According to Zvi Or-Bach, president and CEO of MonolithIC 3D Inc., 28nm will be the last process node following Moore's Law for most designs.

In an earlier column, 28nm – The Last Node of Moore's Law, we pointed out that the change has already happened. It is no longer a matter of forecast or prediction. In this blog, we will start by reviewing some of what has transpired since that column was published. Then we will focus on the ensuing paradigm shift in the semiconductor industry.

The following chart was presented in the IEEE IITC workshop by GlobalFoundries. It illustrates the cost impact of the double patterning required for scaling below 28/22 nm.



Click here for a larger image.

In his coverage of Semicon West, Rick Merritt wrote: "Moore's Law has definitely slowed." He quoted Gartner semiconductor analyst Bob Johnson as saying, "No matter what Intel says, Moore's Law is slowing down. Only a few high-volume, high-performance apps can justify 20 nm and beyond."

Soon thereafter, in a Semiconductor Manufacturing & Design blog post about ConFab 2014, Peter Singer quoted Dr. Gary Patton, vice president of semiconductor research and development center at IBM, as saying: "The challenge we're facing now is two-fold. Number one, we're struggling to get that 0.7X linear scaling. It

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krisi thank you Colin, interesting info...2 years to volume production sounds very aggressive

11/20/2014
2:14:11 PM

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More recently, in early August, we finaly got more information from Intel about its upcoming 14nm technology node. In our blog Intel vs. Intel, we articulated that Intel's numbers indicate that Moore's Law stopped at the 28/22nm nodes, both in terms of the required bringup time and the cost of the new technology nodes.

It is hard to accept that a trend that has held strong for 50 years, and that kept going many years after multiple predictions of its imminent demise, has really stopped. And it is even harder as we watch the huge effort of bringing up the 14nm and 10nm nodes. Yet it seems that everybody should agree that the semiconductor industry is now going through a paradigm shift and -- for most designs -- 28 nm is, at least for some time, the last node of Moore's Law.

These well-known charts present the reason for that change.

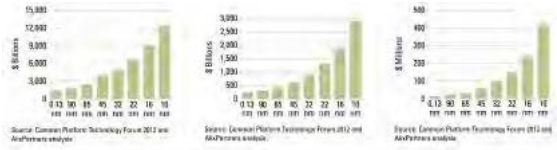
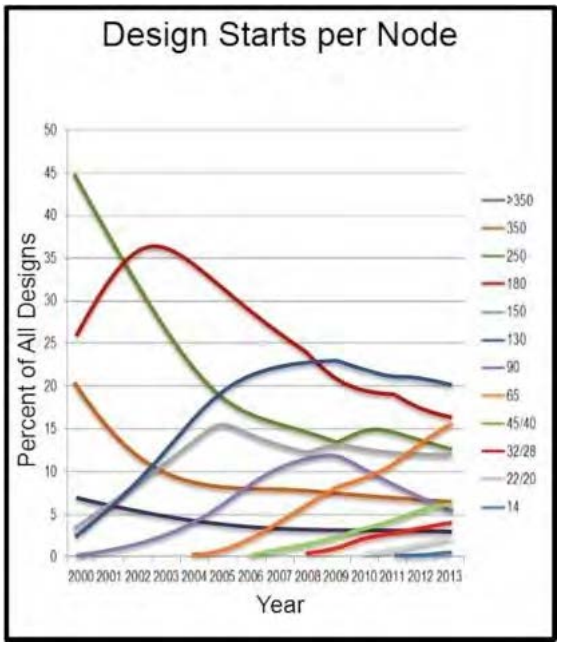


FIGURE 4. (L) Fab Costs by Node (in US$ billions) **FIGURE 5.** (C) Process Technology Development Costs by Node (US$ billions) **FIGURE 6.** (R) Chip Design Costs by Node (US$ millions)

Click here for a larger image.

These charts show that design costs increase by more than $100 million from 32 nm to 16 nm. If we assume a die cost of $10 at 32 nm, and if we assume that the traditional cost reduction per node still holds, then we would need a volume of more than 20 million units just to break even. If one also considers the risk associated with such a design, it would actually require more than 100 million units -- or at least $1 billion of market -- for such device to justify the investment. Clearly, very few designs have the market for 100 million units or $1 billion.

The following chart by IBS presents the past trend in design starts per node. As we see, most new designs are still created at the 130nm node, while the node with the fastest rampup is at 65 nm.



Design starts per year; click here for a larger image.
(Source: IBS Dec 2012)

A 2016 forecast from Anysilicon on semiconductor technology nodes is illustrated in the following pie chart.

Cartoon Contest

October 2014 Cartoon Caption Winner!

And then there were harmonics Jim never saw coming.

26 comments

ALL CARTOONS

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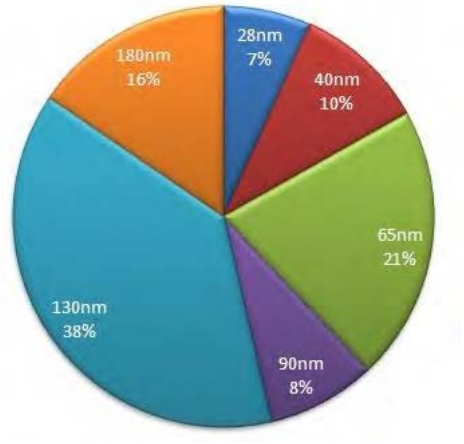
Huey Lewis returns: It's hip to be square . . .
NJ Mike on November Cartoon ...

Where'd he go?: Nerd camouflage.
dt_hayden on November Cartoon ...

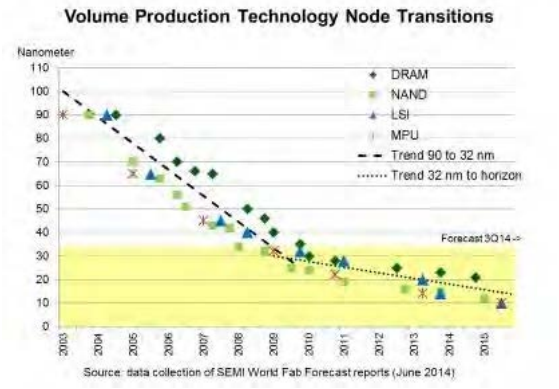
November Cartoon: Kevin doesn't know it yet but he's about to be e-waste.
BinaryJudy on November Cartoon ...

Re: failing fast: @Susan...how long is a piece of string....I think one of the ESA guys said exactly that. I did pose a question on one of their blogs about...
David Ashton on Rosetta & the Comet ...

MMU/MPU issues: As someone who is actively attempting to develop an MMU/MPU in a new SoC system, I'd like to share some



Yet again, this indicates a very slow shift to more advanced nodes, and the expectation is that -- even in 2016 -- most new designs will still be implemented at the 130nm node. This is clearly a paradigm shift in the industry, which is responding accordingly. Just before Semicon West 2014, we saw the conclusions of the SEMI's World Fab Forecast. This forecast uses a bottom-up methodology, providing high-level summaries and graphs, along with in-depth analyses of capital expenditures, capacities, technology, and products by fab. The following chart illustrates this new paradigm.



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The report states:

> The cost per wafer has become an increasing concern below the 32nm node. The expected cost reduction benefit of production at smaller nodes is diminishing and is not keeping pace with the scaling benefits in many cases. This has widespread and fundamental implications for an industry long following the cadences of Moore's Law…
>
> These may be contributing factors as to why some volume fabs are exhibiting a lag in beginning production of a new technology node. Now evident quantitatively for the first time, there is evidence of a clear slowdown in volume production scaling of leading technology node transitions. [Emphasis added]

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Flash Poll

Which of the following must a device withstand - and still function properly - to be considered an "industrial-grade" device in the electronics industry? (Select all that apply.)

- [ ] Intermittent shaking and kicking
- [ ] Dropping off the back of the delivery truck (or loading dock)
- [ ] Being used as a hockey puck
- [ ] Being run over by a forklift
- [ ] Rapid, repeated blows from a massive, blunt object
- [ ] Shipping via the Post Office
- [ ] A direct lightning strike

USER RANK
MANAGER

Mark Bohr on continued decline of cost/transistor
sranje 9/12/2014 6:56:50 PM

NO RATINGS
LOGIN TO RATE

"One of the fundamental benefits of Moore's Law is smaller feature sizes, primarily to get lower cost per transistor so we can do more things" in a similarly sized chip, he said. Intel already announced it has started making in volume chips using a 14 nm process at a lower cost per transistor than its prior 22 nm generation. It also said it is in development of a 10 nm process that it believes will deliver lower cost per transistor.

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BLOGGER

Other options
DrFPGA 9/7/2014 10:19:44 AM

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When fpgas are used to dynamically adapt and accelerate algorithms their transistors can get used and reused for multiple functions. Maybe this is one option to improve cost performance...

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ROOKIE

Monolitihic 3D enabling ultra-large energy efficient systems
Zeev00 9/5/2014 1:35:59 PM

NO RATINGS
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One point that was not, perhaps, stressed enough is the huge energy saving at the system level enabled by monolithic 3D.

We all understand the energy savings because of shortened interconnect in 3D layers. Yet it seems that for large system this saving is limited to about a factor of 2 at best. Actually, it is potentially much more. For large-scale processing such as HPC, most of the energy goes to shuttling data off-chip across multiple processors and multiple memory subsystems. One cannot assume multiple layer HPC processors, as the heat -- even if sinked across layers -- needs to be dissipated. But one can imagine a 3D layer of processor and memory subsystems sandwich that is arrayed on a huge wafer-sized chips. There is almost no off-chip driving of data in such an array, the memory is very close to the processors, and the "only" problem is reliability (Amdahl growls here :-). Yet having a 3D redundancy layer that is able to correct for hundreds of faults in the processor logic, neatly works around the reliability issue. And power has a much larger area to be dissipated from.

In other words, new 3D-enabled architectures could allow for almost inifinitely-sized chips, overcoming the biggest energy barrier in HPC and exascale computing.

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Re: Moore's "lag"
Or_Bach 9/5/2014 5:04:10 AM

NO RATINGS
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3D Guy, I am glad that you like the term - Moore's "lag" - but the credit should go to Max Maxfield (The EE Times editor).

As to the VC returning to the semiconductor space let me make the following points:

A. For VC investments it takes years before real high volume is resulted, so even if you are correct about these technologies being niche there is no contradiction there

B. The escalating chip designs cost associated with dimension scaling drove out the VCs from semi. Once the market will develop alternative technologies to add value cost of masks and all other NRE related cost will trend down and with lower investment requirements more VC would consider again these type of ventures

C. If you believe that IOT and wearable are anything close to the many trillions of dollar that Cisco and other are forecasting than you have to agree that vibrant venture activity is a must which lead to the kind of environment that VCs are part of.

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ROOKIE

Re: Heterogeneous integration
Or_Bach 9/5/2014 4:41:39 AM

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Packaging has an important role as off-chip interconnect is 1,000x worse than on-chip interconnect. Any improvment would impact the end system power and performance BUT keeping the cost down has been the problem so far.

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- Being splashed with hot coffee
- Recovery from the ocean floor
- A day in a closed car in the desert sun
- Spending the night outside in a Siberian winter
- A reversed and/or leaking battery
- Other (Specify in the comments section)

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