Exhibit 1

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(12) **United States Patent**
Leedy

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(45) **Date of Patent:** **Mar. 20, 2007**

(54) **THREE DIMENSIONAL STRUCTURE INTEGRATED CIRCUIT**

(75) Inventor: **Glenn J Leedy**, Saline, MI (US)

(73) Assignee: **Elm Technology Corporation**, Saline, MI (US)

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H01L 29/04 (2006.01)
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(58) **Field of Classification Search** 257/74, 257/686, 723, 724; 438/17, 18, 123; 714/30, 714/718, 719
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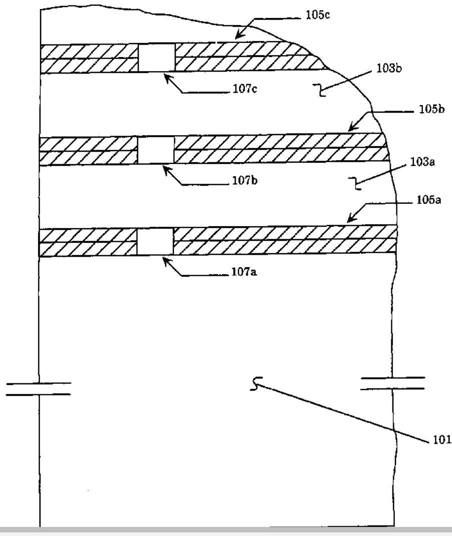
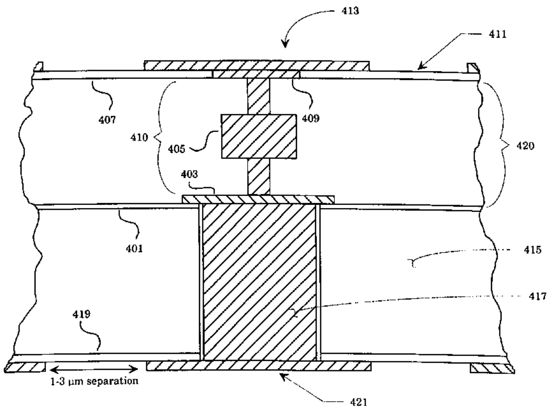
Primary Examiner—Zandra V. Smith
Assistant Examiner—Pamela E Perkins
(74) *Attorney, Agent, or Firm*—Fish & Neave IP Group of Ropes & Gray LLP; Robert W. Morris; Jeffrey D. Mullen

(57) **ABSTRACT**

A Three-Dimensional Structure (3DS) Memory allows for physical separation of the memory circuits and the control logic circuit onto different layers such that each layer may be separately optimized. One control logic circuit suffices for several memory circuits, reducing cost. Fabrication of 3DS memory involves thinning of the memory circuit to less than 50 μm in thickness and bonding the circuit to a circuit stack while still in wafer substrate form. Fine-grain high density inter-layer vertical bus connections are used. The 3DS memory manufacturing method enables several performance and physical size efficiencies, and is implemented with established semiconductor processing techniques.

79 Claims, 9 Drawing Sheets





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