THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., Defendants.	:	C.A. No. 14-1430-LPS-CJB
ELM 3DS INNOVATIONS, LLC Plaintiff, v. MICRON TECHNOLOGY, INC., et al. Defendants.	:	C.A. No. 14-1431-LPS-CJB
ELM 3DS INNOVATIONS, LLC Plaintiff, v. SK HYNIX INC., et al. Defendants.	:	C.A. No. 14-1432-LPS-CJB

ORDER

At Wilmington this **13th** day of **April, 2020**:

For the reasons set forth in the Memorandum Opinion issued this date,

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IT IS HEREBY ORDERED that the following claim terms of U.S. Patent Nos. 7,193,239; 7,474,004; 7,504,732; 8,035,233; 8,410,617; 8,629,542; 8,653,672; 8,791,581; 8,796,862; 8,841,778; 8,907,499; 8,928,119; and 8,933,570 are construed as follows:

Term 1	**Court's Construction**
"substantially flexible substrate" "substantially flexible . . . substrate" "substrate is substantially flexible" "substrate substantially flexible" "substrate . . . is . . . substantially flexible" "substantially flexible . . . semiconductor layer" ['239 patent claims 1, 13] ['617 patent claims 36, 51] ['542 patent claims 1, 40, 44] ['672 patent claims 17, 84, 129, 143] ['581 patent claims 36, 54, 78, 116, 136] ['862 patent claims 30, 34, 36, 135-37, 147] ['778 patent claims 2, 8, 31, 44, 52, 53] ['499 patent claims 1, 24, 53, 83, 132] ['119 patent claims 1, 7, 17] ['570 patent claims 58, 67]	Not indefinite. "A semiconductor substrate/semiconductor layer that is thinned to 50 µm or less and subsequently polished or smoothed such that it is largely able to bend without breaking"

Term 2	**Court's Construction**
"dice is substantially flexible" "die is substantially flexible" ['239 patent claims 60, 70]	"A dice/die that is thinned to 50 µm or less and subsequently polished or smoothed such that it is largely able to bend without breaking"

Term 3	**Court's Construction**
"substantially flexible integrated circuit[s]" "substantially flexible integrated circuit layer[s]" "integrated circuits is substantially flexible" "integrated circuit . . . is . . . substantially flexible" "substantially flexible circuit layer[s]" "substantially flexible stacked integrated circuit structure" "substantially flexible circuit" "substantially flexible . . . structure" ['004 patent claims 1, 22, 23] ['732 patent claims 1, 13, 14] ['542 patent claims 1, 40]	Not indefinite. "An integrated circuit/integrated circuit layer/circuit layer/circuit structure/circuit/structure that is largely able to bend without breaking and contains a substantially flexible semiconductor substrate, that is thinned to 50 µm or less and subsequently polished or smoothed such that it is largely able to bend without breaking, and a sufficiently low tensile stress dielectric material."

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['862 patent claims 30, 135, 147] ['778 patent claims 8, 44, 46] ['499 patent claims 1, 12, 13, 24, 36-38, 49, 53, 83, 86, 87, 132] ['119 patent claims 1, 33] ['570 patent claim 58]	

Term 4	Court's Construction
"have stress of about 5×10^8 dynes/cm^2 or less" "have a stress of about 5×10^8 dynes cm^2 or less" "having a stress of 5x10^8 dynes/cm^2 or less" "a stress of about 5×10^8 dynes/cm^2 or less" "having a stress of 5×10^8 dynes/cm^2 tensile or less" "[have] a stress of about 5×10^8 dynes/cm^2 tensile or less" "having[/has] a stress of less than 5×10^8 dynes/cm^2 tensile" "with a tensile stress of less than 5×10^8 dynes/cm^2" "with a stress of less than 5×10^8 dynes/cm^2 tensile" "has[/having] a tensile stress of less than 5×10^8 dynes/cm^2" ['239 patent claims 11, 12, 19, 20, 62, 63, 72, 73] ['004 claim 20] ['542 patent claims 2, 41] ['732 patent claim 10] ['617 patent claim 36] ['672 patent claims 17, 22, 84, 129, 131, 145, 152] ['581 patent claims 12, 36, 54, 78, 116, 136] ['862 patent claims 135, 137, 138, 147] ['778 patent claims 1, 2, 8, 14] ['499 patent claims 1, 12, 13, 24, 53, 83, 86, 87, 132] ['119 patent claims 7, 18] ['570 patent claims 60, 67]	Indefiniteness unable to be resolved at this stage of the case

Term 5	Court's Construction
"low stress dielectric" "low stress dielectric layer" "low stress . . . dielectric material" "low-stress . . . dielectric material"	Indefiniteness unable to be resolved at this stage of the case

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"low-stress . . . dielectric layer" "low stress . . . dielectric layer" ['239 patent, claims 10, 18, 61, 71] ['004 patent, claims 1, 21, 22, 23] ['732 patent, claims 1, 13, 14] ['672 patent, claim 95] ['862 patent, claims 30, 34]	

Term 6	Court's Construction
"vertically interconnected circuit block stacks" ['581, claims 1, 5, 113, 133] "vertically interconnected circuit blocks" ['499 patent claim 49]	"Vertically electrically connected circuit block stacks" and "vertically electrically connected circuit blocks"

Term 7	Court's Construction
"a plurality of vertical interconnect segments interconnecting the first and second integrated circuit layers, wherein each vertical interconnect segment forms an interconnection only between a pair of adjacent integrated circuits" ['570 patent claim 58]	"vertical electrical connections"

Term 8	Court's Construction
"Said plurality of first interconnection and said plurality of second interconnections are substantially aligned with each other, and said plurality of first interconnections and said plurality of second interconnections are electrically coupled together to form a plurality of vertical interconnections, including redundant vertical interconnections" ['004 patent claim 1]	"vertical electrical connections"

Term 9	Court's Construction
"At least one interconnection between two of the plurality of substrates" ['672 patent claim 84]	"at least one electrical connection between two of the plurality of substrates"

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Claim Term 10	Court's Construction
"a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof " ['239 patent claim 1]	"a bonding layer physically joining together the adjacent substrates, the bonding layer being formed by physically joining first and second substantially planar surfaces having a bond forming material throughout a majority of the surface area thereof"
"a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice" ['239 patent claim 60]	"a bonding layer physically joining together the adjacent dice, the bonding layer physically joining first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice"

Claim Term 11	Court's Construction
"Wherein the semiconductor die is attached to the first surface of the substrate by one or more bonds including one bond located other than at the edges of the semiconductor die" ['239 patent claim 70]	"wherein the semiconductor die is attached to the first surface of the substrate by one or more physical connections, including one physical connection located other than at the edges of the semiconductor die"

Claim Term 12	Court's Construction
"A first integrated circuit having circuitry formed on a front surface thereof, the front surface or a back surface being bonded to the circuit substrate." ['542 patent claim 1]	"the front surface or a back surface being physically joined to the circuit substrate"

Claim Term 13	Court's Construction
"the first and second substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal"	"physically joined in a fixed relationship to one another at least mostly with metal, or at least mostly with silicon-based dielectric material and metal"

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