THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC

Plaintiff,

v.

C.A. No. 14-1430-LPS-CJB

SAMSUNG ELECTRONICS CO., LTD.,

Defendants.

ELM 3DS INNOVATIONS, LLC

Plaintiff,

C.A. No. 14-1431-LPS-CJB v.

MICRON TECHNOLOGY, INC., et al.

Defendants.

ELM 3DS INNOVATIONS, LLC

Plaintiff,

C.A. No. 14-1432-LPS-CJB v.

SK HYNIX INC., et al.

Defendants.

ORDER

At Wilmington this **13th** day of **April**, **2020**:

For the reasons set forth in the Memorandum Opinion issued this date,



IT IS HEREBY ORDERED that the following claim terms of U.S. Patent Nos.

7,193,239; 7,474,004; 7,504,732; 8,035,233; 8,410,617; 8,629,542; 8,653,672; 8,791,581;

8,796,862; 8,841,778; 8,907,499; 8,928,119; and 8,933,570 are construed as follows:

Term 1	Court's Construction
"substantially flexible substrate"	Not indefinite. "A semiconductor
"substantially flexible substrate"	substrate/semiconductor layer that is
"substrate is substantially flexible"	thinned to 50 µm or less and
"substrate substantially flexible"	subsequently polished or smoothed such
"substrate is substantially flexible"	that it is largely able to bend without
"substantially flexible semiconductor layer"	breaking"
['239 patent claims 1, 13]	
['617 patent claims 36, 51]	
['542 patent claims 1, 40, 44]	
['672 patent claims 17, 84, 129, 143]	
['581 patent claims 36, 54, 78, 116, 136]	
['862 patent claims 30, 34, 36, 135-37, 147]	
['778 patent claims 2, 8, 31, 44, 52, 53]	
['499 patent claims 1, 24, 53, 83, 132]	
['119 patent claims 1, 7, 17]	
['570 patent claims 58, 67]	

Term 2	Court's Construction
"dice is substantially flexible" "die is substantially flexible" ['239 patent claims 60, 70]	"A dice/die that is thinned to 50 µm or less and subsequently polished or smoothed such that it is largely able to bend without breaking"

Term 3	Court's Construction
"substantially flexible integrated circuit[s]"	Not indefinite. "An integrated
"substantially flexible integrated circuit layer[s]"	circuit/integrated circuit layer/circuit
"integrated circuits is substantially flexible"	layer/circuit structure/circuit/structure
"integrated circuit is substantially flexible"	that is largely able to bend without
"substantially flexible circuit layer[s]"	breaking and contains a substantially
"substantially flexible stacked integrated circuit	flexible semiconductor substrate, that is
structure"	thinned to 50 µm or less and
"substantially flexible circuit"	subsequently polished or smoothed such
"substantially flexible structure"	that it is largely able to bend without
['004 patent claims 1, 22, 23]	breaking, and a sufficiently low tensile
['732 patent claims 1, 13, 14]	stress dielectric material."
['542 patent claims 1, 40]	



['862 patent claims 30, 135, 147]	
['778 patent claims 8, 44, 46]	
['499 patent claims 1, 12, 13, 24, 36-38, 49, 53,	
83, 86, 87, 132]	
['119 patent claims 1, 33]	
['570 patent claim 58]	

Term 4	Court's Construction
"have stress of about 5×10 ⁸ dynes/cm ² or less"	Indefiniteness unable to be resolved at
"have a stress of about 5×10^8 dynes cm ² or less"	this stage of the case
"having a stress of 5x10 ⁸ dynes/cm ² or less"	
"a stress of about 5×10^8 dynes/cm ² or less"	
"having a stress of 5×10^8 dynes/cm ² tensile or	
less"	
"[have] a stress of about 5×10^8 dynes/cm ² tensile	
or less"	
"having[/has] a stress of less than 5×10^8	
dynes/cm ² tensile"	
"with a tensile stress of less than 5×10^8	
dynes/cm ² "	
"with a stress of less than 5×10^8 dynes/cm ²	
tensile"	
"has[/having] a tensile stress of less than 5×10^8	
dynes/cm ² "	
['239 patent claims 11, 12, 19, 20, 62, 63, 72, 73]	
['004 claim 20]	
['542 patent claims 2, 41]	
['732 patent claim 10]	
['617 patent claim 36]	
['672 patent claims 17, 22, 84, 129, 131, 145, 152]	
['581 patent claims 12, 36, 54, 78, 116, 136]	
['862 patent claims 135, 137, 138, 147]	
['778 patent claims 1, 2, 8, 14]	
['499 patent claims 1, 12, 13, 24, 53, 83, 86, 87,	
132]	
['119 patent claims 7, 18]	
['570 patent claims 60, 67]	

Term 5	Court's Construction
"low stress dielectric"	Indefiniteness unable to be resolved at
"low stress dielectric layer"	this stage of the case
"low stress dielectric material"	
"low-stress dielectric material"	



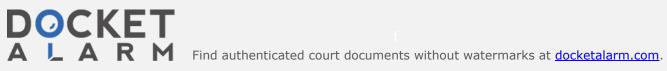
"low-stress dielectric layer"	
"low stress dielectric layer"	
['239 patent, claims 10, 18, 61, 71]	
['004 patent, claims 1, 21, 22, 23]	
['732 patent, claims 1, 13, 14]	
['672 patent, claim 95]	
['862 patent, claims 30, 34]	

Term 6	Court's Construction
"vertically interconnected circuit block stacks"	"Vertically electrically connected circuit
['581, claims 1, 5, 113, 133]	block stacks" and "vertically electrically connected circuit blocks"
"vertically interconnected circuit blocks"	
['499 patent claim 49]	

Term 7	Court's Construction
"a plurality of vertical interconnect segments interconnecting the first and second integrated circuit layers, wherein each vertical interconnect segment forms an interconnection only between a pair of adjacent integrated circuits"	"vertical electrical connections"
['570 patent claim 58]	

Term 8	Court's Construction
"Said plurality of first interconnection and said	"vertical electrical connections"
plurality of second interconnections are	
substantially aligned with each other, and said	
plurality of first interconnections and said plurality	
of second interconnections are electrically coupled	
together to form a plurality of vertical	
interconnections, including redundant vertical	
interconnections"	
['004 patent claim 1]	

Term 9	Court's Construction
"At least one interconnection between two of the plurality of substrates" ['672 patent claim 84]	"at least one electrical connection between two of the plurality of substrates"

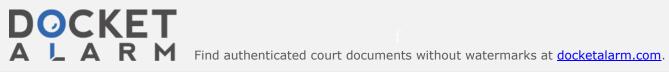


Claim Term 10	Court's Construction
"a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof" ['239 patent claim 1]	"a bonding layer physically joining together the adjacent substrates, the bonding layer being formed by physically joining first and second substantially planar surfaces having a bond forming material throughout a majority of the surface area thereof"
"a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice" ['239 patent claim 60]	"a bonding layer physically joining together the adjacent dice, the bonding layer physically joining first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice"

Claim Term 11	Court's Construction
"Wherein the semiconductor die is attached to the	"wherein the semiconductor die is
first surface of the substrate by one or more bonds	attached to the first surface of the
including one bond located other than at the edges	substrate by one or more physical
of the semiconductor die"	connections, including one physical
['239 patent claim 70]	connection located other than at the
	edges of the semiconductor die"

Claim Term 12	Court's Construction
"A first integrated circuit having circuitry formed on a front surface thereof, the front surface or a back surface being bonded to the circuit substrate." ['542 patent claim 1]	"the front surface or a back surface being physically joined to the circuit substrate"

Claim Term 13	Court's Construction
"the first and second substrates are bonded	"physically joined in a fixed relationship
together in fixed relationship to one another at	to one another at least mostly with metal,
least predominantly with metal, or at least	or at least mostly with silicon-based
predominantly with silicon-based dielectric	dielectric material and metal"
material and metal"	



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