Exhibit I

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Within the last few years, backside thinning of fully processed IC wafers has become a widely used technique in the search for high speed in advanced package technologies. Figure 1 shows the trend in finished IC thickness used in advanced packaging based on thickness figures quoted by various sources over the last ten years. The market potential for ultra-thin wafers, with backside metallization, is estimated by market researchers to be above 40% of the wafer market by the year 2010.

Ultra-thin semiconductor wafer applications and processes

The ongoing development in functionality of integrated circuits is now targeted on the integration of all of the electronic elements in the total system. This research is working from a base of many differing semiconductor processes. Each of these processes will have a different attibute in terms of functionality sucah as speed, power etc.

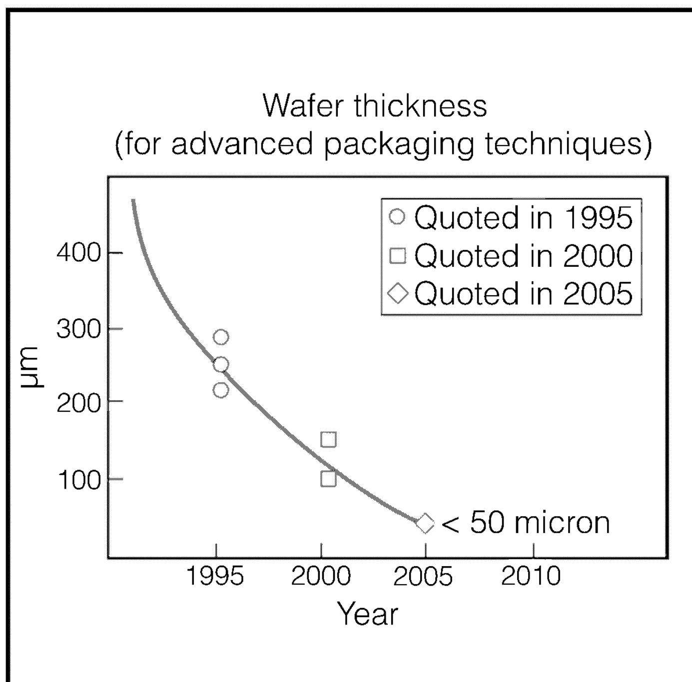

Figure 1. Trend in ultra thin wafers for advanced packaging.

Three factors have concentrated development on thinner wafers: the demand for a low package height for chip cards and RFIDs, the requirement for higher power, and the search for Systems in a Pack (SiP) using chip stack methods. The premise is that the heat flow through the chip is greatly enhanced and through holes in the wafer create direct interconnection to adjacent die. All of this is advantageous to chip stack technology, high speed and increased power. It is unusual to have three improvements take effect without some loss of functionality.

GaAs is extremely useful in the field of high-speed circuits, but its performance in terms of light emission is inhibited by its poor dissipation of the heat that accompanies light emission. Ultra-thin GaAs chips allow greater thermal dissipation and also assist in the vertical interconnection through the chip by the use of vias. Many systems have this basic makeup: GaAs high-speed circuits in the front end of systems, complex logic control circuitry in the middle, and power capability at the back end.

This feature looks at the various processes used and being developed in order to exploit the virtues of speed, power and integration into systems that are offered by thin wafer devices. Currently, device chip stacks lead the way, but wafer processing by wafer bonding as against chip processing will be vigorously explored in order to achieve cost effectiveness. Chip processing will

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need to overcome serious obstacles to acceptable yield.

Thinning by grinding

Back grinding is the conventional method for reducing wafers from their original thickness to a diminished thickness suitable for final packaging of die after dicing. Grinding is fast and produces low variation and good surface finishes. For new, emerging applications that use very thin and ultra-thin die, grinding remains the common thinning method, but some process modifications and additional techniques are required.

Precisely controlled grinding rate

Modern grinders rotate the wafer on a vacuum chuck and feed the rotating grind wheel into the backside of the wafer at a precisely controlled rate. The delicate grinding wheels employ graded diamond abrasives embedded in specially engineered binders on the wheel edge. The current production limit for grinding reduces wafers from an average starting thickness of 750 μm to as thin as 150 μm. Yield loss considerations from grinding and downstream processes (debonding from carrier) have made it very difficult to thin below 150 μm in production. Research projects on the other hand are consistently working below the 150 μm level and creeping towards the 50 μm level.

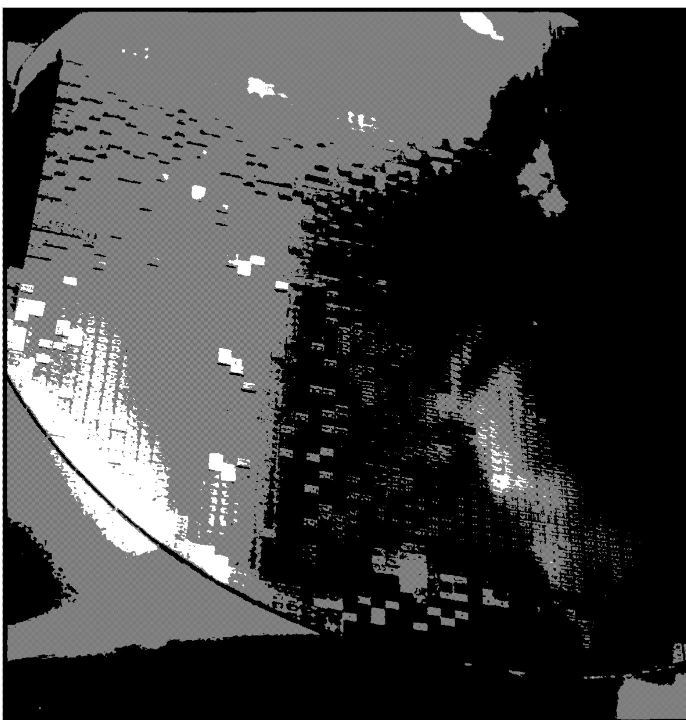
Ground surface finishing processes

Three methods are currently employed to remove grinding damage and improve the final surface finish:

- traditional loose-abrasive polishing;
- wet etching;
- dry plasma etching.

The first method typically integrates a polishing step into the grinder itself, a method that offers the advantage of integrating the damage removal into the grinder tool and builds upon traditional CMP (chemical-mechanical-polishing) technology. CMP, however, has the disadvantage of low removal rates and perpetuates the surface profile.

The second method uses familiar wet-etching processes to remove surface damage. Wet chemical etching is one of the most common thinning techniques. To etch one side of the wafer, one approach is spin etching, in which a thin stream of an etching agent is moved periodically over the surface of the rotating wafer. The front surface of the wafer is protected either by additional layers, or by applying special chucks that allow the processing of thin wafers without surface protection layers or tapes.



This is an ANADIGICS GaAs wafer that has been thinned (after die separation). The die on this wafer have been partially removed from the wafer.

The third method uses atmospheric dry plasma etching to remove surface damage. This method offers the advantage that the surface damage is removed, the edges are improved by rounding the sharp edge, and the surface roughness can be controlled where needed for adhesion.

Wafer handling

In order to handle delicate thin wafers the device wafer is bonded to a rigid carrier substrate prior to the back-thinning process. The originally thick device wafer is bonded with its active surface to a carrier wafer using an adhesive bonding layer. After backside processing, including the thinning process and eventually further process steps (lithography, etching, etc.), the thin device wafer, supported by the rigid carrier substrate, has to be released from the carrier wafer, enabling dicing and packaging processes in the final stages.

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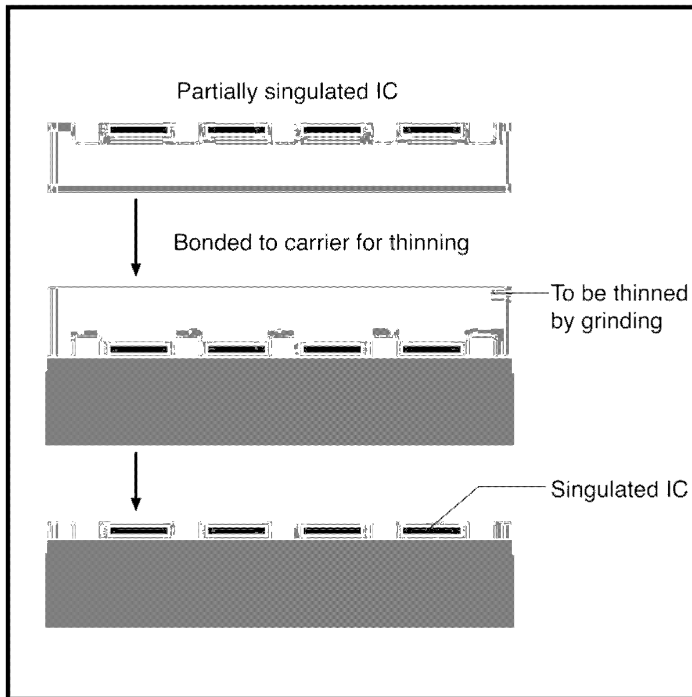

Figure 2. Singulating by back grinding.

The adhesives used for temporary bonding allow the release of the device wafer by using different approaches: UV release adhesives debond after exposure to UV light, thermal release adhesives have to be heated above a release temperature, and solvent release adhesives have to be dissolved in a chemical solvent for debonding of the device wafer from the carrier.

The temporarily bonded stack, consisting of device wafer, intermediate layer and carrier wafer, is generally further processed using several different techniques (e.g. lithography, etching, etc.) Several different aspects, therefore, must be taken into account before selection of the intermediate layer for the targeted application. Temperature capability, chemical resistance, ease of processing and thickness variations are just some of the parameters that need to be considered when choosing the adhesive method to be used between carrier and wafer.

Temporary bonding and debonding with waxes

Reversible wafer bonding, using low- or high-temperature waxes (up to 170°C), requires a wax coating step in liquid phase. The highest level of uniformity for the spin-coated wax is essential.

The bonding strength for a wax layer is large enough to withstand even harsh mechanical processes such as grinding and polishing. For the release of the device wafer from the carrier substrate, two methods can be used: The wax can be dissolved in a solvent or it can be softened and released by heating.

Temporary bonding and debonding with dry-film laminates

The recently increasing popularity of dry-film adhesive tapes, especially for thermal-release bonding, can be attributed mainly to the ease of the application and the enhanced thermal release temperature.

A novel thinning technique

The mechanical properties of ultra-thin and compound semiconductor wafers, such as brittleness, generate difficulties in wafer handling through the multistep processes involving cleaning, coating, lithography, etching or thin-film deposition. Whenever standard silicon material thickness falls below 100 μm the material properties become similar to those of brittle compound semiconductor materials such as GaAs.

A new method of singulating by back etching/grinding is shown in Figure 2. Front side grooves are cut in the wafer streets before back grinding. Chip separation takes place during backside thinning when finally the front side grooves are opened. If the last step is a backside spin-etching process, grooves are rounded by the etchant and possible residual micro-cracks are removed. The etchant can also act as stress relief to the singulated chips.

Conclusions

All the necessary processes to create ultra-thin devices are available and only need to be refined. The fragility of the wafer structure before singulation demands special procedures in order to complete the processing. After the wafer has been singulated into chips, the problems of fragility diminish. The development of through-hole interconnect and chip stack, be it in chip or wafer form, brings the back end process into the fab. This implies greater process control from start to finish. Back-end processing has always been considered as outside the fab environment. Bringing it inside will only benefit the final device reliability.

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