Exhibit G

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Thinning Wafers For Flip Chip Applications, High Density Interconnect

May, High Density Interconnect

By David Francis **Introduction**

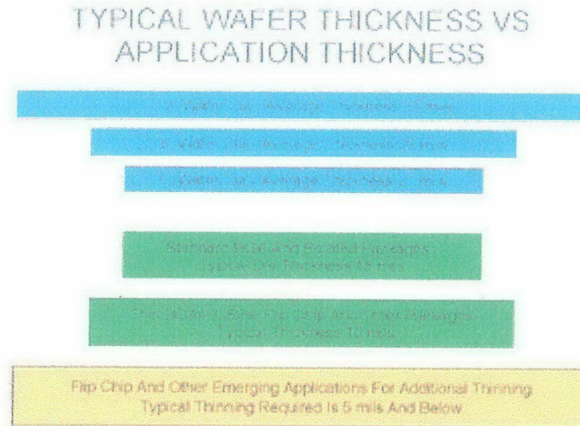
Historically, wafer thinning has been used on flip chip devices when necessary to achieve a uniform thickness across multiple devices in high perfomance MCMs. Individually packaged flip chip devices, where heat was not a problem were seldom. Where heat was a problem, itwas necessary to thin wafers in order to achieve a more consistent thermal path from the die to the external heat sink. The poor thermal conductivity of most interface materials made the gap between the back of the die and the package lid or heat spreader, a very key thermal parameter.

For most applications, flip chip wafers were not thinned. Today, that is changing. A number of new packages and applications are requiring that all die used in these packages must be thinned whether they are wire, TAB or flip chip bonded. The amount of thinning depends onthe specific package and how it is being used. Flip chip packages and applications requiring thinner die: Ball Grid Arrays (BGAs), Chip Scale Packages (CSPs), Multichip Modules (MCMs for uniform thermal and dimensional properties), Smart Cards, Flip Chip On Board, TAB On Board (includes Flex).

Flip chip technology is growing due to the need for higher I/O and increased performance. Where several hundred I/O was considered high, new generations of devices will have thousands of I/O and operate at frequencies greater than 1 GHz. As these flip chip devices begin to be used in these new packages and applications, the problem of thinning wafers that are to be bumped becomes a major problem.

Removal Requirements Increasing

Wafer thickness is increasing as wafer size increases. The following figure shows the increase in wafer thickness for increasing wafer diameter.



At the same time, the trend is to thinner die. Standard BGA and other semiconductor packages typically require die to have a thickness of 20 mils (500 microns) or more while the new, thinner packages are requiring die to have a thickness of 10 mils (250 microns) or less. New flip chip and emerging applications are requiring thickness levels below 250 microns with some down to 50 microns and below. The thinner the requirement and the larger the wafer, the greater the amount of silicon that must be removed. The following figure shows the amount of silicon (in cubic inches) that must be removed from various wafer sizes in order to achieve the desired thickness.

How To Thin

Grinding

The first method used to thin wafers was grinding, and early processes caused warpage of the wafer and other damage. Warpage could be as much as 25 mils across a 6" wafer. This warpage combined with the surface damage caused by grinding, made it relatively easy to crack wafers during subsequent processing operations.

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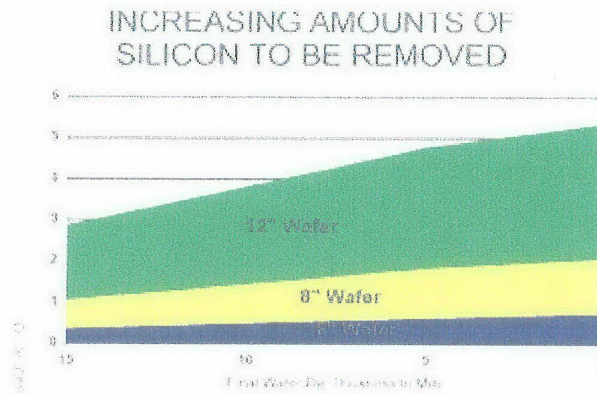

There have been numerous improvements to the grinding operation from better machine and feed design to the use of multiple grinding steps. The first or coarse grind is typically followed by a finer grinding step. The coarse grind removes most of the material while the fine grind step reduces the damage done to the back surface of wafer. The grinding process is the most efficient process for removing relatively large amounts of silicon at a very modest cost and with high throughput for thickness' above 10 mils (250 microns). Below 10 mils, the fragile nature of the silicon material increasingly dominates, and gentler methods are required. While it is possible to further reduce the damage on the back side of the wafer by using finer grinding methods, this process rapidly becomes uneconomical. The result is that grinding is not a satisfactory end process for most wafer thinning requirements.

Wet Etching

A big improvement in wafer thinning came with the addition of wet chemical etching. This process follows the grinding step and it can be used to remove the damaged layers from the back surface of the wafer.

Industry experts indicate that the damage depth can be as much as 50-100 microns of the back surface of a wafer can remain damaged after grinding. The first 10% of the damage contains surface damage and micro-cracks with the remaining region containing varying degrees of structural damage. Depending on the application, this structural damage can cause degradation of electrical properties.

A drawback with any wet etching process is that protection of the front surface of the wafer is required so that it is not damaged during processing. The need to protect the front surface of the wafer adds to several steps to the process as well as increasing the overall wafer cost.

The benefits of wet etching are that it can substantially reduce the stress level in the wafer and reduce the warpage. Removal of the micro-cracks and the lattice dislocations results in a much stronger wafer which can be handled and shipped less breakage.

It is not practical to use a wet etching process with bumped wafers. Wet etching will also find increasing difficulty as wafer thinning requirements drop below 10 mils. The need to protect the front surface of the wafer from the etching process requires the application (and removal) of some type of protective film or resist. The thinner the wafer becomes, the more likely this process will begin to impact the process yield.The extra steps required and the increasing fragility of wafer will result in increased damage to the wafer.

Plasma Etching (Dry Etching)

Plasma etching has previously been done using a vacuum, but this process is very slow and not suitable for mainstream production.

A new process that results in orders of magnitude faster rapid removal of silicon than vacuum plasma etching and which does not contact the front surface of the wafer is atmospheric downstream plasma (APD) etching. This new process is an ideal process for very thin die or wafers and those with bumps.

The ADP process provides etch rates that are at least 20X higher than comparable vacuum plasma systems. In addition, vacuum pumps and chambers are not required and all of the environmental problems associated with wet etching are also eliminated.

The ADP system brings the gases to the plasma region where they are 100% decomposed and available for reaction at the surface of the wafer. Because the reaction occurs at atmospheric pressure, any charged particles quickly recombine outside the plasma area so that dielectric surfaces do not become charged.

Wafers do not touch the holder surface during processing. Using a modified Bernoulli lifting force, gas flowing over the wafer surface prevents contact. Vortices create an additional lifting force on the wafer. The gas escapes the holder at the edge of the holder and this causes the wafer to remain centered. The escaping gas from the holder prevents the front side wafer from reaching etch gases on the front side circuitry. Most important, the holder does not constrain the wafer in any way, and therefore, does not stress the wafer.

The ADP system will remove 200 microns on 200 mm wafers with 3 microns in one sigma. For applications requiring a thickness less than 10 mils, the best process is to use coarse grinding to an intermediate thickness (e.g. 10-15 mils) followed by ADP plasma etching.

The ADP process is well-suited for handling bumped wafers and for wafers destined to be thinned to thickness' well under 10 mils. After a coarse grind and cleaning, the wafers are run through the ADP process to remove all of the micro-cracks and stress from the wafer. This process provides a robust wafer that has sufficient strength to withstand whichever flip chip bumping process is used.

For wafers that are to be thinned to 5 mils and below, the ADP process is sufficiently rapid and benign so that wafers can be thinned to

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their final thickness. The ADP etch process is a development of Tru-Si Technologies (www.trusi.com, Sunnyvale, CA, Ref. 1).

When To Thin

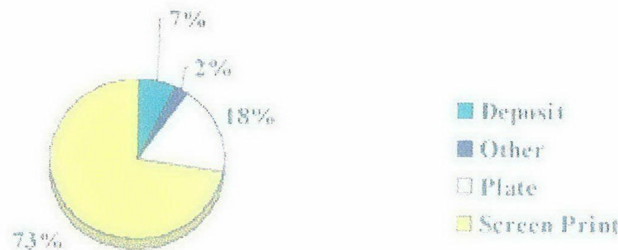
In working with flip chip wafers, WHEN TO THIN becomes a major issue. It would be highly desirable to thin the wafers to their final thickness before bumping, but once the thickness drops below 10 mils, the current bumping processes begins damaging wafers. There are a wide variety of bumping processes with a general breakdown of the major methods shown in the following pie chart.

Screen printing is the method used to produce the largest volume of wafers and this process requires the wafer be placed in a suitable fixture and vacuum clamped while the solder paste is applied through a screen or stencil. This is a relatively rugged process and using wafers thinned to less than 10 mils is not really viable. The problem becomes more acute as the wafer size increases.

The other bumping processes, while not as stressful, do require handling of the wafer, clamping to a suitable fixture, and other steps that can easily break a thin wafer.

To thin a wafer that has already been bumped has been impractical until recently because there has been no practical process for doing so. The ADP process by Tru-Si Technologies is the first approach that offers a viable approach to thinning wafers after the bumps have been applied.

FLIP CHIP BUMPING METHODS



Some applications require a wafer thickness below 10 mils together with some type of bumping. The recommended process is to grind the wafer to a convenient thickness such as 15 mils or 20 mils and then use the ADP process to remove approximately 25 microns of material to produce a wafer that is sufficiently rugged to withstand the bumping operation. Once the bumping operation (inspection and testing) is completed, the wafers can be returned to be thinned to their final thickness. Since no front side protection is required, wafers can be thinned to whatever thickness is desired for the final application after bumping.

New Applications Require Thinner Wafers And Die (Why ?)

A number of new applications (Ref. 2) are emerging that will require wafer thinning below 10 mils. Some of these are:

- Reduce stress on solder bumps
- Smart cards
- CSPs for handheld, portable and miniature applications (e.g. memory modules)
- 3D stacking applications and other emerging applications.

Although focus in this article is primarily on flip chip, we will discuss some of other advantages to thinning flip chip wafers below 10 mils.

Reduced Solder Bump Stress

The thermal expansion mismatch between silicon and most other packaging materials is well known. For highest reliability, it is best to mount flip chip devices on a material that matches the expansion coefficient of silicon as closely as possible. While this is the best solution, it also tends to be the most expensive one. A much lower cost solution is to use organic materials made of epoxy glass. These materials have an expansion coefficient about five times larger than that of silicon.

Whether the application is BGA, CSP or flip chip on laminate (FCOB), the stress level generated in the solder joint is much less if the wafer/chip is substantially thinned.

Normally the weakest part of a flip chip solder joint is the place where the solder attaches to the pads on the IC. This is because the IC pads typically have the smallest area and when this is combined with the rigid nature of relatively thick silicon, it is relatively easy to generate stress cracks where the solder attaches to the pad metallization.

The problem of solder joint failure can be reduced by using a suitable underfill material which acts to spread the applied stress over the entire surface of the ball rather than allow it to be concentrated at the weakest part.

However, increases in the number of I/O are requiring that the solder ball size be made ever smaller. The smaller solder ball size combined with the increasing difficulty of getting underfill to flow under the chip when the spacing becomes very small makes thinning of the flip chip wafer even more important.

Smart Cards

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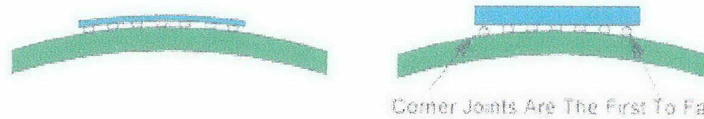
Smart cards frequently fail because of high mechanical stress that is applied to cards during normal use. Whether the cards are in someone's wallet, used in imprinters or in point-of-sale terminals, the stress levels can periodically be very high.

A THINNED FLIP CHIP DEVICE IS BETTER ABLE TO WITHSTAND STRESSES CAUSED BY BOARD FLEXING OR TEMPERATURE CYCLING



Corner Joints Are The First To Fail

The typical card thickness is 0.030" and if room is allowed for the interconnect structure and the housing this leaves about 0.011" as the maximum die thickness. However, at this thickness, the silicon still behaves like an unbendable slab. One solution to this problem is to thin the chip to 4-7 mils or less. The thinner the chip, the more flexible the chip becomes. Assuming the right process is used, the thinner the chip, the better the long term reliability because the chip becomes more flexible, and thus the amount of stress generated is much lower.

In addition to thinning, the stress can also be reduced by locating the surface of the chip as close to the neutral plane of the card as possible. This is illustrated in the following figure. Assuming that 19 of the 30 mils of thickness is spent on the interconnect and the housing, it is impossible to use a die of standard thickness and still have it in the proper location.

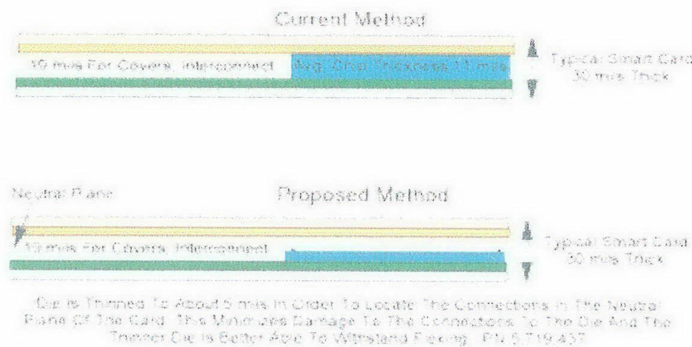
Another benefit of making the chip thinner is that many smart cards use RF coupling to transfer information between the chip and the reader. Silicon is a material that attenuates RF signals. The thinner the die, the less the attenuation. This means that with less attenuation, the coupling distance between the card and the reader is less critical.

Smart cards can contain more than a single chip. Cards may contain multiple die including microprocessors, memory, voltage or data conditioning die as well as passive components.

Advanced Memory Modulee and 3D Stacking Applications

Standard memory modules are those used in computer equipment whereas advanced memory modules are those used in cameras and similar products.

LOCATING THIN DIE IN A SMART CARD TO MINIMIZE MECHANICAL DAMAGE



Die Is Thinned To About 5 mils In Order To Locate The Connections In The Neutral Plane Of The Card. This Minimizes Damage To The Connections To The Die And The Thinner Die Is Better Able To Withstand Flexing. Pat 5,719,437

There is a wide range of these small memory cards and the market for these products is growing rapidly. The smaller the card size, the more desirable the product and the larger the amount of memory that can be used by the application. Typically the average digital camera picture requires about a megabyte of storage so that the size of the memory card determines how many pictures can be taken and stored on a single 32 Mbyte card. As picture resolution increases, so does the demand for more memory storage. Being able to stack memory makes it possible to greatly increase memory capacity. A number of companies make 3D memory modules because it provides the greatest concentration of memory in the smallest volume of area and this translates into the highest performance. The following figure illustrates in a simplistic way, the benefits of thinning memory devices, particularly when they are to be stacked.

Several companies have developed approaches for stacking memory devices. One company is Irvine Sensors (www.irvinesensors.com) which stacks the chips and then forms the interconnect structure on the edge surface of the stack. The stacks are flip chip bonded to the next level interconnect.

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