Exhibit B

A Review of 3-D Packaging Technology

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***Abstract*— This paper reviews the state-of-the-art in three-dimensional (3-D) packaging technology for very large scale integration (VLSI). A number of bare dice and multichip module (MCM) stacking technologies are emerging to meet the ever increasing demands for low power consumption, low weight and compact portable systems. Vertical interconnect techniques are reviewed in details. Technical issues such as silicon efficiency, complexity, thermal management, interconnection density, speed, power etc. are critical in the choice of 3-D stacking technology, depending on the target application, are briefly discussed.**

***Index Terms*— Bare dice stacking, MCM stacking, 3-D MCM technology, 3-D packaging, vertical interconnection.**

I. Introduction

As the complexity of portable electronic systems increases, such as in the shift from the mobile phone toward the Interactive Mobile Multimedia Personal Communicator (IM^3PC) paradigm [1], greater demands are being placed on the production of low power, low weight and compact packaging technologies for VLSI integrated circuits. Likewise many aerospace and military applications are following this trend. In order to meet this demand, many new three-dimensional (3-D) packaging technologies are now emerging where either bare dice or MCM's are stacked along the z-axis, resulting in dramatic improvement in compactness. As this z-plane technology results in a much lower overall interconnection length, parasitic capacitance and thereby system power consumption can be reduced by as much as 30% [2].

Section II will discuss the advantages of 3-D packaging technology and its effect on system performance. Section III will provide a brief discussion of the different vertical interconnection methods used in 3-D packaging, while Section IV will address the limitations of the 3-D technology.

II. Advantages of 3-D Packaging Technology

The following subsections discuss briefly how 3-D packaging technology enhances system performance and provides performance factors that cannot be achieved using conventional packaging technologies.

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A. Size and Weight

By replacing single chip packages with a 3-D device, substantial size and weight reductions are achieved. The magnitude of these reductions depends, in part, on the vertical interconnection density and accessibility, which will be discussed in Section II-G, thermal characteristics, and robustness required. It has been reported that 40 to 50 times reduction in size and weight is achievable using 3-D technology compared to conventional packaging. As an example, volume and weight comparisons between TI's 3-D bare dice packaging and discrete and planar packaging (MCM) are presented in Tables I–VII. It is evident from these tables that a five to six times reduction in volume is possible over MCM technology and a ten to 20 times reduction over discrete packaging technology. Moreover, a two to 13 times reduction in weight is also achievable compared to MCM technology and a three to 19 times reduction compared to discrete components. All of these reductions result from eliminating the overhead weight and size associated with conventional technologies. Furthermore, in the case of the Aladdin parallel processor [3], the reduction in size and volume against the Cray X-MP benchmark was by about 660 and 2700 times, respectively.

B. Silicon Efficiency

One of the main issues in packaging technology is the chip footprint, which is the printed circuit board area occupied by the chip [5] as defined in Fig. 1. In the MCM case, the footprint is reduced by 20–90% because of the use of bare dice. Three-dimensional packaging results in a even more efficient utilization of silicon real estate, which is referred to as "silicon efficiency." We can define silicon efficiency as the ratio of the total substrate area in a stack to the footprint area. Consequently 3-D technology exceeds a 100% silicon efficiency compared to other two-dimensional (2-D) packaging technologies.

C. Delay

Delay refers to the time required for a signal to travel between the functional circuit blocks in a system. In high speed systems, the total delay time is limited primarily by the time of flight, which is defined as the time taken for the signal to travel (fly) along the interconnect [6]. The time of flight, t, is directly proportional to the interconnect length. So reducing the delay requires reducing the interconnect length which is the case when using 3-D packaging, as shown in Fig. 2. The resultant reduction in interconnect length, results in a reduction of the interconnect associated parasitic capacitance and inductance, hence reducing signal propagation delays. For example, the signal delay as a result of using MCM's is reduced by about 300%. Furthermore, the delay would be less in case of 3-D

TABLE I
3-D MASS MEMORY VOLUME AND WEIGHT COMPARISONS BETWEEN OTHER TECHNOLOGIES AND TEXAS 3-D TECHNOLOGY IN cm^3/Gbit [4]

	Type	Capacity	Discrete	2D	3D	Discrete /3D	2D /3D
Weight	SRAM	1 Mbit	1678	783	133	12.6	5.9
		4 Mbit	872	249	41	21.3	6.1
	DRAM	1 Mbit	1357	441	88	15.4	5.0
		4 Mbit	608	179	31	19.6	5.0
		16 Mbit	185	69	69	16.8	6.2
Volume	SRAM	1 Mbit	3538	2540	195	18.1	13.0
		4 Mbit	1588	862	145	10.9	5.9
	DRAM	1 Mbit	2313	1542	132	17.5	11.6
		4 Mbit	862	590	113	7.6	5.2
		16 Mbit	363	227	113	3.2	2.0

TABLE II
A LIST OF MOST OF THE COMPANIES AND INSTITUTIONS WORKING IN THE AREA OF 3-D PACKAGING [78]

Bare Die stacking		Packaged Die stacking	
Standard ICs	**Custom ICs**	**Standard Package**	**Custom Package**
Actel	IBM	Mitsubishi	CTS
Implex	Irvine Sensors	Thomson-CFS	Dense-Pac
Matsushita (MEI)	Fujitsu	Samsung Electronics	Grumman
Thomson-CFS	Hughes	Texas Instruments	Harris
Hitachi & Intel	Texas Instruments	nChip, Inc.	Hitachi
Valtronic, Inc.	Matsushita	NEC Corp.	Motorola
AT&T		Irvine Sensors	RTB Technology
		Cray Research, Inc.	Staktek
		Harris	Trymer

TABLE III
TABLE II CONTS

MCM stacking	Wafer stacking
Custom Modules	**Custom Wafers**
AT&T	Mass Memory Technology
Raytheon (E-Systems)	Hughes
General Electric	ATT
Hughes	NTT and Thomson-CSF
Matra Marconi Space	General Electric &
Matsushita (MACO)	USAF Philips Lab.
Motorola	Cubic Memory
Honeywell and Coors	
RCMT@Berlin Uni	
Lockheed	
Jet Propulsion Lab.	

technology because the electronic components are in close proximity to each other, as shown in Fig. 2.

D. Noise

Noise in general can be defined as unwanted disturbances superimposed upon a useful signal, which tend to obscure its information content. In high performance systems, noise management is a major design issue. Noise can limit the achievable system performance by degrading edge rates, increasing delays, and reducing noise margins and can cause false logic switching. The noise magnitude and frequency are closely tied to the packaging and interconnect scheme used. In a digital system four major sources of noise can be identified as:

1) reflection noise;
2) crosstalk noise;
3) simultaneous switching noise;
4) electromagnetic interference (EMI) [7].

The magnitude of all of these noise sources depends on the rise time of the signals passing through the interconnect. The faster the rise time, the worse the noise. The role of 3-D technology in reducing noise is in the reduction of interconnection length, and hence reduction of the associated parasitics which translate into performance improvements. On

TABLE IV
AN EVALUATION OF COMPANIES WHICH PROVIDE PERIPHERY INTERCONNECTION BETWEEN STACKED IC's

Company	Application	Country	Interconnection Technique
Matsushita	Memories	Japan	Stacked TAB carrier (PCB)
Fujitsu	Memories	Japan	Stacked TAB carrier (leadframe)
Dense-Pac	Memories	USA	Solder dipped stacks to create vertical conductors on edge
Micron Technology	Memories	USA	Solder filled holes in chip carriers and spacers
Hitachi	Memories	Japan	Solder connections between plated through hole
Irvine Sensors	Memories/ASICs	USA	Thin film 'T-connects' and sputtered metal conductors
Thomson-CFS	Memories/ASICs	France	Direct laser write traces on epoxy cube face
Mitsubishi	Memories	Japan	PC boards soldered on two sides of TSOP packages
Texas Instruments	Memories/ASICs	USA	Array of TAB leads soldered to bumps on silicon substrate
Grumman Aerospace	ASICs	USA	A flip-chip bonded to faces of the stack
General Electric	ASICs	USA	Folded flex circuits
Harris	ASICs	USA	Folded flex circuits
MCC	ASICs	USA	Folded flex circuits
Matra Marconi	Memories	France	Wire bonded to an MCM substrate directly
Voltonic	ASICs	USA	Wire bonded to a substrate through an IC

TABLE V
AN EVALUATION OF COMPANIES WHICH PROVIDE AREA INTERCONNECTION BETWEEN STACKED IC's

Company	Application	Country	Interconnection Technique
Fujitsu	ASIC	Japan	Flip-chip bonded Stacked Chips without spacers
University of Colorado & UCSD	Optoelectronic	USA	Flip-chip bonded Stacked Chips with spacers
Hughes	ASIC	USA	Microbridge springs and thermomigration vias

TABLE VI
AN EVALUATION OF COMPANIES WHICH PROVIDE PERIPHERY INTERCONNECTION BETWEEN STACKED MCM's

Company	Application	Country	Interconnection Technique
Matsushita	Memories	USA	Solder leads on stacked MCMs
General Electric	ASIC	USA	HDI-thin film interconnect laminated to side of stack
Harris	Memories	USA	Blind castellation interconnection
CTS Microelectronics	Memories	USA	Blind castellation interconnection
Trymer	Guidance Systems	USA	Solder dipped stacks to create vertical conductors on edge

TABLE VII
AN EVALUATION OF COMPANIES WHICH PROVIDE AREA INTERCONNECTION BETWEEN STACKED MCM's

Company	Application	Country	Interconnection Technique
Raytheon (E-Systems)	ASIC	USA	Fuzz buttons in plastic spacer and filled vias in substrate
Technical University of Berlin	ASIC	Germany	Elastomeric connectors with electrical feedthroughs
AT&T	ASIC / multi-processor array	USA	Compliant anisotropic conductive material
Hughes	ASIC / avionics	USA	Microbridge springs and thermomigration vias
Motorola	Not in Use	USA	Solder balls on top and bottom of substrate layers
Micron Technology	Memories	USA	Stacked silicon wafers with filled vias
Lockheed	ASIC / IR processors	USA	Stacked silicon wafers with filled vias

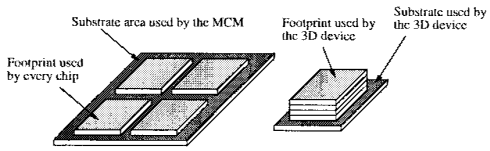

Fig. 1. A graphical illustration of the silicon efficiency between MCM's and 3-D technology.

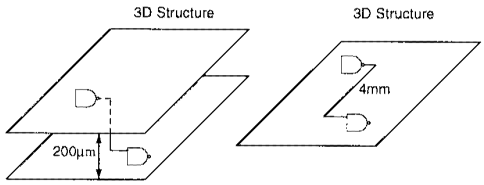

Fig. 2. A comparison between the wiring lengths in 2-D and 3-D structures [79].

the other hand, the noise could be problematic in a system if the used 3-D technique does not address the noise. For example, if the interconnections have not got a uniform impedance along the line or its impedance does not match the source and destination impedance, there is the potential for reflection noise. Furthermore, if the interconnects are not spaced enough there is also a potential for crosstalk noise. Simultaneous is reduced because of the shortened interconnects and consequent reduction of the associated parasitics, so producing less simultaneous noise for the same number of interconnections.

E. Power Consumption

In an electronic system the energy dissipated, E, due to the interconnect parasitic capacitance, C, is given by, $E = CV^2$, and therefore the power consumption is $P = fCV^2$, where V is the voltage swing across the C and f is the number of transitions per second. As the parasitic capacitance is proportional to the interconnection length, the total power consumption is reduced because of the reduced parasitics. For example, let us say that 10% of the system power consumption is dissipated in the interconnects when mounted on a PWB. If the product was implemented using MCM technology, the power consumption will be reduced by a factor of five. Hence, the product would consume 8% less power than the PWB-base product [8]. Furthermore, when such a product is implemented using 3-D technology the saving will be much more because of the reduced interconnect length and the associated parasitics.

F. Speed

The power saving achieved using 3-D technology can allow the 3-D device to run at a faster rate of transitions per second (frequency) with no increase in power consumption. In addition, the reduction in parasitics (capacitances and inductances), size and noise of a 3-D device, allow for higher transitions per second which would increase the overall system performance. For example, the Aladdin parallel processor, achieved 35 000 and 10 800 in MIPS and FLOPS per unit volume improvement

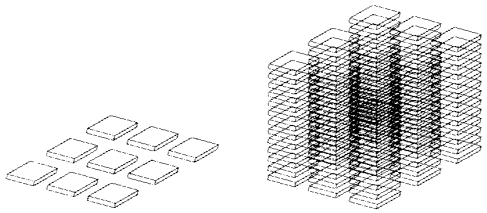

Fig. 3. A comparison between 2-D and 3-D packaging interms of the accessability and useablity of interconnection.

over the Cray X-MP as a result of integration using 3-D MCM technology [3].

G. Interconnect Usability and Accessibility

The use of a 3-D packaging configuration provides access to 116 neighbors within an equal interconnect length to a centre element in the stack, in contrast to eight neighbors to the centre element in the case of 2-D packaging technology, while assuming a typical die thickness of 0.6 mm [9], [10] as illustrated in Fig. 3. Hence, reduction of the interconnect length in the stack results in reduction of propagation delay between chips. Furthermore, the available vertical interconnection results in maximum utilization of the available interconnects in contrast to traditional packaging technologies where such utilization is limited by physical structures such as vias or holes or by previously routed interconnects (Fig. 4). The accessibility in case of 3-D packaging technology depends on the type of vertical interconnection employed as it is proportional to the available vertical interconnect density—which is defined as the number of signal layers per average wire pitch [11], [12]. So, area interconnection provides the most accessibility and usability in contrast to peripheral interconnections, where the usability and accessibility are limited by the periphery length of the stacked element.

H. Bandwidth

Interconnect bandwidth, especially memory bandwidth, is often the performance limiter in many computing and communications systems. Thus low latency (delay) and wide buses are very desirable. For example, in the well known Intel Pentium Pro, the CPU and Level 2 cache are packaged together in the same multi-cavity Pin Grid Array to obtain a large memory bandwidth. The exciting possibility is whether 3-D packaging technologies can be used to integrate a CPU and memory chips while avoiding the cost of the multicavity Pin Grid Array.

III. Vertical Interconnections in 3-D Electronics

Vertical Interconnections [13], [14] refer to the interconnections needed to route power, ground, and signals to the layers within the 3-D Module. The following subsections will describe briefly the different types of vertical interconnections.

A. Periphery Interconnection Between Stacked ICs

The following subsections will list interconnection techniques used to interconnect stacked chips using the stack periphery.

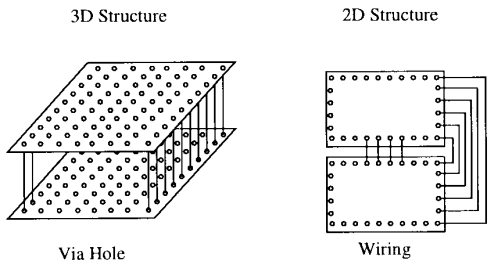

Fig. 4. A comparison between 3-D and 2-D structures in terms of the possible number of interconnections assuming one routing layer for the 2-D structure [79].

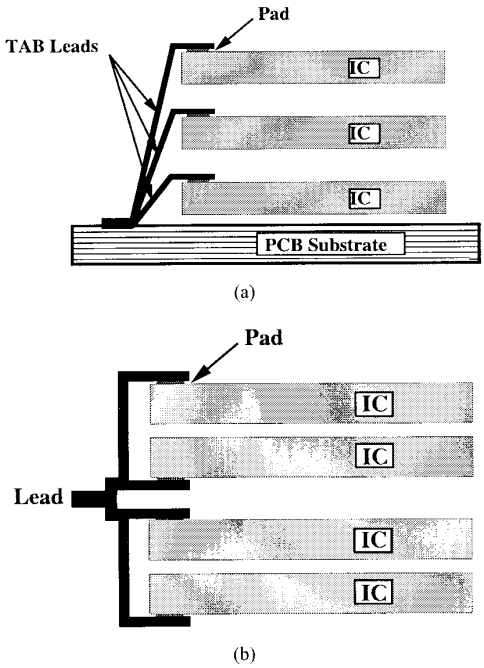

Fig. 5. Two variants of the stacked tape carrier vertical interconnect: (a) stacked TAB on PCB and (b) stacked TAB on leadframe.

1) Stacked Tape Carrier: Stacked tape carrier is a method for interconnecting IC's using TAB technology. This method could be divided further into stacked TAB on PCB and stacked TAB on leadframe as illustrated by the schematic diagram shown in Fig. 5. The TAB on PCB method is used by Intel Japan [15] and Matsushita Electric Industrial Company [16], [17], [18]. In Matsushita's case, they used this approach for designing high density memory cards. The second method is used by Fujitsu in designing DRAM chips [19], [20].

2) Solder Edge Conductors: Solder edge conductor bonding is a process where vertical interconnections between IC's are performed by soldering edge conductors. There are four variants of this method as follows.

a) *Solder dipped stacks to create vertical conductors on edge:* In this approach, the leads of the stacked IC's that are to be connected, are brought into contact using a static molten solder bath and simultaneously soldered. A schematic diagram on how such interconnections are performed is shown in Fig. 6(a). This method is used by Dense-Pac for designing high density memory modules [21], [22], [23].

b) *Solder-filled holes in chip carriers and spacers:* In this approach the vias are filled with a conductive material to interconnect the stacked IC using carriers and spacers as shown in Fig. 6(b). This method is used by Micron Technology in designing DRAM and SRAM chips [24]. A similar technique was developed and patented by Hughes Electronics [25].

c) *Solder connections between plated through-hole:* In this approach the IC leads are brought by TAB then interconnected using a small PCB called a PCB frame, which has vias through it. The vertical interconnections are achieved using these vias and by stacking these frames using a solder joint bonding technique as shown in Fig. 6(d). Hitachi has developed this method and used it in the design of high density DRAM's [26].

d) *Edge array solder balls:* In this approach, solder balls are placed along the edge of the chip and the chip is edge mounted on the substrate using solder reflow. For example, Hughes achieved this by dicing through the solder ball [27]. MCNC has achieved this by shaping the solder ball so that it "overhangs" the chip edge [28]. MCNC is also capable of rerouting the pads to the edge of the chip as shown by the photograph of an early prototype in Fig. 7.

3) Thin Film Conductors on Face-of-a-Cube: A thin film is a layer of conductive material either sputtered or evaporated onto a substrate in a vacuum to form conductors. 'Thin film conductors on face-of-a-cube' is a method where vertical interconnections are performed on the cube face. There are two variants of this method as follows.

a) *Thin film "T-connects" and sputtered metal conductors:* This method was jointly developed by Irvine Sensors and IBM. In this method, after the I/O signals are rerouted to one edge of the chip, a thin film metal layer is patterned on the surface of the stacked chips. Then, two processes, called lift-off photolithography and sputter-deposition, are performed on the face of the stack to form pads and buslines, creating what is called "T-connections" [29] as shown in Fig. 8.

b) *Direct laser write traces on epoxy cube face:* In this method, the interconnect pattern on the sides of the cube is generated by laser trimming. This pattern is designed to intersect with the IC's wires cross section on the face of the cube [30], [31] as shown in Fig. 9. This method is used by Thomson-CFS DOI for high density memories [30], microcameras [32], [33], medical applications and smart munitions [34], [31].

4) An Interconnection Substrate Soldered to the Cube Face: In this method a separate substrate is soldered to the face of the cube as will be explained by the following variants of the method.

a) *Array of TAB leads soldered to bumps on silicon substrate:* This method was developed and used by Texas Instruments in the design of very high density memories [35], [36], [37]. The vertical interconnections are

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