

Exhibit L

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application Type:	Utility	Status Date:	09-23-2015
Examiner Name:	<u>CHIU, TSZ K</u>	Location:	ELECTRONIC
Group Art Unit:	2822	Location Date:	-
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First Named Inventor:	Glenn J. Leedy , Parkland, FL (US)	Issue Date of Patent:	-
First Named Applicant:	-	International Registration Number (Hague):	-
Entity Status:	Small	International Registration Publication Date:	-
AIA (First Inventor to File):	No		

Title of Invention: THREE DIMENSIONAL STRUCTURE MEMORY

AMENDMENT

Sir:

Please amend the claims as follows:

Amendments of the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1-87. (canceled)

88. (Currently amended) A stacked integrated circuit memory comprising:

at least one logic integrated circuit, wherein the at least one logic integrated circuit is one of: a thin substantially flexible integrated circuit, and capable of forming a thin substantially flexible integrated circuit;

at least one thin substantially flexible memory integrated circuit positioned in a stacked relation to said at least one logic integrated circuit; and

interconnections electrically connecting the at least one logic integrated circuit and the at least one thin substantially flexible memory integrated circuit;

wherein at least one of the at least one logic integrated circuit and the at least one thin substantially flexible memory integrated circuit comprises a monocrystalline semiconductor substrate of one piece; and

wherein the at least one of the at least one logic integrated circuit and the at least one thin substantially flexible memory integrated circuit has formed thereon a ~~low stress silicon based dielectric layer having a stress of less than 5×10^8 dynes/cm² tensile~~ plurality of dielectric layers having a combined thickness and including one or more

silicon-based dielectric layers that are flexible, the one or more dielectric layers that are flexible comprising a majority of the combined thickness.

89. (Currently amended) The stacked integrated circuit memory of claim 88, wherein the interconnections electrically connecting the at least one logic integrated circuit and the at least one thin substantially flexible memory integrated circuit are vertical interconnections internal to the stacked integrated circuit memory; and wherein the one or more silicon-based dielectric layers that are flexible have a stress of less than 5×10^8 dynes/cm² tensile.

90. (Currently amended) The stacked integrated circuit memory of ~~claim 88~~ claim 89, wherein at least one of the logic integrated circuit and the at least one thin substantially flexible memory integrated circuit comprises one of a single crystal semiconductor material and polysilicon semiconductor material.

91. (Currently amended) The stacked integrated circuit memory of ~~claim 88~~ claim 89, wherein at least one of the at least one logic integrated circuit and the at least one thin substantially flexible memory integrated circuit have a thickness of less than about 50 microns.

92. (Currently amended) The stacked integrated circuit memory of ~~claim 88~~ claim 89, wherein at least one of the at least one logic integrated circuit and the at least one thin

substantially flexible memory integrated circuit have a thickness of less than about 10 microns.

93. (Currently amended) The stacked integrated circuit memory of ~~claim 88~~ claim 89, wherein the at least one thin substantially flexible memory integrated circuit has a different process technology from the at least one logic integrated circuit.

94. (Previously presented) The stacked integrated circuit memory of claim 93, wherein the different process technology is one of DRAM, SRAM, FLASH, EEPROM, EPROM, Ferroelectric and Giant Magneto Resistance.

95. (Currently amended) The stacked integrated circuit memory of ~~claim 88~~ claim 89, wherein at least one of the at least one logic integrated circuit and the at least one thin substantially flexible memory integrated circuit comprise active circuit devices and passive circuit devices.

96. (Currently amended) The stacked integrated circuit memory of ~~claim 88~~ claim 89, wherein the at least one logic integrated circuit comprises at least two logic integrated circuits, wherein a plurality of data bytes are transferred between the logic integrated circuits with at least some of the interconnections.

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