IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; AND MICRON CONSUMER PRODUCTS GROUP, INC., DEFENDANTS.	)	C.A. NO. 14-01431-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG ELECTRONICS AMERICA, INC., AND SAMSUNG AUSTIN SEMICONDUCTOR, LLC, DEFENDANTS.	)	C.A. NO. 14-01430-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. SK HYNIX INC., SK HYNIX AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC., AND SK HYNIX MEMORY SOLUTIONS INC., DEFENDANTS.	)	C.A. NO. 14-01432-LPS-CJB JURY TRIAL DEMANDED

DECLARATION OF JOHN KAPPOS IN SUPPORT OF DEFENDANTS' CLAIM CONSTRUCTION BRIEF

I, John Kappos, hereby declare the following:

1. I am a partner with the law firm of O'Melveny & Myers and am admitted to practice *pro hac vice* before this Court. I submit this declaration in support of the Defendants' Claim Construction Brief. The facts set forth in this declaration are known to me personally. If called as a witness, I could and would testify competently concerning these matters.

2. Attached hereto as Exhibit A is a true and correct copy of the Declaration of Richard B. Fair Regarding Claim Construction, dated January 17, 2019.

3. Attached hereto as Exhibit B is a true and correct copy of the Responsive Declaration of Dr. Richard B. Fair Regarding Claim Construction, dated February 1, 2019.

4. Attached hereto as Exhibit C is a true and correct copy of the Declaration of Dr. Steven Murray Regarding Claim Construction, dated January 18, 2019.

5. Attached hereto as Exhibit D is a true and correct copy of the Rebuttal Declaration of Dr. Steven Murray Regarding Claim Construction, dated February 1, 2019.

6. Attached hereto as Exhibit E is a true and correct copy of the Declaration of Shefford Baker, dated January 25, 2019.

7. Attached hereto as Exhibit F is a true and correct copy of the Final Written Decision from *inter partes* review proceeding IPR2016-00389 (Paper No. 66). The parties intended to include the Final Written Decision for IPR2016-00389 as an exhibit to their Joint Claim Construction Chart but inadvertently omitted the correct document. *See* D.I. 166-1 at 10; D.I. 166-2 at 5.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that this declaration is executed this 4th day of November 2019, at Newport Beach, California.

/s/ John Kappos

John Kappos

EXHIBIT A

**IN THE UNITED STATES DISTRICT COURT
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**DECLARATION OF DR. RICHARD B. FAIR
REGARDING CLAIM CONSTRUCTION**

I, Dr. Richard B. Fair, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Consumer Products Group, Inc. (collectively "Micron"); and Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC (collectively, "Samsung") as an independent expert in connection with the above-captioned lawsuit to provide my analyses and opinions in certain technical aspects of this dispute. I understand that SK hynix Inc., SK hynix America Inc., Hynix Semiconductor Manufacturing America Inc., and SK hynix Memory Solutions, Inc. (collectively, "SK hynix") join all parts of this declaration except for Sections VI.D-VI.E.

2. The purpose of this Declaration is to analyze and explain how a person of ordinary skill in the art at the time of the alleged inventions would understand certain claim terms in U.S. Patent Nos. 7,193,239 (the "'239 patent"), 7,504,732 (the "'732 patent"), 8,035,233 (the "'233 patent"), 8,410,617 (the "'617 patent"), 8,629,542 (the "'542 patent"), 8,653,672 (the "'672 patent"), 8,791,581 (the "'581 patent"), 8,796,862 (the "'862 patent"), 8,824,159 (the "'159 patent"), 8,841,778 (the "'778 patent"), 8,907,499 (the "'499 patent"), 8,928,119 (the "'119 patent"), and 8,933,570 (the "'570 patent") (collectively, the "Asserted Patents"), which I understand are owned and asserted by Elm 3DS Innovations, LLC ("Elm"). My opinions and the bases for my opinions are set forth below.

3. I am being compensated at my ordinary and customary consulting rate of $600 per hour for my work. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

4. I am competent to testify to the matters stated in this Declaration and have

personal knowledge of the facts and statements herein. Each of the statements is true and correct.

II. BASIS FOR OPINION

A. Qualifications

5. I have summarized in this section my educational background, career history, publications, and other relevant qualifications. A more detailed account of my work experience, qualifications, and publications is included in my curriculum vitae, attached as **Exhibit A** to this declaration.

6. I have been a professor in the Department of Electrical and Computer Engineering at Duke University since 1981. My current tenured position is the Lord-Chandran Professor of Engineering in the Pratt School of Engineering.

7. I received my Bachelor of Science degree in Electrical Engineering from Duke University in 1964. In 1966, I received a Master of Science degree in Electrical Engineering from Penn State University. In 1969, I received a Ph.D. in Electrical Engineering from Duke University.

8. Since 1969, I have been involved in the research, teaching, development, design, and manufacturing of semiconductor devices and processes. For example, I have experience with thin film processes such as physical and chemical vapor deposition methods, modeling semiconductor technology, designing integrated circuits and semiconductor chips, designing high-density memory and analog circuit layouts, and fabricating and packaging integrated circuits. In addition, I have experience in the design, layout, and simulation of analog and digital integrated circuits.

9. From 1969 to 1981, I worked at Bell Laboratories and I had direct experience with the manufacturing, design, and testing of numerous semiconductor devices and integrated

circuits, including metal-oxide-semiconductor (MOS) dynamic memory chips. I researched and developed numerous semiconductor devices, including silicon and gallium arsenide transistors, analog and digital integrated circuits, photovoltaic devices, and thin film transistors ("TFTs") fabricated in laser recrystallized polycrystalline silicon.

10. During my time at Bell Laboratories, I worked on advanced silicon process development in the areas of photolithography, thin film deposition, metallization, etching, cleaning, plasma-assisted processing, LPCVD, ion implantation doping, and annealing/oxidation.

11. In 1981, I became Professor of Electrical Engineering at Duke University. At the same time, I also served in a joint role as Vice President of the Microelectronics Center of North Carolina ("MCNC") in Research Triangle Park, North Carolina. During 1990-1993, I led the Center for Microelectronic Systems. The MCNC and the Center for Microelectronic Systems were devoted to the development of advanced technologies for fabricating integrated circuits and for improvements in semiconductor manufacturing processes in general. My areas of responsibility as Vice President included analog and digital integrated circuit design, system design, semiconductor fabrication technology, advanced multichip module packaging, and studies in electronic materials, including amorphous semiconductors and multi-layered aluminum and copper interconnects. In my division at MCNC, we designed, fabricated, and tested the world's first one-million-transistor processor chip in 1987. I also was responsible for the MCNC analytical lab, which included electron microscopy, atomic composition analysis, and sample preparation for reverse engineering studies.

12. While at MCNC, I helped set up a state-of-the-art CMOS processing facility and directed research on semiconductor processing including photolithography, wafer cleaning, annealing, ion implantation, plasma-enhanced CVD of thin dielectric films, metallization, and

anisotropic etching processes. We conducted research on multi-level metal interconnects, barrier metallurgy, organic and inorganic inter-metal dielectrics, anti-reflective coatings, via and trench etching processes, 3-point wafer bending stress effects, and selective tungsten deposition for via filling. We also had an active research program in characterizing point defects in ion implanted amorphous and single crystal silicon, with the goal of understanding implantation defect annealing effects on dopant impurity diffusion.

13. In 1994, I returned to Duke University full-time. Since then I have continued to teach courses on (1) the design and analysis of analog and digital integrated circuits, (2) semiconductor devices, (3) the chemistry and physics of transistor and integrated circuit fabrication, and (4) thin-film microfluidic devices, fluid dynamics, and applications. In addition, I have an active funded research program that involves undergraduate and graduate students. Areas of research have included silicon cantilever beam sensors, silicon wafer processing by rapid thermal annealing, and microfluidic devices.

14. I have published over 170 papers in refereed and peer-reviewed journals and conference proceedings, contributed chapters to 12 books, edited nine books or conference proceedings, given over 130 invited talks in the field of electrical engineering, and I am a named inventor on 35 granted U.S. patents and 8 pending U.S. patent applications.

15. I am also a Life Fellow of the Institute of Electrical and Electronic Engineers ("IEEE"), a Fellow of the Electrochemical Society, past Editor-in-Chief of the Proceedings of the IEEE, and past Associate Editor of the IEEE Transactions on Electron Devices. I have been listed in Who's Who in America, Who's Who in Engineering, Who's Who in the Semiconductor Industry, Who's Who in Frontiers of Science and Technology, Who's Who in Technology Today, and American Men and Women in Science. I am a recipient of the IEEE Third

Millennium Medal, and I was awarded the Solid State Science and Technology Medal of the Electrochemical Society in April 2003.

16. Based on my over 49 years of experience in thin film and bulk semiconductor device design, processing technology research and development, integrated circuit fabrication, research in point defects in amorphous and single crystal silicon, and the acceptance of my publications and professional recognition by societies in my field, I believe that I am considered to be an expert in the art of semiconductor processing, semiconductor device design and fabrication, and integrated circuit design and fabrication. I have been qualified numerous times as an expert, and I have given expert opinion testimony relating to semiconductor processing, including dielectric material properties, stress analysis, stacked 3D ICs, bonding of stacked layers, and layer-to-layer interconnection. Additionally, I have extensive publications in the field of semiconductor technology, and my accomplishments have been recognized by both academic and professional societies.

B. Materials Considered

17. As part of my preparation for writing this Declaration, I reviewed the Asserted Patents, their prosecution histories, the parties' proposed constructions, and the extrinsic evidence cited in this declaration.

III. LEGAL STANDARDS FOR CLAIM CONSTRUCTION

18. I understand that the words of a claim are generally given the ordinary and customary meaning that the term would have to a person of ordinary skill in the art at the time of the invention.

19. I understand that to determine how a person of ordinary skill would understand a claim term, courts may consider both "intrinsic" and "extrinsic" evidence. I understand that courts look first to the intrinsic evidence of record, which includes the patent itself (including the

claims and specification) and the prosecution history. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises.

20. I understand that a person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which it appears, but also in the context of the entire patent, including the specification and prosecution history. Thus, any explicit definitions of terms or intentional disclaimers or disavowals of claim scope in the specification or prosecution history must be considered in determining the meaning of a claim term.

21. I understand that particular embodiments appearing in the written description do not limit claim language that has broader effect, and that the scope of the claims is not necessarily limited to inventions that look like the ones shown in the figures and described in the specification. However, I also understand that the patentee is required to define precisely what he claims his invention to be, and the claims must be construed in a manner consistent with the specification.

22. I am informed that a term must be interpreted with a full understanding of what the inventors actually invented and intended to include within the scope of the claim as set forth in the patent itself. Thus, claim terms should not be broadly construed to encompass subject matter that is technically within the broadest reading of the term, but is not supported when the claims are viewed in light of the invention described in the specification.

23. I understand that the prosecution file history of the patent provides additional evidence of how both the Patent Office and the inventors understood the terms of the patent, particularly in light of what was known in the prior art. I understand that arguments and amendments made during prosecution may further require a narrow interpretation of a claim term, even if that term is used more broadly in the specification.

24. I understand that differences among claims can also be a useful guide in understanding the meaning of particular claim terms. For example, I am familiar with the doctrine of "claim differentiation" where the presence of dependent claims that add a particular limitation to an independent claim gives rise to a presumption that the limitation in question is not present in the independent claim. However, I understand that "claim differentiation" is not a rigid rule and it cannot overcome a contrary construction dictated by the written description or prosecution history.

25. I understand that patent claims must particularly point out and distinctly claim the subject matter which the inventors regard as the invention. I understand that if a claim term, when interpreted in light of the specification and the prosecution history, fails to inform those skilled in the art about the scope of the claimed invention with reasonable certainty, then the claim term and all claims reciting such term are indefinite. For example, a relative term or term of degree may be indefinite if the patent at issue fails to provide some standard for measuring the degree intended.

IV. THE ASSERTED PATENTS

A. The '239 Patent[1] Specification

26. The '239 patent is entitled "Three Dimensional Structure Integrated Circuit." '239 patent, Cover; 1:1-2. The '239 patent is directed to stacked integrated circuit memory. *Id.*, 1:19-20. The '239 patent describes fabrication methods for three-dimensional integrated circuits

[1] All of the Asserted Patents are related and claim priority to a common application. The specifications of the Asserted Patents are substantially similar. Thus, by identifying portions of the '239 patent specification, this declaration also incorporates all corresponding portions of the patent specification in each of the remaining Asserted Patents.

which include the steps of thinning substrates, bonding the substrates to form a vertical stack, and forming vertical interconnections passing through the substrates. *Id.* at 7:36-11:25.

27. The ’239 patent describes “[g]rind[ing] the backside or exposed surface of the second circuit substrate to a thickness of less than 50 µm and then polish[ing] or smooth[ing] the surface.” *Id.* at 9:25-27; *see also id.* at 11:1. The ’239 patent describes that, by thinning the substrate to a thickness of less than 50 µm and then polishing or smoothing the surface, “[t]he thinned substrate is now a substantially flexible substrate.” *Id.* at 9:25-28; *see also* 3:18-19 (“Thinning of the memory circuit to less than about 50 µm in thickness forming a substantially flexible substrate with planar processed bond surfaces and bonding the circuit to the circuit stack while still in wafer substrate form[.]”). Next, the backside of the substrate is processed to form interconnections that pass through the substrate. *Id.* at 9:57-10:28. The resulting structure is illustrated in Figure 4, reproduced below:

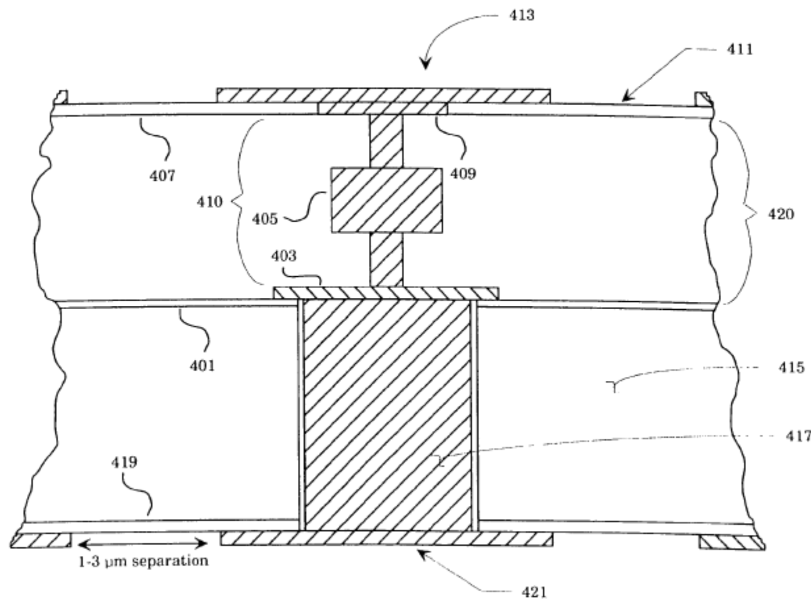

Figure 4

Id. at Fig. 4. As shown in Figure 4, a “feed-through 417” passes through a thinned “substrate 415.” *Id.* at 10:21-24. A “‘DRAM processed’ portion 420 of the wafer” over the thinned

substrate 415 "includes various dielectric and metal layers." *Id.* at 10:13-15. The dielectric and metal layers may include, for example, three metal layers. *Id.* at 10:16-20. Contacts 413 and 421 are formed at matching locations on the top-side (i.e., the transistor-forming side) and bottom-side of the integrated circuit. *Id.* at 10:16-20, 10:26-27.

28. The '239 patent further explains that the substrates, such as that shown in Figure 4 above, are stacked and interconnected to form a three-dimensional integrated circuit. *See id.* at 10:21-30, Figs. 1a-1c. The specification discloses that the substrates are preferably bonded together using thermal diffusion metal bonding. *Id.* at 7:62-64; *see also id.* at 6:52-60, 8:12-54, 9:63-10:5, 11:15-24. Thermal diffusion bonding refers to a process of using heat and pressure to fuse together two metallic surfaces without using additional adhesive or bonding materials. *See id.* at 8:12-54. The specification explains that the "preferred bonding material is pure aluminum or an alloy of aluminum," but that other conductive materials including "Sn [tin], Ti [titanium], In [indium], Pb [lead], Zn [zinc], Ni [nickel], Cu [copper], Pt [platinum], Au [gold] or alloys of such metals" and "highly conductive polysilicon" can also be used. *Id.* at 8:29-40. Although the bonding surfaces may include some non-conductive areas composed of "silicon oxide," there must be some conductive surfaces being bonded in order to form "vertical interconnections" that electrically connects the two circuits. *Id.* at 8:34-45. Indeed, the specification explains that native surface oxides over the conductive pads must be removed prior to bonding in order to avoid "increase[ing] the resistance in the vertical interconnections formed by the bond." *Id.* at 8:41-54.

29. The specification discloses other approaches to bond multiple substrates to form a 3D circuit, such as using "anisotropically conductive epoxy adhesive … to form interconnects between the two" stacked substrates. *Id.* at 6:52-60. An "anisotropically conductive epoxy adhesive" is an adhesive material that conducts electricity in one direction (e.g., in a direction

perpendicular to the substrate surface) but not in another direction (e.g., in a direction parallel to the substrate surface). When "anisotropically conductive epoxy adhesive" is used to bond between two stacked layers, such as two of the circuits show in Figure 4 above, it would form vertical interconnects between the two layers to electrically connect them. *See id.* The specification discloses using conventional input/output ("I/O") bonding methods, such as wire bonding, to connect the stacked 3D integrated circuit to a package substrate or other structures (*see, e.g., id.* at 9:63-10:5, 10:47-50, 11:15-24), but the body of the specification does not disclose using any method other than using vertical, through-silicon interconnects to interconnect multiple layers within a stacked 3D integrated circuit.

30. The specification and claims of the '239 patent also recite the use of low tensile stress dielectrics. *See, e.g.*, *id.* at 8:66-9:16, claim 2. The specification acknowledges that the use of such dielectrics was described years before the earliest alleged priority date of the '239 patent by the named inventor in *Leedy '695*: "The thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication. Such low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695 of the present inventor, incorporated herein by reference." *Id.* at 8:66-9:7. The '239 patent explains that "[t]he use of dielectrics with conventional stress levels could be used in the assembly of" the described 3D ICs, but that "if more than a few layers comprise the stacked assembly, each layer in the assembly will have to be stress balanced so that the net stress of the deposited films of a layer is less than 5×10^8 dynes/cm^2." *Id.* at 9:7-9:12. Other than referencing the disclosure of *Leedy '695*, the specification of the '239 Patent does not contain any other disclosure regarding the structure

and properties of low tensile stress dielectrics.

B. Asserted Claims

31. I understand that Elm has asserted the following claims in this litigation, where brackets indicate a claim asserted only against Samsung Defendants and parentheses indicate claims asserted only against SK hynix Defendants and Micron Defendants:

Asserted Patent	Asserted Claims
U.S. Pat. No. 7,193,239	10, 11, 12, 18, 19, 20, 60, 61, 62, 63, 67, 70, 71, 72, 73, 77
U.S. Pat. No. 7,474,004	20, 21, 22, 23
U.S. Pat. No. 7,504,732	10, [11], 13, 14
U.S. Pat. No. 8,035,233	34
U.S. Pat. No. 8,410,617	51
U.S. Pat. No. 8,629,542	1, 2, 3, 30, 31, 33, 40, 41, 44
U.S. Pat. No. 8,653,672	17, 22, 95, 129, [130], 131, 132, 145, 146, 152
U.S. Pat. No. 8,796,862	34, 36, 135, 136, 137, 138, 147
U.S. Pat. No. 8,841,778	32, 44, 46, 54
U.S. Pat. No. 8,907,499	12, 13, 24, [36], [37], 38, (49), 53, 83, 86, 87, 132
U.S. Pat. No. 8,928,119	18, (33)
U.S. Pat. No. 8,933,570	58, 60, [61], 67
U.S. Pat. No. 8,791,581	(1), 12, 36, 54, 78, 116, 136

32. Claims 1[2], 10, 11, and 60 of the ’239 patent, excerpted below, recite many of the same components and other features described above in the specification.

> **1.** Circuitry comprising: a plurality of monolithic substrates having integrated circuits formed thereon and stacked in layers such that each layer comprises only one of the substrates, wherein at least one of the plurality of substrates is a substantially flexible

[2] Claim 1 is not asserted in this case but is excerpted here because other claims asserted in this case (e.g., claims 10, 11) depend from claim 1.

substrate, and wherein a major portion of the monolithic substrate is removed; and between adjacent substrates, a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof.

10. The apparatus of claim 1, wherein the circuitry is formed with a low stress dielectric.

11. The apparatus of claim 10, wherein the low stress dielectric is at least one of a silicon dioxide dielectric, an oxide of silicon dielectric, and caused to have stress of about $5x10^8$ dynes/cm^2 or less.

60. An integrated circuit structure comprising: a plurality of semiconductor dice, each die having an integrated circuit formed thereon, said dice being stacked in layers, wherein at least one of the plurality of dice is substantially flexible, and wherein at least one of the plurality of dice has at least one of polycrystalline active circuitry formed thereon, reconfiguration circuitry formed thereon, and passive circuitry formed thereon; and between adjacent dice, a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice.

33. Claims 12 and 13 of the ’499 patent, excerpted below, also recite the components and other features described above in the specification.

12. A thin and substantially flexible circuit comprising: a thin monocrystalline semiconductor layer of one piece; a silicon-based dielectric layer formed on the thin semiconductor layer and having a stress of less than $5x10^8$ dynes/cm^2 tensile; and circuitry supported by the thin semiconductor layer and the dielectric layer defining an

integrated circuit die having an area, wherein the thin semiconductor layer extends throughout a substantial portion of the area of the integrated circuit die.

13. The thin and substantially flexible circuit of claim **12,** comprising: a vertical interconnect conductor extending vertically through the thin semiconductor layer and coupled to said circuitry; and a vertical silicon-based dielectric insulator extending vertically through the thin semiconductor layer and around the interconnect conductor and having a stress of less than $5x10^8$ dynes/cm^2 tensile.

C. Relevant Prosecution History

‘499 patent

34. Application No. 13/734,874 (which later issued as the asserted ’499 patent) was filed on January 4, 2013, as a continuation of application No. 12/788,618 (which later issued as the asserted ’672 Patent). On May 29, 2013, the Examiner issued a Non-Final Rejection in which he rejected all pending claims (i.e., claims 1-5, 7-17, and 19-32). Claims 7, 12, 19, and 24 were objected to for reciting “substantially flexible,” which, according to the Examiner, rendered “the claims unclarity, since the resulting claims do not clearly set for the metes and bounds of the patent protection desired.” Office Action (May 29, 2013) at 3. The Examiner rejected Claims 1-5, 7-17, and 19-32 on the ground of non-statutory obviousness-type double patenting over claims 1-62 of U.S. Patent No. 8,410,617. Claims 1, 26, and 30 were also rejected as being anticipated by U.S. Patent No. 4,104,418 (Park). Claim 14 was found to be obvious in light of Park. The Examiner explained that Park discloses a flexible substrate with a low-stress dielectric layer. *Id.* at 7.

35. In response, the Applicant distinguished Park on two grounds. First, the Applicant argued that Park discloses depositing a dielectric layer on a dielectric substrate for flat panel displays, and that Park thus failed to disclose a semiconductor substrate. Second, the

Applicant argued that Park discloses forming a low compressive stress dielectric layer, whereas the claims were amended to require a low tensile stress dielectric layer. Applicant's Amendment and Response (June 20, 2013).

36. To overcome the objection that "substantially flexible" is indefinite, the Applicant stated:

> With respect to the language "substantially flexible," the meaning of this phrase as used in the claims is clearly explained in the specification including, for example, at page 18, lines 1-3. As described in this passage, a semiconductor substrate is caused to be substantially flexible by thinning it to 50 microns or less and polishing or smoothing the thinned semiconductor substrate to relieve stress. The phrase "substantially flexible" is used in the claims consistent with this description, which is unambiguous.

Id. at 9.[3]

37. Based on the Applicant's response, the Examiner withdrew his rejections for indefiniteness of the term "substantially flexible" and in view of Park, while maintaining the double-patenting rejection. Office Action (July 8, 2013). The Examiner rejected Claims 1 and 26 as being anticipated by U.S. Patent No. 4,637,029 (Hayakawa), which the Examiner stated discloses a flexible semiconductor substrate having a low tensile stress dielectric. *Id.* at 6-7. Claims 14 and 30 were rejected as being obvious in light of U.S. Patent 4,892,894 (Corrie) and Hayakawa. *Id.* at 7-9. The Examiner stated that Corrie discloses a thin semiconductor substrate having an integrated circuit formed thereon. *Id.* at 8.

38. The Applicant conducted an interview with the Examiner on July 16, 2013 and

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[3] Page 18, lines 1-3 of the application (as filed on 4/4/2013) correspond to '239 patent at 9:25-28.

argued that Hayakawa discloses "cladding layers [that] are semiconductor layers, not dielectric layers as claimed." The Examiner apparently agreed with the applicant during the interview. Applicant's Response (July 22, 2013) at 8. The applicant also submitted terminal disclaimers to resolve the double-patenting rejections.

'239 patent

39. Application No. 10/614,067 was filed on July 3, 2003, as a divisional application of Application No. 09/607,363, which issued as U.S. Patent No. 6,632,706 (not asserted). This application continues the prosecution of claims 88-101 from the '363 Application that were cancelled in response to a July 31, 2001 restriction requirement.

V. LEVEL OF ORDINARY SKILL IN THE ART

40. Based on my review of the Asserted Patents and their file histories, I believe a person of ordinary skill in the art around the time of the purported invention would have had at least a bachelor-level degree in electrical engineering, materials science, physics, or equivalent thereof, and at least 3–5 years of experience of experience in the relevant field, e.g., semiconductor processing.

41. In determining the level of ordinary skill in the art, I was asked to consider, for example, the type of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. I also understand that the parties and the Patent Trial and Appeal Board ("PTAB") applied this level of ordinary skill in the art during various *Inter Partes* Review proceedings relating to the Asserted Patents.

42. My opinions concerning the Asserted Patents are from the perspective of a person of ordinary skill in the art as set forth above.

VI. OPINIONS ON UNDERSTANDINGS OF ONE OF ORDINARY SKILL

A. "substantially flexible" substrate

43. The parties' proposed constructions for "“substantially flexible substrate" / "substantially flexible … substrate" / "substrate is substantially flexible" / "substrate substantially flexible" / "substrate … is … substantially flexible" / "substantially flexible … semiconductor layer" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, which is a substrate / semiconductor layer that is largely able to bend without breaking.	"[substrate / semiconductor layer] that has been thinned to a thickness of less than 50 microns and subsequently polished or smoothed"

44. In my opinion, the phrase "substantially flexible" is not a term of art that has an accepted plain and ordinary meaning in the field of semiconductor processing. Moreover, it is my opinion that the term "substantially flexible" is a term of degree, and there is no commonly accepted standard in the semiconductor industry for determining whether a structure is "substantially flexible." It is a subjective term that may mean different things to different people in the field.

45. In my opinion, a person of ordinary skill in the art would understand that to be consistent with the disclosure in the Asserted Patents, a "substantially flexible" substrate or semiconductor layer means a substrate or layer that has been "thinned to a thickness of less than 50 microns and subsequently polished or smoothed," as proposed by Defendants.

46. The specification of the '239 patent describes a "substantially flexible" substrate as follows: "Grind the backside or exposed surface of the second circuit substrate to a thickness of less than 50 μm and then polish or smooth the surface. The thinned substrate is now a substantially flexible substrate." '239 patent at 9:25-28; *see also id.* at 3:18-21, 4:33-38. Thus, a

person of ordinary skill in the art would understand that, according to the specification, a "substantially flexible" semiconductor substrate or layer refers to a substrate or layer that has been thinned to a thickness of less than 50 µm and subsequently polished or smoothed. *See also id.* at 8:55-9:16. The specification does not describe any other structure as a "substantially flexible" semiconductor substrate.

47. The specification describes "Memory Device Fabrication Sequence[s]." *Id.* at 9:18-11:25. After describing that "[g]rind[ing] the backside or exposed surface of the second circuit substrate to a thickness of less than 50 µm and then polish[ing] or smooth[ing] the surface" results in a thinned, "substantially flexible" substrate (step 2A), *id.* at 9:25-28, the specification describes several alternative manufacturing methods, including the use of parting layers and reusable substrates. *Id.* at 9:45-49. However, the specification does not state that these alternative methods produce a "substantially flexible" substrate. Thus, a person skilled in the art would understand the applicant to define a "substantially flexible" substrate as a substrate thinned to less than 50 µm and subsequently polished or smoothed.

48. Moreover, the specification of the '239 patent discloses several possible materials for the substrate, including at least silicon and quartz. *See id*. at 7:44-55. Quartz and silicon have very different mechanical properties, including different rigidity. However, regardless of its starting material, the specification discloses only a single method of making a "substantially flexible" substrate—thinning to a thickness of less than 50 microns and subsequently polishing or smoothing. *See id.* at 9:25-28.

49. The prosecution history of the '499 patent supports this construction of the "substantially flexible" substrate. During prosecution of the '499 patent, the Examiner objected to the term "substantially flexible" as indefinite. *See* Office Action (May 29, 2013). The

Applicant overcame the objection by arguing that "substantially flexible" is "unambiguous" because its "meaning… is clearly explained in the specification":

> With respect to the language "substantially flexible," the meaning of this phrase as used in the claims is clearly explained in the specification including, for example, at page 18, lines 1-3. As described in this passage, a semiconductor substrate is caused to be substantially flexible by thinning it to 50 microns or less and polishing or smoothing the thinned semiconductor substrate to relieve stress. The phrase "substantially flexible" is used in the claims consistent with this description, which is unambiguous.

Response to Office Action (June 20, 2013) at 9.

50. Similarly, during prosecution of related U.S. Patent Application Nos. 12/497,652 and 12/497,653 (which share the same specification as the '499 patent), the Applicant attempted to distinguish prior art by representing to the Patent and Trademark Office that "[a] substantially flexible semiconductor substrate may be achieved by grinding until considerably thin, for example to a thickness of less than 50 microns, and polishing the resulting surface." (2013-9-26 Response to Office Action for the '652 application and 2013-10-24 Response to Office Action for the '653 application.)

51. Other patents that are cited in the Asserted Patents and share the same inventor as the Asserted Patents support the construction that "substantially flexible" means "thinned to a thickness of less than 50 microns and subsequently polished or smoothed." *See, e.g.*, U.S. Patent No. 5,354,695 (issued October 11, 1994): "This invention relates to methods for fabricating integrated circuits on and in flexible membranes, and to structures fabricated using such methods." '695 patent at 1:7-9. The fabrication method of the "flexible membranes" is claimed as follows: "16. A method of making an integrated circuit comprising the steps of: forming a substrate having a thickness of less than about 50 μm; forming semiconductor devices on a principal surface of the substrate…" '695 patent at 48:39-44. Another patent by the same

inventor, U.S. Patent No. 5,592,007 (issued January 8, 1997), claims a "flexible" dielectric membrane less than 50 microns thick: "A field effect transistor comprising: a **flexible** free-standing dielectric membrane having a principal surface and a thickness **less than 50 µm**." *Id.* at 46: 45-46 (emphasis added).

52. Other references cited by the Asserted Patents also support the construction that "substantially flexible" means "thinned to a thickness of less than 50 microns and subsequently polished or smoothed." *See, e.g.,* U.S. Patent No. 4,633,031 (issued December 30, 1986) at 2:1-10: "A multi-layer, thin-film, flexible silicon alloy solar cell is described in which the multiple layers extend perpendicularly to the incident light. The flexible cell is mass-produced by rolling and laminating two thin ribbons of silicon alloy having thicknesses of the order of 10 to 50 microns with each ribbon passing through multiple rolling stages employing a ceramic metallic glass semi-conductor alloy of silicon having approximately a zero coefficient of thermal expansion/contraction." *See also* U.S. Patent No. 5,324,687.

53. In view of the intrinsic evidence cited above, one of ordinary skill in the art would have understood that "substantially flexible" means "thinned to a thickness of less than 50 microns and subsequently polished or smoothed."

54. This claim construction is consistent with what one of ordinary skill in the art would have understood about thin silicon layers at the priority date of the Asserted Patents. For example, it was known that thin film, flexible solar cells could be made of 10-50 µm thick silicon films bonded with silicon alloy. *See*, *e.g.* U.S. Patent No. 4, 633,031, issued Dec. 30, 1986 (Abstract, 2:1-10). In addition, flexible, monocrystalline silicon structures 10 to 30 µm thick had been used in fabricating mechanical sensors. *See*, *e.g.* T. Bourouina, et al., "Silicon Etching Techniques and Application to Mechanical Devices," *see also* Appl. Surface Sci, 65,536

(1993), p.537. Also, as noted above, U.S. Patent No. 5,354,695 teaches methods for the fabrication of semiconductor devices of a thickness of less than about 50 µm on flexible membranes. Thus, at the time the Asserted Patents were filed, it was already known that wafers that were thinned to 50 µm and below became more flexible and more stable, and could bend and twist while maintaining strength. *See*, *e.g.* ’031 Patent, T. Bourouina, et al., and ’695 Patent.

55. I understand Elm is arguing that “substantially flexible” means “largely able to bend without breaking.” I disagree with Elm’s argument that one of skill in the art would understand a “substantially flexible” substrate to refer to a substrate that is largely able to bend without breaking for several reasons.

56. First, Elm’s proposed construction replaces an ambiguous term of degree with an equally ambiguous definition. The proposed construction of “largely able to bend without breaking” does not provide any standard to those of skill in the art for measuring the degree of bending required to meet this claim limitation. For example, it is unclear whether a structure that can sustain a 1° bend without breaking satisfies this limitation, or whether a 5° bend would constitute “largely able to bend,” or whether a 30° bend would meet the claim limitation. Thus, if Elm’s construction is adopted, one of ordinary skill in the art would be unable to determine the scope of the claimed invention with reasonable certainty because there are no objective criteria for measuring the degree of bending necessary to satisfy the “largely able to bend” requirement. It is equally unclear whether “without breaking” refers to structural or functional failure of a substrate, which may occur at different degrees of bending. Thus, the patent examiner’s rejection for indefiniteness, which was removed only after the applicant provided a thickness definition, is not resolved by Elm’s proposed construction.

57. Second, Elm’s construction alters the meaning of the claim term by changing a

flexibility requirement to a non-fracture requirement. The Asserted Patents do not include any disclosure relating to the fracture point of semiconductor substrates. The level of stress at which a silicon wafer would break is significantly higher than the stress levels disclosed in the specification of the Asserted Patents. The difference between the breakage stress reported in the literature and the stress levels described in the specification would be at least an order of magnitude or more. *See, e.g.*, Chong et al., "Mechanical Characterization in Failure Strength of Silicon Dice," 2004 Inter Society Conference on Thermal Phenomena. Chong et al. discloses, in Fig. 6 (reproduced below), failure stress in the range of 500 - 1000 MPa (i.e., $5x10^9$ - $1x10^{10}$ dynes/cm^2), which is 10-20x higher than the upper limit contemplated in the Asserted Patents (i.e., $5x10^8$ dynes/cm^2).

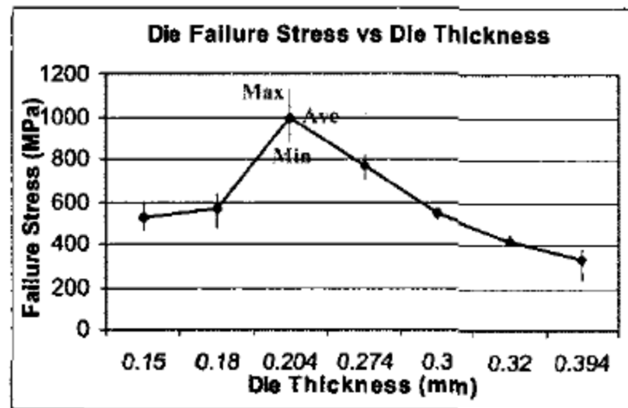

Fig 6. Die Failure Stress for Different Die Thickness.

58. Another article, Wacker et al., found that ~300 MPa ($3x10^9$ dynes/cm^2) could be considered the breakage stress for ultra-thin (thickness ≤ 20 μm) chips. Wacker et al., "Stress Analysis of Ultra-thin Silicon Chip-on-foil Electronic Assembly Under Bending," Semiconductor Science and Technology 29, 095007 (2014). To obtain this breakage stress value, Wacker investigated the bending-induced uniaxial stress at the top of ultra-thin (thickness ≤ 20 μm) single-crystal silicon chips adhesively attached with epoxy glue to a soft polymeric

substrate through combined theoretical and experimental methods. Wacker discloses in Fig. 6 (reproduced below) the variation of the tensile uniaxial stress in the central area of the chip, as a function of both bending radius and curvature. For radii of less than R=7 mm, the bending-induced uniaxial stress at the top of the chip increases rapidly. The breaking tests performed on ultra-thin Si-chips with CMOS circuitry, adhesively attached to thin substrates, revealed a breaking frequency of ~60 % for R=6 mm.

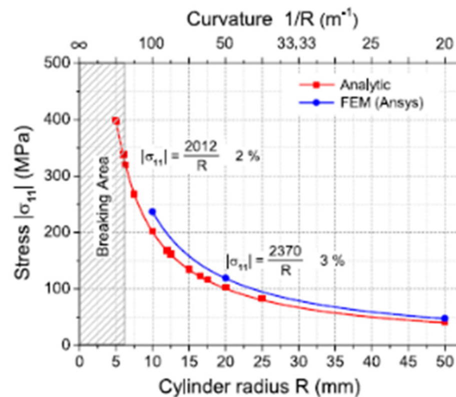

Figure 6. Variation of the tensile uniaxial stress σ_{11} (at the top of the Si-chip) with radius R and curvature $1/R$, estimated analytically and numerically. The analytical results are obtained for the applied load ($|M|$, $|F| \cong 0.05$ MPa · mm).

59. Therefore, a stress of ≅ 300 MPa can be considered the critical stress in Fig. 6, indicating a stress level beyond which most similarly processed 20 µm thick chips break. Thus, the radius of bending of Wacker's chips is R=6mm. Wacker discloses in Fig. 1 a chip bending on a cylinder of radius R. As seen in Fig. 1, at stress levels approaching the breaking stress, the curvature in the chip is significant. The breaking stresses discussed in Wacker and similar articles are significantly higher than the stress levels contemplated by the Asserted Patents, and the radius of bending discussed in these articles is also significantly higher than that expected from a stacked IC device. Thus, it is clear that the amount of bending without breaking is highly variable depending on the material and the thickness. And the determination of whether a material is largely able to bend without breaking will vary from one person skilled in the art to

another.

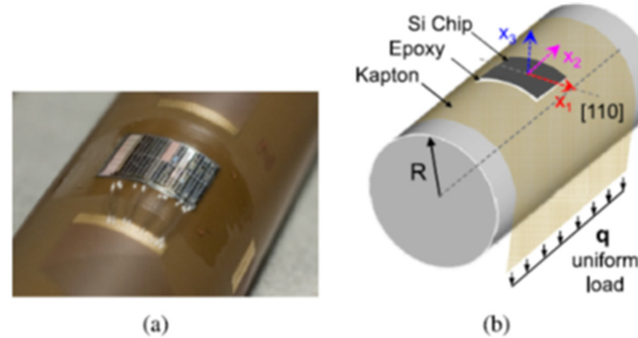

Figure 1. (a) Bending of ultra-thin Si-chip on flexible substrate; (b) schematic representation of the three-layer system bent on a cylinder of radius *R*.

60. Elm's proposed construction of "substantially flexible substrate" is incorrect because it focuses on bending, and bending to some extent without breaking. Both of these concepts conflict with the subject matter of the Asserted Patents, which focus on the stacking of IC layers. *See, e.g.*, '239 patent at 1:18-20, "Field of Invention: "The present invention relates to stacked integrated circuit memory;" *id.* at 3:10-13, "Summary of the Invention" ("The present 3DS memory technology is a stacked or 3D circuit assembly technology."). One of ordinary skill in the art would have understood that in order to bond and stack memory circuit layers, the substrate would need to be "sufficiently planar" as described in the specification. According to the specification of the '239 patent:

> The surface of the circuits to be bonded are smooth and **sufficiently planar** as is the case with the surface of an unprocessed semiconductor wafer or a processed semiconductor wafer that has been **planarized** with the CMP (Chemical Mechanical Processing) method with a **surface planarity of less than 1 µm and preferably less than 1,000 Å** over at least the area of the surface of the circuit (formed on the substrate) to be bonded. The metal bonding material on the surfaces of the circuits to be bonded are patterned to be mirror images of each other and to define the various vertical interconnect contacts as indicated in FIG. 2a, FIG.2b, FIG.2c and FIG. 5. The step of bonding two circuit substrates results in simultaneously forming the vertical interconnection between the two respective circuit layers or substrates.

'239 patent at 7:62-8:11 (emphasis added).

61. Thus, bending a large amount without breaking would interfere with the ability of

memory circuits to bond together so as to be stacked in layers. In other words, the "flexibility" required for stacking IC circuit layers, as contemplated by the specification of the Asserted Patents, has nothing to do with the amount of bending the wafer can sustain before breaking. Indeed, un-thinned substrates greater than 50 μm in thickness are able to bend more than desirable for stacking IC circuit layers. Elm's proposed construction shifts the focus away from the desired property disclosed in the specification—minimizing bending such that the layers can be stacked—and instead focuses on the other extreme—bending a large amount without breaking.

62. In addition, as discussed above, the patent specification discloses several possible materials for the substrate, including at least silicon and quartz. *See id*. at 7:44-55. Quartz and silicon have very different mechanical properties, including different fracture stress. (G. R. Trott and A. Shorey, "Glass Wafer Mechanical Properties: A Comparison To Silicon," available at http://www.corning.com/media/worldwide/global/documents/semi%20Glass_Wafer_Mechanical_Properties_A_Comparison_to_Silicon.pdf.) In other words, a silicon substrate manufactured according to the method disclosed in the specification (i.e., thinned to 50 μm and polished and smoothed) and a quartz substrate manufactured according to the same method (i.e., also thinned to 50 μm and polished and smoothed) would have different breakage points and endure different degrees of "bending" before breaking.

63. Third, the breakage of substrates can occur via different fracturing mechanisms. The mechanism can vary depending on the particular application, material, and other factors. One of ordinary skill in the art would not use the ability to "bend without breaking" in determining the flexibility of a substrate because the fracture may occur at different stress levels, depending on how the substrate was thinned and finished. In addition, the location of the force

applied to bend the material will affect the fracturing mechanism. And as shown in Fig. 6 in Chong above, the failure stress varies significantly with the die thickness, and even within a given die thickness, the variation of breakage stress can be as large as 200 MPa ($2x10^9$ dynes/cm^2).

64. Fourth, the specification of the Asserted Patents lacks any mention of breakage, fracture, or failure due to bending. Elm's proposed construction thus lacks support from the specification.

65. Finally, the plaintiff's proposed construction of "largely able to bend without breaking" specifies a particular deflection type – bending, but does not explain why this particular deflection type is the one intended by the term "flexible" rather than tensional loading, torsional loading, or other potential loading modes. Even after specifying that flexibility refers in particular to bending, this construction remains indefinite due to the failure to specify what numeric degree of bending would qualify as "largely able to bend without breaking," compared to what degree would not so qualify. Several potential methods of quantification could be used depending on the loading mode in question: 1) **a substrate's vertical deflection** before breaking in tension under an applied load, 2) a certain **radius of curvature** in substrate bending, and 3) a **number of degrees of twisting** of the substrate before breaking in torsion.

66. In sum, the intrinsic record of the Asserted Patents defines "substantially flexible" to mean "thinned to a thickness of less than 50 microns and subsequently polished or smoothed." The Applicant affirmed that definition during the prosecution of the patents by (1) arguing that a semiconductor substrate is caused to be substantially flexible by thinning it to 50 microns or less and polishing or smoothing, thereby overcoming the Examiner's indefiniteness objection, and (2) using that definition to distinguish a prior art reference and thus overcoming a prior art rejection.

In my opinion, Elm's proposal that "substantially flexible" means "largely able to bend without breaking" is inconsistent with the understanding of one of ordinary skill in the art as of the time of the priority date of the asserted patents.

B. "substantially flexible" integrated circuit

67. The parties' proposed constructions for the terms "substantially flexible integrated circuit[s]" / "substantially flexible integrated circuit layer[s]" / "integrated circuits is substantially flexible" / "integrated circuit … is … substantially flexible" / "substantially flexible circuit layer[s]" / "substantially flexible stacked integrated circuit structure" / "substantially flexible circuit" / "substantially flexible … structure" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, which is an integrated circuit/ integrated circuit layer/ circuit layer/ circuit structure/ circuit/ structure that is largely able to bend without breaking.	"[integrated circuit[s] / integrated circuit layer[s] / stacked integrated circuit structure / structure] that contains a substantially flexible substrate where the dielectric material used in processing the substrate has a stress of $5x10^8$ dynes/cm^2 tensile or less"

68. As explained in Section VI.A, the phrase "substantially flexible" is not a term of art that has an accepted plain and ordinary meaning in the field of semiconductor processing. Moreover, it is my opinion that the term "substantially flexible" is a term of degree, and there is no commonly accepted standard in the semiconductor industry to determine whether a structure is "substantially flexible."

69. In my opinion, a person of ordinary skill in the art would understand that to be consistent with the disclosure in the Asserted Patents, a "substantially flexible" integrated circuit ("IC") means an IC that "contains a substantially flexible substrate where the dielectric material used in processing the substrate has a stress of $5x10^8$ dynes/cm^2 tensile or less" as proposed by Defendants.

70. The ’239 patent specification explains that each “circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 µm and typically less than 10 µm in thickness” (*id.* at 4:35-38). The specification also states that “[t]he thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2).” *Id.* at 8:66-9:4.

71. During prosecution of related U.S. Patent Application No. 12/497,652, which shares the same specification as the Asserted Patents, the Applicant attempted to distinguish prior art by explaining to the Examiner that “substantially flexible” integrated circuit layer requires two features: (i) “the semiconductor material must be sufficiently thin, e.g., 50 microns or less,” and (ii) “the dielectric material used in processing the semiconductor material must be sufficiently low stress,” which, “[a]s set forth in the present specification, stress of 5×10^8 dynes/cm^2 or less has been demonstrated to satisfy this requirement.” Response to Office Action (April 5, 2013) at 28.

72. The Applicant confirmed this definition during prosecution of related U.S. Patent Application No. 12/497,653, stating that “a substantially flexible semiconductor substrate is a *necessary* but not a *sufficient* condition for a substantially flexible circuit layer” because, “[f]or a circuit layer to be substantially flexible, Applicant has found that the dielectric material must have low tensile stress, for example, 5×10^8 dynes/cm^2 tensile.” Response to Office Action (October 24, 2013) at 2-3.

73. Therefore, in view of the prosecution history, a “substantially flexible circuit layer” must include the same requirements as a “substantially flexible semiconductor substrate,” and have the additional requirement of “where the dielectric material used in processing the substrate has a stress of $5 \text{x} 10^8$ dynes/cm^2 tensile or less.”

74. For reasons described above and the reasons explained in Section VI.A., it is my opinion that a person of ordinary skill in the art would not understand "substantially flexible" integrated circuit to mean an IC that is "largely able to bend without breaking."

75. In sum, it is my opinion that the term "substantially flexible" integrated circuit means an integrated circuit "that contains a substantially flexible substrate where the dielectric material used in processing the substrate has a stress of $5x10^8$ dynes/cm^2 tensile or less," which is consistent with the disclosure in the specification and the prosecution history of the patents.

C. "dice is substantially flexible" / "die is substantially flexible"

76. The parties' proposed constructions for "dice is substantially flexible" / "die is substantially flexible" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, which is a dice/die that is largely able to bend without breaking.	"diced substantially flexible integrated circuit" (see construction of "substantially flexible integrated circuit")

77. In my opinion, a person of ordinary skill in the art would understand from the specification that "substantially flexible" when used to modify "die" or "dice" is "a die [dice] having a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed, and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm^2 tensile or less."

78. The support for my opinion is set forth above in Sections VI.A and IV.B.

D. "have stress of $5x10^8$ dynes/cm^2 or less"

79. The parties' proposed constructions for "have stress of about 5×10^8 dynes/cm^2 or less" / "have a stress of about 5×10^8 dynes cm^2 or less" / "having a stress of $5x10^8$ dynes/cm^2 or less" / "having a stress of $5x10^8$ dynes/cm^2 tensile or less" / "[have] a stress of about 5×10^8

dynes/cm^2 tensile or less" / "having[/has] a stress of less than 5×10^8 dynes/cm^2 tensile" / "a stress of about 5×10^8 dynes/cm^2 or less" / "with a tensile stress of less than 5×10^8 dynes/cm^2" / "with a stress of less than 5×10^8 dynes/cm^2 tensile" / "has[/having] a tensile stress of less than 5×10^8 dynes/cm^2" are in the table below.

Plaintiff's Proposal	**Defendants' Proposal**
No construction necessary.	Indefinite Micron and Samsung: to the extent these terms are found not to be indefinite, they should be construed to mean: "having stress in the dielectric layer that is between 0 and 5x10^8 dynes/cm^2 in tensile"

80. In my opinion, the term "have stress of about 5×10^8 dynes/cm^2 or less" and all similar terms are indefinite because these terms, when interpreted in light of the specification and the prosecution history, fail to inform those skilled in the art about the scope of the claimed invention with reasonable certainty.

81. In an integrated circuit device, there are generally many different **types** of stress. For example, there is growth stress arising during the film or material growth or deposition process, thermal stress arising from the mismatch of the coefficients of thermal expansion between a substrate and film material, interface stress arising in a film or material from interactions with adjacent features or geometries (*e.g.*, patterned features), and external stresses arising from external loads (*e.g.*, applied forces, bending). In addition, the literature at the time of the alleged invention is replete with references to residual stress, total stress, intrinsic stress, extrinsic stress, surface stress, among other types of "stress." *See, e.g.*, T.J. Garino and M. Harrington, "Residual stress in PZT thin films and its effect on ferroelectric properties," MRS Proceedings Symposium G – Wide Band-Gap Semiconductors, vol. 243, p. 341 (1991) (discussing "residual stress"); U.S. Patent No. 5,061,574 (discussing and claiming "total film

stress”); M. Stadtmueller, Mechanical Stress of CVD-Dielectrics, J. Electrochem. Soc., Vol. 139, No. 12, December 1992 (discussing “intrinsic stress” and “thermal stress” of dielectric film); Kim *et al*., Pulsed laser deposition of VO_2 thin films, Appl. Phys. Lett. 65 (25), 19 December 1994 (discussing “extrinsic stress” of oxide); Itakura *et al*., “Surface Stress in Thin Oxide Layer Made by Plasma Oxidation with Applying Positive Bias,” Applied Surface Science 159-160 (2000) 62-66 (discussing “surface stress” of oxide).

82. In my opinion, it would have been unclear to one of ordinary skill in the art, after reading the Asserted Patents and considering the intrinsic record, which “stress” was being claimed, and what must be included in the recited “stress” value. Indeed, the Patentee has inconsistently referred to “stress” in the intrinsic record—*e.g.*, at times referring to “intrinsically low … stress,” at other times referring to “extrinsic net surface stress,” and at still other times referring to “inherently low stress films.” For example, the Patentee has expressed in the Asserted Patent specifications that an “intrinsically low stress deposited film is … preferred.” *See* ’239 patent at 9:7-12. However, in the ’695 patent, which the Asserted Patents incorporate by reference regarding its disclosure of “low stress dielectrics” (*see* ’239 patent at 8:66-9:7), the Patentee describes these dielectrics as having low surface stress caused by mismatch of coefficients of thermal expansion. *See, e.g.*, ’695 patent at 6:22-38. For example, the ’695 patent describes “matching the coefficient of thermal expansion of the semiconductor material and the various dielectric materials being used” for the goal of minimizing the “extrinsic net surface stress” of the dielectric membrane. *Id.* at 6:26-30; *see also id.* at 24:68-25:5. The ’695 patent also distinguishes conventional, thermally-grown dielectrics for being “strongly compressive” and having “compressive surface stress.” *Id.* at 6:30-33. The ’695 patent discloses using a chemical vapor deposition technique at a relatively low temperature of 400 °C for the

formation of “low stress dielectric circuit membranes.” *Id.* at 11:40-65. The ’695 patent states that the resulting dielectric material has “[a]cceptable surface stress levels.” *Id.* at 11:37-39. In a further contradictory manner, the Patentee argued around prior art in the IPRs by explaining the prior art “does not address inherently low-stress films.” *See* IPR2016-00390, Patent Owner’s Preliminary Response (April 6, 2016) at 58 (emphasis added). In my opinion, these contradictory references to different types of “stress” in the intrinsic record further confirm that one of ordinary skill would not be reasonably certain what type of “stress” was being claimed.

83. Depending on the type of “stress,” the value of “stress” will differ. For example, film growth stress could be very low, while other stresses such as surface stress or thermal stress resulting from temperature excursions could be very high or vice versa. *See, e.g.*, T.J. Garino and M. Harrington, “Residual Stress in PZT Thin Films and Its Effect on Ferroelectric Properties,” MRS Proceedings Symposium G – Wide Band-Gap Semiconductors, vol. 243, p. 341 (1991). The claims are silent as to the type of “stress” to be limited. Thus, the term would not have a clear and definite meaning to one of ordinary skill in the art because it does not specify what kind of “stress” is contemplated.

84. In addition to “stress” varying depending on **type** of stress, the **value** (*e.g.*, magnitude and direction (tensile or compressive)) of the “stress” in an integrated circuit device also generally varies according to the specific spatial location in the layer or material of the device considered. For example, stresses generally may be assumed to vary linearly throughout the thickness of an individual layer or material, but there also may be nonlinear, steep stress gradients at the film boundaries. *See, e.g.,* H. Uchida, *et al*., “Measurement Technique for the Evaluation of Residual Stress in Epitaxial Thin Films by Asymmetric X-Ray Diffraction,” J. Ceramic Society Japan, 107 [7] 606 (1999). One of ordinary skill in the art would also

understand stresses at the lateral edge of a layer or material would differ from stresses at locations at the vertical edge of the layer or material, which would differ from stresses at locations in the middle of the layer or material. *See, e.g.,* S.C. Jain, *et al*., "Edge-induce Stress and Strain in Stripe Films and Substrates: A Two-dimensional Finite Element Calculation," J. Appl. Phys., 78, 1630 (1995).

85. In my opinion, it would have been unclear to one of ordinary skill in the art whether the recited "stress" value having a magnitude (between 0 and $5x10^8$ dynes/cm^2) and a direction (in tensile) reflected a "stress" value at a particular location in the layer or material (*e.g*, center, edge, pattern, or interface). Indeed, one of ordinary skill in the art would not be reasonably certain whether one measurement taken at one location was sufficient to know whether one was operating within or outside the scope of the claims.

86. The uncertainty regarding these claim limitations is magnified further given the fact that, in an integrated circuit device, the value of "stress" further varies depending on how the measurement of stress is made. There is no direct method of measuring stress in a layer or material within an integrated circuit device. Instead, there are a number of different indirect approaches to estimate stresses that were known at the time of the alleged invention, including at least curvature changes due to distortion as stresses arise or relax,[4] x-ray diffraction (atomic strain gauge), hard x-rays (atomic strain gauge), neutrons (atomic strain gauge), ultrasonics (stress effects on elastic wave velocity), magnetic (stress effects on magnetic domains), electron diffraction, and Raman spectroscopy. *See*, *e.g*., P.J. Withers, "Residual Stress: Part 1 –

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[4] For stacked integrated circuits, attempts to measure stress based on curvature are further complicated by the sequential layer removal required to estimate the stress induced by each successive layer. The layer removal process for performing stress measurements at each layer may alter the underlying layers and affect the detected stress levels.

Measurement Techniques," Materials Science and Technology, 17, 355 (2001) ("*Withers*"); K. Kimoto, et al., Jpn. J. Appl. Phys. 32, L211 (1993); M.Y. Tsai, C.H. Chen, "Evaluation of Test Methods for Silicon Die Strength," Microelectronics Reliability, 48, 933 (2008).

87. These indirect approaches rely on a combination of measurement and modeling. In particular, a measurement is performed on the structure in question and the data from that measurement are mathematically modeled depending on assumptions regarding the properties of the material(s) and structure being measured. *See, e.g.*, I. De Wolf, "Micro-Raman Spectroscopy to Study Local Mechanical Stress in Silicon Integrated Circuits," Semicond. Sci. Technol. 11 (1996) 139-154 ("The number of techniques used for stress measurements is very large; however, none of them is without shortcomings when applied to materials encountered in microelectronics."). A summary of stress measurement techniques assembled by *Withers* is shown below in Table 1. *Withers* at 357. Differences in measurement accuracy of each method listed are shown along with comments.

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Table 1 Summary of various measurement techniques and their attributes: values of resolution and penetration quoted are broadly representative of technique concerned and ⟨II⟩ represents volume averaged type II stresses

Method	Penetration	Spatial resolution	Accuracy	Comments
Hole drilling (distortion caused by stress relaxation)	~1·2 × hole diameter	50 μm depth	±50 MPa, limited by reduced sensitivity with increasing depth	Measures in-plane type I stresses; semidestructive
Curvature (distortion as stresses arise or relax)	0·1–0·5 of thickness	0·05 of thickness; no lateral resolution	Limited by minimum measurable curvature	Unless used incrementally, stress field not uniquely determined; measures in-plane type I stresses
X-ray diffraction (atomic strain gauge)	<50 μm (Al); <5 μm (Ti); <1 mm (with layer removal)	1 mm laterally; 20 μm depth	±20 MPa, limited by non-linearities in $\sin^2 \psi$ or surface condition	Non-destructive only as a surface technique; sensitive to surface preparation; peak shifts: types I, ⟨II⟩; peak widths: type II, III
Hard X-rays (atomic strain gauge)	150–50 mm (Al)	20 μm lateral to incident beam; 1 mm parallel to beam	$\pm 10 \times 10^{-6}$ strain, limited by grain sampling statistics	Small gauge volume leads to spotty powder patterns; peak shifts: type I, ⟨II⟩, II; peak widths: types II, III
Neutrons (atomic strain gauge)	200 mm (Al); 25 mm (Fe); 4 mm (Ti)	500 μm	$\pm 50 \times 10^{-6}$ strain, limited by counting statistics and reliability of stress free references	Access difficulties; low data acquisition rate; costly; peak shifts: type I, ⟨II⟩ (widths rather broad)
Ultrasonics (stress related changes in elastic wave velocity)	>10 cm	5 mm	10%	Microstructure sensitive; types I, II, III
Magnetic (variations in magnetic domains with stress)	10 mm	1 mm	10%	Microstructure sensitive; for magnetic materials only; types I, II, III
Raman	<1 μm	<1 μm approx.	$\Delta\lambda \approx 0{\cdot}1\ cm^{-1} \equiv 50$ MPa	Types I, II

Withers and Bhadeshia Residual stress: Part 1 357

88. As confirmed by *Withers* (Table 1) and other references, depending on which measurement technique is applied, one of ordinary skill in the art would expect the value of the "stress" to differ. *See also* H. Uchida, *et al.*, "Measurement Technique for the Evaluation of Residual Stress in Epitaxial Thin Films by Asymmetric X-Ray Diffraction," J. Ceramic Society Japan, 107 [7] 606 (1999).

89. There are a number of reasons why the value of the "stress" extracted differs depending on the measurement technique applied. First, the different techniques are measuring different things. For example, measuring the die or wafer curvature by laser beam reflection methods or surface profilometry can result in an estimate for ***average*** stress over the entire die or wafer. *See, e.g.*, D.S. Gardner and P.A Flinn, "Mechanical Stress as a Function of Temperature for Aluminum Alloy Films," J. Appl. Phys. 67, 1831 (1990); *see also* G. Stoney, Proc. R. Soc. London, 9, 172 (1909). Curvature, however, provides no lateral resolution and merely assumes that the stress is uniform over the entire die or wafer. This is a questionable assumption since the composition of a deposited layer typically varies across a wafer and layer composition is a key determinant of layer stress. Other techniques, such as x-ray diffraction and Raman spectroscopy, for example, provide some lateral resolution, and as a result measure over a different scale than and also rely on a different set of assumptions than curvature. *See, e.g.*, *Withers*. Indeed, it is extremely difficult to use Raman to measure the stress in insulating dielectric films like silicon dioxide or silicon nitride deposited on a wafer because the strength of the Raman signal scattered from the dielectric is completely overcome by the signal from the crystalline silicon wafer. *See, e.g.,* A. Chabli, "Optical Characterization of Layers for Silicon Microelectronics," Microelectronic Engineering, 40, 263, 273 (1998) ("Unfortunately the substrate contribution to the response of the samples is often large and can even mask the very small contribution of the silica layers. This is the reason why Raman spectroscopy is not used for these studies.").

90. Neither the Asserted Patents, nor U.S. Patent No. 5,354,695, which the Asserted Patents incorporate by reference, describe a specific measurement technique or protocol for measuring the claimed "stress." In my opinion, it would have been unclear to one of ordinary skill in the art, which measurement technique was to be applied.

91. Given this and the fact that one of ordinary skill in the art would have arrived at a different "stress" value depending on the particular measurement applied, this adds further uncertainty as far as interpreting whether a given "stress" measurement result is within or outside the scope of the claims.

92. Whichever measurement method is applied, there is uncertainty regarding the determination of a "stress" value given that the claim terms in question concern a dielectric layer or material in an integrated circuit, and in particular a stacked layer integrated circuit. Because there is no direct method of measuring the stress level of a single dielectric layer within a layer stack on an integrated circuit, those skilled in the art must make a number of assumptions and use computer or analytical models to attempt to calculate an average stress value for the layer from indirect measurements. However, these "average" values are in effect estimates based on assumptions made about the way in which stress is distributed through the thickness of the layer.

93. In addition, the determination of a "stress" value of a layer or material in a stacked integrated circuit is further complicated by the fact that these layers or materials are patterned structures with other layers of differing compositions and patterns stacked above or below the layer or material in question.

94. It is thus my opinion that the claim terms are indefinite for failing to inform those skilled in the art about the scope of the claimed invention with reasonable certainty because the Asserted Patents do not specify what stress is claimed; how and where that stress is measured; and the measurement techniques available yielded only estimates of stress that would not provide one of ordinary skill with reasonable certainty that the actual stress was truly within the claimed range.

95. To the extent the terms are not indefinite, it is my opinion that the terms mean

having stress in the dielectric layer that is between 0 and 5×10^8 dynes/cm^2 in tensile.

96. No matter how interpreted, the "have stress of 5×10^8 dynes/cm^2 or less" and similar terms do not embrace stress balancing. The specification discusses two alternatives to make the dielectrics used in 3DS devices—one using dielectrics having stress of 5×10^8 dynes/cm^2 or less and the other using conventional stress dielectrics. As to the former, the specification states, "The thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication." '239 at 8:66-9:4. As to the latter, the specification states, "The use of dielectrics with conventional stress levels could be used in the assembly of a 3DS DRAM circuit, however, if more than a few layers comprise the stacked assembly, each layer in the assembly will have to be stress balanced so that the net stress of the deposited films of a layer is less than 5×10^8 dynes/cm^2." *Id.* at 9:7-12. The specification then states, "The use of intrinsically low stress deposited films is the preferred method of fabrication versus the use of the method where the stress of individually deposited films are not equal but are deposited to create a net balanced lower stress," again distinguishing low stress deposited films from net balanced lower stress. '239 at 9:12-16. In light of the specification, a person skilled in the art would have understood that the term "have stress of 5×10^8 dynes/cm^2 or less" and similar terms refer to low stress deposited films and not to net balanced lower stress or stress balancing.

97. The file history of related applications further makes it clear that dielectrics that "have stress of 5×10^8 dynes/cm^2 or less" are distinct from dielectrics that are stress-balanced. During the prosecution of Patent Application No. 12/268,386 (which is a pending Division

application of the ’004 patent, one of the Asserted Patents), the applicant amended the claims “to more clearly distinguish the claims from… co-pending cases.” The applicant made the following argument:

> Each of independent claims 88, 107, 328, 333, 338, 343 and 348 has been amended. The amendments are made in part to more clearly distinguish the claims from those of related co-pending cases, in particular 12/405,237. More specifically, Applicant has amended the present Application and 12/405,237 by claiming separate features of Applicant's invention in the separate applications. The claims in the present Application now claim a stack of depositions over a semiconductor substrate in which ***the majority of the thickness of the stack is from silicon-based dielectrics.*** In contrast, in 12/405,237, the claims have been amended to recite that a stack of depositions have been ***stress balanced so that the circuit layer(s) in which it is formed are substantially flexible.***

February 3, 2016 Response to Office Action (emphasis in original).

98. During the prosecution of another related application, Patent Application No. 12/405,237 (which is a Division application of the ’732 patent, one of the Asserted Patents), “[v]arious claims were rejected… with respect to the claimed feature of ‘stress balancing.’” In response, the applicant amended various claims and explained as follows:

> Independent claims 1, 18, 66, 86 and 106 have been nevertheless been amended, consistent with the explicit teachings of the specification, to make clear that stress balancing may apply to fewer than all of the depositions (e.g., to dielectric material depositions only). With this amendment, the rejection under Section 112, first paragraph is believed to be overcome. The dependent claims (numerous claims in the range of claims 383 to 500) have also been amended to specify—net balanced lower stress—instead of “net low stress.” This change is believed to improve the clarity of the claims.

June 2, 2017 Response to Office Action at Remarks.

99. Because the specification and related prosecution history clearly distinguish between dielectrics that “have stress of $5x10^8$ dynes/cm^2 or less” from dielectrics with “conventional stress levels” that must be stress-balanced to achieve a net lower stress, the Patent Trial and Appeal Board (PTAB) concluded as follows: “We, further, do not construe the term

'low stress dielectric' to require the stress-balancing of multiple dielectrics because the Specification of the '542 patent has distinguished 'low stress dielectrics' from those of 'conventional stress levels' that require stress-balancing to achieve a similar result." IPR2016-00390, Paper No. 13, Decision - Institution of *Inter Partes* Review (July 1, 2016) at 12-13. The "have stress of $5x10^8$ dynes/cm^2 or less" and similar terms thus refer to low stress ($5x10^8$ dynes/cm^2 or less) deposited films, not stress balancing.

100. Elm's arguments regarding stress-balancing before the PTAB further support that "have stress of $5x10^8$ dynes/cm^2 or less" and similar term refer to stress in the dielectric layer, not low net stress created by stress balancing. During *inter partes* review of the '542 patent, Elm sought to distinguish prior art ("*Kowa*") on the basis that *Kowa* discloses "stress-balanced" layers, rather than "inherently low-stress films" as follows: "*Kowa* discloses depositing stress-balanced alternating silicon nitride (SiN) layers. Kowa also discloses a plasma CVD method for 'alternately stacking a thin film having compressive stress and a thin film having tensile stress . . . .' Ex. 1007 at 8. *Kowa* does not address ***inherently low-stress films***." IPR2016-00390, Patent Owner's Preliminary Response (April 6, 2016) at 58 (emphasis added). It is clear that the "have stress of $5x10^8$ dynes/cm^2 or less" and similar terms do not encompass stress balancing. But the term is still indefinite because, as explained above, it is unclear what stress must be included in the recited value, among other issues (*see, e.g.*, ¶ 94 above). The specification of the Asserted Patents incorporate by reference the disclosure of the '695 patent as it relates to dielectric materials. *See, e.g.*, '239 Patent at 8:66-9:16. And the specification (including the incorporated by reference '695 patent) refers to different types of stresses, as discussed above, none of which are expressly recited or excluded by the asserted claims. *See* ¶ 82 above.

101. Additionally, the stress in the dielectric layer refers to tensile stress. When the

patent specification discusses the use of a low stress dielectric, it incorporates by reference dielectrics that are in tensile stress. According to the specification, "[t]he thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication. Such low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695 of the present inventor, incorporated herein by reference." '239 patent at 8:66-9:7. According to the '695 patent, these dielectrics are required to be in tensile stress because the '695 Patent claims circuits in free-standing dielectric layers where the only support for the layer comes from the substrate material around the edge of the structure. *See, e.g.,* '695 patent at Figs. 1i and 1j; 2:34-37; 5:62- 6:5. The '695 patent states that "[l]ow stress is defined relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being **less than 8×10^8 dynes/cm^2 (preferably 1×10^7 dynes/cm^2) in tension.**" '695 patent at 11:33–37 (emphasis added); *see also id.* at 1:53-58 ("In accordance with the invention, an integrated circuit is formed on a **tensile low stress dielectric** membrane comprised of one layer or a partial layer of semiconductor material in which are formed circuit devices and several layers of dielectric and interconnect metallization.") (emphasis added).

102. The prosecution history of the '499 patent further confirms that the alleged invention limits its dielectric films to those in tensile stress. During prosecution of the '499 patent, the Applicant overcame a prior art rejection by arguing that the "low stress dielectric layer" referred to tensile stress and by amending the claims. The Applicant argued that the '695 patent, incorporated by reference in the Asserted Patents, describes the "unsuitability of compressive stress for achieving a substantially flexible circuit membrane." Response to Office

Action (June 20, 2013). The Applicant also argued that "the word 'tensile' does in effect appear in the present specification." *See id.* at pp. 8-9 (emphasis added):

> As discussed during the interview, support for low tensile stress (as opposed to compressive stress) is found at col. 6 line 62 to col. 6, line 5 and elsewhere of U.S. Patent 5,354,695, incorporated by reference at page 17 lines 5-15 of the present specification. The ***unsuitability of compressive stress for achieving a substantially flexible circuit membrane*** is described also at col. 6 line 162 to col. 6, line 5 of 5,354,695. Incorporation by reference is the same as if the document incorporated were set forth verbatim in the specification. Hence, the word "tensile" does in effect appear in the present specification by virtue of the incorporation by reference.

103. Thus, it is my opinion that the term "have stress of about 5×10^8 dynes/cm^2 or less" is indefinite. To the extent the term is not indefinite, it is my opinion that the term means stress in the dielectric layer that is between 0 and $5x10^8$ dynes/cm^2 in tensile.

E. "low stress dielectric"

104. The parties' proposed constructions for "low stress dielectric" / "low stress dielectric layer" / "low stress dielectric material" / "low-stress … dielectric material" / "low-stress … dielectric layer" / "low stress … dielectric layer" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
"a dielectric having a stress of less than 8 x 10^8 dynes/cm^2"	Indefinite Micron and Samsung: to the extent these terms are found not to be indefinite, they should be construed to mean: "having stress in the dielectric layer that is between 0 and $5x10^8$ dynes/cm^2 in tensile"

105. In my opinion, the phrase "low stress dielectric" is not a term of art that has an accepted plain and ordinary meaning in the field of semiconductor processing. In the context of semiconductor processing, "low stress" is a term of degree that has different meanings in different context, and there is no commonly accepted standard in the semiconductor industry for determining when a stress level is "low."

106. Thus, in my opinion, the term "low stress dielectric" is indefinite because the

term, when interpreted in light of the specification and the prosecution history, fails to inform those skilled in the art about the scope of the claimed invention with reasonable certainty.

107. First, the term "low stress" is a relative term for which there is no agreed-upon range in the art. Patents and publications from around or before the time of the alleged invention used the term "low stress" to refer to a wide range of stress values, spanning at least two orders of magnitude. Some examples are identified below, which show that different publications refer to different levels of stress (ranging from $1x10^7$ dynes/cm^2 to $6x10^9$ dynes/cm^2) as "low stress":

108. U.S. Patent No. 5,279,865 (issued January 18, 1994): "Using the present invention, it is possible to achieve oxide deposition rates of 6000 Angstroms per minute and above, with film stress below **$1.5x10^9$ dynes/cm^2**. Furthermore, using the methodology of the present invention, these deposition rates and film stresses are obtained with a high degree of uniformity from wafer to wafer. It is the inventors opinion that this low temperature, **low stress** process will enhance the reliability of the underlying aluminum interconnect layer." '865 patent at 2:34-42 (emphasis added).

109. U.S. Patent No. 5,500,312 (issued March 19, 1996): "As stated previously, it is advantageous, in the context of mask fabrication, if the multilayer film has **very low stress** so that the pattern introduced into the film will not distort to an unacceptable degree. Therefore, it is advantageous if the film has a stress of about 5 MPa **[$5x10^7$dynes/cm^2]** to about -5 MPa if the film is used as a mask in x-ray lithography. If the film is used as a mask for e-beam lithography, it is advantageous if the film has a stress of about -50 MPa to about 50 MPa **[$5x10^8$dynes/cm^2]**. If the film is used as a mask for ion beam lithography, it is advantageous if it has a stress of about 0 to about 10 MPa **[$1x10^8$dynes/cm^2]**." '312 patent at 3:58-67 (emphasis added).

110. Temple-Boyer et al., "Residual stress in low pressure chemical vapor deposition

SiN_x films deposited from silane and ammonia," J. Vac. Sci. Technol. A 16(4) Jul/Aug. 1998: "Varied SiN_x films have been deposited by low pressure chemical vapor deposition from silane SiH_4 and ammonia NH_3 and the influences of the deposition parameters (temperature, total pressure and NH_3 /SiH_4 gaseous ratio) on the film deposition rate, refractive index (assessed at 830 nm wavelength), stoichiometry and thermomechanical stress are investigated and correlated. **Low stress** (≈600 MPa **[$6x10^9$dynes/cm^2]**) Si_3N_4 films are obtained for the highest deposition temperature and the lowest total pressure but the gaseous ratio is shown to be the dominant parameter."

111. Suzuki et al., "Silicon Nitride Films with Low Hydrogen Content, Low Stress, Low Damage and Stoichiometric Composition by Photo-Assisted Plasma CVD," Japanese J. Appl. Phys. 28, L2316 (1989): "Silicon nitride films with low hydrogen content, **low stress**, low damage and stoichiometric composition by photo-assisted plasma cvd." *Id.* at 2316. "The tensile stress of **0.5-$3x10^9$dynes/cm^2** was induced in PAP-CVD SiN films. . . . The compressive stress of about $3x10^9$ dynes/cm^2 was induced without radiation." Id. at 2318.

112. Cheng, et al., "Ultralow-Stress Silicon-Rich Nitride Films for Microstructure Fabrication," Sensors and Materials, 11, No. 6, 349 (1999): "We have set up a low-pressure chemical vapor deposition (LPCVD) system enabling us to deposit ultralow stress (≤ 10Mpa [sic]), single layer silicon-rich nitride films at high temperatures …" Cheng, et al. were later cited in a paper by J.M. Olsen in which Olsen referred to Cheng's ultra-low stress nitride as LSN (low stress nitride): "Cheng and co-workers [11] observed that the residual stress varies with both DCS/NH_3 ratio and temperature but that the dependence on gas flow is secondary to the effect of temperature. They employed temperatures on the order of 900 °C in their experiments and achieved LSN with residual stresses less than 10 MPa." (J.M. Olsen, "Analysis of LPCVD

Process Conditions for the Deposition of Low Stress Silicon Nitride. Part I: Preliminary LPCVD Experiments," Materials Science in Semiconductor Processing, 5, 51 (2002)). Thus, stress ≤ 10MPa (**≤$1x10^8$dynes/cm^2)** is not clearly viewed as low stress or ultra-low stress.

113. Given the wide range of values in the literature at the time of filing the Asserted Patents (ranging from $1x10^7$ dynes/cm^2 to $6x10^9$ dynes/cm^2, which reflects a difference of a factor of 600), one of ordinary skill in the art would not understand "low stress" to have a clear and well-defined meaning. Instead, the understanding of what is "low stress" will vary from one person skilled in the art to another.

114. Second, the term "low stress dielectric" is indefinite because the stress value varies depending on where and how the measurement is made, and several different approaches to measure the stress level in a dielectric were known in the art at the time of invention. *See* discussion in Section VI.D above.

115. Finally, the term would not have clear and definite meaning to one of ordinary skill in the art because it does not specify what kind of stress is contemplated, as explained in Section VI.D above.

116. Thus, it is my opinion that the "low stress" claim terms are indefinite. To the extent the terms are not indefinite, it is my opinion that the terms mean stress in the dielectric layer is between 0 and $5x10^8$ dynes/cm^2 in tensile. This is the only stress level described by the specification as suitable for the alleged invention.

117. The specification of the '239 patent describes that "low stress" dielectrics are "less than 5×10^8 dynes/cm^2": "The thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher

stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication." '239 patent at 8:66-9:4. The specification never mentions the 8 x 10^8 dynes/cm^2 value in Plaintiff's proposed construction, and this value appears only in the Leedy '695 prior art. *See id.*; Leedy '695 at 11:36.

118. Moreover, the intrinsic evidence limits the "low stress dielectric" to dielectric layers having tensile stress for the reasons stated above in Section VI.D.

119. In sum, the term "low stress dielectric" would not have a clear and definite meaning to a person of ordinary skill in the art because "low stress" is a term of degree that has been used to describe a wide range (i.e., two orders of magnitude) of stress values in the art. To the extent the term is not indefinite, it is my opinion that the term means stress in the dielectric layer that is between 0 and 5x10^8 dynes/cm^2 in tensile.

F. Interconnection / Bonding / Conductive Path Terms

120. The parties' proposed constructions for "vertically interconnected circuit block stacks" and "vertically interconnected circuit blocks" are in the table below.

Plaintiff's Proposal	**Defendants' Proposal**
Plain and ordinary meaning, which is "vertically electrically connected circuit block stacks" and "vertically electrically connected circuit blocks."	"[stacks of circuit layer blocks / blocks of circuit layers] electrically connected by conductors that pass vertically through at least one of the circuit layers"

121. The parties' proposed constructions for "a plurality of vertical interconnect segments interconnecting the first and second integrated circuit layers, wherein each vertical interconnect segment forms an interconnection only between a pair of adjacent integrated circuits" are in the table below.

Plaintiff's Proposal	**Defendants' Proposal**

Plain and ordinary meaning of "vertical interconnect segments," which is "vertical electrical connections."	"vertical interconnect segments" means "segments of electrical conductors that pass vertically through a circuit layer"

122. The parties' proposed constructions for "said plurality of first interconnection and said plurality of second interconnections are substantially aligned with each other, and said plurality of first interconnections and said plurality of second interconnections are electrically coupled together to form a plurality of vertical interconnections, including redundant vertical interconnections" are in the table below.

Plaintiff's Proposal	**Defendants' Proposal**
Plain and ordinary meaning of "vertical interconnections," which is "vertical electrical connections."	"vertical interconnections" means "electrical connections provided by conductors that pass vertically through a circuit layer"

123. The parties' proposed constructions for "at least one interconnection between two of the plurality of substrates" are in the table below.

Plaintiff's Proposal	**Defendants' Proposal**
Plain and ordinary meaning, which is "at least one electrical connection between two of the plurality of substrates."	"interconnection between two of the plurality of substrates" means "electrical connection between two substrates provided by conductors that pass through one or more of the substrates"

124. The parties' proposed constructions for "a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof" and "a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, which is "a bonding layer physically joining together the adjacent substrates, the bonding layer being formed by physically joining first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof" or "a bonding layer physically joining together the adjacent dice, the bonding layer physically joining first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice."	"a layer physically joining a majority of the surface area of first and second substantially planar surfaces of adjacent substrates to form interconnects between the two surfaces" / "a layer, having a portion not at the edges of the adjacent dice, physically joining the substantially planar surfaces of adjacent dice to form interconnects between the two surfaces"

125. The parties' proposed constructions for "wherein the semiconductor die is attached to the first surface of the substrate by one or more bonds including one bond located other than at the edges of the semiconductor die" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, which is "wherein the semiconductor die is attached to the first surface of the substrate by one or more physical connections, including one physical connection located other than at the edges of the semiconductor die."	"one location of the semiconductor die, other than at its edges, is physically joined to the first surface of the substrate to form interconnects therebetween"

126. The parties' proposed constructions for "a first integrated circuit having circuitry formed on a front surface thereof, the front surface or a back surface being bonded to the circuit substrate" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning of "the front surface or a back surface being bonded to the circuit substrate," which is "the front surface or a back surface being physically joined to the circuit substrate."	"the front surface or a back surface being bonded to the circuit substrate" means "the front surface or a back surface [of the first integrated circuit] is physically joined to the circuit substrate to form interconnects therebetween"

127. The parties' proposed constructions for "the first and second substrates are

bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal" and "two of the plurality of substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, which is "physically joined in a fixed relationship to one another at least mostly with metal, or at least mostly with silicon-based dielectric material and metal" or "physically joined in fixed relationship to one another at least mostly with metal, or at least mostly with silicon-based dielectric material and metal."	"[the first and second substrates / two of the plurality of substrates] are physically joined in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon- based dielectric material and metal to form interconnects therebetween"

128. The parties' proposed constructions for "a second substrate bonded to the first surface of the first substrate to form conductive paths between the first substrate and the second substrate" and "a semiconductor die having an integrated circuit formed thereon bonded to the first surface of the substrate with conductive paths between the substrate and the die" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, which is "physically joined to the first surface of the first substrate to form electrically conductive paths between the first substrate and the second substrate" or "physically joined to the first surface of the substrate with electrically conductive paths between the substrate and the die."	"[a second substrate / a semiconductor die having an integrated circuit formed thereon] physically joined to the first surface of the [first substrate / substrate] to form interconnects therebetween"

129. The parties' proposed constructions for "conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate" and "conductive paths between the interconnect

contacts supported by the first surface of the first substrate and of the interconnect contacts supported by the second substrate" are in the table below.

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, which is "electrically conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate" or "electrically conductive paths between the interconnect contacts supported by the first surface of the first substrate and of the interconnect contacts supported by the second substrate."	"electrical connections formed by joining the first and second substrates so as to connect the interconnect contacts supported by the [topside / first] surface of the first substrate to the interconnect contacts supported by the second substrate"

130. In the Background of the Invention, the Asserted Patents acknowledge that "[a]ssembling die in a stacked or three dimensional (3D) manner," including with regard to memory, was known in the art at the time of the alleged invention. '239 patent, 2:34-48. The Asserted Patents explain that "conventional DRAM circuits in die form were stacked and the interconnect between each DRAM in the stack was formed along the outside surface of the circuit stack." *Id.* at 2:41-44. These interconnections along the outside surface of the circuit stack were typically wire bonds, which interconnect different dice by extending electrical connections between bond pads placed along the peripheral surface of the dice. The Asserted Patents recognize that "[t]hese products have been available for the past several years and have proved to be too expensive for commercial applications." *Id.* at 2:44-48. In addition, the specification criticized this approach of stacking for suffering excessive interconnect delay. *See id.* at 3:27-34 (explaining that access time is slower in these conventional products compared to the alleged invention). Thus, the Asserted Patents criticize the use of conventional wire bonding between stacked DRAM dice, which makes clear to a person skilled in the art that the purported invention is to use an interconnection approach other than wire bonding to interconnect stacked

DRAM dice.

131. The "invention" described in the Asserted Patents, which is referred to as a "3DS (Three Dimensional Structure) memory device," allegedly improves upon such conventional stacked memory products by, among other things, interconnecting stacked integrated circuit layers via a fine-grain vertical interconnect comprised of electrical conductors that pass through a circuit layer as opposed to wire bonds. The Asserted Patents provide an explicit definition for the term "fine-grain inter-layer vertical interconnect":

> The term fine-grain inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 μm and more typically less than 10 μm, but not limited to a pitch of less than 2 μm, as best seen in FIG. *2a* and FIG. *2b.* The fine-grain inter-layer vertical interconnect also functions to bond together the various circuit layers.

Id. at 4:10-20. This definition makes clear to a person skilled in the art that vertical interconnections must both (i) pass through circuit layers and (ii) bond together the circuit layers.

132. According to the Asserted Patents, the "present invention" furthers the "following objectives:"

> 1. Several-fold lower fabrication cost per megabyte of memory than circuits conventionally made solely with monolithic circuit integration methods.
> 2. Several-fold higher performance than conventionally made memory circuits.
> 3. Many-fold higher memory density per IC than conventionally made memory circuits.
> 4. Greater designer control of circuit area size, and therefore, cost.
> 5. Circuit dynamic and static self-test of memory cells by an internal controller.
> 6. Dynamic error recovery and reconfiguration.
> 7. Multi-level storage per memory cell.
> 8. Virtual address translation, address windowing, various address functions such as indirect addressing or content addressing, analog circuit functions and various graphics acceleration and microprocessor functions.

Id. at 2:57-3:8. For reasons explained in detail below, several of these objectives—e.g., items 1-4—require the use of vertical interconnections that pass through circuit layers.

133. Not only are vertical interconnections crucial to meet the "objectives" of the alleged invention, the "Summary of the Invention" section of the specification begins by listing four "features" of the alleged invention:

> The present 3DS memory technology is a stacked or 3D circuit assembly technology. Features include:
> 1. Physical separation of the memory circuits and the control logic circuit onto different layers;
> 2. The use of one control logic circuit for several memory circuits;
> 3. Thinning of the memory circuit to less than about 50 μm in thickness forming a substantially flexible substrate with planar processed bond surfaces and bonding the circuit to the circuit stack while still in wafer substrate form; and
> **4. The use of fine-grain high density inter layer vertical bus connections.**

Id. at 3:11-23 (emphasis added). One of these critical "features" of the alleged invention is to use "fine-grain high density inter layer vertical bus connections."

134. Similarly, the Asserted Patents allege that the "3DS memory manufacturing method enables several performance and physical size efficiencies." *Id.* at 3:24-27. For example, a ***conventional*** DRAM "made with a 0.25 μm process could have a die size of 84 mm^2, a memory area to die size ratio of 40% and a access time of about 50 ns for 8 Mbytes of storage." *Id.* at 3:27-30. In comparison, "a ***3DS*** DRAM IC made with the same 0.25 μm process would have a die size of 18.6 mm^2, use 17 DRAM array circuit layers, a memory area to die size ratio of 94.4% and an expected access time of less than 10 ns for 64 Mbytes of storage." *Id.* at 3:30-34 (emphasis added); *see also id.* at 6:5-22.

135. The Asserted Patents also allege that the "3DS DRAM IC manufacturing method represents a scalable, many-fold reduction in the cost per megabyte versus that of conventional DRAM IC manufacturing methods." *Id.* at 3:34-37. Thus, according to the Asserted Patents,

"the 3DS memory manufacturing method represents, at the infrastructure level, a fundamental cost savings." *Id.* at 3:37-40; *see also id.* at 6:23-51.

136. According to the Asserted Patents, these alleged improvements are due, at least in part, to the "fine-grain vertical interconnect between all circuit layers," which refers to "electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 um and more typically less than 10 um, but not limited to a pitch of less than 2 um." *Id.* at 4:10-19. The Asserted Patents explain that, in addition to electrically interconnecting the stacked circuit layers, this fine-grain vertical interconnect "also functions to bond together the various circuit layers." *Id.* at 4:19-20.

137. The Asserted Patents describe various techniques for forming the fine-grain vertical interconnect with each technique resulting in both bonding and interconnecting two adjacent circuit layers. For example, the Asserted Patents explain that there are "two principal fabrication methods for 3DS memory circuits" (i.e., Method A and Method B). *Id.* at 7:36-38; *see also id.* at 9:18-11:25. These "two 3DS memory fabrication methods . . . have a common objective which is the thermal diffusion metal bonding (also referred to as thermal compression bonding) of a number of circuit substrates." *Id.* at 7:37-43. As the Asserted Patents explain, thermal diffusion bonding of two 3DS memory circuits can be achieved by bonding together "two metal surfaces, typically aluminum" (*id.* at 7:62-64), but other "metals that provide acceptable surface bond diffusion capabilities at acceptable temperatures and forming periods" may be used instead (*id.* at 8:29-34). To form the interconnects during bonding, "[t]he metal bonding material on the surfaces of the circuits to be bonded are patterned to be mirror images of each other and to define the various vertical interconnect contacts as indicated in FIG. 2a, FIG. 2b, FIG. 2c and FIG. 5." *Id.* at 8:4-8. The Asserted Patents also describe techniques to avoid the

formation of unsatisfactory bonds or interconnects during the surface bonding process, such as removing or reducing the formation of surface oxides, which may "inhibit[] the forming of a satisfactory bond or may increase the resistance in the vertical interconnections formed by the bond." *Id.* at 8:41-54. Oxides, as one of ordinary skill would have understood, are insulators. Such oxides inhibit electrical conduction. Thus, it is not surprising that the Asserted Patents, which describe the use of bonding to provide electrical interconnection, would want to remove or reduce those surface oxides from the conductive bonding materials. The Asserted Patents disclose the use of conductive materials, such as metal for "bonding two circuit substrates" and "simultaneously forming the vertical interconnection between the two respective circuit layers or substrates." *Id.* at 8:8-11.

138. While "thermal diffusion metal bonding is preferred, . . . the invention contemplates bonding of separate memory controller and memory array substrates by any of various conventional surface bonding methods, such as anisotropically conductive epoxy adhesive." *Id.* at 6:52-60. For example, the "bonding material is not limited to metal, and could be a combination of bonding materials, such as highly conductive polysilicon, some of which are non-conducting such as silicon dioxide." *Id.* at 8:34-40. However, all contemplated surface bonding methods "form interconnects between the two [substrates] to provide random access data storage." *Id.* at 6:52-60.

139. Referring to the two principal fabrication methods for 3DS memory circuits, Method A "assumes the several circuit layers will be bonded to a common support substrate and subsequently thinned in place" (*id.* at 9:18-21) and Method B "assumes that a circuit substrate will first be bonded to a transfer substrate, thinned and then bonded to a common substrate as a layer of the circuit stack," after which "[t]he transfer substrate is then released" (*id.* at 10:53-56).

These are sometimes referred to as face-down bonding (Method A) and face-up bonding (Method B), respectively. In either case, the bond and interconnect interface includes dielectric-to-dielectric areas and metal-to-metal interfaces (i.e., fine-grain vertical interconnect). For example, as explained with respect to Method A, Step 3 involves "[p]rocess[ing] the thinned backside of the second substrate to form vertical interconnections such as that shown in FIG. 4 with the bonded surface side of the second substrate." *Id.* at 9:57-59. This process "typically comprises conventional semiconductor processing steps of dielectric and metal deposition, lithography and RIE," and "result[s] in a patterned metal layer that is similar to the topside bond material pattern to facilitate the subsequent bonding of an additional circuit substrate." *Id.* at 9:59-66. A similar process is described in Step 3 of Method B. *Id.* at 11:2-11. No other techniques for bonding and / or interconnecting stacked circuit layers is described or contemplated.

140. While both Method A and Method B mention wire bonding, they do so only in the context of a terminal pattern for connecting the 3DS memory device to a printed circuit board, a higher-level multi-die package, or another 3DS memory device, and not for interconnecting stacked circuit layers. Specifically, two alternative situations where wire bonds are contemplated are:

(1) "a terminal pattern such as a conventional I/O IC bond pad (wire bonding) pattern, a pattern for thermal diffusion bonding of the 3DS memory circuit to another die (either another 3DS circuit or a conventional die), or a pattern for insertion interconnection, conventional DCA (Direct Chip Attach) or FCA (Flip-Chip Attach)" (*id.* at 9:63-10:5; *see also id.* at 11:12-24), and

(2) "a 3DS memory circuit can be bonded face up to a conventional IC in die form or MCM substrate and wire bonding used to form conventional I/O interconnections" (*id.* at 10:47-50).

141. The first alternative for packaging the 3DS memory device above is describing

the patterning process for packaging. In the second alternative for packaging the 3DS memory device above, the wire interconnection is not related to interconnecting the stacked circuit layers in the 3DS memory device itself, as was discussed for the conventional products and criticized in the Background of the Invention as having too high a cost to manufacture. To illustrate, referring to FIG. 1c, the Asserted Patents contemplate using wire bonding to connect 3DS DRAM IC stack 100 to a larger conventional IC or another 3DS IC 107, but not for connecting the circuit layers within the 3DS DRAM IC stack 100 (i.e., layers 101 and 103 shown in FIGS. 1a and 1b) to one another.

142. Neither wire bonding nor wire interconnection is described or otherwise contemplated in the Asserted Patents for the interconnection between circuit layers within the 3DS circuit stack. Indeed, the Asserted Patents, in their Background of the Invention as discussed above, expressly distinguished their invention from the prior art 3D circuit stacks, which relied on such conventional interconnections.

143. My understanding of conventional I/O bond pads or interconnects, as discussed in the Asserted Patents, is consistent with statements made by the applicant during prosecution of the application leading to U.S. Patent No. 8,035,233, which is related to and shares the same specification as the ’239 patent. Specifically, the applicant explained that the conventional I/O bond pads discussed in the Asserted Patents refer to pads that “may be connected to package leads via bond wires, solder balls, etc.,” “[w]hen the disclosed stacked integrated circuit is *packaged*.” Ex. 15-21 at 4-5. Thus, these I/O bond pads, which are part of the “topmost ‘bond-out’ layer . . . visible in Figure 1A,” do not bond together and interconnect different integrated circuit layers of a stacked integrated circuit. *Id.* Instead, inner bond layers perform these functions: “The bond layers 105a-105c [in FIG. 1b], on the other hand, are not present in a

single-layer integrated circuit. They serve to bond together and interconnect different integrated circuit layers of a stacked integrated circuit." *Id.* at 5.

144. In fact, in my opinion, other bonding and interconnect techniques that do not use the disclosed fine-grained vertical interconnect would defeat the objectives and advantages of the 3DS memory device described in the Asserted Patents. For example, as I discussed above, the Asserted Patents describe these techniques as lowering cost, improving device performance, and increasing memory density compared to conventional wire bonded circuit layers, including conventional stacked memory devices.

145. According to the Asserted Patents, the fine-grained vertical interconnect lowers cost because it requires shorter interconnection lengths compared to other types of interconnections, such as wire bonds. As explained in the Asserted Patents, the fine-grained vertical interconnect refers to vertical "electrical conductors that pass through a circuit layer with or without an intervening device element." '239 Patent at 4:13-19. Because these electrical conductors run vertically, less metal or other conductive material is required to interconnect different dice than if a conventional technique like wire bonding was used. In comparison, wire bonded dice must run both vertically, laterally, and around the edges of the stacked dice. That is, wire bonding stacked memory dice requires interconnections that extend first from the memory core to the edge of the die where a pad is located, a wire then extends from the pad to a pad located on a different die, and finally a wire runs from the pad on the different die to the core of the different die. The shorter interconnection lengths provided by the fine-grained vertical interconnect also lower cost by reducing power consumption and dissipation.

146. Additionally, the fine-grained vertical interconnect is efficiently formed during a batch process, in that all of the interconnects are formed at the same time during bonding across

the entire wafer (not only across a die). In comparison, conventional wire bonding involves forming each wire bond in separate steps for each die (rather than across the entire wafer), which would result in increased costs. The lowering of cost is one of the key "objectives" stated in the specification of the Asserted Patents. *See, e.g.*, '239 Patent at 2:57-3:8. As a result, the Asserted Patents teach away from wire bonding stacked memory dice.

147. According to the Asserted Patents, because the fine-grained vertical interconnect is high density and much shorter than dice interconnected along the outside edges of the dice with wires, the fine-grained vertical interconnect also significantly improves overall device performance. For example, the 3DS DRAM IC techniques described in the Asserted Patents allegedly provides "an expected access time of less than 10 ns for 64 Mbytes of storage" for a 64 Mbit DRAM made with a 0.25 μm process whereas conventional techniques only provide an "access time of about 50 ns for 8 Mbytes of storage." *Id.* at 3:27-34. These performance improvements are due to the short length and high density of the fine-grained vertical interconnect compared to wire bonds, which have low density (due to surface perimeter constraints) and require long wiring.

148. The short length of the fine-grained vertical interconnect reduces latency, resistance, and heat while the high density of interconnects increases bandwidth. One of ordinary skill would have understood that latency, which reflects the time delay for a signal to travel from one location on the IC to another location, would naturally be smaller for shorter interconnection lengths (fine-grained interconnects) than for longer interconnection lengths (conventional wire bonds).

149. One of ordinary skill would have understood that the resistance of an interconnect is proportional to the length of the interconnection (i.e., $R = \rho L/A$, where R is the resistance, ρ is

the resistivity of the interconnection (which is a property of the interconnect material), L is the interconnect length, and A is the cross-sectional area of the interconnection). Because the fine-grained vertical interconnect described in the Asserted Patent is shorter than conventional wire bonds, the resistance of the fine-grained vertical interconnect would be less than for longer interconnection lengths, such as the lengths of conventional wire bonds.

150. Additionally, the Asserted Patents claim that the "fine-grain vertical interconnect method allows thousands of interconnects per block at an increase in die area of only a few percent." *Id.* at 6:7-9. According to the Asserted Patents, "[t]he only limitation on the number of vertical interconnections is the overhead such vertical interconnections impose on the cost of the circuit." *Id.* at 6:5-7. The improvement of performance is another of the key "objectives" stated in the specification of the Asserted Patents. *See, e.g., id*. at 2:57-3:8.

151. The Asserted Patents also describe additional alleged benefits provided by the reduced latency and increased bandwidth of the fine-grained vertical interconnect. For example, unlike with conventional interconnection techniques, the fine-grained vertical interconnect allows one to mix and match different dice that not only are manufactured using different process steps but also different manufacturing technologies. As explained in the Asserted Patents, this allows for the 3DS memory device to "decouple[] control functions that normally would be found adjacent the memory cells of monolithic memory circuits and segregates them to the controller circuit." *Id.* at 6:23-26. According to the Asserted Patents, the ability to physically segregate the control logic and the memory arrays onto different dice simplifies and reduces the cost of fabrication:

> This physical segregation by function also allows fabrication process segregation of the two very different fabrication technologies used for the control logic and the memory array, again realizing additional fabrication cost savings versus the more complicated combined logic/memory fabrication process used for conventional

> memory. The memory array can also be fabricated in a process technology without consideration of the process requirements of control logic functions. This results in the ability to design higher performance controller functions at lower cost than is the case with present memory circuits. Furthermore, the memory array circuit can also be fabricated with fewer process steps and nominally reduce memory circuit fabrication costs by 30% to 40% (e.g., in the case of a DRAM array, the process technology can be limited to NMOS or PMOS transistors versus CMOS).

Id. at 6:36-51. The ability to segregate the control logic and the memory is yet another of the key "objectives" stated in the specification of the Asserted Patents. *See, e.g., id.* at 2:57-3:8.

152. Additionally, "[t]he control functions, rather than occurring on each memory array layer as in conventional memory ICs, occur only once in the controller circuit." *Id.* at 6:26-28. "This creates an economy by which several memory array layers share the same controller logic, and therefore, lowers the net cost per memory cell by as much as a factor of two versus conventional memory design." *Id.* at 6:28-32.

153. According to the Asserted Patents, the segregation of the control logic and the memory arrays onto different layers also increases memory density. This is because the area conventionally reserved for the control logic is now available for additional memory arrays. The Asserted Patents also describe that memory density can be increased by using fine-grained vertical interconnect over wire bonding because die surface area is no longer restricted by wire bond pads that would normally be placed on the outside surface of the die. Additionally, the fine-grained vertical interconnect, while significantly increasing the number of interconnections, requires less die surface area compared to conventional devices that use wire bonds. As noted above, the Asserted Patents explain that "[t]he fine-grain vertical interconnect method allows thousands of interconnects per block at an increase in die area of only a few percent." *Id.* at 6:7-9. The result is a significantly higher memory area to die size ratio compared to conventional

memory circuit designs, as explained in the Asserted Patents with reference to FIG. 2b:

> As an example, the overhead of the vertical interconnect shown in FIG. 2 b for a DRAM memory block of 4 Mbits with two read/write ports and implemented in 0.35 µm or 0.15 µm design rules consists of approximately 5,000 connections and is less than 6% of the total area of the memory array block. Therefore, the vertical interconnect overhead for each memory array circuit layer in the 3DS DRAM circuit is less than 6%. This is significantly less than that presently experienced in monolithic DRAM circuit designs where the percentage of non-memory cell area can exceed 40%. In a completed 3DS DRAM circuit the percentage of non-memory cell area is typically less than 10% of the total area of all circuits in the stacked structure.

Id. at 6:10-22; *see also id.* at 3:24-34 (describing an increase of the memory area to die size ratio from 40% for wire bonded dice to 94.4% for dice interconnected with the fine-grained vertical interconnect). The improvement of memory density is yet another of the key "objectives" stated in the specification of the Asserted Patents. *See, e.g., id*. at 2:57-3:8.

154. Likewise, "[t]he segregation of the control functions to a separate controller circuit allows more area for such functions (i.e., an area equal to the area one or several of the memory array blocks)." *Id.* at 6:33-36. The increased area allows for higher performance controller functions (at lower cost). *Id.* at 6:36-51. While such a segregation could be implemented with wired peripheral contacts as in the conventional products described in the Background of the Invention, the physical delay in many of the interconnect paths would result in long access times and low memory bandwidth, such that the improvements and advantages described in the Asserted Patents could not be achieved.

155. Accordingly, to meet the alleged objectives and advantages of the 3DS memory device described in the Asserted Patents, the alleged invention of the Asserted Patents requires a fine-grained vertical interconnect between layers in the 3DS device. Other types of interconnections, such as conventional wire interconnection techniques are disparaged as too expensive in the Background of the Invention, and are not contemplated for such interlayer

connection and would defeat these objectives and advantages. In particular, wire bonds would be more expensive, would not provide the same performance, would not provide the same ratio of memory area to die size, and would have limited speed capability if the control logic and the memory arrays are on different die in the stacked device.

1. Interconnection Path Terms

156. For the reasons discussed above (in paragraphs 130-155), it is my opinion that:

- "vertically interconnected circuit block stacks" and "vertically interconnected circuit blocks" mean "[stacks of circuit layer blocks / blocks of circuit layers] electrically connected by conductors that pass vertically through at least one of the circuit layers"
- "vertical interconnect segments" in "a plurality of vertical interconnect segments interconnecting the first and second integrated circuit layers, wherein each vertical interconnect segment forms an interconnection only between a pair of adjacent integrated circuits" means "segments of electrical conductors that pass vertically through a circuit layer"
- "vertical interconnections" in "said plurality of first interconnection and said plurality of second interconnections are substantially aligned with each other, and said plurality of first interconnections and said plurality of second interconnections are electrically coupled together to form a plurality of vertical interconnections, including redundant vertical interconnections" means "electrical connections provided by conductors that pass vertically through a circuit layer"
- "interconnection between two of the plurality of substrates" in "at least one interconnection between two of the plurality of substrates" means "electrical connection between two substrates provided by conductors that pass through one or more of the substrates"

157. My opinion with respect to the meaning of these terms is consistent with the description and objectives of the alleged invention in the specification, as discussed above, which describes only the use of a fine-grain inter-layer vertical interconnect to interconnect adjacent circuit layers or substrates in the 3DS memory device of the alleged invention. As also discussed above, the term fine-grain inter-layer vertical interconnect is defined in the specification to mean electrical conductors that pass through a circuit layer. The electrical

connections provided by conductors that pass through a circuit layer are the only type of connection described or suggested by the specification of the Asserted Patents for carrying out the alleged invention, and are the only type of connection that provides the objectives and advantages described in the Asserted Patents related to 3DS memory devices, including lower cost, improved device performance, and increased memory density.

2. Bonding Terms

158. For the reasons discussed above (in paragraphs 130-155), it is my opinion that:

- "a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof" means "a layer physically joining a majority of the surface area of first and second substantially planar surfaces of adjacent substrates to form interconnects between the two surfaces"

- "a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice" means "a layer, having a portion not at the edges of the adjacent dice, physically joining the substantially planar surfaces of adjacent dice to form interconnects between the two surfaces"

- "wherein the semiconductor die is attached to the first surface of the substrate by one or more bonds including one bond located other than at the edges of the semiconductor die" means "one location of the semiconductor die, other than at its edges, is physically joined to the first surface of the substrate to form interconnects therebetween"

- "a first integrated circuit having circuitry formed on a front surface thereof, the front surface or a back surface being bonded to the circuit substrate" means "the front surface or a back surface being bonded to the circuit substrate" means "the front surface or a back surface [of the first integrated circuit] is physically joined to the circuit substrate to form interconnects therebetween"

- "the first and second substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal" and "two of the plurality of substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal" mean "[the first and second substrates / two of the plurality of substrates] are

physically joined in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal to form interconnects therebetween"

- "a second substrate bonded to the first surface of the first substrate to form conductive paths between the first substrate and the second substrate" and "a semiconductor die having an integrated circuit formed thereon bonded to the first surface of the substrate with conductive paths between the substrate and the die" mean "[a second substrate / a semiconductor die having an integrated circuit formed thereon] physically joined to the first surface of the [first substrate / substrate] to form interconnects therebetween"

159. My opinion with respect to the meaning of these terms is consistent with the specification, as discussed above, which describes bonding adjacent circuit layers using thermal diffusion metal bonding or other surface bonding methods (e.g., conductive epoxy) to form interconnects between the two layers. No other bonding method is described or suggested for carrying out the alleged invention, as the bonding method must form a fine-grain inter-layer vertical interconnect to interconnect adjacent circuit layers or substrates in a 3DS memory device. As also discussed above, the term fine-grain inter-layer vertical interconnect is defined in the specification to mean electrical conductors that pass through a circuit layer. The interconnections provided by conductors that pass through a circuit layer are the only type of connection described or suggested by the specification of the Asserted Patents for carrying out the alleged invention, and are the only type of connection that provides the objectives and advantages described in the Asserted Patents related to 3DS memory devices, including lower cost, improved device performance, and increased memory density. Therefore, bonding as used in the terms above must result in the formation of interconnects between the bonded circuit layers.

3. Conductive Path Terms

160. For the reasons discussed above (in paragraphs 130-155), it is my opinion that:

- "conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate" and "conductive paths between the interconnect contacts supported by the first surface of the first substrate and of the interconnect contacts supported by the second substrate" mean "electrical connections formed by joining the first and second substrates so as to connect the interconnect contacts supported by the [topside / first] surface of the first substrate to the interconnect contacts supported by the second substrate"

161. My opinion with respect to the meaning of these terms is consistent with the specification, as discussed above, which describes a fine-grain inter-layer vertical interconnect as the one way to provide conductive paths between adjacent circuit layers or substrates in a 3DS memory device. As also discussed above, the term fine-grain inter-layer vertical interconnect is defined in the specification to mean electrical conductors that pass through a circuit layer. The conductive paths provided by conductors that pass through a circuit layer are the only type of connection described or suggested by the specification of the Asserted Patents for carrying out the alleged invention, and are the only type of connection that provides the objectives and advantages described in the Asserted Patents related to 3DS memory devices, including lower cost, improved device performance, and increased memory density.

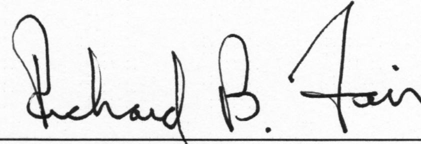
VII. OTHER COMMENTS

162. My opinions are subject to change based on any expert opinions that Elm may later present and information I may receive in the future or additional work I may perform. With this in mind, based on the analysis I have conducted and for the reasons set forth above, I have reached the conclusions and opinions in this Declaration.

163. I understand that the Court does not generally hear expert testimony during the claim construction hearing. However, if I am called to testify, in connection with my anticipated testimony in this action, I may use as exhibits various documents produced in this case that refer or relate to the matters discussed in this Declaration. I have not yet selected the particular

exhibits that might be used. In addition, I may create or assist in the creation of certain demonstrative evidence to assist me in testifying, and I reserve the right to do so, to further support the positions in this Declaration.

164. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.



Dated: January 17, 2019

Dr. Richard Fair

EXHIBIT A

RESUME

Richard B. Fair
3414 CAMBRIDGE RD.
DURHAM, NORTH CAROLINA 27707

EDUCATION AND HONORS

BSEE - Duke University, Durham, N.C., 1964, Presbyterian Church Scholarship, 1961.
MSEE - Penn State University, University Park, Pa., 1966, Sylvania Fellow, 9-64/6-66.
Ph.D. - Duke University, Durham, N.C., 1969, NDEA Fellow, 9-66/6-69.

Awards

(1) Outstanding Paper Award - IEEE Spring Symp., Duke University, 1969.
(2) "Outstanding Young Men of America" Award, 1973.
(3) "Outstanding Young Electrical Engineer of the Year" Award, 1974 -National Award from Eta Kappa Nu.
(4) American Men and Women in Science, 1979 - Present
(5) Who's Who in Technology Today, 1980, 81.
(6) Adjunct Professor, Dept. of Electrical Eng., Duke University, 1980-81.
(7) Who's Who in Frontiers of Science and Technology, 1985, 1986
(8) Who's Who in the Semiconductor Industry, 1986.
(9) Fellow Award, IEEE, 1990
(10) Who's Who in Engineering, 1991, 1993
[11] Who's Who in America, 1991, 1993
(12) Fellow Award, Electrochemical Society, 1994
(13) Professor James F. Gibbons Achievement Award, 4th International Conference on Advanced Thermal Processing, 1996
(14) Third Millennium Medal, IEEE, 2000
(15) Solid State Science and Technology Award – The Electrochemical Society, 2003

MEMBERSHIPS / PROFESSIONAL ACTIVITIES

(1) Member, Sigma Xi
(2) Fellow, Electrochemical Society
- a. Session Chairman numerous times, 1975-present
- b. Symposium Chairman - "Diffusion Processes in Semiconducting Materials," St. Louis, 1980
- c. Member of Electronics Division Executive Committee, 1987 -
- d. Organizing Committee - 6th International Symposium on ULSI Science and Technology
- e. Organizing Committee - 1st Inter. Conf. On ULSI Process Integration - 1999.

f. Organizing Committee - Joint Electronics/Dielectric General Session - 1997-
g. Co-chair, Sixth International Symposium on ULSI Science and Technology, Montreal (1997)

(3) Life Fellow- IEEE
a. Session Chairman at 1977-78 International Electron Device Meetings (IEDM)
b. Chairman, Solid State Device Committee for 1978 IEDM
c. Member, Integrated Circuit Technology Subcommittee for 1982 IEDM
d. Member of Editorial Board - Proceedings of the IEEE - 1988-
e. Editor, Proceedings of IEEE - 1993- 2001
f. Associate Editor - Trans. Electron Devices - 1990-1993
g. Guest Editor, Special Issue on NSF Engineering Research Centers, Proceedings of IEEE, Jan. 1993.
h. Member, IEEE Publications Board - 1993-

(4) Electronic Materials Committee of AIME - 1985 - 1989
(5) Materials Research Society
a. Symposium Co-Chairman - "Impurity Diffusion and Gettering in Silicon" - 1984
b. Member of Editorial Board - Bulletin of Materials Research Society - 1985-1987
(6) Co-chair, 1st International Rapid Thermal Processing Conference, Phoenix (1993).
(7) Co-chair, 2nd International Rapid Thermal Processing Conference, Monterey (1994).
[8] Co-chair, 3rd International Rapid Thermal Processing Conference, Amsterdam (1995).
(9) Co-chair, 4th International Rapid Thermal Processing Conference, Boise (1996).
(10) Co-chair, 5th International Rapid Thermal Processing Conference, New Orleans (1997).
(11) Co-Chair, Fourth International Workshop on Meas., Characterization, and Modeling of Ultra- shallow Doping Profiles in Semiconductors, Research Triangle Park, (1999).
(12) Member of Editorial Advisory Board, Journal Microfluidics and Nanofluidics, (2008-

International Activities

(1) Instructor, CEI Europe - 1985 - present
(2) Member, International Advisory Panel, Microelectronics Systems '91 Conference, Kuala Lumpur, Malaysia
(3) Member, International Advisory Committee, Annual Semiconductor Conference '92-99, Bucharest, Romania
(4) Member, International Advisory Committee, 1993 Symposium on Semiconductor Modeling and Simulation, Taipei, Taiwan
(5) Member, Program Committee, Inter. Symposium on Advanced Microelectronic Devices and Processing - 1993, Sendai, Japan

Employment Experience

Present- - Lord-Chandran Professor of Engineering, Pratt School of Engineering

1993-1994 - Director, Microfabrication Technology and the associated Research Institute of MCNC; Professor, Electrical Engineering, Duke University

1990-1993 - Vice President, MCNC and Executive Director, Center for Microelectronic Systems Technologies; Professor, Electrical Engineering, Duke University

1986-1990 - Vice President, Design Research and Technology, MCNC; Professor, Electrical Engineering, Duke University

10/88-3/89 - Acting President, MCNC; Professor, Electrical Engineering, Duke University

1981-1985 - Vice President, Research Program Management, MCNC; Professor, Electrical Engineering, Duke University

1973-1981 - Supervisor, Bell Laboratories, Reading, PA.

1969-1973 - Member of Technical Staff, Bell Laboratories, Reading, PA.

Board Memberships

1992-1994 - Advanced Technology Applications, Inc.
1993- Microelectronic Technology Corp.
1995- present -Engineering Advisory for the Aurora Fund.
1996- present - Technical Advisory Board, Thunderbird Technologies, Inc.
2003- present - Technical Advisory Board, R.J. Mears, Inc.
2004-present – Chairman, Scientific Advisory Board, Advanced Liquid Logic

Courses Taught

EE218 (Integrated Circuit Engineering) Spring Semester 1982-present
EE163 (Introduction to Integrated Circuits) Fall/Spring Semester, 1995-99
EE62 (Introduction to Semiconductor Devices), Spring Semester, 1999-present
ECE299 (Biochip Engineering), Fall Semester, 2005-2007

U.S Patents

(1) U.S. Patent 4,033,027 - Dividing Metal Plated Semiconductor Wafers -
July 5, 1977

(2) U.S. Patent 6,911,132 – Apparatus for Manipulating Droplets by Electrowetting-based Techniques – June 28, 2005
(3) U.S. Patent 6,989,234 – Method and Apparatus for Non-Contact Electrostatic Actuation of Droplets – January 24, 2006
(4) U.S. Patent 7,329,545 – Methods for Sampling a Liquid Flow – February 12, 2008
(5) U.S. Patent 7,439,014 – Droplet-based Surface Modification and Washing – October 21, 2008
(6) U.S. Patent 7,569,129 – Methods for manipulating droplets by electrowetting-based techniques – August 4, 2009
(7) U.S. Patent 7,727,723 – Droplet-based pyrosequencing – June 1, 2010.
(8) U.S. Patent 7,759,132 – Methods for performing microfluidic sampling – July 20, 2010.
(9) U.S. Patent 8,048,628 – Methods for nucleic acid amplification on a printed circuit board – Nov. 1, 2011
(10) U.S. Patent 8,147,668 – Apparatus for manipulating droplets – April 3, 2012.
(11) U.S. Patent 8,221,605 – Apparatus for manipulating droplets – July 17, 2012.
(12) U.S. Patent 8,287,711 – Apparatus for manipulating droplets – October 16, 2012.
(13) U.S. Patent 8,313,895 – Droplet-based surface modification and washing – Nov. 20, 2012
(14) U.S. Patent 8,349,276 – Apparatus and methods for manipulating droplets on a printed circuit board – Jan. 8, 2013.
(15) U.S. Patent 8,388,909 – Apparatus and methods for manipulating droplets – Mar.5, 2013.
(16) U.S. Patent 8,389,297 – Droplet-based affinity assay device and system – Mar.5, 2013.
(17) U.S. Patent 8,394,249 – Methods for manipulating droplets by electrowetting-based techniques – Mar.12, 2013.
(18) U.S. Patent 8,613,889 – Droplet-based washing – December 24, 2013.
(19) U.S. Patent 8,541,176 – Droplet-based surface modification and washing – September 24, 2013.
(20) U.S. Patent 8,524,506 – Methods for sampling a liquid flow – September 3, 2013.
(21) U.S. Patent 8,492,168 – Droplet-based affinity assays – July 23, 2013.
(22) U.S. Patent 8,470,606 – Manipulation of beads in droplets and methods for splitting droplets – June 25, 2013.
(23) U.S. Patent 8,685, 754 – Droplet actuator devices and methods for immunoassays and washing – April 1, 2014.
(24) U.S. Patent 8,846,414 – Detection of cardiac markers on a droplet actuator – Sept. 30, 2014.
(25) US Patent 8,871,071, "Droplet manipulation device", Oct. 28, 2014.
(26) US Patent 8,906,627, "Apparatuses and methods for manipulating droplets", Dec. 9, 2014.
(27) US Patent 8,951,721, "Droplet-based surface modification and washing," Feb. 10, 2015
(28) US Patent 8,980,198, "Filler fluids for droplet operations," Mar. 17, 2015
(29) US Patent 9,046,514, "Droplet actuator devices and methods employing magnetic beads," - June 2, 2015
(30) US Patent 9,110,017, "Apparatuses and methods for manipulating droplets", Aug. 18, 2015.
(31) US Patent 9,180,450 "Droplet manipulation system and method," Nov. 10, 2015.
(32) US Patent 9,243,282, "Droplet-based pyrosequencing," Jan. 26, 2016.
(33) US Patent 9,395,361, "Bead incubation and washing on a droplet actuator," July 19, 2016.
(34) US Patent 9,476,856, "Droplet-based affinity assays," Oct. 25, 2016.
(35) US Patent 9,638,662, "Apparatuses and methods for manipulating droplets," May 2, 2017.
(36) US Patent 10,022,719, "Dropletmanipulation device," July 17, 2018.

U.S. Applications:

1 20160231268 DROPLET-BASED SURFACE MODIFICATION AND WASHING
2 20160114320 Droplet Manipulation Device
3 20160108433 SYSTEMS, APPARATUS, AND METHODS FOR DROPLET-BASED MICROFLUIDICS CELL PORATION
4 20150336098 Apparatuses and Methods for Manipulating Droplets
5 20150314293 Droplet Actuator Devices and Methods Employing Magnetic Beads
6 20150174577 Filler Fluids for Droplet Operations
7 20150148238 DROPLET-BASED SURFACE MODIFICATION AND WASHING
8 20150060284 Apparatuses and Methods for Manipulating Droplets

WO and EP Patents

1. EP1859330B1
2. EP2016189B1
3. EP1479365B1
4. EP2016091B1
5. WO/2009/111723A1
6. WO/2009/111723A9
7. EP2016189A2
8. EP2016091A2
9. EP1859330A2
10. WO/2007/120241A3
11. WO/2007/120241A2
12. WO/2007/120240A2
13. WO/2007/120240A3
14. WO/2006/081558A2
15. WO/2006/081558A3
16. EP1554568A4
17. EP1554568A2
18. WO/2004/030820A2
19. WO/2004/029608A1
20. WO/2004/029585A1
21.

PUBLICATIONS
REFEREED ARCHIVAL JOURNALS

(1) R. B. Fair, "A Wide Slit Scanning Method for Measuring Electron and Ion Beam Profiles," J. Phys. E., 4, 35 (1971).
(2) R. B. Fair, "A Self-Consistent Method of Estimating Non-Step Junction Doping Profiles from Capacitance - Voltage Measurements," J. Electrochem. Soc.,118, 971 (1971).
(3) R. B. Fair, "Analysis and Design of Ion Beam Deposition Apparatus," J. Appl. Phys., 42, 3176 (1971).
(4) R. B. Fair, "Harmonic Distortion in the Junction Field-Effect Transistor with Field-Dependent Mobility," IEEE Trans. Electron Dev., ED-19, 9 (1972).

(5) R. B. Fair, "Profile Estimation of High Concentration Arsenic Diffusion," J. Appl. Phys., 43, 1278 (1972).
(6) R. B. Fair, "High Concentration Arsenic Diffusion in Silicon form A Doped Oxide Source," J. Electrochem. Soc., 119, 1389 (1972).
(7) R. B. Fair and G. R.Weber, "The Effect of Complex Formation on the Diffusion of Arsenic in Silicon," J. Appl. Phys., 44, 273 (1973).
(8) R. B. Fair,"Quantitative Theory of Retarded Base Diffusion in Silicon NPN Structures with Arsenic Emitters," J. Appl. Phys., 44, 283 (1973).
(9) Total Arsenic Concentration in Heavily Doped n and p Type Silicon," J. Appl. Phys., 44, 280 (1973).
(10) R. B. Fair, "Explanation of Anomalous Base Regions in Transistors," Appl. Phys. Lett., 22, 186 (1973).
(11) R. B. Fair,"Optimum Low-Level Injection Efficiency of Silicon Transistors with Shallow Arsenic Emitters," IEEE Trans. Electron Devices, Vol. ED-20, 642 (1973).
(12) R. B. Fair, "Correction of Calculated Vacancy Diffusion Length at 1000 C in Silicon," J. Appl. Phys., 44, 3794 (1973).
(13) R. B. Fair, "Cooperative Effects Between Arsenic and Boron in Silicon During Simultaneous Diffusions from Ion-Implanted and Chemical Source Predepositions," Solid State Electronics, 17, 17 (1974).
(14) R. B. Fair, "Graphical Design and Iterative Analysis of the DC Parameters of GaAs FETS," IEEE Trans. Electron Devices, Vol. ED-21, 357 (1974).
(15) R. B. Fair, "Boron Diffusion in Silicon-Concentration and Orientation Dependence, Background Effects and Profile Estimation," J. Electrochem. Soc., 122, 800 (1975).
(16) R. B. Fair and P.N. Pappas, "Diffusion of Ion Implanted Boron in High Concentration P and As-Doped Silicon," J. Electrochemical Soc., 122, 1241 (1975).
(17) R.B. Fair and P.N. Pappas, "The Gettering of Boron by an Ion-Implanted Antimony Layer in Silicon," Solid State Electrons, 18, 1131 (1975).
(18) R. B. Fair, "Performance Estimation and Optimized Design Considerations for Microwave Power GaAs FETS," IEEE Trans. Electron Dev., ED-22, (1975).
(19) R. B. Fair and J. C. C. Tsai, "The Diffusion of Ion-Implanted As in Si," J. Electrochem. Soc., 122, 1689 (1975).
(20) R. B. Fair and J. C. C. Tsai, "Profile Parameters of Implanted-Diffused Arsenic Layers in Silicon," J. Electrochem. Soc., 123, 583 (1976).
(21) R. B. Fair, "Transistor Design Considerations for Low-Noise Preamplifiers," IEEE Trans. Nuclear Sci., Vol. NS-23, 218 (Feb. 1976).
(22) R. B. Fair, H. W. Wivell, "Zener and Avalanche Breakdown in As-Implanted Low-Voltage Si n-p Junctions," IEEE Trans. Electron Dev., Vol. ED-23, p. 512 (May 1976).
(23) R. B. Fair and J. C. C. Tsai, "A Quantitative Model of the Diffusion of Phosphorus in Silicon and the Emitter Dip Effect," J. Electrochem Soc., Vol. 124, 1107 (1977).
(24) R. B. Fair, "Analysis of Phosphorus-Diffused Layers in Silicon," J. Electrochem. Soc., 125, 323-327 (Feb. 1978).
(25) R. B. Fair, "Quantified Conditions for Emitter-Misfit Dislocation Formation in Silicon," J. Electrochem. Soc., 125, 928-926 (June, 1978).
(26) R. B. Fair and J. C. C. Tsai, "Discussion of A Quantitative Model for the Diffusion of Phosphorus in Silicon and the Emitter Dip Effect," J. Electrochem. Soc, 125, 997-998 (June 1978).

(27) R. B. Fair and J. C. C. Tsai, "Theory and Direct Measurement of Boron Segregation in SiO2 During Dry, Near Dry, and Wet O2 Oxidation, J. Electrochem. Soc., 125, 2050 (1978).
(28) R. B. Fair, "Effect of Strain-Induced Band Gap Narrowing on E-centre Concentrations in Si," Inst. Phys. Conf. Ser., No. 46, Chapter 9, 559 (1979).
(29) R. B. Fair, "The Effect of Strain-Induced Band-Gap Narrowing on High Concentration Phosphorus Diffusion in Silicon," J. Appl. Phys., 50, 860 (1979).
(30) R. B. Fair, "Modeling Laser-Induced Diffusion of Implanted Arsenic in Silicon," J. Appl. Phys., 50, 6552 (1979).
(31) R. B. Fair, "On the Role of Self-Interstitials in Impurity Diffusion in Silicon," J. Appl. Phys., 51, 5828 (1980).
(32) R. B. Fair, "Oxidation, Impurity Diffusion and Defect Growth in Silicon - An Overview," J. Electrochem. Soc., 128, 1360 (1981).
(33) R. B. Fair and R. C. Sun, "Threshold Voltage Instability in MOSFET's, Due to Channel Hot Hole Emission," IEEE Trans. Electron. Devices, ED-28, 83 (1981).
(34) R. B. Fair, "Molecular Transport and Diffusion in Solids," Sensors and Activators, 1, 305 (1981).
(35) R. B. Fair and A. Carim, "On the Doping Dependence of Oxidation-Induced Stacking Fault Shrinkage in Silicon," J. Electrochem Soc., 129, 2319 (1982).
(36) R. B. Fair, "The Silicon Process Balancing Act for VLSI," Solid State Tech., 25, 220 (1982).
(37) W. G. Meyer and R. B. Fair, "Dynamic Behavior of the Build-up of Fixed Charge and Interface States During Hot Carrier Injection in Encapsulated MOSFET's," IEEE Trans. Electron Dev., Vol. ED-30, 96 (1983).
(38) R. B. Fair, "MCNC-Organizing Research on the State Level," IEEE Spectrum, Vol. 20, p. 58 (1983).
(39) R. B. Fair, J. J. Wortman, J. Liu, M. Tischler and N.A. Masnari, "Modeling Physical Limitations on Junction Scaling for CMOS," IEEE Trans. Electron Dev., Vol ED-31, 1180 (1984).
(40) R. B. Fair, J. J. Wortman and J. Liu, "Modeling Rapid Thermal Diffusion of Arsenic and Boron in Silicon," J. Electrochem. Soc., 131, 2387 (1984).
(41) R. B. Fair, "The Role of Vacancies and Self-Interstitials in Impurity Diffusion in Silicon," Materials Science Forum , Vol. 1. (Trans. Tech. Pub. Switzerland) pp. 109-132 (1984).
(42) W. B. Wilson, H. Z Massoud, E. T. Swanson, R. T. George and R. B. Fair "Measurement and Modeling of Charge Feedthrough in n-Channel MOS Analog Switches," IEEE J. Solid State Cir. Vol. SC-20, pp. 1206-1213 (1985).
(43) J. Liu, J. J. Wortman and R. B. Fair, Shallow p +-n Junction for CMOS VLSI Application Using Germanium Preamorphization, IEEE Trans. Electron. Dev., Vol ED-32, 2533 (1985).
(44) R.B. Fair, "Modeling of Dopant Diffusion During Rapid Thermal Annealing," J. Vac. Sci. Technology A4, 926 (1986).
(45) R. B. Fair, M. L. Manda and J. J. Wortman, "The Diffusion of Antimony in Heavily Doped n- and p-type Silicon," J. Mates. Res., 1,705 -717 (1986).
(46) J. C. C. Tsai, D. G. Schimmel, R. B. Fair and W. Maszara, "Point Defect Generation During Phosphorus Diffusion in Silicon-1. Concentrations Above Solid Solubility," J. Electrochem. Soc., .134, 1508 (1987).
(47) R. Subrahmanyan, H. Z. Massoud and R. B. Fair, "The Influence of HCl on the Oxidation - Enhanced Diffusion of Boron and Arsenic in Silicon," J. Appl. Phys., 61, 4804 (1987).

(48) J. C. Tsai, D. G. Schimmel, R. E. Ahrens and R. B. Fair, "Point Defect Generation During Phosphorus Diffusion in Silicon II. Concentrations below Solid Solubility, Ion-Implanted Phosphorus," J. Electrochem. Soc., 134, 2348 (1987).
(49) R. B. Fair, "Reply to Comments of F. F. Morehead," J. Mater. Res., 2, 539 (1987).
(50) R. B. Fair, ."Low-Thermal Budget Process Modeling with the PREDICT Computer Program," IEEE Trans. Electron. Dev., .35, 285 (1988).
(51) A. C. Ajmera, G. A. Rozgonyi and R. B. Fair "Point Defect/Dopant Diffusion Considerations Following Preamorphization of Silicon via Si+ and Ge+ Implantation," Appl. Phys. Lett., 52 (10), 813 (1988).
(52) R.B. Fair and J.E. Rose, "Process Simulation of Submicron Technologies" Semicond. Int.,13, 72, (1987).
(53) M. C. Ozturk, J. J. Wortman and R. B. Fair,."Very Shallow P+n Junction Formation by Low Energy BF2+ Ion Implantation into Crystalline and Germanium Preamorphized Silicon," Appl. Phys. Lett., 52 (12), 963 (1988).
(54) R. Subrahmanyan, H. Z. Massoud and R. B. Fair, "Experimental Characterization of Two-Dimensional Dopant Profiles in Silicon Using Chemical Staining," Appl. Phys. Lett., 52 (25), 2145 (1988).
(55) Y. Kim, H.Z. Massoud and R.B. Fair, "Boron Profile Changes During Low-Temperature Annealing of BF2+-implanted Silicon," Appl. Phys. Lett., .53, 2197 (1988).
(56) Y. Kim, H.Z. Massoud and R.B. Fair, "The Effect of Ion-Implantation Damage on Dopant Diffusion in Silicon During Shallow-Junction Formation," J. Electronic Mater., 18, 143 (1989).
(57) R.B. Fair, "The Role of Transient Damage Annealing in Shallow Junction Formation," Nuclear Instr. and Methods, B37/38, 371 (1989).
(58) W.B. Rogers, H.Z. Massoud, R.B. Fair, U.M. Gosele, T.Y. Tan and G.A. Rozgonyi, "The Role of Silicon Self-Interstitials Supersaturation in the Retardation of Oxygen Precipitation in Czochralski Silicon," J. Appl. Phys., 65, 4215-4219 (1989).
(59) R.B. Fair, "Point Defect Charge-State Effects on Transient Diffusion of Dopants in Si," J. Electrochem. Soc., 137, 667 (1990).
(60) R.B. Fair and G.A. Ruggles, "Thermal Budget Issues for Deep Submicron ULSI," Solid State Tech., .33, 107 (1990).
(61) R.B. Fair, "Damage Removal/Dopant Diffusion Tradeoffs in Ultra-Shallow Implanted p+-n Junctions," IEEE Trans. Electron Dev., vol 37, 2237 (1990).
(62) Y. Kim, H.Z. Massoud and R.B. Fair, "The Effect of Annealing Ambient on Dopant Diffusion in Silicon during Low Temperature Processing, J. Electrochem. Soc. 137, 2599-2603 (1990).
(63) R.B. Fair (Invited), "Challenges to Manufacturing Submicron, Ultra-Large Scale Integrated Circuits," Proc. IEEE, .78, pp. 1687-1705, Nov. 1990.
(64) R. Subrahmanyan, H.Z. Massoud and R.B. Fair, "Comparison of Measured and Simulated Two Dimensional Profiles in Si," J. Electrochem Soc., 137, 1573 (1990).
(65) R.B. Fair, C.L. Gardner, M.J. Johnson, S.W. Kenkel, D.J. Rose, J.E. Rose and R. Subrahmanyan, "Two-Dimensional Process Simulation Using Verified Phenomenological Models," IEEE Trans. Computer-Aided Design, vol. 10, p. 643 (1991).
(66) M.R. Mirabedini, S.H. Goodwin-Johansson, H.Z. Massoud and R.B. Fair, "Subquarter-micrometer Elevated Source and Drain MOSFET Structure using Polysilicon Spacers," Electronic Lett., 30, 1631 (1994).

(67) R.B. Fair and R.A. Gafiteanu, "Modeling Boron Difusion in Thin Oxide p+ Si Gate Technology," IEEE Electron Dev. Lett., 17, 497-499 (1996).
(68) R.B. Fair, "Oxide Thickness Effect on Boron Diffusion in Thin Oxide p+ Si Gate Technology," IEEE Electron Dev. Lett., 17, 242 (1996).
[69] R.B. Fair, "Physical Models of Boron Diffusion in Ultrathin Gate Oxides," J. Electrochem. Soc., 144, 708 (1997).
(70) R.B. Fair, "Modeling Boron Diffusion in Ultrathin Nitrided Oxide p+ Si Gate Technology," IEEE Electron Dev. Lett., 18, 244 (1997).
(71) G. Chen, T. Borca-Tasciuc, and R.B. Fair, "Photon Effect on Radiative Properties of Silicon During Rapid Thermal Processing," J. Appl. Phys. 82, 830 (1997).
[72] R.B. Fair, "History of Some Early Developments in Ion Implantation Technology Leading to Silicon Transistor Manufacturing," Proc. of IEEE, 86, 111 (1998).
(73) R.B. Fair and S. Li, "Photonic Effects in the Deactivation of Ion Implanted Arsenic," J. Appl. Phys., 83, 4081 (1998).
(74) N. Vasudevan, R.B. Fair, and H.Z. Massoud, "Energy Considerations During the Growth of a Molten Filament in Metal-to-metal Amorphous-silicon Antifuses," J. Appl. Phys., 84, 4979 (1998).
(75) T.W. Tsuei, R.L. Wood, C.K. Malek, M.M. Donnelly, and R. B. Fair, "Tapered Microvalves Fabricated by Off-axis X-ray Exposures," Microsystem Technologies, 4, 201 (1998).
(76) N. Vasudevan, R.B. Fair, and H.Z. Massoud, "ON-state Reliability of Amorphous-silicon Antifuses, J. Appl. Phys., 84, 6440 (1998).
(77) N. Vasudevan, H.Z. Massoud, and R.B. Fair, "A Thermal Model for the Initiation of Programming in Metal-to-Metal Amorphous-Silicon Antifuses," J. Electrochem. Soc., 146, 1536-1539 (1999).
(78) R.B. Fair, "Anomalous B Penetration Through Ultrathin Gate Oxides During Rapid Thermal Annealing," IEEE Electron Dev. Lett., 20, 466 (1999).
(79) Y. Wu, H. Niimi, H. Yang, G. Lucovsky, and R.B. Fair, "Suppression of Boron Transport Out of p+ Polycrystalline Silicon at Polycrystalline Silicon Dielectric Interfaces," J. Vac. Sci. Technol. B, 17(4), 1813-1822 (1999).
(80) T. Zhang, A. Dewey, and R.B. Fair, "A Heirarchical Approach to Stochastic Discrete and Continuous Performance Simulation Using Composable Software Components," J. Microelectronics, 31 (1999).
(81) M.G. Pollack, R.B. Fair, and A.D. Shenderov, "Electrowetting-Based Actuation of Liquid Droplets for Microfluidic Applications," *Appl. Phys. Lett*., 77, 1725 (2000).
(82) T. Zhang, F. Cao, A. Dewey, R.B. Fair, and K. Chakrabarty, "Performance Analysis of Microelectrofluidic Systems Using Hierarchical Modeling and Simulation," IEEE Trans. Circuits and Systems II: Analog and Digital Processing, vol. 48, 482 (2001).
(83) J. Ding, K. Chakrabarty and R. B. Fair, "Scheduling of Microfluidic Operations for Reconfigurable Two-Dimensional Electrowetting Arrays", *IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems*, 29, 1463-1468 (2001).
(84) T. Zhang, K. Chakrabarty and R. B. Fair, "Design of Reconfigurable Composite Microsystems Based on Hardware/Software Co-design Principles," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems,* 21, 987 (2002).
(85) M.G. Pollack, A.D. Shenderov, and R.B. Fair, “Electrowetting-based Actuation of Droplets for Integrated Microfluidics,” *Lab on a Chip*, vol. 2, pp. 96-101, 2002.

(86) T. Zhang, K. Chakrabarty and R. B. Fair, "Integrated hierarchical design of microelectrofluidic systems using SystemC", *Microelectronics Journal*, vol. 33, pp. 459-470, May 2002.
(87) H. Ren, R. B. Fair, M. G. Pollack and E. J. Shaughnessy**, "**Dynamics of Electro-wetting Droplet Transport**,** *Sensors and Actuators B: Chemical,* Volume 87, Issue 1, 15 November 2002, Pages 201-206.
(88) P. Paik, V.K. Pamula, M.G. Pollack, and R.B. Fair, "Electrowetting-Based Droplet Mixers for Microfluidic Systems," *Lab on a Chip*, vol. 3, pp.28-33 (2003).
(89) H. Ren, R.B. Fair, and M. Pollack, "Automated On-Chip Droplet Dispensing with Volume Control by Electrowetting Actuation and Capacitance Metering", *Sensors and Actuators B*, 98, 319-327 (2004).
(90) P. Paik, V.K. Pamula, and R.B. Fair, "Rapid Droplet Mixers for Digital Microfluidic Systems," *Lab, on a Chip*, vol. 3, pp.253-259 (2003).
(91) V. Srinivasan, V.K. Pamula, and R.B. Fair, "Droplet-based microfluidic lab-on-a-chip for glucose detection," *Analytica Chimica Acta*, Vol. 507, 145-150 (2004).
(92) T. Zhang, K. Chakrabarty, and R.B. Fair, "Behavioral Modeling and Performance Evaluation of Microfluidics-Based PCR Systems Using System C", IEEE Trans, Computer-Aided Design of Integrated Cir. And Sys., vol. 23, 843 (2004).
(93) V. Srinivasan, V.K. Pamula, and R.B. Fair, "An Integrated Digital Microfluidic Lab-on-a-Chip for Clinical Diagnostics on Human Physiological Fluids," Lab-On-A-Chip, 4, 310 (2004).
(94) F. Su, K. Chakrabarty, and R.B. Fair, "Microfluidics-Based Biochips: Technology Issues, Implementation Platforms, and Design Automation Challenges," *IEEE Trans. Computer-Aided Des. Of Integ. Cir. And Sys.*, vol. 25, pp. 211-223 (2006).
(95) R.B. Fair, "Digital Microfluidics: is a true lab-on-a-chip possible?" *J. Microfluidics and Nanofluidics*, vol. 3, 245-281 (2007). (Invited)
(96) R.B. Fair, A. Khylstov, T.D. Tailor, V. Ivanov, R.D. Evans, V.Srinivasan, V.K. Pamula, M.G. Pollack, P.B. Griffin, J. Zhou, "Chemical and Biological Applications of Digital Microfluidic Devices," *IEEE Design and Test of Computers*, 24, No. 1, pp.10-24, Jan-Feb (2007). (Invited)
(97) J. Zhou, L. Lu, K. Byrapogu, D. Wootton; P. Lelkes, and R. Fair, "Electrowetting Based Multi-microfluidics Array Printing of High Resolution Tissue Construct with Embedded Cells and Growth Factors," *Virtual and Physical Prototyping*, 2:4, 217 – 223 (2007).
(98) L. Luan, R.D. Evans, N.M. Jokerst, and R.B. Fair, "Integrated Optical Sensor in a Digital Microfluidic Platform," IEEE Sensors J., vol. 8, pp. 628-635 (2008).
(99) R. B. Fair and M. A. Shannon and O. K. Tan and O. Geschke and C. H. Ahn and O. Kaynak and M. J. Vellekoop, *Introduction for the special issue on sensors for microfluidic analysis systems*, IEEE Sensors Journal, (2008), vol. 8, pp. 427 – 429.
(100) R.B. Fair, "What is a lab-on-a-chip?" ACM/SIGDA Newsletter, vol. 38, No. 12, (2008)
(101) J.H. Song, R. Evans, Y.-Y. Lin, B.-N. Hsu, and R.B. Fair, "A Scaling Model for Electrowetting-on-Dielectric Microfluidic Actuators," Microfluid Nanofluid Online First, Nov. 2008. In print: vol. 7, 75-89 (2009)
(102) K. Chakrabarty, R.B. Fair, and J. Zeng, "Design Tools for Digital Microfluidic Biochips: Toward Functional Diversification and More than Moore," IEEE Trans. Computer-Aided Des. Integrated Cir. And Sys., vol 29, No. 7,pp. 1001-1017 (2010).

(103) Y-Y Lin, R.D. Evans, E. Welch, B-N Hsu. A.C. Madison and R.B. Fair, Low-voltage electrowetting-on-dielectric platform using multi-layer insulators," Sensors and Actuators B: Chemical, v. 150, 465-470 (2010)
(103) E.R. Welch, Y-Y Lin, A. Madison, R.B. Fair, "Picoliter DNA sequencing chemistry on an electrowetting-based digital microfluidic platform," BioTechnology Journal, v. 6, pp. 165-176 (2011)
(104) D.J. Boles, J.L. Benton, G.J.Siew, M.H. Levy, P.K. Thwar, M.A. Sandahl, J.L. Rouse, L.C. Perkins, A.P. Sudarsan, R. Jalili, V.K. Pamula, V. Srinivasan, R.B. Fair, P.B. Griffin, A.E. Eckhardt, M.G. Pollack, "Droplet-based pyrosequencing using digital microfluidics," Anal. Chem, 83, 8439 (2011)
(105) L. Luan, M.W. Royal, R. Evans, R.B. Fair, and N.M. Jokerst, "Chip scale microresonator sensors integrated with embedded thin film photodetectors on electrowetting digital microfluidics platforms," IEEE Sensors Journal, v. 12, pp. 1794-1800, (2012)
(106) Y-Y Lin, E.F. Welch, R.B. Fair, "Low voltage picoliter droplet manipulation utilizing electrowetting-on-dielectric platforms," Sensors & Actuators, B: Chem. v. 173, pp. 338-345 (2012), http://dx.doi.org/10.1016/j.snb.2012.07.022
(107) M.W. Royal, N.M. Jokerst, and R.B. Fair, "Integrated sample preparation and sensing: polymer microresonator sensors embedded in digital electrowetting microfluidic systems," IEEE Photonics J., 4, 2126-35 (2012)
(108) M.W. Royal, N.M. Jokerst, and R.B. Fair, "Droplet-based sensing: Optical microresonator sensors embedded in digital microfluidics systems, IEEE Sensors J., 13, 4733-42, Dec. 2013.
(109) L. Chen and R.B. Fair, "Digital microfluidics chip with integrated intra-droplet magnetic bead manipulation," Microfluid Nanofluid, published online 24 September, 2015. Print: vol. 19, No. 6, pp. 1335-1348, Dec, 2015.
(110) A.C. Madison, M.W. Royal, and R.B. Fair, "Fluid transport in partially shielded electrowetting on dielectric digital microfluidic device," J. Microelectromechanical Sys., vol. 25, 593-605 (2016).
(111) J.A. Moore, N. Nemat-Gorgani, A.C. Madison, M.A. Sandahl, S. Punnamaraju, A.E. Eckhardt, M.G. Pollack, F.M Vigneault, G.M. Church, R.B. Fair, M.A. Horowitz and P.B. Griffin, "Automated electrotransformation of E. Coli on a digital microfluidic platform using bioactivated magnetic beads," Biomicrofluidics, vol. 11, p. 014110 (2017).
(112) R.B. Fair, "Demonstration of Automated Analysis of Multiple Analytes on an Integrated Digital Microfluidic Platform," Clinical Chem., Published online March 15, 2017.
(113) Andrew C. Madison, Matthew W. Royal, Frederic Vigneault, Liji Chen, Peter B. Griffin, Mark Horowitz, George M. Church, and Richard B. Fair, "Scalable device for automated microbial electroporeation in a digital microfluidic platform," ACS Synthetic Biology, vol. 6, pp. 1701-1709 (2017)
(114) Andrew Madison, Mathew Royal, and Richard Fair," Piezo-driven acoustic streaming in an electrowetting-on-dielectric digital microfluidics device," Microfluid Nanofluid, 21, 176 (2017).
(115) L. Chen, A.C. Madison and R.B. Fair, "Cell manipulation and detection enhancement enabled by a microelectromagnet integrated with a digital microfluidic device,"Biosensors and Bioelectronics Open Access, 2018, issue 04,

REFEREED CONFERENCE PROCEEDINGS

(1) A. B. El-Kareh, R. B. Fair and C. R. Marsh, "A Machine-Scan Electron Beam Device," Proc. 8th Electron and Laser Beam Symp., p. 331 (1966).
(2) R. B. Fair,"Quantitative Theory of Retarded Base Diffusion in Silicon NPN Structures with Arsenic Emitters," 1972 IEDM Tech. Dig., p. 96 (1972).
(3) R. B. Fair, "Recent Advances in Implantation and Device Modeling for the Design and Process Control of Bipolar ICs, in Semiconductor Silicon 1977, Eds. H. R. Huff and E. Sirtl, pp. 968-987, (The Electrochemical Soc.) 1977.
(4) R. B. Fair, "Modeling Laser-Induced Diffusion of Implanted Arsenic in Silicon," "Proc. of Laser and Electron Beam Processing of Electronic Materials," (Ed. by C. L. Anderson, G. K. Celler, G. A. Rozgonyi, The Electrochem. Soc., Princeton) p. 204.
(5) R. B. Fair and R. C. Sun, "Threshold Voltage Instability in MOSFET's Due to Channel Hot Hole Emission," in Tech. Digest of the Inter. Electron Device Meeting, p. 746 (1980).
(6) R. B. Fair, "Modeling Anomalous Phenomena in Arsenic Diffusion in Silicon," in Semiconductor Silicon/1981. Eds. H. R. Huff, R. J. Krogler and Y. Takeishi. (The Electronic Society, Inc., Pennington, N.J., 1981) p.963.
(7) R. B. Fair and W. G. Meyer, "Anomalous Junctions Formed by Cross-contamination of Phosphorus During Arsenic Implantation in Silicon," in Silicon Processing, ASTM STP804, D.C. Gupta, Ed., American Society for Test and Mater., 1983, pp. 290-305.
(8) R. B. Fair, "Impurity Concentration Doping Effects on Impurity Diffusion in Silicon," Semiconductor Processing and Equipment Sym. Tech. Proc., p. 230 (1983).
(9) R. B. Fair, "Modeling of Dopant Diffusion and Associated Effects in Silicon" in Defects in Semiconductors II, Mat. Res. Soc. Symp. Proc. Vol. 14 (Elsevier, Amsterdam), pp.\ 61-74 (1983).
(10) R. B. Fair, "MCNC - A New Multi-Institutional Thrust in ManufacturingTechnology," Proceedings UGIM-83, IEEE, p. 10, 1983.
(11) R. B. Fair, J. J. Wortman, J. Liu, "Modeling Rapid Thermal Annealing Processes for Shallow Junction Formation in Silicon," 1983 IEDM Tech. Dig., pp. 658-661 (1983).
(12) B. Rogers, R. B. Fair, W. Dyson and G. A. Rozgonyi, "Computer Simulation of Oxygen Precipitation and Denuded Zone Formation," in VLSI Science and Technology 1984, Proceedings of the 2nd International Symposium on VLSI Science and Technology, Vol. 84-7 (The Electrochemical Society, Pennington, NJ) pp. 74- 84 (1984).
(13) R. B. Fair, "Observations of Vacancies and Self-Interstitials in Diffusion Experiments in Silicon," in Thirteenth Inter. Conf. on Defects in Semiconductors, Vol. 14a (Metallurgical Soc., Warrendale, PA.) ed. L. C. Kimberling and J. M. Parsey, pp. 173-185 (1984).
(14) R.B. Fair and R. Subrahmanyan, "PREDICT-A New Design Tool for Shallow Junction Processes," Proc., Adv. Applications of Ion Implantation, Vol. 530 (The Inter. Society for Optical Engineering, Bellingham, WA) ed. M.I. Current and D. K. Sadana, pp. 88-96 (1985).
(15) R. B. Fair and J. E. Rose, "A deep Decision Tree Approach to Modeling Submicron Silicon Technologies," in ICCAD Dig. of Tech. Papers, (Computer Society Press, Los Angeles, CA), pp. 248-251 (1987).
(16) R. B. Fair, "Process Models for Ultra-Shallow Junction Technologies," IEDM Tech. Digest, pp. 260-263 (1987).
(17) R.B. Fair, "The Role of Transient Damage Annealing in Shallow Junction Formation," Proc. Shanghai Workshop on Ion Implantation, Ed. Z. Shichang (Academia Seneca, Shanghai), 1989 pp.12-22.

(18) R.B. Fair, "Oxidation-induced Defects and Effects in Silicon During Low-Thermal-Budget Processing" in The Physics and Chemistry of SiO2 and the Si-SiO2 Interface, eds. C.R. Helms and B.E. Deal (Plenum, New York), 1989, pp.459-468.
(19) G.A. Ruggles, S.N. Hong, J.J. Wortman, M. Ozturk, E.R. Meyers, J.J. Hren and R.B. Fair, "A Comparison of Low Energy BF2 Implantation in Si and Ge Preamorphized Silicon," in Mat. Res. Symp. Proc.,vol. 128 (Mat. Res. Soc., Pittsburgh, 1989), p. 611.
(20) R. Subrahmanyan, H.Z. Massoud and R.B. Fair, "Accurate Junction-Depth Measurements Using Chemical Staining," in Semiconductor Fabrication: Technology and Metrology ASTM STP 990, D.C. Gupta, ed. (Am. Soc. for Testing and Materials, 1989), p. 126.
(21) R.B. Fair, "The Role of Transient Damage Annealing in Shallow Junction Formation," Proc. First Inter Symp. on Adv. Materials for ULSI, vol 88-19, M. Scott, Y. Akasaka and R. Reif, eds. (The Electrochem. Soc., Pennington, N.J., 1988) pp. 123-135.
(22) R.B. Fair and R. Subrahmanyan, "Phenomenological Versus Point-Defect-Based Process Modeling-Where Should You Put Your Money?, in Proc. 2nd Inter. Symp. on ULSI Science andTech., vol. 89-9, C.M. Osburn and J.M. Andrews, eds. (The Electrochem. Soc. Pennington, N.J., 1989) pp, 133-143.
(23) R.B. Fair, "Shallow Junctions-Modeling the Dominance of Point Defect Charge States During Transient Diffusion," IEDM Tech. Digest, pp. 691-693 (1989).
(24) R.R. Ward, H.Z. Massoud and R.B. Fair, "The Thermal Oxidation of Heavily Doped Silicon in the Thin-Film Regime: Dopant Behavior and Modeling Growth Kinetics," in Semiconductor Silicon 1990, Proceedings of the Sixth Inter. Symp. on Si Mater. Sci. and Tech., Eds. H.R. Huff, K.G. Barraclough and J. Chikawa, Vol. 90-7 (The Electrochem. Soc., Pennington) pp. 405-416, 1990.
(25) R.B. Fair, "Process Model for Simulating the Effect of Amorphizing Implants on Phosphorus Diffusion," ibid, pp. 429-436, 1990.
(26) Y. Kim, H.Z. Massoud, S. Chevacharoeukul and R.B. Fair, "The Role of End-of-Range Dislocation Loops as a Diffusion Barrier," ibid, pp. 437-446, 1990.
(27) Y. Kim, H.Z. Massoud, U.M. Gosele, and R. B. Fair, "Physical Modeling of the Time Constant of Transient Enhancement in the Diffusion of Ion-Implanted Dopants in Silicon," in Process Physics and Modeling in Semiconductor Technology, Proceedings of the 2nd International Sym., Eds. G.R. Srinivasan, J.D. Plummer and S.T. Pantelides, vol. 91-4 (The Electrochem Soc. Inc., Pennington) pp. 254-272 (1991).
(28) Y. Kim, Y.T. Tan, H.Z. Massoud and R.B. Fair, "Modeling the Enhanced Diffusion of Implanted Boron in Silicon," ibid pp. 304-320 (1991).
(29) R.B. Fair, "Challenges and Priorities for Two Dimensional Process Simulation," ibid, pp. 689-702 (1991).
(30) R.B. Fair and I. Turlik, "Proof-of-Concept Collaboration Model for Advanced Packaging Research at MCNC", 1993 Proceedings, International Conference on Multichip Modules, p.552 (1993).
(31) R.B. Fair, "Junction Formation in Silicon by RTA," in 1st International Rapid Thermal Processing Conference - RTP'93", Ed. R.B. Fair and B. Lojek, RTP'93, Phoenix , p. 174 (1993).
(32) M.R. Neuman, R.B. Fair, M. Mehregany and H.Z. Massoud,
Micro-electromechanical Systems: A New Technology for Biomedical Applications," in Proc. of the 15th Annual Intern. Conf. of the IEEE Engineering in Medicine and Biology Society, A.Y.J. Szeto and R.M. Rangayyan, eds. IEEE Cat. No. 93CH3339-9, Piscataway, N.J., 15, 1545 (1993).

(33) R. B. Fair, "Prospects for Ion Implantation in Scaled Devices," in Proceedings of Inter. Conf. on Adv. Microelectronic Devices and Processing, Eds. S. Ono, T. Ohmi and Y. Sawada, Sendai, p.689 (1994).
(34) R.B. Fair. "Physically Based Modeling of Boron Diffusion in Thin Gate Oxides: Effects of F, H2, N, Oxide Thickness and Injected Si Interstitials," IEDM Tech Digest, p.85, December, 1995.
(35) R.B. Fair. " Rapid Thermal Annealing Issues in Silicon Processing" in Transient Thermal Processing Techniques in Electronic Materials, Eds. N.M. Ravindra and R.K. Singh, (The Minerals, Metals and Materials Society, Warrendale, Pa.) p. 91 (1996).
(36) R.B. Fair and W. Richards, "Process Simulation of Dopant Atom Diffusion in SiO2," in Process Physics and Modeling in Semiconductor Technology, eds. G.R. Srinivasan, C.S. Murthy, and S.T. Dunham, vol 96-4 (The Electrochemical Society, Pennington, NJ) pp. 179-194 (1996).
(37) R.B. Fair, "Boron Diffusion in Ultrathin Silicon Dioxide Layers," in The Physics and Chemistry of SiO2 and the Si-SiO2 Interface -3, eds. H.Z. Massoud, E.H. Poindexter, and C.R. Helms, vol. 96-1, (The Electrochemical Society, Pennington, NJ) pp. 200-213 (1996).
(38) G. Chen, T. Borca-Tasciuc, and R. B. Fair. "Fundamental Limit of the Use of Pyrometry in Rapid Thermal Processing," in 4th International Conference on Advanced Thermal Procesing of Semiconductors, eds. R.B. Fair, M.L. Green, B. Lojek, and R.P.S Thakur, p. 157 (1996)
[39] R.B. Fair, "Trends in Rapid Thermal Processing for Large Diameter Silicon Processes," in Proceedings of 2nd International Symp. on Advanced Science and Technology of Silicon Materials, ed. M. Umeno, Japan Soc. for Promotion of Science, pp. 7-15 (1996).
[40] S. Bobbio, S. Goodwin-Johansson, T. DuBois, F. Tranjan, S. Smith, R. Fair, C. Ball, J. Jacobson, C. Bartlett, N. Eleyan, H. Makki, and R. Gupta, "Integrated force array: positioning drive applications", Proc SPIE Symp,
3046, 248-254 (1997).
[41] R.B. Fair and M. Shen, "Ultrashallow 2D Dopant Profile Simulation Versus Experimental Measurement in the Low Thermal Budget Regime," Proceedings of Fourth International Workshop on Measurement, Characterization and Modeling of Ultra-shallow Doping Profiles in Semiconductors, Research Triangle Park, NC, April, 1997 pp. 3.1 - 3.9
[42] R.B. Fair, "Boron Penetration of Thin Polysilicon Gates/Ultrathin Gate Dielectrics from B+ Implantation and Thermal Processing," in ULSI Science and Technology 1997, eds. H.Z. Massoud, H. Iwai, C. Claeys, and R.B. Fair (The Electrochemical Society, Pennington, NJ) vol. 97-3, 247-261 (1997).
[43] R.B. Fair, V. Pamula, and M. Pollack, "MEMS-based Explosive Particle Detection and Remote Particle Stimulation," Proceedings of SPIE - Detection and Remediation Technologies for Mines and Minelike Targets II, vol. 3079, 671 (1997).
[44] R.B. Fair, "Dopant Diffusion in Si and SiO2 during RTA," Extended Abstracts of International Conference on Solid State Devices and Materials, SSDM'97, Hamamatsu, Japan, Sept. 1997, p. 104.
(45) R.B. Fair, M. Pollack, and V. Pamula, "MEMS Devices for Detecting the Presence of Explosive Material Residues in Mine Fields," SPIE Aerosense Conf., Orlando, vol. 3392, 409, April, 1998.
(46) V.K. Pamula and R.B. Fair, "Detection of Nanogram Explosive Particles with a MEMS Sensor," Proceedings of SPIE, Detection and Remediation Technologies for Mines and Minelike Targets IV, vol. 3710, pp. 321-327 (1999).

(47) A. Dewey and R.B. Fair, "Microelectromechanical Systems (MEMS) Design and Design Automation Research at Duke University," International Conf. Modeling and Simulation of Microsystems, April 1998.
(47a) V.K. Pamula and R.B. Fair, " Detection of Dissolved TNT and DNT in Soil with a MEMS Explosive Particle Detector," *Proceedings of the SPIE - The International Society for Optical Engineering*, v 4038, pt.1-2, 2000, p 547-52
(48) T. Zhang, K. Chakrabarty, and R.B. Fair, "Design of Reconfigurable Composite Microsystems Based on Hardware/Software Co-design Principles," Tech. Proc. Of Fourth International Conf. Modeling and Simulation of Microsystems, p. 148, March, 2001.
(49) J. Jopling, D. Rose, and R.B. Fair, "The Coupled-Domain System Simulation/Simulatability Problem," Tech. Proc. Of Fourth International Conf. Modeling and Simulation of Microsystems, p. 116, March, 2001.
(50) J. Ding, K. Chakrabarty, and R.B. Fair, "Reconfigurable Microfluidic System Architecture Based on Two-Dimensional Electrowetting Arrays," Tech. Proc. Of Fourth International Conf. Modeling and Simulation of Microsystems, p. 181, March, 2001.
(51) R.B. Fair, "A Historical View of the Role of Ion-Implantation Defects in PN Junction Formation for Devices," in Si Front End Processing- Physics and Technology of Dopant-Defect Interactions, Materials Research Society, vol 610, pp. B4.1.1-12, (2001).
(52) R. B. Fair, M.G. Pollack, R. Woo, V.K. Pamula, H. Ren, T. Zhang, and J. Venkatraman, "A Microwatt Metal-Insulator-Solution-Transport (MIST) Device for Scalable Digital Bio-Microfluidic Systems," Technical Digest, Inter. Electron Device Meeting, pp. 367-370 (2001).
(53) H. Ren, V. Srinivasan, and R.B. Fair, "Design and Testing of an Interpolating Mixing Architecture for Electrowetting-Based Droplet On-Chip Chemical Dilution," Digest of Technical Papers Transducers, 2003, pp. 619-622 (2003).
(54) R.B. Fair, V. Srinivasan, P. Paik, H. Ren, V.K. Pamula, and M.G. Pollack, "Electrowetting-Based On-Chip Sample Processing for Integrated Microfluidics, IEDM 2003, Washington, DC, December 10, 2003.
(55) V. Srinivasan, V.K. Pamula, M.K. Pollack, and R.B. Fair, "Clinical diagnostics on human whole blood, plasma, serum, urine, saliva, sweat, and tears on a digital microfluidic platform. Proceedings of MicroTAS 2003 1287-1290 (2003)
(56) V. Srinivasan, V. Pamula, P. Paik, and R.B. Fair, "Protein Stamping for MALDI Mass Spectrometry Using an Electrowetting-Based Microfluidic Platform," in Lab-on-a-Chip: Platforms, Devices, and Applications, L.A. Smith and D. Sobek, eds., Proc. Of SPIE, vol. 5591, pp. 26-34, Dec. 8, 2004.
(57) R.B. Fair, A. Khlystov, V. Srinivasan, V.K. Pamula, K.N. Weaver, "Integrated Chemical/Biochemical Sample Collection, Pre-concentration, and Analysis on a Digital Microfluidic Lab-on-a-Chip Platform," in Lab-on-a-Chip: Platforms, Devices, and Applications, L.A. Smith and D. Sobek, eds., Proc. Of SPIE, vol. 5591, pp. 113-124, Dec. 8, 2004.
(58) V.K. Pamula, V. Srinvasan, H. Chakrapani, R.B. Fair, and E.J. Toon, "A Droplet-Based Lab-On-A-Chip for Coplorimetric Detection of Nitroaromatic Explosives," Proceedings of IEEE Inter. Conference on Micro Electro Mechanical Systems (MEMS 2005), pp. 722-725, (2005)
(59) R. Evans, L. Luan, N.M. Jokerst, and R.B. Fair, "Optical detection heterogeneously integrated with a coplanar digital microfluidic lab-on-a-chip platform," 6th IEEE Conf. Sensors, IEEE Sensors 2007, Atlanta, GA, Oct.28, 2007.
(60) C. Geisler, D.M. Wootton, P.I. Lelkes, R.B. Fair, and J.G. Zhou, "Material study of electrowetting-based multimicrofluidics array printing of high resolution tissue construct with

embedded cells and growth factors," ASME 2010 First Global Congress NanoEngineering for Medicine and Biology, Houston, TX, Feb. 7-10, 2010.
(61) R.B. Fair, "Parallel Processing of Multifunctional, Point-of-Care Bio-Applications on Electrowetting Chips, μTAS 2010, Oct. 3-7 (2010), pp. 2095-2097.
(62) M.W. Royal, R.B. Fair, and N.M. Jokerst, "Integrated sample preparation and sensing: Microresonator optical sensors embedded in digital electrowetting microfluidics systems," IEEE Sensors, p. 4 (2011)
(63) B. -N. Hsu, A. C. Madison and R. B. Fair "Accelerate Sepsis Diagnosis by Seamless Integration of DNA Purification and qPCR," Proceedings of the 16th International Conference on Miniaturized Systems for Chemistry and Life Sciences (MicroTAS 2012), Okinawa, Japan, October 28-November 1, 2012, pp. 830-832.
(64) M. Sandahl, S. Punnamaraju, A. Madison, J. Harrington, M. Royal, R. Fair, A. Eckhardt, A. Sudarsan, and M. Pollack, "Software automated genomic engineering (SAGE) enabled by electrowetting-on-dielectric digital microfluidics," 17th Inter. Conf. on Miniaturized Systems for Xhemistry and Life Sciences, MicroTAS 2013, v2, pp1260-126, 2013

BOOK CHAPTERS

(1) R. B. Fair, "Concentration Profiles of Diffused Dopants in Silicon," in Impurity Doping Processes in Silicon, Ed. by F. Y. Want in the series Material Processing: Theory and Practices, North Holland Press, Amsterdam (1981) pp. 317-442.
(2) R. B. Fair, "Physics and Chemistry of Impurity Diffusion and Oxidation of Silicon," in Processing Technologies, Ed. D. Khang in Applied Solid State Science, Academic Press, New York (1981), Supplement 2B, pp. 1-108.
(3) R. B. Fair, "Diffusion in Silicon," in Advances in Electronic Materials, Ed. by B. W. Wessels and G. Y. Chin, American Society for Metals, Metals Park, Ohio (1986) pp. 119-145.
(4) R.B. Fair, "Diffusion and Ion Implantation in Silicon," in Semiconductor Materials and Process Technology Handbook, Ed. G.E. McGuire, Noyes Publication (1988), pp. 455-538.
(5) R.B. Fair, "Diffusion and Oxidation of Silicon," Eds. K.F. Jensen and D. Hess, American Chemical" Society-Advances in Chemistry Series No. 221, Wash, D.C. (1989).
(6) R.B. Fair, "Diffusion in Silicon," Ed. L.C. Kimerling, Concise Encyclopedia of Electronic and.Optoelectronic Materials, (Pergamon Press, Oxford) Suppl. Vol. 2, pp. 901-904, 1990.
[7] R.B. Fair, "Junction Formation in Silicon by Rapid Thermal Annealing", in Rapid Thermal Processing: Science and Technology, Ed. R.B. Fair, (Academic Press, Boston), pp. 169-226, 1993.
[8] R.B. Fair, "Rapid Thermal Processing - A Justification", in Rapid Thermal Processing: Science and Technology, Ed. R.B. Fair, (Academic Press, Boston), pp. 1-11, 1993.
(9) R.B. Fair, "Conventional and Rapid Thermal Processing," in ULSI Technology, Ed. C.Y. Chang and S.M. Sze (McGraw Hill, New York), pp. 144-204, 1996.
(10) R.B. Fair, "Doping," Ed. J.D. Atwood, Inorganic Reactions and Methods, Sections 17.2.6-17.2.6.5, John Wiley & Sons, New York (1999)
(11) T. Zhang, K. Chakrabarty, R.B. Fair, "A Hierarchical Design Platform for Microelectrofluidic Systems," Vol. 1, MEMS/NEMS Handbook, Ed. L. Cornelius (Springer), 2006.

(12) R.B. Fair, “Scaling Fundamentals and Applications of Digital Microfluidic Microsystems,” in Microfluidics Based Microsystems, Ed. S. Kakac, B. Kosoy, D. Li, and A. Pramuanjaroenkij (Springer), pp. 285-304 (2010).

BOOKS EDITED/WRITTEN

[1] "Impurity Diffusion and Gettering in Silicon," Materials Research Society Symposia Proceedings, Vol. 36, Eds. Richard B. Fair, Charles W. Pearce and Jack Washburn, Materials Research society, Pittsburgh, PA., (1985).
[2] "Rapid Thermal Processing: Science and Technology", Ed. R.B. Fair, Academic Press, Boston, (1993).
(3) "1st International Rapid Thermal Processing Conference - RTP'93", Ed. R.B. Fair and B. Lojek, RTP'93, Phoenix (1993)
(4) "2nd International Rapid Thermal Processing Conference - RTP'94", Ed. R.B. Fair and B. Lojek, RTP'94, Monterey (1994)
(5) "3rd International Rapid Thermal Processing Conference - RTP'95", Ed. R.B. Fair and B. Lojek, RTP'95, Amsterdam (1995)
(6) "4th International Conference on Advanced Thermal Procesing of Semiconductors - RTP'96", Ed. R.B. Fair, M.L. Green, B. Lojek, and R.P.S. Thakur, RTP'96, Boise (1996)
(7) "ULSI Science and Technology 1997", Eds. H.Z. Massoud, H. Iwai, C. Claeys, and R.B. Fair (The Electrochemical Society, Pennington, NJ) vol. 97-3, Montreal (1997)
(8) "5th International Conference on Advanced Thermal Processing of Semiconductors - RTP'97", Ed. R.B. Fair, M.L. Green, B. Lojek, and R.P.S. Thakur, RTP'97, New Orleans (1997)
(9) “Microelectrofluidic Systems – Modeling and Simulation,” CRC Press, Boca Raton, (2002).

INVITED LECTURES/TALKS

(1) "Transistor Design Considerations in Low-Noise Pre-Amplifiers," IEEE Nuclear Science Symposium, San Francisco (1975).
(2) "Recent Advances in Implantation and Device Modeling for the Design and Process Control of Bipolar IC's," Electrochemical Society Meeting, Philadelphia (1977).
(3) "Some New Insights into Process Modeling," Nat. Bureau of Standards, Washington, DC (1978).
(4) "Recent Developments in Process Modeling," Stanford University Seminar, Stanford (1979).
(5) "Thermal and Laser-Induced Diffusion of Dopants in Silicon," Sandia Laboratories Seminar, Albuquerque (1979).
(6) "The Multiple-Charge State Vacancy Model for Impurity Diffusion in Silicon," Gordon Research Conf., Meriden, NH (1979).
(7) "Impurity Diffusion in Silicon - The Long and the Short of It," ECS Society Lecture, North Texas Section, Dallas (1979).
(8) "Point Defects and Diffusion in Silicon - The Current Controversies," Stanford University Seminar (1979).
(9) "The Multiple-Charge-State Vacancy Model of Diffusion," Electrochemical Society Meeting, St. Louis (1980).
(10) "Molecular Transport and Diffusion in Solids:, NATO Advanced Study Institute on Chemical Sensors," Hightstown, NJ (1980).

(11) "A Consistent Model of Oxidation, Impurity Diffusion and Defect Growth in Silicon," Electronic Materials Conf., Cornell (1980).
(12) "Diffusion in Silicon," Seminar at Texas Instruments, Inc., Dallas (1980).
(13) "LSI Research Areas - Peeling the IC Technology Onion," Duke University, Durham, NC (1980).
(14) "The Role of H2 in SiO2 on Integrated Circuit Reliability," Penn State University, State College, PA (1980).
(15) "LSI Research Areas," Howard University, Washington, DC (Nov. 1980).
(16) "LSI Research Areas - Peeling the IC Technology Onion," Western Electric, Merimack Valley, April 1981.
(17) "Limitations and Benefits of Standard High Temperature processing in Producing Device Quality Silicon Surface Layers," Lasers in Microelectronics Workshop, MIT, Boston, May 1981.
(18) "Modeling Anomalous Phenomena in Arsenic Diffusion in Silicon," Electrochemical Society Meeting, Minneapolis, MN, May 1981.
(19) "The Role of the Microelectronics Center of North Carolina in University Research," Sigma Xi Lecture, North Carolina A&T State University, Greensboro, NC, Nov. 1981.
(20) "Anomalous Junctions Formed by Cross-Contamination of Phosphorus During Arsenic Implantation in Silicon," Symposium on Silicon Processing, San Jose, CA., Jan. 1982.
(21) "Materials Research Areas in Silicon Technology," North Carolina State University, Raleigh, NC, 1981.
(22) "The Impact of Defects and Diffusion on Integrated Circuit Technology," North Carolina State University, Raleigh, NC, 1982.
(23) "Impurity Diffusion in Silicon-Key to the VLSI Process Balancing Act," SIA Lecture at Stanford University, Stanford, CA, 1982.
(24) "Developments in Microelectronics: Science and Industry," East Carolina University, Greenville, NC, 1982.
(25) "Modeling of Dopant Diffusion and Associated Effects in Si," Materials Research Society, Boston, 1982.
(26) "Research Interests and Goals of the Microelectronics Center of North Carolina," University of North Carolina, Chapel Hill, 1982.
(27) "The Microelectronics Center - A New Force in Cooperative VLSI Signal Processing Research," University of Southern California, Los Angeles, 1982.
(28) "Point Defects in Silicon," Katholieke University, Leuven Belgium,1983.
(29) "Impurity Concentration Doping Effects on Impurity Diffusion in Silicon," Semicon/Europa '83, Zurich, Switzerland, 1983.
(30) "The Future of Microelectronics in North Carolina," ORT Seminar, Raleigh, 1983.
(31) "An Overview of Technology Requirements for VLSI," Computer Science Seminar, NASA Langley Research Center, Hampton, Va., 1983.
(32) "MCNC - A New Multi-Institutional Thrust in Manufacturing Technology Research," 5th University/Government/Industry Microelectronics Symposium, College Station, Texas, 1983.
(33) "The Evolution of Digital Integrated Circuit Technologies," Keynote speech at Digital Integrated Circuits Workshop, John Wiley & Sons, Durham, N.C. 1983.
(34) "Scaling of Junctions for CMOS," Symposium on Computer-Aided Design and Manufacturing of Integrated Circuits, Stanford University, 1983.
(35) "Limitations in Scaling Junctions for CMOS,"Burroughs Corp., San Diego, 1983.

(36) "The Role of the Microelectronics Center of North Carolina in Industrial Development of North Carolina," keynote talk, Quality in Electronics Conference, Raleigh, N. C., 1983.
(37) "The Role of Vacancies and Self-Interstitials in Impurity-Diffusion in Silicon," Indo./U.S.Workshop on Diffusion in Solids, Bombay, India, 1984.
(38) "The Formation of Fixed Charge and Interface States During Hot Carrier Injection in MOSFET's," DEC, Hudson, Massachusetts, 1984.
(39) "Cooperative Research at MCNC," Third Symposium on Semiconductor Processing, San Jose, California, 1984.
(40) "The Role of Point Defects in Processing Phenomena in Silicon," Monsanto Corporation, St. Louis, 1984.
(41) "Modeling Rapid Thermal Diffusion of Dopants in Silicon," Semiconductor Seminar, Research Triangle Park, 1984.
(42) "Modeling Rapid Thermal Diffusion of Dopants in Silicon," Microelectronics Seminar Series, UNCC, Charlotte, N.C., 1984.
(43) "Observations of Vacancies and Self-Interstitials in Diffusion Experiments in Silicon," International Conference on Defects in Semiconductors, San Diego, CA, 1984.
(44) "Silicon Diffusion," Materials Science Seminar for American Society of Metals, Detroit, 1985.
(45) "Microelectronics in North Carolina," Luncheon speaker to ASTM Committee F-1, Raleigh, 1984.
(46) "Impurity Diffusion During RTA," Materials Research Society Meeting, Boston, 1984.
(47) "PREDICT__A New Design Tool for Shallow Junction Processes," SPIE Meeting on Advanced Applications of Ion Implantation, Los Angeles, 1985.
(48) "The Self-Interstitial Versus Vacancy Debate in Silicon-Coincidences, Convictions and Controversies," Gordon Research Conference on Point Defects, Line Defects and Interfaces in Semiconductors, Plymouth, NH, 1985.
(49) "On the Role of Rapid-Thermal Processing Scaled CMOS," Canadian VLSI Conference, Toronto, 1985.
(50) "Process Modeling" - IEDM Short Course, Washington, D.C., 1985.
(51) "Shallow Junction Technology for Sealed CMOS," SRC Topical Research Conference, Cornell University, Ithaca, 1985.
(52) "New Results on Point Defects in Silicon," Seminar at Katholieke University, Leuven Belgium, 1985.
(53) "Diffusion and Ion Implantation," Annual Davos Seminars on Semiconductor Materials and Devices, Davos Switzerland, 1985.
(54) "Diffusion Simulation," MCC Workshop on Process and Device Simulation, Austin, Texas, 1986.
(55) "Diffusion and Ion Implantation," Annual Davos Seminars on Semiconductor Materials and Devices, Davos Switzerland, 1986.
(56) "Modeling Low Thermal Budget Silicon Processing - The Long and the Short of it," RPI, Troy, NY, 1986.
(57) "Diffusion and Ion Implantation," Annual Davos Seminars on Semiconductor Materials and Devices, Davos Switzerland, 1987- 1992.
(58) "The Future of Ion Implantation," R. B. Fair, Greater Silicon Valley Implant User's Group, San Jose (1987).
(59) "Pitfalls of Low-Thermal Budget Processing," Sematech Workshop, Denver

(1987).
(60) "Pitfalls of Low-Thermal Budget Processing," Hewlett-Packard, Fort Collins (1987).
(61) "Process Models for Ultra-Shallow Junction Technologies," Digital Equip. Corp. Seminar, Hudson, MA (1988).
(62) "Challenges for Submicron Silicon Processing," Fifth International Sym. on Semiconductor Processing, Santa Clara, CA (1988).
(63) "Rapid Thermal Processing Issues in the Manufacturing of Semiconductor Devices," S.P.I.E. Conf. on Advanced Processing of Semiconductor Devices II, Newport Beach, CA (1988).
(64) "Oxidation-Induced defects in Low-Thermal Budget Silicon Processing," Electrochemical Society Meeting, Atlanta, Georgia, May 1988.
(65) "The Role of Transient Damage Annealing Shallow-Junction Formation," Electrochemical Society Meeting, Atlanta, Georgia, May 1988.
(66) "Rapid Thermal Annealing of Low Energy Implants in Silicon," Shanghai Workshop on Characterization of Ion Implantation in Silicon, Hangzhou,
China, June 1988.
(67) "The Impact of Computing Technology on Design," The Technology Exchange Institute for Engineering Deans", Stanford Univ., Oct. 1988.
(68) "VLSI Research Program at MCNC," 1989 VLSI Group Research Review, Univ.of Waterloo, May 1989.
(69) "Phenomenological vs. Point-Defect-Based Modeling-Where Should You Put Your Money?" Electrochem. Soc. Meeting, Los Angeles, May 1989.
(70) "Challenges and Priorities for Two-Dimensional Process Simulation,"Electrochem. Soc. Mtg., Montreal, May 1990.
(71) "Transient Diffusion in Silicon: Models and Cures," Electronics Materials Conf., Santa Barbara, CA, June 1990.
(72) "Thermal Budget Issues for Submicron ULSI," Oregon Graduate Institute for Science and Technology, Beaverton, Nov. 1990.
(73) "Damage Removal-Diffusion Tradeoffs in Ultra-Shallow Implanted p+ Junctions," Motorola Process Modeling Workshop, Mesa, Nov. 1990.
(74) "A Unified View of Modeling Transient Dopant Diffusion in Silicon," Inter. Workshop on VLSI Process and Device Modeling, Oiso, Japan, May 1991.
(75) "Defects Induced in Silicon During Ion Implantation and Rapid Thermal Annealing," Electrochem Soc. Meeting, Washington, DC, May 1991.
(76) "Computer-Aided Process Modeling and Simulation," Silicon Processing for the VLSI Era, RTP, May 17, 1991.
(77) "Process Simulation for ULSI - Tools, Models and Issues," ASIC Technology Seminar, Kawasaki Japan, September 1991.
(78) "Process Simulation for ULSI," Teksel Seminar, Osaka, Japan, September 1991.
(79) "Process Simulation for ULSI," Intellect, Inc. Seminar, Seoul, Korea, September 1991.
(80) "Process Simulation for ULSI," Exartech Inter. Seminar, Hsinchu, Taiwan, October 1991.
[81] "Challenges in Manufacturing ULSI Devices", SPE Regional Tech. Conf., Research Triangle Park, Nov. 1991.
[82] "Defects in Silicon Induced by Ion Implantation" Symp. on Adv. Science and Tech. of Si Materials, Japan Soc. for Promotion of Science, Kona, Hawaii, Nov. 1991.

[83] "The Role of Consortia in the Development of Materials and Processing Alternatives for Advanced Microelectronics", ISHM Workshop, Ojai, CA, Feb. 1992.
[84] "Defects, Diffusion and Debacles in Shallow pn Junction Formation", AT&T Bell Labs, Murray Hill, N.J., March 1992.
[85] "The Semiconductor Manufacturing Crisis - Opportunity for Global Cooperation?", Keynote speech, ISSMT'92 Conf., Tokyo, May 1992.
[86] "Rapid Thermal Processing - Science and Technology", all seminars, May 1992, Kawasaki, Japan, Science Park, Hsingchu, Taiwan, Yonsei Univ., Seoul, Korea.
[87] "Consortia - Help or Hindrance?", ISHM '92 Meeting, San Francisco, CA, October, 1992
[88] "Junction Formation in Silicon by Rapid Thermal Annealing", Materials Research Socoety, San Francisco, CA, April, 1993
[89] "Proof-of-Concept Collaboration Model for Advanced Packaging Research at MCNC", 2nd Inter. Conf. on Multichip Modules, Denver, April, 1993
(90) "Rapid Thermal Processing," Seminar at SEMI, Mountain View Ca., July, 1993.
(91) "Junction Formation in Silicon by RTA", 1st International Rapid Thermal Processing Conference, RTP'93, Phoenix, Az, Sept. 1993.
(92) "Prospects for Ion Implantation in Scaled Devices," Conference on Advanced Microelectronic Devices and Processing, Sendai, Japan, March, 1994.
(93) "Advances in Microchip Technology - Hitting the Wall in the Microchip Marathon," 8th Annual High Performance Computing and Communications Conference, FGIPC, Research Triangle Park< NC, June, 1994.
(94) " Rapid Thermal Processing - Hot Solution for a Critical Processing Need?" Distinguished Lecture, Micron Technology, Inc., Boise ID, June 1995.
(95) " Rapid Thermal Annealing Issues in Silicon Processing," 125th TMS Annual Meeting, Anaheim, CA, Feb. 1996.
(96) "Modeling the Diffusion Barrier Role of Nitgrogen in Ultrathin Gate Oxides," SRC Topical Research Conference on Ultrathin Gate Dielectrics Technology, Reliability, and Characterization, Raliegh, NC, March, 1996.
(97) "Boron Diffusion in Ultrathin Silicon Dioxide Layers," in The Physics and Chemistry of SiO2 and the Si-SiO2 Interface -3 Symposium, Spring meeting of the Electrochemical Society, Los Angeles (1996).
(98) " Ion Implantation and Annealing Technologies," Cambridge University, England June 1996.
(99) " PREDICTive Process Simulation for the Non-Stanford Graduate Engineer," Computer-Aided Design of IC Processes and Devices Workshop, Stanford University, August, 1996.
[100] "Trend of Rapid Thermal Processing in Large Diameter Silicon Processes," Plenary talk, 2nd International Symposium on Advanced Science and Technology of Silicon Materials, November 25-29, Kona, Hawaii (1996).
[101] "Ultrashallow 2D Dopant Profile Simulation Versus Experimental Measurement in the Low Thermal Budget Regime," Fourth International Workshop on Measurement, Characterization and Modeling of Ultra-shallow Doping Profiles in Semiconductors, Research Triangle Park, NC, April, 1997.
[102] "MEMS Trace Particle, Vapor and Ultrasound Sensor," Aerosense Conference 3079, SPIE, Orlando, FL, April 24, 1997
[103] "MEMS Trace Particle, Vapor and Ultrasound Sensor," Oak Ridge National Labs, May 12, 1997

[104] "Dopant Difusion in Si and SiO2 During Rapid Thermal Annealing," Solid State Devices and Materials - SSDM'97, Hamamatsu, Japan, Sept., 1997.
[105] "Activation of Ion Implanted Dopants in Silicon with Optical Radiation," Gordon Research Conf. on Materials Processes Far from Equilibrium, Meredian, NH., Aug. 1997.
[106] "Dopant Diffusion in Si and SiO2 during RTA," International Conference on Solid State Devices and Materials, SSDM'97, Hamamatsu, Japan, Sept. 1997.
[107] "Sniffing Out Landmines: Mimicing Man's Best Friend," IEEE New Technology Directions Committee Workshop, Atlanta, Georgia, Nov. 1997.
[108] " Advances in Silicon Technology- Hitting the Wall in the Microchip Marathon," keynote talk at 2nd Southeastern Workshop on Mixed-Signal VLSI and Monolithic Sensors," Knoxville, April, 1998.
[109] A. Dewey and R.B. Fair, "Microelectromechanical Systems (MEMS) Design and Design Automation Research at Duke University," Int. Conf. on Modeling and Simulation of Microsystems, Semiconductors, Sensors, and Actuators, MSM98, April, 1998.
[110] R.B. Fair, "PN Junction Profile Engineering," Short course at USJ'99, Research Triangle Park, March, 1999.
[111] R.B. Fair, "A Historical View of the Role of Ion-Implantation Defects in PN Junction Formation for Devices," Materials Research Society, San Francisco, April, 2000.
[112] R.B. Fair, "The Invention of the Self-Aligned Gate MOSFET," N.C. Section of the Materials Research Society, Research Triangle Park, Nov. 10, 2000.
[113] R.B. Fair, "Research in Biochips and BioFLIPS," Workshop on Biomedical Imaging and Bioengineering Opportunities, N.C. State University, May 10, 2001.
[114] R.B. Fair, “Advances in Droplet-Based Bio Lab-on-a-Chip,” BioChips 2003, Boston, June, 2003.
[115] R.B. Fair, A. Khlystov, V. Srinivasan, V. K. Pamula, K.N. Weaver, “Integrated chemical/biochemical sample collection, pre-concentration, and analysis on a digital microfluidic lab-on-a-chip platform,” Lab-on-a-Chip: Platforms, Devices, and Applications, Conf. 5591, SPIE Optics East, Philadelphia, Oct. 25-28, 2004.
[116] R.B. Fair, “Dynamically Reconfigurable Surfaces for Microfluidic Applications,” MRS Spring Meeting, San Francisco, CA., Symp. Q, March 29, 2005.
[117] R.B. Fair, V. Srinivasan, N. Weaver, “Bead-Based and Solution-Based Assays Performed on a Digital Microfluidic Platform,” BMES 2005, Baltimore, MD, Oct. 1, 2005.
[118] R.B. Fair, “Chemical and Biological Applications of Digital Microfluidic Devices,” 5th Inter. Meeting on Electrowetting,” Rochester, NY, June 1, 2006.
[119] R.B. Fair, “Chemical and Biological Pathogen Detection in a Digital Microfluidic Platform,” DARPA/MTO Workshop Microfluidic Analyzers, Keystone, CO, Oct. 4-5, 2006.
[120] R.B. Fair, “Integrated Digital Microfluidic Functions for Chemical and Biological Applications”, Materials Research Society Meeting, San Francisco, CA April 13, 2007.
[121] R.B. Fair, “Integrated Digital Microfluidic Chips for Chemical and Biological Applications,” Drexel University, Philadelphia, PA May 16, 2007.
[122] R.B. Fair, “Digital Microfluidic Biochips,” Materials Research Society, Boston, Nov. 27, 2007.
[123] R.B. Fair, "Reconfigurable digital microfluidic chips for multiple chemical applications", American Chemical Society, Philadelphia, Aug. 20, 2008
[124] R.B. Fair, J.H. Song, R.D. Evans, Y-T Lin, B-N Hsu, “Scaling EWD Actuators for Picoliter Applications,” 6th Inter. Meeting on Electrowetting, Los Angeles, Aug. 21, 2008.

[125] R.B. Fair, "Progress in Reconfigurable Microfluidic Systems for Evolvable Biochips," 8th International Conf. Evolvable Systems, Prague, Sept. 21, 2008. (Keynote)
[126] R.B. Fair, "Is a True Lab-on-a-Chip Possible?", Bioengineering Applications to Address Global Health, Duke Univ., Durham, NC, Nov. 6, 2008.
[127] R.B. Fair, "The $1000 Genome: Sequencing DNA One Drop at a Time." Microfluidics Symposium, Harvard Medical School, January 15, 2009.
[128] R.B. Fair, "Fundamentals of Droplet Flow in Microfluidics," NATO Advanced Study Institute on *Microsystems for Security – Fundamentals and Applications* – August 23 – September 4, 2009, Golden Dolphin Hotel, Cesme-Izmir, Turkey
[129] R.B. Fair, "Implementation of Fluidic Functions in Digital Microfluidics," NATO Advanced Study Institute on *Microsystems for Security – Fundamentals and Applications* – August 23 – September 4, 2009, Golden Dolphin Hotel, Cesme-Izmir, Turkey
[130] R.B. Fair, "Digital Microfluidics for Chemical and Biological Applications," 31st Annual International IEEE EMBS Conference, Minneapolis, Minnesota, USA, September, 2-6, 2009.
[131] R.B. Fair, "Electrowetting Control of Droplets for On-chip Biomedical Applications," APS Mtg., Portland, OR, March 2010.
[132] R.B. Fair, "Parallel Processing of Multifunctional, Point-of-Care Bio-Applications on Electrowetting Chips, µTAS 2010, Oct. 3-7 (2010), Groningen, The Netherlands.
[133] N. M. Jokerst, M. Royal, S. Dhar, M. Brooke, R. Fair, T. Tyler, D. Arora, "Intergated Optical Sensing Ssystems: Sensors, Photonics, and Fluidics," Europtrode XI, Barcelona, April, 2012.
[134] R.B. Fair, "Portable Digital Microfluidic LoCs with Integrated Analog Processing, Adaptive Control, and Sensing," IARPA Workshop, Bedford, MA, Oct. 10, 2012.
[135] R.B. Fair, "Extraction and Detection of Sparse Pathogens from Biological Fluids at the Microfluidics Scale," Microfluidics Congress: USA, Philadelphia, July 11-12. Keynote Talk. 2016.
[136] R.B. Fair and L. Chen, "Enhanced cell manipulation and detectiojn vis magnetic beads on a digital microfluidic device," TechConnect Conference, May14-17, 2017. National Harbor, Md.

OTHER TALKS AND LECTURES

(1) "A Machine-Scan Electron Beam Device," 8th Annual Electron and Laser Beam Symposium," University of Michigan, Ann Arbor (1966).
(2) "High Concentration Arsenic Diffusion in Silicon from Doped Oxide Sources," Electrochemical Society Meeting, Houston (1972).
(3) "Quantitative Theory of Retarded Base Diffusion in Silicon NPN Structures with Arsenic Emitters," Inter. Electron Device Meeting of IEEE, Washington, DC (1972).
(4) "Diffusion of Ion-Implanted Boron in High Concentration P, As and Sb-doped Silicon," Electrochemical Society Meeting, Toronto (1975).
(5) "The Diffusion of Ion-Implanted Arsenic in Silicon," Electrochemical Society Meeting, Dallas (1975).
(6) "Zener and Avalanche Breakdown in As-Implanted Low Voltage Si N-P Junctions," Inter. Electron Device Meeting of IEEE, Washington, DC (1975).
(7) "Quantitative Model of Phosphorus Diffusion in Silicon," Electrochemical Society Meeting, Las Vegas (1976).

(8) "Quantitative Model of the Emitter-Dip Effect," Electrochemical Society Meeting, Las Vegas (1976).
(9) "Analysis of Phosphorus Profiles," Electrochemical Society Meeting, Atlanta (1977).
(10) "The Effect of Strain-Induced Bandgap Narrowing on Phosphorus Diffusion and E-Center Concentrations in Silicon," Inter. Conf. on Defectsand Radiation Effects in Semicond., Nice (1978).
(11) "Theory and Direct Measurement of Boron Segregation in SiO2 During Dry, Near Dry and Wet O2 Oxidation," Electrochemical Society Meeting, Pittsburgh (1978).
(12) "Modeling Laser - Induced Diffusion of Implanted Arsenic in Silicon," Electrochemical Society Meeting, Los Angeles (1979).
(13) "Influence of Strain on Impurity Diffusion in Silicon," Electrochemical Society Meeting, St. Louis (1980).
(14) "Threshold Voltage Instability in MOSFET's Due to Channel Hot Hole Emission," Inter. Electron Device Meeting, Washington, DC (1980).
(15) "The Effects of Impurity Diffusion and Surface Damage on Oxygen Precipitation in Silicon," Electrochemical Society Meeting, Montreal
(1982).
(16) "Dynamic Behavior of the Build-Up of Fixed Charge and Interface States During Hot Carrier Injection in Encapsulated MOSFET's," Electrochemical Society Meeting, Montreal (1982).
(17) "Modeling Physical Limitations on Junction Scaling for CMOS," Device
Research Conference, Burlington, VT (1983).
(18) "Modeling Rapid Thermal Annealing Processes for Shallow Junction Formation in Silicon," International Electron Device Meeting, Washington, DC (1983).
(19) "Computer Simulation of Oxygen Precipitation and Denuded Zone Formation," Electrochemical Society Meeting, Cincinnati, OH (1984).
(20) "Stress Assisted Diffusion of Boron and Arsenic in Silicon," Materials Research Society Meeting, Boston, November 1984.
(21) "Curve Fitting Models for Boron, Phosphorus and Arsenic Ion Implantations in Crystalline Silicon," Electrochemical Society Meeting, Toronto, Canada (1985).
(22) "Shallow p+/n Junction Formation for CMOS VLSI Application Using Germanium Preamorphization," 43rd Device Research Conf., Boulder, CO, 1985.
(23) "Point Defect Generation During Phosphorus Diffusion in Silicon," Electronic Materials Conf., Boulder, CO, 1985.
(24) "Integrated Circuit Process Design Using a Hardwired Simulator" - PREDICT , NUPAD, Santa Clara, CA 1986.
(25) "Point Defect Kinetics During Backside Oxidation Measured by Frontside Stacking Fault Growth," B. Rogers, H. Z. Massoud, R. B. Fair, U. M. Gosele, R. Shaw, H. Korb and M. Guse, Electrochem. Soc. Spring Meeting, Phila. (1987).
(26) "Characterization and Modeling of the Diffusion of B and As in Si in Dry O2/HCl Mixtures," R. Subrahmanyan, H. Z. Massoud and R. B. Fair, Electrochem. Soc. Spring Meeting, Phila. (1987).
(27) "A Deep Decision Tree Approach to Modeling Submicron Silicon Technologies," R. B. Fair and J. E. Rose, ICCAD, San Jose, (1987).
(28) "Process Models for Ultra-Shallow Junction Technologies," R. B. Fair, IEDM, Wash., DC, 1987.

(29) "Accurate Junction-Depth Measurements Using Chemical Staining," R. Subrahmanyan, H. Z. Massoud and R. B. Fair, Fifth International Conference on Silicon Processing, Santa Clara, CA, 1988.
(30) "On the Role of Ion Implantation Damage in Silicon on Dopant Diffusion for Shallow Junction Formation," Y. Kim, R. B. Fair and H. Z. Massoud, Electronic Mater. Conf., Boulder, CO, June 1988.
(31) "Two Dimensional Modeling of Implant Damage Effects on Impurity Diffusion," R. B. Fair, C. Gardner, M. Johnson, S. Kenkel, D. Rose, J. Rose, R. Subrahmanyan, Workshop on Num. Modeling of Processes and Devices for Integrated Circuits, San Diego, May 1988.
(32) "A Comparison of Low Energy BF2 Implantation in Si and Ge Preamorphized Silicon," G.A. Ruggles, S. Hong, J.J. Wortman, M. Ozturk, E.R. Myers, J.J. Hren and R.B. Fair, Materials Research Society Mtg., Boston, Nov. 1988.
(33) "Modeling the Time Constant for Transient Diffusion Enhancement of Ion-Implanted Dopants in Silicon," Y. Kim, H.Z. Massoud and R.B. Fair, Process Simulation Workshop, MCNC, RTP, Nov. 1989.
(34) "Modeling the Oxidation of Heavily Doped Silicon in the Thin Regime," R. Ward, H.Z. Massoud and R.B. Fair, Process Simulation Workshop, MCNC, RTP, Nov. 1989.
(35) "Comparison of Measured and Simulated Two Dimensional P Profiles in Si," R. Subrahmanyan, H.Z. Massoud and R.B. Fair, Process Simulation Workshop, MCNC, RTP, Nov. 1989.
(36) "A Strategy for 2D Process Simulation," R.B. Fair, Process Simulation Workshop, MCNC, RTP, Nov. 1989.
(37) "Shallow-Junctions-Modeling the Dominance of Point Defect Charge States During Transient Diffusion," IEDM, Wash., D.C., Dec. 1989.
(38) "Technology Transfer at MCNC," SRC Workshop, Melbourne, FL, March, 1990.
(39) "Physical Modeling of the Time Constant of the Transient Enhancement in Diffusion of Ion-implanted Dopants in Silicon," Y. Kim, H.Z. Massoud, U. Gosele and R.B. Fair, Electrochem. Soc. Meeting, Montreal, May 1990.
(40) "Modeling The Enhanced Diffusion of Implanted Boron in Silicon," Y. Kim, T.Y. Tan, H.Z. Massoud and R.B. Fair, Electrochem. Soc. Mtg., Montreal, May 1990.
(41) "The Thermal Oxidation of Heavily Doped Silicon in the Thin-Film Regime: Dopant Behavior and Modeling Growth Kinetics," R.R. Ward, H.Z. Massoud and R.B. Fair, Electrochem. Soc. Mtg., Montreal, May 1990.
(42) "The Effect of Amorphizing Implants on Phosphorus Diffusion in Silicon," R.B. Fair, Electrochem. Soc. Mtg., Montreal, May 1990.
(43) "The Role of End-of-Range Dislocation Loops as a Diffusion Barrier," Y. Kim, H.Z. Massoud, S. Chevacharoeukul and R.B. Fair, Electrochem. Soc. Mtg., Montreal, May 1990.
(44) "Technology Transfer Utilizing the Proof-of-Concept Facility," R.B. Fair and J.F. Freedman, Adv. Semicond. Manuf. Conf. & Workshop, Boston, October 1991.
(45) "Spinoff Strategy for University-Based Applications Effort in Microsystems," Engineering Foundation Conference on Commercialization of Microsystems, Banff, Canada, Sept. 1994.
(46) "Physically Based Modeling of Boron Diffusion in Thin Gate Oxides:
Effects of F, H2, N, Oxide Thickness and Injected Si Interstitials," IEDM, Wash. DC, December, 1995.

(47) "Process Simulation of Dopant Atom Diffusion in SiO2," in Process Physics and Modeling in Semiconductor Technology Symposium, Spring meeting of the Electrochemical Society, Los Angeles (1996).
(48) G. Chen, T. Borca-Tasciuc, and R. B. Fair "Fundamental Limit of the Use of Pyrometry in Rapid Thermal Processing," in RTP'96, Boise, ID, Sept. 1996.
[49] R.B. Fair, "Boron Penetration of Thin Polysilicon Gates/Ultrathin gate Dielectrics from B+ Implantation and Thermal Processing," Electrochemical Society Meeting, Montreal, May 6, 1997
[50] R.B. Fair, "Boron Penetration of Thin Polysilicon Gates/Ultrathin Gate Dielectrics from B+ Implantation and Thermal Processing," Spring Meeting, Electrochemical Soc., Montreal, May, 1997.
[51] T.W. Tsuei, R.L. Wood, C.K. Malek, M.M. Donnelly, and R.B. Fair, "Tapered Microvalves Fabricated by Off-Axis X-ray Exposures," HARMST 97
(52) R.B. Fair, M. Pollack, and V. Pamula, "MEMS Devices for Detecting the presence of Explosive Material Residues in Mine Fields," SPIE Aerosense Conf., Orlando, vol. 3392, 409, April, 1998.
(53) J.M. Zara, S. Bobbio, R. Fair, S. Goodwin-Johannson, and S.W. Smith, "A Forward Looking Intracardiac Ultrasound Scanner Using MEMS Technology," ONR Transducer Materials and Transducers Workshop, State College, PA, May, 1998.
(54) Y. Wu, H. Niimi, H. Yang, G. Lucovsky, and R. Fair, "Microscopic Model for Boron-Atom Penetration Through Silicon Dioxide and Suppression of Boron Transport Through Silicon Nitride," 29th IEEE Semiconductor Interface Specialists Conference, San Diego, Dec., 1998.
(55) V.K. Pamula and R.B. Fair, "Detection of Explosive Residues with a MEMS Sensor," SPIE Aerosense Conf., Orlando, April, 1999.
(56) A. Dewey and R.B. Fair, "Microelectromechanical Systems (MEMS) Design and Design Automation Research at Duke University," International Conf. Modeling and Simulation of Microsystems, April 1998.
(57) A. Dewey, R. Fair, J. Jopling, T. Zhang, F. Cao, B. Schreiner, and M. Pollack, "Towards Microfluidic System (MEFS) Computing Architecture,", Third Inter. Conf. on Modeling and Simulation of Microsystems, San Diego,Mar. 27-29, 2000.
(58) V.K. Pamula and R.B. Fair, "Detection of Dissolved TNT and DNT in Soil with a MEMS Explosive Particle Detector," ," SPIE Aerosense Conf., Orlando, April, 2000.
(59) T. Zhang, K. Chakrabarty, and R.B. Fair, "Design of Reconfigurable Composite Microsystems Based on Hardware/Software Co-design Principles, "International Conf. Modeling and Simulation of Microsystems, March, 2001.
(60) H. Ren, A. Jog, and R.B. Fair, "Statistical Optimal Design of Microelectromechanical Systems (MEMS), 4th Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.
(61) J. Jopling, D. Rose, and R.B. Fair, "The Coupled-Domain System Simulation/Simulatability Problem," 4th Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.
(62) V.K. Pamula, A. Jog, and R.B. Fair, "Mechanical Property Measurement of Thin-Film Gold using Thermally Actuated Bimetallic Cantilever Beams," 4th Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.
(63) J. Ding, K. Chakrabarty, and R.B. Fair, "Reconfigurable Microfluidic System Architecture Based on Two-Dimensional Electrowetting Arrays," 4th Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.

(64) V. Srinivasan, A. Jog, and R.B. Fair, "Scalable Maxromodels for Microelectromechanical Systems," 4th Inter. Conf. On Modeling and Simulation of Microsystems, March, 2001.
(65) V.K. Pamula, P. Paik, M.G. Pollack, and R.B. Fair, “Microfluidic Reconfigurable Droplet Mixer,” BioMEMS and Nano Technology World 2001, Columbus, Ohio, September, 2001.
(66) P. Kolar and R.B. Fair, “Non-contact Electrostatic Stamping for DNA Microarray Synthesis,” Smalltalk 2001, San Diego, CA, August, 2001.
(67) M.G. Pollack, R.B. Fair, V.K. Pamula, and A. Shenderov, “Electrowetting Microfluidics for High Throughput Screening,” Smalltalk 2001, San Diego, CA, August, 2001.
(68) V.K. Pamula, P.Y. Paik, J. Venkatraman, M.G. Pollack, and R.B. Fair, “Microfluidic Electrowetting-Based Droplet Mixing,” MEMS Conference, Berkeley, CA, August, 2001.
(69) T. Zhang, K. Chakrabarty and R.B. Fair, “Performance Comparison between Continuous-flow and Droplet-based Microelectrofluidic Systems,” Fifth International Conference on Modeling and Simulation of Microsystems, San Juan, Puerto Rico, April 22-25, 2002.
(70). R. B. Fair, M.G. Pollack, R. Woo, V.K. Pamula, H. Ren, T. Zhang, and J. Venkatraman, “A Microwatt Metal-Insulator-Solution-Transport (MIST) Device for Scalable Digital Bio-Microfluidic Systems,” Paper 16.4, Inter. Electron Devices Meeting (IEDM), Washington, DC (Dec. 2001).
(71) H. Ren and R.B. Fair, “Micro/Nano Liter Droplet Formation and Dispensing by Capacitance Metering and Electrowetting Actuation,” IEEE Nano-2002, Arlington, VA (August, 2002).
(72) V. Srinvasan, V. K. Pamula, M.G. Pollack, and R.B. Fair, “A Digital Microfluidic Biosensor for Multianalyte Detection,” 16th IEEE MEMS 2003 Conf., Kyoto, Jan. 2003.
(73) H. Ren, V. Srinivasan, and R.B. Fair, “Design and Testing of an Interpolating Mixing Architecture for Electrowetting-Based Droplet On-Chip Chemical Dilution,” Transducers, 2003, Boston, June, (2003).
(74) V. Srinivasan, V.K. Pamula, K.D. Rao, M.G. Pollack, J.A. Izatt, and R.B. Fair, "3-D imaging of moving droplets for microfluidics using optical coherence tomography," Seventh International Conference on Miniaturized Chemical and Biochemical Analysis Systems (µTAS 2003), Lake Tahao, October, 2003.
(75) V. Srinivasan, V.K. Pamula, M.G. Pollack, and R.B. Fair, "Clinical diagnostics on human whole blood, plasma, serum, urine, saliva, sweat, and tears on a digital microfluidic platform," Seventh International Conference on Miniaturized Chemical and Biochemical Analysis Systems (µTAS 2003), Lake Tahao, October, 2003.
(76) M. G. Pollack, P. Y. Paik, A. D. Shenderov, V. K. Pamula, F. S. Dietrich, and R. B. Fair, "Investigation of electrowetting-based microfluidics for real-time PCR applications Seventh International Conference on Miniaturized Chemical and Biochemical Analysis Systems (µTAS 2003), Lake Tahao, October, 2003.
(77) H. Ren, V. Srinivasan, M.G. Pollack, and R.B. Fair, “Automated Electrowetting-Based Droplet Dispensing with Good Reproducibility,” Seventh International Conference on Miniaturized Chemical and Biochemical Analysis Systems (µTAS 2003), Lake Tahao, October, 2003.
(78) R.B. Fair, V. Srinivasan, P. Paik, H. Ren, V.K. Pamula, and M.G. Pollack, “Electrowetting-Based On-Chip Sample Processing for Integrated Microfluidics, IEDM 2003, Washington, DC, December 10, 2003.
(79) V. Srinivasan, V.K. Pamula, P. Paik, and R.B. Fair, “Protein Stamping for MALDI Mass Spectrometry Using an Electrowetting-based Microfluidic Platform,” Lab-on-a-Chip: Platforms, Devices, and Applications, Conf. 5591, SPIE Optics East, Philadelphia, Oct. 25-28, 2004.

(80) D. Vissani, K.N. Weaver, V. Srinivasan, R.B. Fair, and J.A. Stenken, "Adapting Theophylline Quantitation via Alkaline Phosphatase Inhibition to a Micro-Total Analytical System," Southern Regional Meeting of ACS, Research Triangle Park, NC, Nov. 10-13, 2004.
(81) V.K. Pamula, V. Srinvasan, H. Chakrapani, R.B. Fair, and E.J. Toon, "A Droplet-Based Lab-On-A-Chip for Coplorimetric Detection of Nitroaromatic Explosives," 18th IEEE Inter. Conference on Micro Electro Mechanical Systems (MEMS 2005), Miami, Jan. 30 (2005).
(82) P.B. Griffin, R.B. Fair, "A Continuous Flow Microchannel-based DNA Sequencing Scheme," Advances in Genome Biology and Technology Conf., Marco Island, FL, Feb. 9, 2006.
(83) Y. Ma, A. Khlystov, V. Ivanov, R.B. Fair, "Digital Microfluidic Impactor for Determination of Sulfate in Ambient Aerosol," Inter. Aerosol Conf., St. Paul. MN, Sept. 15, 2006.
(84) L. Luan, R.D. Evans, D. Schwinn, R.B. Fair, and N.M. Jokerst, "Chip Scale Integration of Optical Microresonator Sensors with Digital Microfluidics Systems," LEOS-2008, Newport Beach, CA, Nov. 9-13, 2008.
(85) P. Thwar, J.L. Rouse, A.E. Eckhardt, P. Griffin, M.G. Pollack and R.B. Fair, "Digital Microfluidic DNA Sequencing," Advances in Genome Biology and Technology (AGBT) Meeting, Marco Island, Florida, Feb., 2009.
(86) C.G. Geisler, J.G. Zhou, D.M. Wootton, P.I. Lelkes1, R. Fair, "Electrowetting-based Multi-microfluidics Array Printing of High Resolution Tissue Construct with Embedded Cells and Growth Factors," International Cartilage Repair Society, ICRS, Miami, May 23, 2009.
(87) R.D. Evans, B-N Hsu, Y-Y You, and R.B. Fair, "Electrostatic Printing of Sub-nanoliter Droplets for Tissue Engineering with Precise Concentration Control Via Digital Microfluidics," 13th ICACS International Conference on Surface and Colloid Science, New York, June 14-19, 2009.
(88) C. Geisler, D.M. Wootton, P.I. Lelkes, R.B. Fair, and J.G. Zhou, "Material study of electrowetting-based multimicrofluidics array printing of high resolution tissue construct with embedded cells and growth factors," ASME 2010 First Global Congress NanoEngineering for Medicine and Biology, Houston, TX, Feb. 7-10, 2010.
(89) B. -N. Hsu, A. C. Madison and R. B. Fair "Accelerate Sepsis Diagnosis by Seamless Integration of DNA Purification and qPCR," Proceedings of the 16th International Conference on Miniaturized Systems for Chemistry and Life Sciences (MicroTAS 2012), Okinawa, Japan, October 28-November 1, 2012, pp. 830-832.
(90) Kai Hu, Bang-Ning Hsu, Andrew Madison, Krishnendu Chakrabarty and Richard Fair, "Fault Detection, Real-Time Error Recovery, and Experimental Demonstration for Digital Microfluidic Biochips," Design Automation Technology Europe, paper # 586, Grenoble, March, 2013.
(91) A. Madison, M. Royal, R. Fair, M. Sandahl, J. Harrington, S. Punnamaraju, A. Eckhardt, A. Sudarsan, and M. Pollack, "Software automated genomic engineering (SAGE) enabled by electrowetting-on-dielectric digital microfluidics," MicroTAS 2013, Freiburg, Oct. 2013.
(92) A. Madison, M,W. Royal, and R.B. Fair, "An electrowetting on dielectric lab on a chip for multiplex automated genome engineering," 9th Inter. Meeting on Electrowetting, Cincinnati, June, 2014.
(93) L. Chen, A. Madison, and R.B. Fair, "Intra-droplet magnetic bead manipulation on a digital microfluidic chip," MicroTAS 2014, Oct. 26, 2014, San Antonio.
(94) K. Hu, M. Ibrahim, L. Chen, Z. Li, K. Chakrabarty, and R.B. Fair, "Experimental Demonstration of Error Recovery in an Integrated Cyberphysical Digital-Microfluidic Platform", BIOCAS 2015, Atlanta, Oct. 22-25, 2015.

EXHIBIT B

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; AND MICRON CONSUMER PRODUCTS GROUP, INC., DEFENDANTS.	)	C.A. NO. 14-01431-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG ELECTRONICS AMERICA, INC., AND SAMSUNG AUSTIN SEMICONDUCTOR, LLC, DEFENDANTS.	)	C.A. NO. 14-01430-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. SK HYNIX INC., SK HYNIX AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC., AND SK HYNIX MEMORY SOLUTIONS INC., DEFENDANTS.	)	C.A. NO. 14-01432-LPS-CJB JURY TRIAL DEMANDED

RESPONSIVE DECLARATION OF DR. RICHARD B. FAIR
REGARDING CLAIM CONSTRUCTION

I, Dr. Richard B. Fair, declare as follows:

I. Introduction

1. I have been retained by Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Consumer Products Group, Inc. (collectively "Micron"); and Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC (collectively, "Samsung") as an independent expert in connection with the above-captioned lawsuit to provide my analyses and opinions in certain technical aspects of this dispute. I understand that SK hynix Inc., SK hynix America Inc., Hynix Semiconductor Manufacturing America Inc., and SK hynix Memory Solutions, Inc. (collectively, "SK hynix") also join this declaration.

2. I previously submitted a Declaration of Dr. Richard B. Fair Regarding Claim Construction dated January 17, 2019 (hereafter, the "Opening Fair Declaration"), which in incorporated herein by reference. The purpose of the Opening Fair Declaration is to analyze and explain how a person of ordinary skill in the art at the time of the alleged inventions would understand certain claim terms in U.S. Patent Nos. 7,193,239 (the "'239 patent"), 7,504,732 (the "'732 patent"), 8,035,233 (the "'233 patent"), 8,410,617 (the "'617 patent"), 8,629,542 (the "'542 patent"), 8,653,672 (the "'672 patent"), 8,791,581 (the "'581 patent"), 8,796,862 (the "'862 patent"), 8,824,159 (the "'159 patent"), 8,841,778 (the "'778 patent"), 8,907,499 (the "'499 patent"), 8,928,119 (the "'119 patent"), and 8,933,570 (the "'570 patent") (collectively, the "Asserted Patents"), which I understand are owned and asserted by Elm 3DS Innovations, LLC ("Elm").

3. I understand that an expert retained by Elm, Dr. Shefford Baker, submitted a declaration on January 25, 2019 (hereafter, the "Baker Declaration"). The purpose of this Declaration is to respond to certain statements and opinions stated in the Baker Declaration.

4. As stated in the Opening Fair Declaration, I am being compensated at my ordinary and customary consulting rate of $600. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding. I am competent to testify to the matters stated in this Declaration and have personal knowledge of the facts and statements herein. Each of the statements is true and correct. My qualifications and experience are set forth in the Opening Fair Declaration and its Exhibit A, which are incorporated herein by reference.

II. Dr. Baker's Claim Construction Approach

5. In Section III of the Opening Fair Declaration, I provided a summary of my understanding as to the legal standard and requirements associated with interpreting the language of a patent claim. In Section IV of the Opening Fair Declaration, I provided a brief overview of the technology relating to the Asserted Patents. These sections are incorporated herein by reference.

6. In the Baker Declaration, Dr. Baker provided his own description of the alleged invention disclosed by the Asserted Patents, and his opinions on the interpretation of certain terms. I will address those claim terms in Sections III and IV of this Declaration. I have, however, several high level observations about Dr. Baker's claim construction analysis and description of the alleged invention.

A. Dr. Baker's Interpretation of the Claim Language Encompasses Admitted Prior Art

7. I disagree with Dr. Baker's opinions that certain claim limitations should be interpreted by simply looking at the functions they serve. For example, Dr. Baker opines that the "substantially flexible" requirement should be viewed as "flexible enough to facilitate die stacking for the purpose of making 3-D integrated circuits" (Baker Declaration at pp. 34-35), and

that the "low stress" requirement is simply "low enough to achieve a certain function" such as stacking of multiple integrated circuit chips (*id.* at p. 33). I disagree with these functional, result-driven interpretations of the claim limitations because these interpretations would broaden certain claim limitations that allegedly differentiate prior art to encompass technology that was already known.

8. The specification of the Asserted Patents acknowledges that stacking of integrated circuit chips was already known. For example, the specification identified the Leedy '695 prior art patent as well as prior art products from "Texas Instruments of Dallas Tex., Irvine Sensors of Costa Mesa Calif. and Cubic Memory Corporation of Scotts Valley Calif." as examples of prior art disclosures of stacked integrated circuit devices. *See* '239 Patent at 2:34-48. In each of these prior art products, the stacked layers would have been "flexible enough" to facilitate die stacking for making a 3D integrated circuit device, and the stress of the dielectrics in the stacked layers would have been "low enough" to enable stacking.

9. For example, an article cited in Elm's Identification of Extrinsic Evidence—Said F. Al-sarawi et al, "A Review of 3-D Packaging Technology," IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B, Vol. 21, No. 1 (February 1998)—describes different types of stacked integrated circuits that were already available around the filing of the Asserted Patents, including several of the products acknowledged as prior art by the Asserted Patents. For example, the Al-sarawi article describes products made by Irvine Sensors:

> *Thin film "T-connects" and sputtered metal conductors:*
> This method was jointly developed by Irvine Sensors and IBM. In this method, after the I/O signals are rerouted to one edge of the chip, a thin film metal layer is patterned on the surface of the stacked chips. Then, two processes, called lift-off photolithography and sputter-deposition, are

> performed on the face of the stack to form pads and buslines, creating what is called "T-connections" [29] as shown in Fig. 8.

Id. at 5.[1] Irvine Sensors' "T-connects" stacking arrangement is illustrated in Figure 8, below.

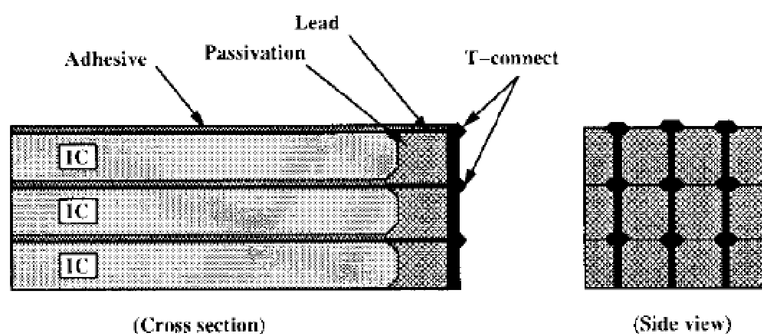


Fig. 8. Thin film metal "T-connects" for vertical interconnections.

10. An article published by NASA in 1993, "Mission Accomplished," NASA Tech Briefs, Vo. 17, No. 7, pp. 14-16 (May 1993), shows a picture of a stacked memory device from Irvine Sensors. As shown in the image reproduced below, the Irvine Sensors product includes a ten-layer stack of DRAM memory chips. *Id.* at p. 14 (annotations added in red). As explained in the caption below the image, the bottom half of the image shows ten layers of DRAM chips stacked vertically on a processor chip, and the top half of the image shows a circuit board containing a processor and a number of non-stacked DRAM chips. *Id.* According to the article, the stacked design not only decreases device size but also improves device performance by increasing speed and lowering power. *See id.*

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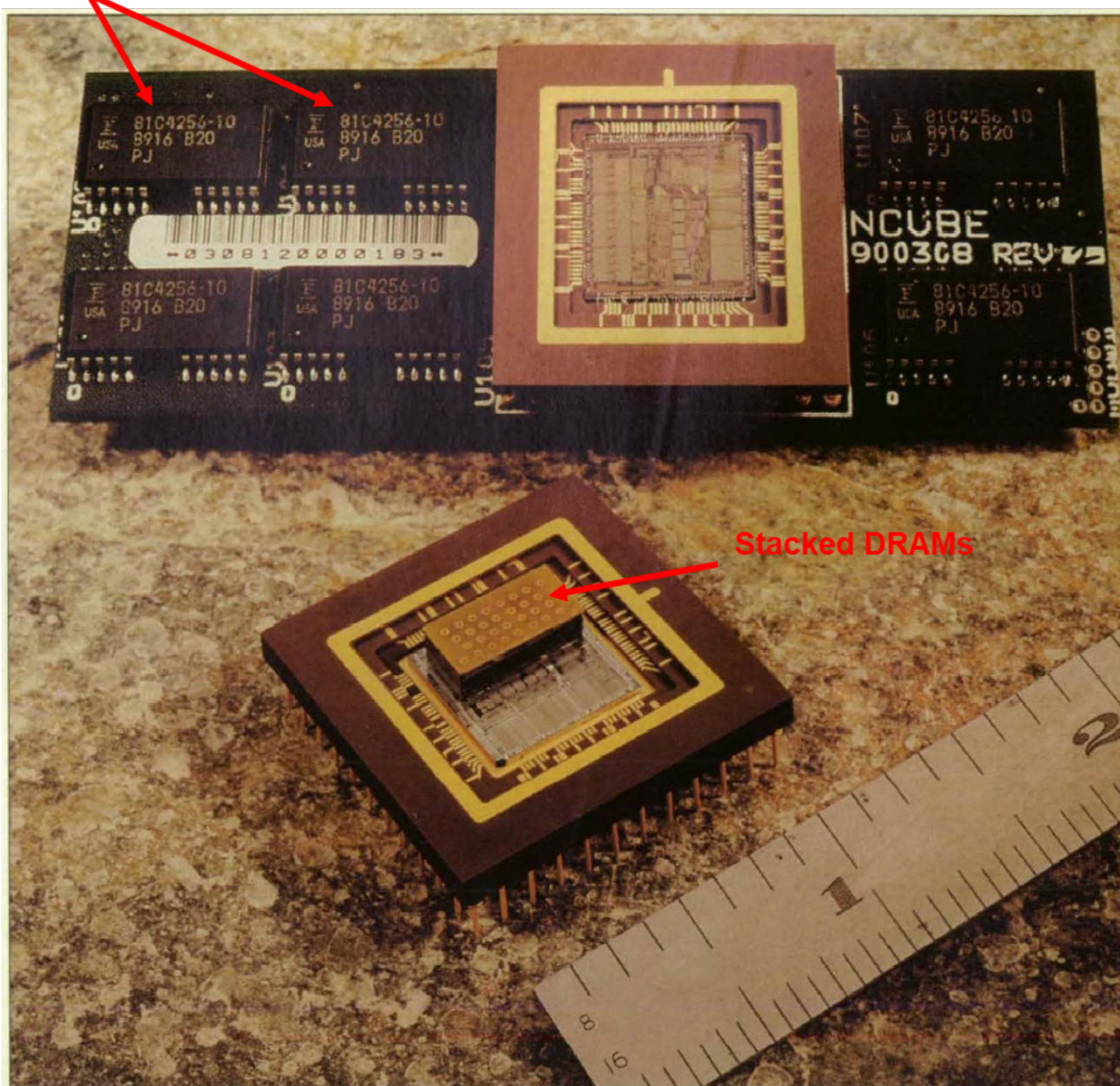
[1] Although the Al-sarawi paper was published in February 1998, its manuscript was submitted on April 30, 1997. The products discussed in the paper predate the Asserted Patents. For Irvine Sensors' "T-connects" design, the Al-sarawi paper cites a 1992 paper: J. A. Minahan, A. Pepe, R. Some, and M. Suer, "The 3-D stack in short form (memory chip packaging)," in Proc. 1992 42nd Electron. Comp. Technol. Conf., San Diego, CA, May 1992. The Minahan paper, which discusses Irvine Sensors' 3D stacked design, predates the Asserted Patents by almost five years.



Innovative chip-stacking technology from Irvine Sensors Corp. dramatically reduces memory footprint and offers such performance benefits as faster processing speeds and lower power requirements. In the foreground above is a processor incorporating a chip stack that contains ten 4-megabit DRAMs. The stack replaces the ten DRAMs on the processor board in the background.

11. In addition to the stacked DRAM products illustrated above, I understand that Irvine Sensors developed, marketed, and sold several other stacked integrated circuit products prior to the filing of the Asserted Patents, including at least HYMOSS, Advanced HYMOSS,

HDICOI, WWSRAM, 3D Active, and Multi-mode Modular Computer (MMC). *See generally* Defendants' Fourth Amended Invalidity Contentions.

12. The specification of the Asserted Patents admits that Irvine Sensors' stacked memory products are prior art to the Asserted Patents. *See* '239 Patent at 2:34-48 ("Furthermore, assembling die in a 3D manner has been attempted with regard to memory. Texas Instruments of Dallas Tex., Irvine Sensors of Costa Mesa Calif. and Cubic Memory Corporation of Scotts Valley Calif., have all attempted to produce stacked or 3D DRAM products."). As shown above, the Irvine Sensors stacked device includes multiple, stacked integrated circuit layers. Thus, Dr. Baker's interpretation that the claim limitations simply mean the substrates are "flexible enough" or that the stress is "low enough" for stacking would not distinguish the alleged invention from the prior art designs, including the Irvine Sensors design above, which had stacked integrated circuit layers and necessarily included dielectric insulators. Because the Irvine Sensors product illustrated above includes a 3D stacked structure, its IC layers must be "flexible enough" to facilitate stacking, and its dielectric stress must be "low enough" to enable stacking.

13. Dr. Baker's interpretation of the claim language is also inconsistent with his own identification of thinning and "low stress" as the two primary aspects of the alleged invention. *See* Baker Declaration at p. 22 ("The asserted patents teach about two important concepts that facilitate the manufacture of 3-D integrated circuits. The first is thinning the substrate to make the die 'substantially flexible.' The second is the use of 'low stress' dielectrics."). In other words, because others have already achieved stacking of multiple layers, the alleged invention cannot be about making the layers "flexible enough" or using dielectrics that have stresses "low enough" to facilitate stacking.

B. Dr. Baker Did Not Address the Prosecution Histories

14. The Baker Declaration does not address the prosecution histories of the Asserted

Patents. Dr. Baker did not identify the prosecution histories among the documents he considered and states that he did not address those portions of the reports where I quote the prosecution history (*see* Baker Declaration at p. 5), nor does he acknowledge the prosecution history statements cited in the Opening Fair Declaration.

15. In fact, several of Dr. Baker's opinions, as explained in greater detail below, contradict statements made by Elm during prosecution of the patents. For example, Dr. Baker opines that "stress is stress" without regard to the type of stress involved (*see* Baker Declaration at p. 15), which is inconsistent with multiple arguments Elm made before the PTO. *See* Opening Fair Declaration at ¶¶ 96-100. Dr. Baker also opines that "low stress dielectric" within the scope of the claims can be a compressively stressed dielectric film (*see* Baker Declaration at pp. 32-33), even though Elm explicitly disparaged the use of compressively stressed films during prosecution. *See* Opening Fair Declaration at ¶¶ 101-102.

16. I understand that claim terms must not only be interpreted in the context of the particular claim in which it appears, but also in the context of the entire patent, including the specification and prosecution history. Thus, I disagree with Dr. Baker's approach of interpreting the claim limitations without considering the prosecution histories before the PTO that led to the issuance of the asserted claims.

C. Dr. Baker's Constructions Do Not Define the Metes and Bounds of the Claim Terms

17. I understand that patent claims must particularly point out and distinctly claim the subject matter which the inventors regard as the invention. I understand that if a claim term, when interpreted in light of the specification and the prosecution history, fails to inform those skilled in the art about the scope of the claimed invention with reasonable certainty, then the claim term and all claims reciting such term are indefinite. With respect to functional

limitations, I understand that to be definite, the claims must recite sufficient structural limitations to perform the function. Particularly with respect to an allegedly novel result, the claim must be limited to how a functional result is achieved and cannot simply claim all structures that perform the claimed function.

18. In my opinion, Dr. Baker's function-based interpretation of the claim limitations as requiring films to be "flexible enough" or having stress "low enough" to satisfy the practitioner's goals does not inform those skilled in the art about the structural scope of the claimed invention with reasonable certainty. These interpretations do not identify what structure provides enough flexibility and low enough stress. Instead, Dr. Baker's interpretation suggests that if a stacked memory device works, it must be flexible enough with low enough stress in the dielectric layer. In other words, Dr. Baker interprets the claims to cover all stacked integrated circuit structures. I understand that it is impermissible to limit a claim only by the desired result. Dr. Baker's interpretation does not limit the structures required to achieve those results.

III. The "Stress" Terms

19. In Sections VI.D and VI.E of the Opening Fair Declaration, I addressed certain "stress" related claim terms, which are listed in ¶¶ 79 and 104 of the Opening Fair Declaration. Dr. Baker disagreed with certain aspects of my analysis. I provide the following responses.

A. The Articles I Cited In My Declaration Demonstrate the Lack of a Recognized Standard for "Low Stress"

20. In ¶¶ 108-112 of the Opening Fair Declaration, I cited various patents and articles to show that there is no agreed standard for determining when a dielectric film is "low stress." Dr. Baker asserts that the example references I cited in my declaration refer to "widely differing materials in wildly differing technologies" (Baker Declaration at p. 25), and therefore a person with ordinary skill in the art of semiconductor manufacturing would not have considered these

references to be in the context of integrated circuit manufacturing. Overall, Dr. Baker argues that the cited references are outside of the context of "integrated circuit manufacturing," and therefore do not demonstrate that the "low stress" terms have different meanings with the relevant context. *See* Baker Declaration at pp. 23-26. I disagree. Below I have listed these cited references and the technical context in which their expressed teachings are directed. As explained below, each of these references relates to the stress of dielectric thin films in semiconductor devices—the same dielectrics claimed in the Asserted Patents.

21. U.S. Patent No. 5,279,865, cited in ¶ 108 of the Opening Fair Declaration, is a prior art patent filed by Digital Equipment Corporation, a major computer and integrated circuit company in the 1990s. *See* '865 Patent at Cover. This patent explicitly discusses using "plasma enhanced chemical vapor deposition (PECVD)" to form "good quality interlevel dielectric (ILD)" materials. *See, e.g., id.* at 1:41-53, 3:4-4:60. The specification states: "The present invention relates generally to oxide deposition during the processing of semiconductor wafers, and particularly to a process for filling very narrow interlevel gaps, such as gaps between parallel metal lines, with silicon oxide." *Id.* at 1:1-9. Oxide deposition is referenced in the first six rows of Baker Figure 5 as a dielectric used in silicon manufacturing in the early 1990s. *See* Baker Declaration at p. 25. Silicon oxide is also one of the two types of dielectric films described in the Asserted Patents. *See* '239 Patent at 9:1-2. Thus, the '865 Patent directly relates to the stress of dielectrics used for integrated circuit manufacturing. *See id.* Dr. Baker did not explain why this patent would be inapplicable.

22. U.S. Patent No. 5,500,312, cited in ¶ 109 of the Opening Fair Declaration, is a prior art patent filed by AT&T scientists working in Murray Hill, New Jersey. *See* '312 Patent at Cover. The Murray Hill location is one of the locations of AT&T Bell Laboratories (commonly

called "Bell Labs"), which is the research lab that originally invented the semiconductor transistor. As stated in the Opening Fair Declaration, I worked at Bell Labs from 1969 to 1981, conducting research on semiconductor devices and processes. The first named inventor of the '312 Patent, Dr. Lloyd R. Harriott, is currently a professor at the University of Virginia who specializes in semiconductor microelectronics, and he was previously the Director of Advanced Lithography Research at Bell Labs.[2] The '312 Patent generally describes "[a] process for controlling the stress of multilayer films formed on a substrate," typically a "silicon wafer." *See* '312 Patent at Abstract, 3:13-30. While the patent specification describes using layers of Mo (molybdenum) on silicon as one example, the specification also explicitly references the stress of dielectric thin films such as silicon nitride (SiN_x). *See id.* at 3:51-57 ("Materials such as Si, SiN_x, and carbon (C) are typically under compressive stress when formed into films with a thickness of about 0.5 nm to about 10 nm. Therefore, one embodiment of the present invention contemplates a multilayer film that contains periods with a layer made of Si, SiN_x or C . . . ."). Silicon nitride deposition is referenced as Si_3N_4 deposition by a plasma process in Figure 5 of the Baker Declaration, and it is a dielectric used in silicon manufacturing in the early 1990s. *See* Baker Declaration at p. 25. Silicon nitride is also one of the two types of dielectric films described in the Asserted Patents. *See* '239 Patent at 9:1-2. Thus, Dr. Baker's argument that the '312 Patent does not "even refer to stresses in dielectrics" (Baker Declaration at p. 25) is factually incorrect.

23. Temple-Boyer et al., "Residual stress in low pressure chemical vapor deposition SiN_x films deposited from silane and ammonia," J. Vac. Sci. Technol. A 16(4) Jul/Aug. 1998,

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[2] *See* https://engineering.virginia.edu/faculty/lloyd-r-harriottz.

cited in ¶ 110 of the Opening Fair Declaration, relates to the deposition of "silicon nitride Si_3N_4" films through "chemical vapor deposition" for use in "microelectronics." *See id*. at 2003. For example, it states: "In this article, we report the deposition of Si_3N_4 and SiN_x films by low pressure chemical vapor deposition (LPCVD) from silane SiH_4 and ammonia NH_3 in order to obtain low stress (silicon-rich) silicon nitride films with a good uniformity of thickness and composition on the wafer." *Id.* As discussed above, silicon nitride is one of the two types of dielectric films described in the Asserted Patents. *See* '239 Patent at 9:1-2. In fact, the Leedy '695 Patent, which is incorporated by reference in each of the Asserted Patents, also describes using SiH_4 and NH_3 to form silicon nitride (which can be written as stochiometic Si_3N_4 or non-stochiometic SiN_x) by chemical vapor deposition. *See* Leedy '695 at 11:28-65. Thus, the Temple-Boyer article not only directly relates to the stress of dielectrics used for integrated circuit manufacturing, it also refers to the same type of material and same deposition technique contemplated by the Asserted Patents.

24. Suzuki et al., "Silicon Nitride Films with Low Hydrogen Content, Low Stress, Low Damage and Stoichiometric Composition by Photo-Assisted Plasma CVD," Japanese J. Appl. Phys. 28, L2316 (1989), cited in ¶ 111 of the Opening Fair Declaration, relates to a "plasma CVD method [that] was developed to deposit high quality silicon nitride films." *Id.* at Abstract. It describes using the disclosed process for the fabrication of "MOSFET [metal-oxide semiconductor field-effect transistors] in LSI [large-scale integration]" devices. *Id* at L2316. It also describes a low-temperature process: "SiN films for the protection layers in LSI and TFT are required to be deposited at a low temperature, below 300ºC." *Id*. The Leedy '695 Patent, which is incorporated by reference in each of the Asserted Patents, similarly describes a plasma CVD process for silicon nitride deposition at a temperature of 400ºC. *See* Leedy '695 at 11:28-

65. Thus, the Suzuki article directly relates to the stress of dielectrics used for integrated circuit manufacturing.

25. Cheng, et al., "Ultralow-Stress Silicon-Rich Nitride Films for Microstructure Fabrication," Sensors and Materials, 11, No. 6, 349 (1999), cited in ¶ 112 of the Opening Fair Declaration, also relates to the deposition of low-stress silicon nitride dielectric films. *Id.* at Abstract. The article describes depositing the dielectric film on silicon wafers, and using the disclosed method for "IC" (integrated circuit) and "microsensor" fabrication. *Id.* at p. 356. It states: "Four-inch p-type silicon (100) wafers were used as substrates. After a standard cleaning procedure, nitride films were deposited under various conditions designed by the Taguchi method as summarized in Table 1." *Id.* at 350. "Silicon-rich nitride films" are one type of silicon nitride and, as discussed above, silicon nitride is one of the two types of dielectric films described in the Asserted Patents. *See* '239 Patent at 9:1-2. Thus, the Cheng article directly relates to the stress of dielectrics used for integrated circuit manufacturing.

26. Each of these articles and patents cited in ¶¶ 108-112 of the Opening Fair Declaration relates to the stress of dielectric thin films in semiconductor devices, including silicon nitride and silicon oxide. These are the same dielectrics described and claimed in the Asserted Patents. Thus, I conclude that all of the references I cited in the Opening Fair Declaration as examples of the term "low stress" fall into the same context as the Asserted Patents—dielectrics used in silicon wafer manufacturing or the use of silicon wafer processing to develop a deposition process on a substrate. All these references describe dielectrics as "low stress" where they fall in a range varying from $1x10^7$ dynes/cm^2 to $6x10^9$ dynes/cm^2, which reflects a difference of a factor of 600 (*see* Opening Fair Declaration at ¶ 113). Thus, I maintain my opinion that one of ordinary skill in the art would not understand "low stress" to have a clear

and well-defined meaning from the wide range of "low stress" values in the literature and within the context of silicon wafer processing.

B. Dr. Baker's Opinions Confirm that "Low Stress" Is Indefinite

27. Dr. Baker agrees that the "low stress" term is a term of degree that depends on context. *See* Baker Declaration at p. 23. Dr. Baker further agrees that "there is no hard line" in defining when a dielectric material is "low stress." *See id.* at p. 27. And Dr. Baker offers multiple definitions of "low stress" within his report, showing that there is no general consensus on the meaning of this term. These opinions actually *support* my conclusion that the "low stress" terms are indefinite.

28. Dr. Baker's inability to define a clear boundary for when "low stress" ends and "conventional stress" begins confirms the indefiniteness of the term. Throughout his declaration, Dr. Baker suggests at least five different possible criteria for what is "low stress":

- On page 31, Dr. Baker states that the "inventor" described stress that is "less than **5×10^8 dynes/cm^2**" as suitable for the alleged invention;
- On page 33, Dr. Baker states that "**8×10^8 dynes/cm^2** fits comfortably into" the range of "low stress";
- On pages 27 and 28, Dr. Baker states that "stresses less than about **10×10^8 dynes/cm^2** would have been considered 'low' at the time of the asserted patents";
- Citing to the Temple article on page 27, Dr. Baker states that "stresses of **13×10^8** – 23×10^8 **dynes/cm^2** . . . could be considered more 'conventional' by the time of the patents," suggesting that stresses below 13×10^8 dynes/cm^2 are considered "low";
- On page 33, Dr. Baker provides yet another definition: "Another context is '**low enough** to achieve a certain function,' in this case to achieve an integrated circuit

chip that is simultaneously flexible enough and flat enough to be stacked."

29. Dr. Baker's inability to provide a single definition underscores the problem—what is a "low stress" will vary from one person to another based on opinion. There are no boundaries that are reasonably ascertainable to persons skilled in the art. Elm's proposed construction for the "low stress dielectric" term is "a dielectric having a stress of less than 8×10^8 dynes/cm^2." Yet Dr. Baker opines that "stresses less than about 10×10^8 dynes/cm^2 would have been considered 'low' at the time of the asserted patents." Baker Declaration at pp. 27-28. And as support, Dr. Baker cites to an article that describes "stresses of 13×10^8" and above as "conventional." *See id.* at p. 27. These inconsistent definitions create a zone of uncertainty between values. For example, a dielectric having a stress of 9 x 10^8 dynes/cm^2 would fall within the scope of "low stress dielectric" according to Dr. Baker's opinion, but would fall outside of the scope of "low stress dielectric" under Elm's proposed construction. Thus, the Asserted Patents fail to inform those skilled in the art about the scope of the claimed invention with reasonable certainty.

30. In addition, Dr. Baker's statements do not actually support Elm's proposed construction of the "low stress" terms. While Dr. Baker states that "a stress of 8 x 10^8 dynes/cm^2 or less would be suitable" for stacking multiple chips, he does not offer any explanation or support for drawing a boundary line at the 8 x 10^8 dynes/cm^2 value. *See* Baker Declaration at p. 33. To the contrary, Dr. Baker expressly opines that a dielectric layer having stress higher than 8 x 10^8 dynes/cm^2 could still be considered "low stress." *Id.* The fact that Elm's own expert cannot support Elm's construction confirms that Elm's construction is incorrect. And the fact that Elm's own expert provides numerous definitions for the term "low stress" confirms that this term is indefinite.

C. Dr. Baker's "Stress Is Stress" Opinion Contradicts the Intrinsic and Extrinsic Evidence

31. On page 15 of the Baker Declaration, Dr. Baker states: "Stress is stress; there are no actual different 'types' of stress, these terms are just shorthand to refer to the stress's origin." He makes similar statements elsewhere in his report at well. *See, e.g.*, *id.* at p. 28. These statements are inconsistent with the intrinsic and extrinsic evidence.

32. As described in ¶ 82 of the Opening Fair Declaration, the specification of the Asserted Patents and the incorporated Leedy '695 Patent distinguish between different types of stress. In addition, Elm relied on the distinctions between different types of stress to distinguish prior art before the PTO. *See id.* at ¶ 82 (citing IPR2016-00390, Patent Owner's Preliminary Response (April 6, 2016) at 58). Thus, regardless of how Dr. Baker characterizes the different types of stress—whether as the stress's "origin" or something else—the distinctions are important because they were relied on during prosecution to overcome prior art. Moreover, as described in ¶ 83 of the Opening Fair Declaration, contemporaneous technical literature also describes different types of stress.

33. Because the claims are silent as to the type of "stress" to be limited, they would not have a clear and definite meaning to one of ordinary skill in the art because the claim language does not specify what kind of "stress" is contemplated. Dr. Baker cannot avoid this problem by arguing that "stress is stress."

D. Dr. Baker's Attempt to Recapture Stress Balancing Ignores Years of Prosecution History

34. On pages 30-31 of the Baker Declaration, Dr. Baker states that he understands "the term 'low stress' applies equally to both" inherently low stress films and stress balanced films. This opinion directly contradicts statements made by Elm before the PTO to support patentability of the Asserted Patents.

35. As described in ¶¶ 96-100 of the Opening Fair Declaration, Elm made numerous representations to the PTO that the "low stress" terms exclude stress balancing. For example, to distinguish the Kowa reference, Elm stated to the PTO: "Kowa discloses depositing stress-balanced alternating silicon nitride (SiN) layers. Kowa also discloses a plasma CVD method for 'alternately stacking a thin film having compressive stress and a thin film having tensile stress . . . .' . . . Kowa does not address inherently low-stress films." IPR2016-00390, Patent Owner's Preliminary Response (April 6, 2016) at 58. Based on these statements, the Patent Trial and Appeal Board (PTAB) concluded as follows: "We, further, do not construe the term 'low stress dielectric' to require the stress-balancing of multiple dielectrics because the Specification of the '542 patent has distinguished 'low stress dielectrics' from those of 'conventional stress levels' that require stress-balancing to achieve a similar result." IPR2016-00390, Paper No. 13, Decision - Institution of *Inter Partes* Review (July 1, 2016) at 12-13.

36. Dr. Baker's opinions cannot be reconciled with the statements made by Elm to the PTO. If, according to Dr. Baker, the term "low stress dielectric" encompasses stress balancing, then Elm's basis for distinguishing Kowa—which discloses using alternating compressive and tensile films to create a low stress stack—would have been groundless. In other words, Dr. Baker's interpretation of the "low stress" limitations would broaden the terms to encompass Kowa and other references distinguished by Elm during prosecution of the Asserted Patents.

E. Dr. Baker Acknowledges That Stress Values Vary Within a Dielectric Layer and Across Different Measurement Methods

37. Dr. Baker acknowledges that stress values in a dielectric film are "inhomogeneous." *See* Baker Declaration at pp. 6, 8, 16, 17, 20-21, 29. This means that the stress levels in a dielectric film can vary from point to point—the stress can be high in certain locations and low in other locations. *See id.* Dr. Baker states: "If one had the ability to measure

the stress at different points in the sample, very different values would be obtained." *Id.* at 29.

38. Dr. Baker also acknowledges that variation in stress could be significant for semiconductor processing because "failures due to cracking, delamination, and other mechanisms occur when the peak stress, not the average stress, reaches a critical value." *Id.* at p. 20. Thus, Dr. Baker's statement indicates that in certain situations, it is a layer's peak stress—not its average stress—that affects whether there would be failure due to cracking or delamination.

39. These statements are consistent with the issue I addressed in ¶¶ 84-85 of the Opening Fair Declaration. For example, I explained that there could be both linear gradients of stress throughout the thickness of a layer, as well as steep, non-linear stress gradients at film boundaries. Because the Asserted Patents do not specify where the stress should be measured, this uncertainty is one of the reasons that the stress-related claim terms are indefinite.

40. In an effort to get around this problem, Dr. Baker opines that "in the vast majority of applications, this [stress variation] does not matter" because "a researcher" can use the "average stress" level. *See* Baker Declaration at pp. 29-30. This statement appears to acknowledge that, in at least some of the applications, the inhomogeneous nature of the stress value *does* matter. In fact, Dr. Baker himself identified a situation where it could matter: "failures due to cracking, delamination, and other mechanisms occur when the peak stress, not the average stress, reaches a critical value." *Id.* at p. 20. In the context of stacking multiple integrated circuit layers, cracking and delamination are serious concerns. Indeed, Dr. Baker acknowledged that stress could cause a layer to "pop off" (which I understand to mean delaminate). *See id.* at 35. Thus, the stress variation in a layer is important to the technology at issue in the Asserted Patents.

41. Many of the asserted claims impose an explicit numeric limitation on the stress value. Dr. Baker does not explain whether a dielectric layer having an average stress above the claimed threshold value, but with some locations having a stress within the claimed range, would infringe these claims. Dr. Baker also does not explain whether a layer having high surface stress above the claimed threshold but lower stress near the center of the layer would infringe these claims. Thus, the claim terms are indefinite for failing to inform those skilled in the art about the scope of the claimed invention with reasonable certainty because the Asserted Patents do not specify where the stress is to be measured.

42. In addition, Dr. Baker also acknowledges that there are different methods to measure the stress of a dielectric layer. *See* Baker Declaration at pp. 20-21, 30. Dr. Baker appears to endorse the curvature method as his preferred method, but acknowledges that this method can only measure the average "layer stress." *See id.* at p. 21. As Dr. Baker admits, the "average stress" of a layer is not sufficient in some situations—failure mechanisms like fracture and delamination are controlled by the peak stress, not average stress. *See id.* at p. 20.

43. Dr. Baker's opinion that the stress limitations refer to an average stress measured by a curvature method is also unsupported by any intrinsic evidence. The specification of the Asserted Patents mentions neither the curvature method nor "average stress." In fact, the Asserted Patents do not specify any particular technique for measuring "stress." Dr. Baker provides no explanation for why a person of ordinary skill in the art, reading the specification and prosecution histories, would conclude that the claims recite a stress limitation as determined by an average stress measured through curvature, especially given that several other measurement techniques were known by those of ordinary skill at the time of the alleged invention. Dr. Baker also does not explain why a person of ordinary skill in the art would reject

other known methods of stress measurement that a person of ordinary skill would have expected to report different values of "stress." He claims that a person of ordinary skill in the art would not even attempt to compare stress values obtained by various methods I outlined in my Opening Fair Declaration at ¶¶ 86-89, because "…they would have known how to obtain good values." *See id.* at p. 30. I disagree with Dr. Baker's unsupported opinion. As I have stated in my declaration at ¶¶ 84-93, no stress measurement technique is without shortcomings when applied to materials used in silicon processing, since they are indirect measurements that rely on certain modeling assumptions.

44. Moreover, Dr. Baker attempts to brush aside variations between different measurement methods as "experimental error." *See* Baker Declaration at p. 30. I disagree. As I explained in the Opening Fair Declaration, it was well known that different measurement methods resulted in significantly different "stress" values. *See* Opening Fair Declaration at ¶¶ 86-93. The Asserted Patents are silent on what "stress" measurement technique should be used. Dr. Baker does not explain whether a film that measures to be outside of the claimed "stress" range using a curvature approach but within the claimed "stress" range using an x-ray approach would fall within the scope of the claims. Thus, the claim terms are indefinite for failing to inform those skilled in the art about the scope of the claimed invention with reasonable certainty because the Asserted Patents do not specify how the stress level is measured, which stress is measured, and where the stress is measured.

IV. The "Substantially Flexible" Terms

45. In Sections VI.A - VI.C of the Opening Fair Declaration, I addressed certain claim terms that include the phrase "substantially flexible," which are listed in ¶¶ 43, 67, and 76 of the Opening Fair Declaration. Dr. Baker disagreed with certain aspects of my analysis. I provide the following responses.

A. Dr. Baker Does Not Support Elm's Proposed Construction For the "Substantially Flexible" Terms

46. In the Baker Declaration, Dr. Baker acknowledges that Elm proposes to construe the "substantially flexible" terms as "largely able to bend without breaking." Baker Declaration at p. 34. But Dr. Baker does not provide any support for Elm's construction.

47. As an initial matter, Dr. Baker does not explain what "largely" able to bend means. While Dr. Baker agrees that flexibility is a term of degree that depends on context (*see id.* at p. 35), he does not provide any guideline or criteria for how much bending is required for a material to be "largely able to bend." He does not explain, for example, whether a 1 degree bend without breaking is sufficiently large, or whether a 30 degree bend without breaking would be required to satisfy Elm's construction.

48. Moreover, even if there is a precise definition for "largely," Dr. Baker appears to agree that the flexibility requirement is not determined by the point at which the degree of bending causes fracture. For example, Dr. Baker states:

- "Interpretation of this [substantially flexible] term in no way requires a specification of a fracture load . . . ." *Id.* at p. 35
- "[T]here is no requirement that a manufacturer be able to predict when fracture might occur in order to understand whether an object is flexible in the context of semiconductor manufacturing described in the patent." *Id.* at p. 36.
- "A person of ordinary skill in the art of semiconductor manufacture would certainly not try to turn a requirement for flexibility into a fracture mechanics study." *Id.* at p. 36.

49. These statements by Dr. Baker confirm my opinion that the technological context of the Asserted Patents has nothing to do how much bending a structure can endure before

breaking. Accordingly, Dr. Baker's statements support my opinion that the "substantially flexible" terms should not be defined as "largely able to bend without breaking" because this construction would have no relationship to the technological context of the Asserted Patents.

B. Dr. Baker's Interpretation of "Substantially Flexible" is Inconsistent with the Intrinsic Evidence

50. Dr. Baker opines that the "substantially flexible" term should be interpreted as "flexible enough to facilitate die stacking for the purpose of making 3-D integrated circuits" or "flexible enough that subsequent die can conform to the shape of the substrate or previously [sic] die on which they are to be stacked." Baker Declaration at p. 35. This interpretation is inconsistent with the specification, the prosecution histories, the language of the claims, and the context of the technology.

51. First, Dr. Baker's interpretation is inconsistent with the specification of the Asserted Patents. The specification cites as admitted prior art various stacked integrated circuit products, such as "3D DRAM products" made by "Texas Instruments of Dallas Tex., Irvine Sensors of Costa Mesa Calif. and Cubic Memory Corporation of Scotts Valley Calif." *See* '239 Patent at 2:34-48. The specification then identifies the formation of "a substantially flexible substrate" as one of the "features" that distinguishes the alleged invention over the prior art. *See id.* at 3:10-23. Indeed, Dr. Baker himself identified "*thinning* the substrate to make the die 'substantially flexible'" as one of the "two important concepts" disclosed in the Asserted Patents. *See* Baker Declaration at p. 22.

52. Dr. Baker's opinion that "substantially flexible" simply means "flexible enough to facilitate die stacking for the purpose of making 3-D integrated circuits" means that each and every prior art 3D product—including those manufactured by Texas Instruments, Irvine Sensors, and Cubic Memory Corporation—would necessarily have implemented this "substantially

flexible" feature. Thus, Dr. Baker's opinion contradicts the specification, which alleges that "substantial flexibility" of substrates and integrated circuits is an inventive aspect of its disclosure.

53. Second, Dr. Baker's interpretation is inconsistent with the prosecution histories. As explained in the Opening Fair Report, the PTO Examiner issued an indefiniteness objection for certain claims during prosecution because the "substantially flexible" terms are ambiguous. *See* Opening Fair Report at ¶¶ 49-50. In response, Elm pointed to the process of thinning a substrate to 50 microns, followed by smoothing or polishing, as the "meaning" of the "substantially flexible" claim terms. *See id.* Elm did not, however, tell the Examiner that "substantially flexible" merely means the layers are "flexible enough" to be stacked. Thus, Dr. Baker's opinion is inconsistent with the prosecution history, which relied on thinning to 50 microns followed by smoothing or polishing to overcome the Examiner's indefiniteness rejection.

54. Third, Dr. Baker's interpretation is inconsistent with the language of the claims because it renders meaningless the "substantially flexible" terms. For example, Claim 1 of the '239 Patent recites "Circuitry comprising: a plurality of monolithic substrates having integrated circuits formed thereon and stacked in layers such that each layer comprises only one of the substrates, ***wherein at least one of the plurality of substrates is a substantially flexible substrate*** . . . ." '239 Patent at Claim 1. If, according to Dr. Baker, "substantially flexible" simply means "flexible enough to facilitate die stacking for the purpose of making 3-D integrated circuits," then all of the "plurality of monolithic substrates" that are "stacked in layers" must be "substantially flexible." Otherwise the stack would delaminate or "pop off" as Dr. Baker states. Thus, Dr. Baker's interpretation is inconsistent with the language of the claims because it would

render redundant and meaningless the clause "wherein at least one of the plurality of substrates is a substantially flexible substrate."

55. Fourth, Dr. Baker's interpretation ignores the technological context of the Asserted Patents. There are many factors that influence whether two layers can be stacked. For example, two layers that are not "flexible" could still be stacked and bonded without delamination if they follow the same contour or curvature, or if there is sufficient adhesive material between the layers to fill gaps. Indeed, the concern addressed by Dr. Baker—that the layers should be flexible to avoid delamination (referred to as "pop off" in the Baker Declaration)—is a concern that is specific to the context of forming vertical interconnections through thermal compression bonding. This is one of the key "features" of the alleged invention (*see* Opening Fair Report at ¶¶ 137-138) that is not even mentioned in Dr. Baker's Declaration. In fact, the "substantially flexible" requirement does not make sense in the other contexts of stacking integrated circuit layers. Thus, the definition provided by Dr. Baker is subjective and varies depending on the method bonding used to stack layers, and therefore it lacks any objective guideline for determining the boundaries of the claims.

56. Accordingly, it is my opinion that the "substantially flexible" claim terms should not be construed as "largely able to bend without breaking," "flexible enough to facilitate die stacking for the purpose of making 3-D integrated circuits," or "flexible enough that subsequent die can conform to the shape of the substrate or previous die on which they are to be stacked." Construing the "substantially flexible" terms under Elm's proposal or under one of Dr. Baker's definitions would render the asserted claims indefinite.

V. Other Comments

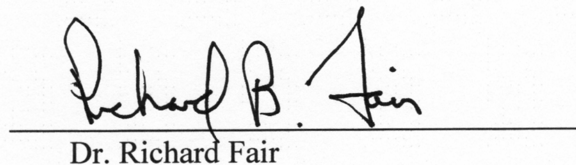
57. My opinions are subject to change based on any expert opinions that Elm may later present and information I may receive in the future or additional work I may perform. With

this in mind, based on the analysis I have conducted and for the reasons set forth above, I have reached the conclusions and opinions in this Declaration.

58. I understand that the Court does not generally hear expert testimony during the claim construction hearing. However, if I am called to testify, in connection with my anticipated testimony in this action, I may use as exhibits various documents produced in this case that refer or relate to the matters discussed in this Declaration. I have not yet selected the particular exhibits that might be used. In addition, I may create or assist in the creation of certain demonstrative evidence to assist me in testifying, and I reserve the right to do so, to further support the positions in this Declaration.

59. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: February 1, 2019



Dr. Richard Fair

EXHIBIT C

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. SK HYNIX INC., SK HYNIX AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC., AND SK HYNIX MEMORY SOLUTIONS INC., DEFENDANTS.	))))))))))))	C.A. NO. 14-01432-LPS-CJB JURY TRIAL DEMANDED

DECLARATION OF DR. STEVEN MURRAY
REGARDING CLAIM CONSTRUCTION

I, Dr. Steven Murray, declare as follows:

I. INTRODUCTION

1. I have been retained by K&L Gates on behalf of the Defendants in C.A. NO. 14-01432-LPS-CJB as an independent expert in connection with the above-captioned lawsuit to provide my analyses and opinions on certain technical aspects of this dispute.

2. In this declaration, I set forth my opinions on how a person of ordinary skill in the art at the time of the alleged inventions would understand certain terms in claims asserted by Elm 3DS Innovations, LLC ("Elm") from the following patents: U.S. Patent Nos. 7,193,239 (the "'239 patent"), 7,504,732 (the "'732 patent"), 8,035,233 (the "'233 patent"), 8,410,617 (the "'617 patent"), 8,629,542 (the "'542 patent"), 8,653,672 (the "'672 patent"), 8,791,581 (the "'581 patent"), 8,796,862 (the "'862 patent"), 8,824,159 (the "'159 patent"), 8,841,778 (the "'778 patent"), 8,907,499 (the "'499 patent"), 8,928,119 (the "'119 patent"), and 8,933,570 (the "'570 patent") (collectively, the "Asserted Patents").

3. I am being compensated at a rate of $525 per hour for my work. My compensation is in not contingent on my opinions, testimony, or the outcome of this litigation.

4. I am competent to testify to the matters stated in this Declaration and have personal knowledge of the facts and statements herein. Each of the statements is true and correct.

II. BASIS FOR OPINION

A. Qualifications

5. Below is an overview of my educational background, work history and other relevant qualifications. A more detailed account of my qualifications is included in my curriculum vitae, attached as Exhibit A to this declaration.

6. In 1996, I received a Bachelor of Science in Mechanical Engineering and a Bachelor of Science in Materials Science and Mineral Engineering from the University of California, Berkeley. In 2000, I received a Ph.D. in Electronic Materials from Massachusetts Institute of Technology. I am currently a licensed Professional Electrical Engineer and a licensed Professional Mechanical Engineer.

7. I am currently Group Vice President and Principal Engineer at Exponent, Inc. My work focuses on failure analysis of electrical and mechanical systems, metallurgy, and the mechanical and electrical properties of materials. I provide electrical materials consulting services to a variety of industries, which includes investigation of various consumer and industrial products. These investigations have involved understanding and analysis of complex electrical and electronic systems, risk assessment, environmental effects, and materials defects. I have conducted multiple investigations related to the mechanical stresses in thin films, and the various measurement techniques which are involved with such stresses. I have also conducted investigations into a wide range of flexible electronics and integrated circuits in general.

8. Prior to working at Exponent, I worked as a Senior Engineer at Mide Technology Corporation where I developed novel technologies using 'smart' materials including piezoelectrics and shape memory alloys.

9. From 2006-2015, I held an appointment as a Consulting Assistant Professor in the School of Engineering at Stanford University where I taught the course *AA252 Techniques of Failure Analysis*. I am also a member of the American Society of Mechanical Engineers, the American Society for Metals, the Institute of Electrical and Electronics Engineers, and a Member of the Advisory Board of the Department of Materials Science and Engineering at the University of California at Berkeley. I also have a position as a trustee at the Lycée Francais de San

Francisco.

B. Materials Considered

10. In forming my opinions for this Declaration, I have relied on my background and qualifications. My opinions are further based on my review of the Asserted Patents, their prosecution histories and the prosecution histories of related patents, the parties' proposed constructions, and the extrinsic evidence cited in this declaration.

III. LEGAL STANDARDS

11. I am not an expert on patent law and have been instructed on certain aspects of patent law by counsel.

12. I understand that the claims of the patent define the limits of the patentees' exclusive rights. In order to determine the scope of the claimed invention, courts typically construe (or define) claim terms, the meaning of which the parties dispute.

13. I understand that the words of a claim are generally given the ordinary and customary meaning that the term would have to a person of ordinary skill in the art at the time of the alleged invention (*i.e.*, the effective filing date of the patent).

14. I understand that patent claims are construed in light of the claim language, the patent specification (including the drawings), and the prosecution history (including the references cited during the prosecution of the patent and the prosecution histories of related patents). I understand this type of evidence is "intrinsic" evidence.

15. I also understand that the Court may consider "extrinsic" evidence to ensure that a claim construction is not inconsistent with clearly expressed and widely held understanding in the pertinent technical field, which is especially the case for technical terms. I have been informed that extrinsic evidence may be in the form of expert and/or inventor testimony,

dictionaries, textbooks, technical treatises, and technical articles.

16. I understand that a person of ordinary skill in the art is deemed to read the claim terms not only in the context of the particular claim in which it appears, but also in the context of the entire patent, including the specification and prosecution history. I understand that in the specification, a patentee may also define his own terms, give a claim term a different meaning than it would otherwise possess, or disclaim or disavow claim scope. A claim term is generally presumed to possess its ordinary meaning. This presumption, however, does not arise when the patentee acts as his own lexicographer by explicitly defining or redefining a claim term. This presumption can also be overcome by statements, in the specification or prosecution history of the patent, of clear disclaimer or disavowal of a particular claim scope. Thus, any explicit definitions of terms or intentional disclaimers or disavowals of claim scope in the specification or prosecution history must be considered in determining the meaning of a claim term.

17. I understand that differences among claims can also be a useful guide in understanding the meaning of particular claim terms. For example, I am familiar with the doctrine of “claim differentiation” where the presence of dependent claims that add a particular limitation to an independent claim gives rise to a presumption that the limitation in question is not present in the independent claim. However, I understand that “claim differentiation” is not a rigid rule and it cannot overcome a contrary construction dictated by the written description or prosecution history.

18. I understand that patent claims must particularly point out and distinctly claim the subject matter which the inventors regard as the invention. I understand that a claim term is indefinite if the claim, when interpreted in light of the specification and the prosecution history, fails to inform those skilled in the art about the scope of the claimed invention with reasonable

certainty. For example, a term of degree may be indefinite if the patent fails to provide some standard for determining or measuring the claimed degree.

IV. LEVEL OF ORDINARY SKILL IN THE ART

19. In this Declaration and in forming my opinions, I have applied the following definition of a person of ordinary skill in the art at the time of invention:

> A person having at least a bachelor-level degree in electrical engineering, materials science, physics, or equivalent thereof, and at least 3–5 years of experience of experience in the relevant field, e.g., semiconductor processing.

20. I understand that the parties and the Patent Trial and Appeal Board applied the above level of ordinary skill in the art during *Inter Partes* Reviews relating to the Asserted Patents.

V. OVERVIEW OF THE ASSERTED PATENTS

A. Asserted Claims

21. I understand that Elm has asserted the following claims against Defendants in this litigation.[1]

Asserted Patent	Asserted Claims
U.S. Pat. No. 7,193,239	10, 11, 12, 18, 19, 20, 60, 61, 62, 63, 67, 70, 71, 72, 73, 77
U.S. Pat. No. 7,474,004	20, 21, 22, 23
U.S. Pat. No. 7,504,732	10, [11], 13, 14
U.S. Pat. No. 8,410,617	51
U.S. Pat. No. 8,629,542	1, 2, 3, 30, 31, 33, 40, 41, 44
U.S. Pat. No. 8,653,672	17, 22, 95, 129, [130], 131, 132, 145, 146, 152
U.S. Pat. No. 8,796,862	34, 36, 135, 136, 137, 138, 147
U.S. Pat. No. 8,841,778	32, 44, 46, 54

[1] Brackets indicate a claim asserted only against Samsung Defendants and parentheses indicate a claim asserted only against SK hynix Defendants and Micron Defendants

U.S. Pat. No. 8,907,499	12, 13, 24, [36], [37], 38, (49), 53, 83, 86, 87, 132
U.S. Pat. No. 8,928,119	18, (33)
U.S. Pat. No. 8,933,570	58, 60, [61], 67
U.S. Pat. No. 8,791,581	(1), 12, 36, 54, 78, 116, 136
U.S. Pat. No. 8,035,233	34

22. Below, I have reproduced certain representative claims from certain Asserted Patents that include exemplary disputed terms relating to the "low stress" terms to be construed by the Court:

23. Claims 1[2], 10, and 11of the '239 patent:

1. Circuitry comprising: a plurality of monolithic substrates having integrated circuits formed thereon and stacked in layers such that each layer comprises only one of the substrates, wherein at least one of the plurality of substrates is a substantially flexible substrate, and wherein a major portion of the monolithic substrate is removed; and between adjacent substrates, a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof.

10. The apparatus of claim 1, wherein the circuitry is formed with a low stress dielectric.

11. The apparatus of claim 10, wherein the low stress dielectric is at least one of a silicon dioxide dielectric, an oxide of silicon dielectric, and caused to have stress of about $5x10^8$ dynes/cm^2 or less.

24. Claim 17 of the '672 patent:

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[2] Claim 1 is not asserted in this case, but is excerpted here because other claims asserted in this case (*e.g.*, claims 10, 11) depend from claim 1.

17. An integrated circuit structure comprising: a first substrate having topside and bottomside surfaces, wherein the topside surface of the first substrate supports interconnect contacts; a substantially flexible semiconductor second substrate having topside and bottom-side surfaces, wherein at least one of the topside surface and the bottom-side surface of the second substrate supports interconnect contacts, and wherein the bottom-side surface of the second substrate is formed by removing semiconductor material from the second substrate and is smoothed or polished after removal of the semiconductor material; and conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate; wherein the first substrate and the second substrate overlap fully or partially in a stacked relationship; and wherein at least one of:

i.) the first and second substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal; and

ii.) the integrated circuit structure further comprises a low-stress silicon-based dielectric material having a stress of 5×108 dynes/cm2 tensile or less.

B. Overview of the Asserted Patents[3]

25. All of the Asserted Patents share a common specification and claim priority to U.S. Patent Application No. 08/835,190. Each Asserted Patent lists Glenn J Leedy as inventor. *See, e.g.*, ’239 patent ad Cover. The Asserted Patents generally relate to 3D stacked integrated

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[3] All of the Asserted Patents are related, claim priority to a common application, and share a substantially similar specification. For convenience, I cite to ’239 patent specification, but this declaration also incorporates by reference all corresponding portions of the patent specification in each of the other Asserted Patents.

circuits, and many claims of the Asserted Patents include limitations requiring ‘low stress’ dielectric material or layers. *See, e.g.*, Claims 1, 10, and 11 of the ’239 patent and claim 17 of the ’672 patent. The shared specification of the Asserted Patents only mentions ‘stress’ in two places:

26. First, the specification states ‘each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 µm and typically less than 10 µm thickness.’ ’239 patent at 4:35-38.

27. Second, the specification states: ‘The thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication. Such low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695 of the present inventor, incorporated herein by reference. The use of dielectrics with conventional stress levels could be used in the assembly of a 3DS DRAM circuit, however, if more than a few layers comprise the stacked assembly, each layer in the assembly will have to be stress balanced so that the net stress of the deposited films of a layer is less than 5×10^8 dynes/cm^2. The use of intrinsically low stress deposited films is the preferred method of fabrication versus the use of the method where the stress of individually deposited films are not equal but are deposited to create a net balanced lower stress.’ *Id.* at 8:66-9:16.

28. U.S. Patent No. 5,354,695 (the ‘’695 patent’), which is incorporated by reference in the specification of the Asserted Patents, generally relates to the fabrication of integrated circuits on tensile low stress dielectric membranes. *See, e.g.* ’695 patent at 1:53-62.

VI. OPINIONS ON CLAIM CONSTRUCTION

A. "low stress dielectric"

29. The parties' proposed constructions for 'low stress dielectric' / 'low stress dielectric layer' / 'low stress dielectric material' / 'low-stress … dielectric material' / 'low-stress … dielectric layer' / 'low stress … dielectric layer' are in the table below.

Plaintiff's Proposal	SK hynix's Proposal
a dielectric having a stress of less than 8 x 10^8 dynes/cm^2	Indefinite

30. The term 'low stress' as applied to a 'dielectric layer', or a 'dielectric material' did not have a commonly accepted meaning to persons of ordinary skill in the art around the time of the alleged invention in the Asserted Patents. Several factors prevent a person of ordinary skill in the art from determining the meaning of 'low stress' with reasonable certainty in the context of the Asserted Claims. In brief, these factors relate to the following: first, stress is a term of degree, and describing a stress as 'low' is not sufficient to determine the threshold between 'low stress' and 'non-low stress' dielectric layers or material; second, stress is not a single mathematical value in a complex three dimensional object but must be described as a tensor field, so reducing stress to a single value requires specification of several mathematical operations; and third, there was no standard procedure recognized for measuring the stress that would be applicable to measurements of dielectric layers or material with a complex three-dimensional shape like the one described in the Asserted Patents.

31. First, stress is a term of degree, and can vary over a wide range of values depending on the source of the stress, the mechanical properties of the material or materials involved, the processing history of those materials, and other factors such as external loads. Depending on the context and use-case for dielectric films or materials, a wide range of values

have been referred to as ‘low-stress’, and persons of ordinary skill in the art would not know with sufficient precision what specific value of stress in a dielectric layer or material would be required to qualify as ‘low’ without a detailed specification.

32. A review of a number of publications in the topic area of thin-film dielectrics for use in integrated circuitry reveals a large number of apparent stress states being referred to as ‘low’ or in some cases ‘ultra-low’. Stress values have been called ‘low’ between $6*10^9$ dynes/cm^2 and $2*10^7$ dynes/cm^2, depending on the material, application, and requirements in each of the publications. This range includes values of stress varying by a factor of 300 between the lowest stress referred to as ‘low’ and the highest stress referred to as ‘low’. This large disparity in numerical values referred to as ‘low’ is due to the fact that stress is a term of degree without a commonly accepted cutoff for ‘low stress.’ Further, in each publication cited below, the stress in the described film or material was ‘low’ relative to some basis, for instance other films commonly used in industry and academia or compared to previously achieved stress values for a given material system. For this reason, referring to a stress in a dielectric film or layer as ‘low’ is not sufficient to define the boundaries of what is and is not covered by claims that include ‘low stress’ with reasonable certainty to a person of ordinary skill in the art. A table below provides a series of references to stress in dielectrics.

Quote	**Stress Value [MPa]**	**Stress Value [dyn/cm^2]**	**Reference**
"Cheng and co-workers [11] observed that the residual stress varies with both DCS/NH3 ratio and temperature but that the dependence on gas flow is secondary to the effect of temperature. They employed temperatures on the order of 900 °C in their experiments and achieved **LSN*** with residual stresses less than 10 MPa. The authors report that they altered the deposition system in order to achieve the	<10	<1*10^8	J.M. Olson / Materials Science in Semiconductor Processing 5 (2002) 51–60

high temperatures necessary for the deposition of these films. While they disclose no details regarding the design of the apparatus, they observed that the challenge in achieving LSN by LPCVD decreased with increasing T. At temperatures exceeding 900 °C, they found that films with very low residual stress could be deposited using a much broader range of gas ratios." ***LSN is defined in the paper as 'Low-stress nitride'**			
"In this study, **ultra-low stress nitride** was deposited at a DCS/NH3 ratios of 4:1 and higher temperatures than traditionally utilized for Si3N4 deposition. Residual stress of 0±10 MPa was achieved at index of refraction of 2.25."	0±10	0±10^8	J.M. Olson / Materials Science in Semiconductor Processing 5 (2002) 51–60
"Due to the compensation on the nitride by its top oxide, an **ultra-low residual** less than 10 MPa can be obtained with proper oxidation scheme."	<10	<1*10^8	B. C. S. Chou, Jin-Shown Shie and Chung-Nan Chen, "Fabrication of low-stress dielectric thin-film for microsensor applications," in IEEE Electron Device Letters, vol. 18, no. 12, pp. 599-601, Dec. 1997.
"The silicon nitride optical test films were prepared by a LP-CVD (Low-Pressure Chemical-Vapor-Deposition) process optimized for **low tensile stress** and refractive index [8]. The 5:1 SiH2Cl2/ NH3 gas ratio employed results in a tensile stress < 100 MPa and optical index greater than 2 [9]."	<100	<1*10^9	Giuseppe Cataldo, James A. Beall, Hsiao-Mei Cho, Brendan McAndrew, Michael D. Niemack, and Edward J. Wollack, "Infrared dielectric properties of low-stress silicon nitride," Opt. Lett. 37, 4200-4202 (2012)
"Diamondlike amorphous C films with exceptionally **low stress** (<10^8 dyn/cm2) have been prepared by a hybrid process involving bias sputtering with ultrapure C electrodes and plasma decomposition of normal butane."	<10	<1*10^8	Joseph Zelez, "Low-stress diamondlike carbon films," Journal of Vacuum Science & Technology A 1:2, 305-307 (1983)

"The stress is very consistent at **low compressive stress** 0.29 X 10^9 dyn/cm^2. This very **low stress level** may be due to combined results of intrinsic tensile stress and the compressive stress exerted by the metal film underneath."		29	2.9*10^8	Y. S. Chen and Homi Fatemi, "Stress measurements on multilevel thin film dielectric layers used in Si integrated circuits," Journal of Vacuum Science & Technology A 4:3, 645-649 (1986)
"Many dielectric materials traditionally used as stress buffers, such as benzocyclobutene (BCB) or polyimide (PI), may still possess unacceptably high residual stress values for these next generation devices. A new class of silicone materials has recently been introduced, which has considerably **lower residual tensile stress** [2]."	-2-8		-2-8*10^7	H. Meynen, M. Vanden Bulcke, M. Gonzalez, B. Harkness, G. Gardner, J. Sudbury-Holtschlag, B. Vandevelde, C. Winters, E. Beyne, "Ultra low stress and low temperature patternable silicone materials for applications within microelectronics," Microelectronic Engineering, Volume 76, Issues 1–4, 2004, Pages 212-218,
"The residual stress σ decreases with an increase of the temperature or a decrease of the total pressure and **low stress** (≈600 MPa) Si3N4 films have been obtained for the highest temperature (775 °C) and the lowest total pressure (27 Pa)."	≈600		6*10^9	P. Temple-Boyer, C. Rossi, E. Saint Etienne, E. Scheid. "Residaul stress in low pressure chemical vapor depoistion SiNx films deposited from Silane and Ammonia". J. Vac. Sci. Technol. A 16(4) 1998. 2003-2007.

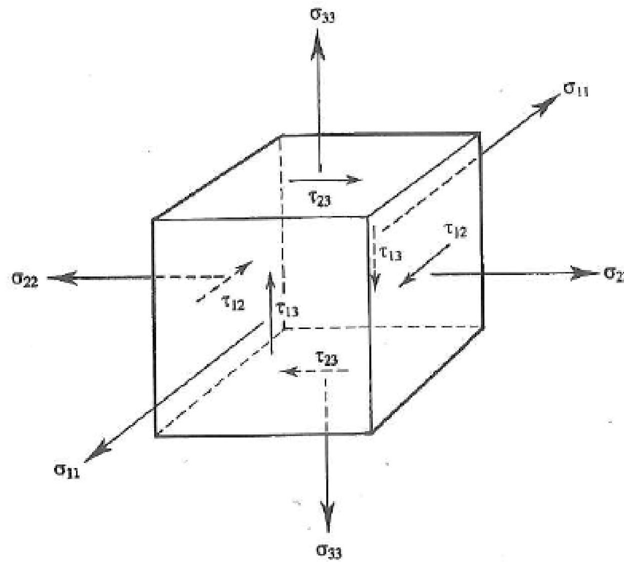
"The aim of our study is deposition of high quality SiN film with low hydrogen content, **low stress**, low damage and stoichlometric composition below 300 °C by the photo-assisted plasma CVD (PAP-CVD) method."	50 - 300	0.5 - 3.0 * 10^9	N. Suzuki, T. Yoshikawa, K. Masu, K. Tsubouchi, N. Mikoshiba. "Silicon Nitride Films with Low Hydrogen Content, Low Stress, Low Damage, and Stoichiometric Composition by Photo-Assisted Plasma CVD". Japanese Journal of Applied Physics, Volume 28, No 12, 1989, 2316-2319.

33. **Table.** Various references to 'low,' 'lower' or 'ultra-low' stress found in literature references related to dielectric materials. Emphasis on 'low stress' terms has been added for clarity.

34. The second factor complicating interpretation of the phrase 'low stress' is that the stress of a dielectric layer or material is not well represented by a single number in a complex three-dimensional object such as the structures described in the Asserted Patents. A full description of the stress state of an object requires the description of six independent values including three principle stress components and three shear stress components. These values are combined into a mathematical object called a tensor. A good description of this behavior is found in the text by Courtney on page 58. In the series of equations labeled 2.15, it can be seen that there are six independent equations required to describe the six independent stress components. In order to reference the 'stress' as a scalar quantity, it is necessary to specify which of the six stress components is referred to, or to cite a mathematical formula to calculate a single value from the tensor. An example would be to calculate the *Von-Mises* stress which can be calculated from the three principle stress components of the stress tensor:

$$\sigma_{Von\ Mises} = \frac{1}{\sqrt{2}}[(\sigma_1 - \sigma_2)^2 + (\sigma_1 - \sigma_3)^2 + (\sigma_2 - \sigma_3)^2]$$

(T. H. Courtney, Mechanical behavior of materials. Long Grove, IL: Waveland Press, 2005, pp. 17-24).



35. **Figure** Illustration of the six components of the stress tensor, including three normal components (σ_1, σ_2, and σ_3) and three shear components (τ_{12}, $_{23}$, and τ_{13}). (T. H. Courtney, Mechanical behavior of materials. Long Grove, IL: Waveland Press, 2005, pp. 57)

36. Furthermore, this stress tensor will not be uniform in an object with micro-patterned structures, such as the dielectric layers described in the Asserted Patents, but will vary in a complex way in all three spatial directions, so the stress is best described as a field, a value that varies depending on three spatial coordinates. Reducing this complex three-dimensional tensor field to a single scalar value requires a specific mathematical operation, such as taking the maximum value, or the average value. The stress in a thin film with discontinuities such as edges and corners will vary significantly in the x and y dimensions, as illustrated qualitatively on page 6 of the Hutchinson text in figure 2.2. John W. Hutchinson, "Stresses and Failure Modes in Thin Films and Multilayers," Technical University of Denmark, Notes for a DCAMM Course, October 1996. We know the stresses will vary, however as stated by Hutchinson: 'Closed form

results for stresses near the edges or corners of the films are not available', meaning that they cannot be calculated in a simple way based on the average stresses.

37. A third difficulty that would be apparent to persons of ordinary skill in the art near the time of the alleged inventions claimed in the Asserted Patents is a technical challenge related to the measurement of dielectric material or film stresses in integrated circuits. The internal stresses of a body in general, including dielectric materials and dielectric layers, can be difficult and complicated to measure. There exist a number of techniques used for estimating or approximating various components of the stress tensor and at certain locations in integrated circuits and during integrated circuit processing, but each of these techniques includes a number of limitations that can preclude their reliable application in certain situations. After a careful review of the technical literature, it is my opinion that there currently does not exist, and at the time of the alleged inventions claimed in the Asserted Patents did not exist, an accepted method to measure the stresses of a dielectric material or layer incorporated into a three-dimensional structures like those described in the Asserted Patents.

38. X-ray diffraction and wafer curvature measurements are common techniques that a person of ordinary skills in the art would be aware of at the time the Asserted Patents were filed to measure stress in thin layers, including in some cases dielectric layers. It is my opinion that neither of these techniques could be used to measure stresses in a dielectric layer in a three-dimensional structure like those described in the Asserted Patents.

39. At the time of the inventions in the Asserted Patents, and afterwards, the 'typical commercial equipment available to determine stress' all 'measure curvature or shape.' (Krisna Seshan, Handbook of Thin Film Deposition Processes and Techniques (Second Edition), William Andrew Publishing, 2001, Pages 266-267). Additionally, "several techniques relying on

differing technologies have been developed to measure film stress, but all basically measure the average radius of curvature of a wafer before and after the film deposition" *Id.* While this was the most common method of thin-film stress measurements at the time of the aforementioned alleged inventions, it is only applicable to films applied to smooth wafers which are measured for curvature before and after film deposition, not to dielectric layers incorporated into a three-dimensional structure. The key difference between samples that would be compatible with the curvature method and three-dimensional integrated circuits in the Asserted Patents is the presence of a high density of internal edges, as well as the fact that the dielectric will not cover the entire surface area but only some fraction of it. The internal edges would produce stress concentration points as well as boundaries for the tensile stress in the layer. Fractional coverage means that the material around dielectric in a stress state will curve to accommodate that stress and areas which do not have the dielectric will not curve. Over a full structure, a reduction only in the amount of area the dielectric coats will reduce the total curvature, appearing to the curvature method as though the stress is decreasing, though this would not be the case.

40. A description of the limitation pertaining to edges is found in the Hutchinson article, where the method of thermal stress determination using curvature presented states that the formulas apply only to 'stresses which develop in the *interior of the film* away from the edges' (Hutchinson 5). In this article, the edges are understood to be at the extremities of the part, but any physical discontinuity, such as a hole in the dielectric film formed around a metal via such as those described in the Asserted Patents, will present a similar limitation. On stress near the edges, Hutchinson writes on page 7 that 'Closed form results for stresses near the edges or corners of the film are not available,' meaning that simple formulas, such as Stoney's equation, do not apply in those locations. An integrated circuit will have many internal edges, as

is apparent from the schematics in the Asserted Patents, so there will likely be no locations that are truly 'away from the edges' in the sense described by Hutchinson.

41. The curvature method also cannot provide information on the variation in space of a stress, which is of critical importance in three-dimensional objects such as those described in the Asserted Patents. Gunda on page 133 clearly states that 'Curvature methods based on Stoney's formula provide only average stresses and there are only a few methods that can measure full-field stresses.' Manideep Gunda *et al*, 'Review of Mechanical Characterization Techniques for Thin Films Used in Flexible Electronics,' Critical Reviews in Solid State and Materials Sciences, Vol. 42, No. 2, 129-159 (2017). Full-field stresses here in the context of the paper include stresses that arise due to complex shapes and discontinuities present in three-dimensional objects, and this level of detail is required to understand the stresses in dielectric layers in integrated circuits.

42. X-ray techniques cannot be used to determine stress of amorphous materials, as they 'use the distance between atomic planes of a crystalline specimen as an internal strain gauge.' (Mary F. Doerner & William D. Nix (1988), Stresses and deformation processes in thin films on substrates, Critical Reviews in Solid State and Materials Sciences, 14:3, 225-268). Silicon nitride and silicon oxide thin films used as dielectrics are typically amorphous as deposited, meaning they lack a regular and periodic arrangement of their atoms as would be found in crystalline materials. Therefore, since thin film dielectric silicon oxide and silicon nitride lack regularly spaced atomic planes, the x-ray diffraction technique cannot be used in a straightforward way to study stresses in these materials.

43. The difficulty in measuring thin film stress is well illustrated by the article by Uchida *et al*. This is an article from near the time of the alleged inventions in the Asserted

Patents, attempting to develop an x-ray technique for the measurement of film stresses in a polycrystalline material. The authors considered their effort a success, stating in the abstract: “Stress values measured by modified $\sin^2\Psi$ method may thus have the precision required for actual application.” H. Uchida *et al*., “Measurement Technique for the Evaluation of Residual Stress in Epitaxial Thin Film by Asymmetric X-Ray Diffraction” Journal of the Ceramic Society of Japan 107 [7] 606-610 (1999). Nonetheless, when compared to the most common stress measurement method, wafer curvature and Stoney’s equation, their results differed by ~1 GPa, or 1×10^{10} dynes/cm^2. This relative error between the different measurement techniques is more than an order of magnitude greater than of any of the stress values discussed in the Asserted Patents. The article attributed this difference to some of the complexities raised above, where precisely the stress value is measured for each technique and the differing influence of stress gradients on each measurement. These measurements were also conducted on a simple sample, a flat uniform thickness film on a flat substrate, and the introduction of additional geometry such as that described in the structures in the Asserted Patents would introduce more stress gradients, and thus more difference between the results from each measurement technique.

44. Moreover, the common specification of the Asserted Patents never describes which method should be used to approximate stress in dielectric layers of materials - curvature, X-ray diffraction, or other. Even U.S. Pat. No. 5,354,695, which is incorporated by reference in the Asserted Patents’ specification and discusses ‘low stress dielectrics’ at length, fails to specify how the stress of dielectric materials and layers should be approximated.

45. The ’695 patent has a more detailed description in the patent language relating to ‘low-stress’ materials, and offers specific equipment and deposition recipes which are stated to produce the materials in question. Specifically, it states that ‘low stress is defined relative to the

silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than $8x10^8$ dynes/cm^2, (preferably 1x107 dynes/cm^2) in tension'. '695 patent at 11:33-37. Based on the text in this paragraph, this statement should not apply to the class of 'low-stress' dielectrics claimed in the Asserted Patents because it is limited to films made by a specific process in a specific deposition system. Furthermore, the same paragraph also states at lines 37-39 that 'Acceptable surface stress levels of different dielectrics made on various equipment may vary widely', which appears to specifically exclude using this particular definition of 'low-stress' as a general one. In the general case, dielectrics can be deposited with a wide variety of equipment and thus would be expected, according to the '695 patent, to experience a wide variety of stresses. Stress that is low enough to be 'acceptable' will vary, so a person of ordinary skill in the art would understand this paragraph to warn against using the proposed stress levels as a general guide.

46. Even if an alternative construction in the form of 'a stress of less than $8x10^8$ dynes/cm^2' (or another specific value) were offered, it would remain indefinite. Although the term now states a degree for the stress, it still fails to specify a mathematical procedure to reduce the three-dimensional tensor field which is required to fully describe the stress in a complex three-dimensional object such as that described in the Asserted Patents. It also does not offer any method to measure or determine this stress, and as previously discussed such a method was not available to a person of ordinary skill in the art that can be applied to measure the stresses in dielectric layers incorporated into the structures described in the Asserted Patents. Furthermore, neither the '695 patent nor the Elm's proposed construction specify which kind of stress is of concern. There are a number of potential varieties of stress, as outlined in the Hutchinson article, including *intrinsic*, *thermal*, *mechanical* and *residual*. *See* Hutchinson at §1.1.

47. While the claims of the Asserted Patents include the indefinite term 'low stress dielectric,' they do not cover stress-balancing, which is another method that can be used to aid the fabrication of thin films like those discussed in the Asserted Patents. The term stress-balancing does not appear in any of the claims of the Asserted Patents, however there is a brief mention of it in the specification of the '239 patent at 9:7-12: 'The use of dielectrics with conventional stress levels could be used in the assembly of a 3DS DRAM circuit, however, if more than a few layers comprise the stacked assembly, each layer in the assembly will have to be stress balanced so that the net stress of the deposited films of a layer is less than $5x10^8$ dynes/cm^2.' This is clearly stated to differentiate stress-balancing from the 'low stress' dielectrics in the claims of the Asserted Patents, because it is directly contrasted with the Asserted Patents' preferred method, namely 'the use of intrinsically low stress deposited films.' '239 patent at 9:12-16.

48. From a technical perspective the purpose of stress balancing is to reduce the stress on an assembly or 'stack' of thin films by compensating for stress in one layer by the addition of another layer with opposing stress. While this method can reduce the final bending of the layer stack, it often does not reduce the stress in the individual layers. The stress of a given layer can be either higher or lower depending on the position of the layer in the film stack and the stresses in the other layers. *See* Hutchinson article at equation 2.8-2.14. In contrast the claims in the Asserted Patents focus only on stresses in the dielectric layers, and always point out that this stress should be low. Since stress balancing does not reference the dielectric layers in particular, and can produce either an increase or decrease in the stress in these layers, the claims in the Asserted Patents cannot include stress balancing.

49. The prosecution history also makes clear that the patentee was aware of this

contrast, and relied on it to overcome a rejection of 'double patenting' between the related '237 and '386 patent applications. In order to overcome this rejection, a number of changes to the claims in the '237 patent were made in amendments filed on February 3, 2016. *See* '237 Application, 02-03-2016 Response to Office Action at Amendments; '386 Application, 02-03-2016 Response to Office Action at 85 ("Applicant has amended the present Application and 12/405,237 by claiming separate features of Applicant's invention in the separate applications.")

50. For example, claim 1 of the of '237 patent application was amended to replace language reading:

> 'that is substantially flexible comprises a low stress silicon based **dielectric layer** formed above the thinned, substantially flexible monocrystalline semiconductor substrate and **having a stress less than 5 x 10^8 dynes/cm^2 tensile**'

with language reading:

> 'further comprises a stack of depositions formed above the thinned, substantially flexible semiconductor substrate, the **stack of depositions** comprising dielectric material deposition and conductive material depositions and **being stress balanced** . . .'.

'237 Application, 02-03-2016 Response to Office Action, Amendments to Claim 1 (emphasis added). The important change here is the substitution of a 'dielectric layer … having a stress less than 5 x 10^8 dynes /cm^2 tensile" for "the stack of depositions … being stress balanced ….' A number of similar amendments were made throughout the claims of the '237 patent application. The claims of the '386 patent application, by contrast, were not amended to include any reference to stress balancing. '386 Application, 02-03-2016 Response to Office Action. This indicates the patentee intended to change the meaning of the '237 patent application claim through this 'stress balancing' substitution, demonstrating that they knew and agreed to the idea

that stress balancing is separate and distinct from dielectric layers or material with stress below a certain value.

51. Although the term ‘low stress’ is indefinite for the reasons outlined above, the prosecution history and specification of the ’695 patent indicate that, whatever the meaning of ‘low stress,’ the scope of this term excludes compressive stresses. First, the ’695 patent (incorporated by reference in the specification of the Asserted Patents) specifies that the stress of the membrane and dielectric films must be tensile:

> “The MDI process requires that the semiconductor membrane forming process (thinning process) produce a highly uniform membrane typically less than 2 in thick and that the surface tension of the semiconductor membrane be in low tensile stress. If the membrane is not in tensile stress, but in compressive stress, surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free-standing membrane.”

’695 patent at 5:62-6:5; *see also* ’695 patent at 6:21-24 (“The MDI process for forming a dielectric membrane requires that the dielectric material be deposited in net surface tensile stress …”). This makes clear that for the alleged invention, the total stresses and stresses in the dielectric layers are tensile. This is further supported by the fact whenever any further information about the stress in the ‘low stress dielectrics’ is mentioned, the word used is ‘tensile.’ The word ‘compressive’ does not appear in the Asserted Patents’ specification or claims, except by way of the incorporation by reference of the ’695 patent, where it is clear the patentee’s alleged invention cannot be used with compressive stress dielectrics.

52. In the ’499 patent prosecution history, the patentee also acknowledges this differentiation between compressive stresses and tensile stresses in the ’695 patent,

distinguishing from prior art where the ‘dielectric is a low *compressive* stress dielectric’ (emphasis in original) and stating that ‘support for low *tensile* stress (as opposed to compressive stress) is found in col. 6 line 62 to col. 6 line 5 and elsewhere of U.S. patent 5,354,695’. ’499 Patent File History, 6-20-13 Response to Office Action (emphasis in original). Thus, whatever the scope of ‘low stress’ in the claims of the Asserted Patents, it does not include compressive stress.

B. ‘5×10^8 dynes/cm^2 or less’

53. The parties’ proposed constructions for ‘have stress of about 5×10^8 dynes/cm^2 or less’ / ‘have a stress of about 5×10^8 dynes cm^2 or less’ / ‘having a stress of $5x10^8$ dynes/cm^2 or less’ / ‘having a stress of $5x10^8$ dynes/cm^2 tensile or less’ / ‘[have] a stress of about 5×10^8 dynes/cm^2 tensile or less’ / ‘having[/has] a stress of less than 5×10^8 dynes/cm^2 tensile’ / ‘a stress of about 5×10^8 dynes/cm^2 or less’ / ‘with a tensile stress of less than 5×10^8 dynes/cm^2’ / ‘with a stress of less than 5×10^8 dynes/cm^2 tensile’ / ‘has[/having] a tensile stress of less than 5×10^8 dynes/cm^2’ are in the table below.

Plaintiff’s Proposal	SK hynix’s Proposal
No construction necessary	Indefinite

54. The addition of a specific value for the stress does not resolve all of the issues discussed above that render the term ‘low-stress’ indefinite. Stress is a term of degree, and here a degree is specified, namely $5x10^8$ dynes/cm^2. A person of ordinary skill in the art would still not be able to determine whether specific dielectric layers or materials would meet this description in a complex integrated device, such as those described in the Asserted Patents, and for this reason the term remains indefinite. This inability arises due to four issues, related to those raised in discussion of the ‘low-stress term’. First, as discussed for the ‘low-stress’ term, stress is not a

single value, but in the general case must be defined by 6 independent stress tensor components and specific tensor components of interest are not fully specified in the claims or in the Asserted Patents. Second, while several of the claims do specify that stress must be 'tensile', in an integrated circuit structure, unlike a flat uniform film on a blank wafer, the stress is expected to vary in all three spatial dimensions within the film. Some mathematical operation to produce a single value from the field of stress values is required to make this term definite. Third, as discussed previously, the terms do not specify which kind of stress is of concern, such as total, intrinsic, thermal, mechanical or residual. Finally, as was previously discussed in the 'low-stress' section, a person of ordinary skill would not know how to measure the stress in the dielectric layers or thin films for the kinds of structures described in the Asserted Patents, so would be unable to determine if a given film would qualify for the term or not.

55. The mathematical description of stress in a solid was discussed previously in the 'low-stress' section, but in brief for a thin film in a complex three-dimensional structure, such as an integrated circuit, the stress cannot be well represented by a single value. The description of the stress in the Asserted Patents, as a 'stress of 5×10^8 dynes/cm^2 or less' does not provide enough information for persons of ordinary skill in the art to understand what specific component stress in which locations are to be measured. Considerations relating to why more information is required are covered in the discussion of the 'low-stress' term.

56. As was also discussed in the section on 'low-stress,' the stress condition will not be uniform in an object with micro-patterned structures such as an integrated circuit, but will vary in a complex way in all three spatial directions, so the stress is best described as a field, a value that varies depending on three spatial coordinates. In order to reduce this complex three-dimensional tensor field to a single value that can be directly compared to the proposed stress

value of 5×10^8 dynes/cm^2 requires a specific mathematical operation, such as taking the maximum value or the average value. Typically, a specific component of the tensor will also be referred to. The terms in question still fail to specify whether the stress in question is the average stress, or the peak stress, or the stress at a specific location within the integrated circuit.

57. The terms naming a specific stress that the dielectrics should fall below, namely 5×10^8 dynes/cm^2 are indefinite because the specification of the Asserted Patents does not describe a method to determine this stress in the dielectric layers in the sort of devices described by the Asserted Patents, and no such technique was widely recognized as being capable of performing this measurement at the time of the invention. A person of ordinary skill in the art would not be able to determine for any given dielectric layer deposited in an integrated circuit if it would meet this requirement or not. Various methods available for approximating and estimating the stress in thin films are discussed extensively in the discussion of the 'low-stress' term. The same considerations apply here to the proposal of a specific stress.

VII. RESERVATION OF RIGHTS

58. The opinions expressed in this Declaration are based on the parties' contentions and my review of the evidence produced at this stage of litigation. My opinions are subject to change based on any additional opinions that Elm may present and information I may receive in the future. With this in mind, based on the analysis I have conducted and for the reasons set forth above, I have reached the conclusions and opinions in this Declaration.

59. If I am called to testify, in connection with my anticipated testimony in this litigation, I may use as exhibits various documents produced in this case that refer or relate to the matters discussed in this Declaration. I may also rely on visual aids and may rely on analogies concerning elements of the patents discussed above, the accused products, the references cited in

this Declaration, or any related technologies. In addition, I may create or assist in the creation of certain demonstrative evidence to assist me in testifying, and I reserve the right to do so.

60. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: January 18, 2019

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Dr. Steven Murray

EXHIBIT D

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; AND MICRON CONSUMER PRODUCTS GROUP, INC., DEFENDANTS.	)	C.A. NO. 14-01431-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG ELECTRONICS AMERICA, INC., AND SAMSUNG AUSTIN SEMICONDUCTOR, LLC, DEFENDANTS.	)	C.A. NO. 14-01430-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. SK HYNIX INC., SK HYNIX AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC., AND SK HYNIX MEMORY SOLUTIONS INC., DEFENDANTS.	)	C.A. NO. 14-01432-LPS-CJB JURY TRIAL DEMANDED

REBUTTAL DECLARATION OF DR. STEVEN MURRAY
REGARDING CLAIM CONSTRUCTION

I, Dr. Steven Murray, declare as follows:

I. INTRODUCTION

1. I have been retained by K&L Gates on behalf of the Defendants in C.A. NO. 14-01432-LPS-CJB as an independent expert in connection with the above-captioned lawsuit to provide my analyses and opinions on certain technical aspects of this dispute.

2. In this declaration, I set forth my opinions addressing Dr. Shefford Baker's declaration on how a person of ordinary skill in the art at the time of the alleged inventions would understand certain terms in claims asserted by Elm 3DS Innovations, LLC ("Elm") from the following patents: U.S. Patent Nos. 7,193,239 (the "'239 patent"), 7,504,732 (the "'732 patent"), 8,035,233 (the "'233 patent"), 8,410,617 (the "'617 patent"), 8,629,542 (the "'542 patent"), 8,653,672 (the "'672 patent"), 8,791,581 (the "'581 patent"), 8,796,862 (the "'862 patent"), 8,824,159 (the "'159 patent"), 8,841,778 (the "'778 patent"), 8,907,499 (the "'499 patent"), 8,928,119 (the "'119 patent"), and 8,933,570 (the "'570 patent") (collectively, the "Asserted Patents").

3. I am being compensated at a rate of $525 per hour for my work. My compensation is in not contingent on my opinions, testimony, or the outcome of this litigation.

4. I am competent to testify to the matters stated in this Declaration and have personal knowledge of the facts and statements herein. Each of the statements is true and correct.

II. BASIS FOR OPINION

A. Qualifications

5. My qualifications are set forth in my January 18, 2019 declaration, which I incorporate by reference as if set forth herein.

B. Materials Considered

6. In forming my opinions for this declaration, I have relied on my background and qualifications, materials considered in my January 18, 2019 declaration, the January 25, 2019 Declaration of Dr. Shefford Baker and the materials cited therein, and the materials cited in this declaration.

III. REBUTTALS OPINIONS ON CLAIM CONSTRUCTION

A. "low stress dielectric"

7. The parties' proposed constructions for 'low stress dielectric' / 'low stress dielectric layer' / 'low stress dielectric material' / 'low-stress … dielectric material' / 'low-stress … dielectric layer' / 'low stress … dielectric layer' are in the table below.

Plaintiff's Proposal	SK hynix's Proposal
a dielectric having a stress of less than 8 x 10^8 dynes/cm^2	Indefinite

8. In his declaration, Dr. Baker attempts to rebut the arguments made in my January 18, 2019 declaration. I previously argued that the plaintiff's proposed construction is indefinite, and contend that Dr. Baker's rebuttal to my arguments is not successful. In this declaration I offer arguments to refute Dr. Baker's declaration and reaffirm the following points made in my previous declaration:

1. Stress is a term of degree and the degree is not described in the Asserted Patents;
2. Stress is a tensor quantity that cannot be well represented by a single value as presented in Elm's proposed construction;
3. The stresses in an integrated circuit are inhomogeneous and it is necessary to specify some operation to produce a single stress value;
4. There was no standard measurement technique that would be appropriate to measure

the stresses in the dielectric layers of complex three-dimensional structures like those described in the Asserted Patents; and

5. The scope of 'low stress' in accordance with the asserted claims relates to making every dielectric layer individually at a "low stress" and excludes stress balancing and compressive stress.

9. In addition to attempting to rebut my argument that the 'low stress' terms are indefinite, Dr. Baker offers some important refinement to the potential scope of the 'low stress' discussed in the Asserted Patents. As Dr. Baker points out, the Asserted Patents discuss two distinct strategies: either using a structure in which each dielectric layer has an intrinsically 'low stress' or using 'stress balancing.' Dr. Baker states that for a structure or process utilizing the intrinsically 'low stress' method without stress balancing, 'each layer has an "intrinsically low stress" (here clearly meant to indicate the stress associated with each single layer is low).' Baker Decl. at p. 31.

10. I will consider the comments made by Dr. Baker in the order of the arguments in my January 18 declaration, and discuss the scope of the claims in the final section.

11. **Point (1)** Stress is a term of degree, and the degree that would apply to the various 'low stress' terms is not specified in the claims in the Asserted Patents. Dr. Baker acknowledges and agrees that stress is a term of degree but also asserts that "a person working in the art of semiconductor manufacturing at the time would have had several clear contexts in which to decide whether a stress qualified as 'low'." Baker Decl. at p. 26. However, Dr. Baker's cited references and data actually support my point that 'low stress' does not provide sufficient information to define a clear boundary between stresses that are 'low' and other stresses.

12. In order to be definite, the claims language must allow a person of ordinary skill

in the art to distinguish with reasonable certainty between infringing and non-infringing stress values. Dr. Baker offers a potential definition of 'low stress' that is not included in the Asserted Patents which he believes would be obvious to the person of ordinary skill: "low relative to the dielectric stresses that were common in conventional integrated circuit manufacturing processes in the past." Baker Decl. at p.26 ¶ 2. He acknowledges that "**there is no hard line in this definition**" *Id at* p. 27, lines 1-2 (emphasis added). And it is this lack of a hard line that makes 'low stress' indefinite.

13. Dr. Baker then refers to his 'Figure 5' for a table of values of "a variety of films used in Si devices," which I assume are examples of the 'conventional stresses' referred to in his potential definition of the word 'low.' *Id.* at p. 25. These 'conventional' stresses range from 2 x 10^8 dynes/cm^2 to 120 x 10^8 dynes/cm^2, so by this standard 'low stresses' would be less than some value within this range of 'conventional values.' *Id.* If these are the conventional stresses, then the claimed 5 x 10^8 dynes/cm^2 is also conventional, not low.

14. Dr. Baker's Figure 5 table identifies a range of "conventional stresses" ranging from 2 x 10^8 dynes/cm^2 to 120 x 10^8. *Id.* at p.25. But this range significantly overlaps with Dr. Baker's examples of 'low stress,' which vary from 1.7 x 10^8 to 50 x 10^8 dynes/cm^2. *Id.* at p. 27. He does not appear to disagree with the variety of examples of 'low stress' in the literature that I cited in my January 18 declaration. This supports my initial opinion that a reference to 'low stress' without an attendant value does not give a clear threshold that a person of ordinary skill in the art would recognize.

15. Dr. Baker himself frequently refers to a value of 10 x 10^8 dynes/cm^2 as the cutoff for 'low stress' (Baker Decl. at pp. 24, 27, 28) ('Although there is no hard line in this definition, inspection of Figure 5 suggests that, by any reasonable standard, stresses less than about 10 × 10^8

dynes/cm^2 would have been considered "low" at the time of the asserted patents.'). This contradicts Plaintiff's proposed construction, which sets this cutoff at 8 x 10^8 dynes/cm^2, while the only number the asserted claims use in connection with the 'low stress' claims is 5 x 10^8 dynes/cm^2. Dr. Baker, however, seems to think that Elm's proposed construction is somehow rendered definite because it is "comfortably less" than Dr. Baker's low stress threshold of 10 x 10^8 dynes/cm^2. *Id.* at p. 28.

16. My understanding is that "comfortably less" is not the legal standard regarding indefiniteness. Indeed, it is not at all clear how a person of ordinary skill in the art would know where to draw the line between 'low stress' dielectrics as opposed to 'conventional' stress dielectrics or 'high' stress dielectrics given these discrepancies. In his own words, Dr. Baker admits that the meaning which a person of ordinary skill in the art would ascribe to the term 'low stress' does not include a 'hard line.' Baker Decl. at p. 27. A hard line is exactly what is required for the construction to be definite. For example, according to Dr. Baker, one of ordinary skill in the art would understand that a value of 9 x 10^8 dynes/cm^2 is 'low stress' yet this value does not meet Elm's proposed construction of 'low stress' as a 'dielectric having a stress of less than 8 x 10^8 dynes/cm^2.' Similarly, 'low relative to the dielectric stresses that were common in conventional integrated circuit manufacturing processes in the past' provides little guidance given that Figure 5, which Dr. Baker claims 'shows a compilation of stresses in a variety of films used in Si devices, as reported in the early 1990s,' shows stresses from 2 x 10^8 dynes/cm^2 to 120 x 10^8 dynes/cm^2. Thus, one of ordinary skill in the art would have no way of knowing whether this value met any 'low stress' claim limitation.

17. Moreover, there is nothing to indicate that a person of ordinary skill in the art would view 10 x 10^8 or 8 x 10^8 dynes/cm^2 as the line from which stresses go from "low" to not

low. Indeed, the value of stress that a person of ordinary skill in the art could consider low would depend on a number of different factors including the application, the specific material properties of the dielectrics used, the environment, and so on. Nothing in the Asserted Patents, the prosecution history, or the extrinsic evidence submitted in this matter provide an objective basis for one of ordinary skill to determine where the boundary of "low" stress and a stress that is not "low" is.

18. **Point (2)** I argued that stress is not well represented by a single number in the structures described in the Asserted Patents, but requires description of 6 independent values, rendering it a tensor quantity. Dr. Baker agrees that stress is a tensor quantity and discusses this concept at some length. Baker Decl. at pp. 6-8. He then states that 'In most situations we *do not need* the full stress tensor to assess the stress in a given application'. *Id.* at p. 10. Dr. Baker then points out that in the simple case of a thin, flat, uniform, and homogeneous film on thick, flat, uniform, homogeneous substrate, that the stress away from the edges can be well represented by a single value, the layer stress, which is defined by Stoney's equation. *Id.* at p. 13. I also discussed Stoney's equation in my January 18 declaration.

19. Dr. Baker's argument that the stress in the dielectric structures of the claims is the single-valued 'layer stress' in Stoney's equation is incorrect. Even if in some limited circumstances the stress of a layer can be simplified to a single value, the relevant question regarding indefiniteness is whether the stress in the dielectric layers of the structures in the asserted claims can be simplified in this way. The answer is definitively no. One key factor in the reduction of the terms of the stress tensor to a single value via Stoney's equation is the assumption that the film and the substrate are both homogeneous. Dr. Baker, however, admits that the layers in an integrated circuit are 'rarely homogeneous,' and in fact are 'typically

inhomogeneous.' *Id.* at p. 17. This alone is enough to render Stoney's equation inapplicable for a 'typical' integrated circuit, including the complex structures claimed by the Asserted Patents. In addition, Stoney's equation applies only to the continuous material in the middle of a thin film; it does not apply at the edges of a sample. But integrated circuits and the structures in the Asserted Patents contain many internal edges and boundaries, distributed throughout the structure, and in and around these boundaries other components of the stress tensor may come to dominate the local stress. Dr. Baker does not assert that a person of ordinary skill in the art would know or want to discount these other stress components.

20. **Point (3)** I noted in my first declaration that besides the stress derived from Stoney's equation there might be other single values one might calculate from the stress tensor, but the single value calculated will in general be different depending on what value you calculate, leaving the claims indefinite. Dr. Baker mischaracterizes this argument as only amounting to the fact that the Asserted patents do not specify where to measure the stress. *Id.* at p. 29. I agree that the asserted claims' failure to specify where to measure stress is a definiteness problem, but it is not the only definiteness problem. While specification of a measurement location would be one method to calculate a single value out of the stress field, and that value might vary from point to point, I also discussed other methods such as taking the largest value or the average value--values that are typically different from each other and generally different from the value at a particular point.

21. Dr. Baker addresses the inhomogeneity of the integrated circuits by assuming it away, saying one can still use Stoney's equation to calculate a 'layer stress' or 'average stress'. In the case of an inhomogeneous structure, where Stoney's equation does not strictly apply, the 'layer stress' now represents the stress that would be present in a hypothetical homogeneous

layer of the same thickness required to produce the observed curvature. Put simply, for computational simplicity, Dr. Baker suggests assuming the inhomogeneity away at the cost of calculating a stress that is different from the real stress.

22. There are several problems with Dr. Baker's claim that this 'layer stress' 'accurately reflects' the 'average stress within the layer.' *Id.* at p. 29. First, Dr. Baker is improperly narrowing the claims by assuming the term 'low stress' refers only to the 'average stress.' Such an 'average stress' is not discussed in the Asserted Patents, nor is it included in the Plaintiff's proposed construction. The Asserted Patents do not use the terms 'average stress' or 'layer stress' in their claims. Instead, a number of other terms are used in the intrinsic record such as 'net stress' ('239 patent at 9:7-16), 'intrinsic[] stress' (*id.*), 'inherent stress' (IPR2016-00390, Patent Owner's Preliminary Response (April 6, 2016) at 58) and 'surface stress' ('695 patent at 11:36-37). Each of these terms has a different technical meaning, and a different numerical value for a given structure. In no part of the asserted claims is the stress in question specified, so a person of ordinary skill in the art would not be able to determine which value should be used, and Dr. Baker's assumption that the 'low stress' limitations refer to an 'average stress' or a 'layer stress' is without support. The fact that the patent does not specifically call out 'average stress' is a reason that one of ordinary skill in the art would not understand which stress the asserted claims referred to, and would not provide a reasonably objective basis to determine whether a product was infringing or not.

23. Second, the degree to which the additional 'layer stress' term Dr. Baker introduces will provide a good estimate of the 'average stress' is uncertain. He states without any cited support that 'if we could obtain the in-plane stress values at every point within the layer and average them together, it is straightforward to show that this average stress will be very close

to the value that would be obtained from measuring the substrate curvature and calculating the stress using Eq. 1.' Baker Decl. at p. 18. It is not clear what Dr. Baker means by 'very close.' In addition, in my opinion, the value of this 'stress' approximation will naturally depend on the geometric details (*e.g.*, thickness, pattern,) of the structure in question, the extent of coverage of the dielectric layer, and many other factors not fully specified in the Asserted Patents.

24. One theme Dr. Baker returns to frequently as justification for use of the 'layer stress' term is that it is by definition the stress that would lead to curvature, but there are other concerns that a person of ordinary skill in the art would have in attempting to understand the Asserted Patents or to follow the process described in them. Dr. Baker notes that: "Inorganic dielectrics have failure stresses on the order of 10 x 10^8 to 100 x 10^8 dynes/cm^2 and elastic moduli on the order of 10,000 x 10^8 dynes/cm^2. This means, by Hooke's law, that the strain to failure is of order 0.1% up to 1%. Strains of this magnitude are easily generated during deposition and thermal processing." *Id.* at p. 24. The specific failure Dr. Baker is referring to in this excerpt is mechanical fracture, or cracking, which is driven specifically by tensile stresses at microscopic flaws. Delamination is another important mode Dr. Baker does not mention. Delamination is caused by interfacial tensile stresses as well as interfacial shear stresses and can occur at a similar range of stress values. These various failure modes, including curvature, delamination, and fracture, are driven by different components in the stress tensor. A person of ordinary skill in the art would know that all of these failure modes would need to be avoided during processing in order to successfully fabricate a structure, and the Asserted Patents do not make clear which failure mode drives the 'low stress' requirement. Since the purpose of the 'low stress' requirement is not disclosed in the Asserted Patents, it would not be obvious that the 'layer stress' is what the claims refer to. Curvature is but one of a number of considerations for a

person of ordinary skill in the art when designing a stacked integrated circuit.

25. **Point (4)** In my declaration, I argued that at the time of the alleged invention of the Asserted Patents there was no accepted standard method to measure the stress in the dielectric layers in a structure such as the one described in the Asserted Patents. Dr. Baker does not effectively dispute this point. He mentions that a person of ordinary skill in the art would only be concerned with the 'layer stress.' As already discussed, however, the layer stress is not the actual stress in the dielectric in the integrated circuit, but the stress that would be present in a hypothetical layer of the same thickness that was uniformly deposited on the substrate, if the substrate were flat and itself uniform. Due to the circularity of the definition of layer stress, the stress of a hypothetical layer could be calculated by Stoney's equation and wafer curvature, but this value is not the actual stress of an integrated circuit layer. Because the assumptions required for Stoney's equation are violated in a typical integrated circuit it will not be equal even to the average stress in the dielectric layer. Dr. Baker claims the layer stress will be 'close to' the average stress, but offers no support for this claim, nor does he offer a method to reliably estimate the error in this assumption.

26. By way of reference, Dr. Baker also mentions two other techniques that can be used to estimate local stress, namely x-ray diffraction and Raman spectroscopy. *Id* at p. 21. As I discussed in my initial declaration, these techniques are generally applied to crystalline materials. The Clemens publication concerns polycrystalline metal interconnects, while the de Wolf publication discusses stresses in crystalline silicon. Dr. Baker also mischaracterizes my discussion of a paper from the literature in which results from both x-ray diffraction and wafer curvature are presented in a refereed journal article from around the time of the alleged inventions in the Asserted Patents (H. Uchida *et al*., "Measurement Technique for the Evaluation

of Residual Stress in Epitaxial Thin Film by Asymmetric X-Ray Diffraction" Journal of the Ceramic Society of Japan 107 [7] 606-610 (1999)). In the reference, these two stress measurement techniques strongly disagreed numerically, while the authors of the paper clearly felt their work had been a success. The inclusion of this article demonstrates that different stress measurement techniques reported significantly different stress values for the structure described in the article, which a person of ordinary skill at the time of the alleged inventions in the Asserted Patents would have anticipated as possibility for complex three dimensional structures.

27. **Point (5)** In addition to the arguments of indefiniteness, my January 18, 2019 declaration also discusses limitations to whatever construction may be proposed for the 'low stress' terms that are based on the prosecution history. Dr. Baker largely seems to agree with one of the key technical points made in Dr. Fair's declaration as well as my own. I argued, and Dr. Baker agrees, that 'intrinsically low stress' and 'stress balancing' are two distinct, and opposed strategies which can be used to avoid curvature in the fabrication of the kinds of three-dimensional structures described in the Asserted Patents.

28. Dr. Baker does not discuss the prosecution history in his declaration, so does not present any argument against my comments regarding the exclusion of stress balancing in the prosecution history. Based on the prosecution history already discussed in my January 18 declaration, the patentee previously limited the scope of the 'low stress' terms in the Asserted Patents to exclude stress balancing in the related '237 and '386 patent prosecution history. Instead, the asserted claims must be understood with respect to the 'low stress' terms to be directed at each and every layer, and cannot be interpreted as a 'net stress' that could be obtained in stress balancing. One of ordinary skill in the art would interpret the asserted claims with the 'low stress' limitations to be directed at each and every dielectric layer and not a net stress

achieved through stress balancing. Further, during the *inter partes* reviews of the asserted patents, the patentee distinguished claims with 'low stress' dielectrics from the Kowa prior art reference disclosing stress balancing. IPR2016-00390, Patent Owner's Preliminary Response (April 6, 2016) at 58.

29. Dr. Baker does make an important technical distinction regarding the use of 'intrinsically low stress' in this context that I would like to emphasize. Dr. Baker claims that one likely goal of the use of 'low stress dielectrics' in the Asserted Patents is to reduce curvature. According to Dr. Baker, when using layers of 'intrinsically low stress' it is necessary that "each layer has an 'intrinsically low stress.'" Baker Decl. at p. 31. In this scenario, each layer, including the metal, semiconducting, and dielectric layers, would need to have a 'low stress' in order to avoid unwanted curvature. As Dr. Baker argues, this is in stark contrast to 'stress balancing'. He makes this distinction very clear, when he states "If the contributions of the stresses in the different layers *to curvature* can be made to compensate each other so that the *curvature* is zero, the 'net stress' (or 'average stress' or 'effective stress') is said to be zero, even if the stresses in the individual layers are quite high." *Id.* at p. 19. So in the 'intrinsically low stress' strategy, the stress in *each* layer should be 'low', while in 'stress balancing' approach, stress in the individual layers can be 'quite high.' I agree with Dr. Baker's comments regarding intrinsically low stress dielectrics, but, as discussed above, Dr. Baker is incorrect that the 'low stress' claim terms also cover 'stress balancing.'

30. I also argue that the term 'low stress' as used in the Asserted Patents should be construed to apply only to dielectric films in tensile stress. Dr. Baker appears to argue that my declaration states that the term 'low stress' in any context only applies to tensile stresses, which is not true. On the contrary, this comment was made to indicate that in the prosecution history, it

is clear the patentee limited the application of the 'low stress' term in order to distinguish the 'low stress dielectrics' in the asserted claims from the prior art.

31. In the '499 patent prosecution history, the patentee acknowledges the differentiation between compressive stresses and tensile stresses in the '695 patent, distinguishing from prior art where the 'dielectric is a low *compressive* stress dielectric' (emphasis in original) and stating that 'support for low *tensile* stress (as opposed to compressive stress) is found in col. 6 line 62 to col. 6 line 5 and elsewhere of U.S. patent 5,354,695'. '499 Patent File History, 6-20-13 Response to Office Action (emphasis in original). Thus, whatever the scope of 'low stress' in the claims of the Asserted Patents, it does not include compressive stress. Dr. Baker ignores statements in the prosecution history distinguishing the 'low stress' dielectrics of the asserted claims from prior art that disclosed compressive low stress dielectrics. Dr. Baker does not discuss the prosecution history in his declaration, so does not present any argument against my comments regarding the exclusion of compressive stress dielectrics in the prosecution history.

32. Further, because the '695 patent is included by reference in the Asserted Patents, and offers the only commentary as to what is meant by the term 'low stress' in the Asserted Patents, a person of ordinary skill in the art would have no other basis on which to interpret the term in the context of the fabrication process described in the Asserted Patents. The '695 patent makes clear the stresses in the dielectric films in question are tensile.

33. Dr. Baker's statement that the '695 patent discusses a different technology is contradicted by the plain language of the Asserted Patents, which incorporate the '695 patent by reference and expressly state that 'Assembling die in a stacked or three dimensional (3D) manner is disclosed in U.S. Pat. No. 5,354,695 of the present inventor, incorporated herein by reference'

and 'Such low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695 of the present inventor, incorporated herein by reference.' '239 patent at 2:34-36. 9:5-7.

B. '5×10^8 dynes/cm^2 or less'

34. The parties' proposed constructions for 'have stress of about 5×10^8 dynes/cm^2 or less' / 'have a stress of about 5×10^8 dynes cm^2 or less' / 'having a stress of 5x10^8 dynes/cm^2 or less' / 'having a stress of 5x10^8 dynes/cm^2 tensile or less' / '[have] a stress of about 5×10^8 dynes/cm^2 tensile or less' / 'having[/has] a stress of less than 5×10^8 dynes/cm^2 tensile' / 'a stress of about 5×10^8 dynes/cm^2 or less' / 'with a tensile stress of less than 5×10^8 dynes/cm^2' / 'with a stress of less than 5×10^8 dynes/cm^2 tensile' / 'has[/having] a tensile stress of less than 5×10^8 dynes/cm^2' are in the table below.

Plaintiff's Proposal	SK hynix's Proposal
No construction necessary	Indefinite

35. As an initial matter, as is evident from both the length and complexity of Dr. Baker's declaration, Dr. Fair's declaration, my own opinions, and the extensive extrinsic evidence, the notion that a person of ordinary skill, let alone a lay juror would understand the low stress term with a specific numerical value without any construction by the Court is incorrect.

36. Dr. Baker's declaration includes section D on page 33 headed '8 x 10^8 dynes / cm^2 or less'. I am assuming here that this is the section in which he intends to discuss the construction for the claims related to the term '5 x 10^8 dynes/cm^2 or less.' In this section Dr. Baker does not introduce any substantive new arguments against my contention that the term '5 x 10^8 dynes / cm^2 or less' is indefinite distinct from those already discussed in the 'low stress' section.

37. Dr. Baker does include a new and unsupported claim that the stress the Asserted Patents are describing in their claims is the 'net stress'. This is the first time Dr. Baker makes this claim, and his justification is not clear. The 'net stress' is also distinct from the 'layer stress' that Dr. Baker discusses previously, so this statement appears to contradict his own statements in the prior sections.

38. Another new claim introduced in this section relates to the strategy the Asserted Patents present to reduce curvature. Dr. Baker states, "… the 'net stress,' which could be made low by ensuring that all (or nearly all) of the individual layers have low stress, or by stress balancing." Baker Decl., p. 33. The inclusion of the '(or nearly all)' phrase here is not explained or justified, and I disagree that the limitation is accurate. Dr. Baker states that 'each layer' should have low stress, which is accurate. Baker Decl., p. 31. Even one layer of sufficiently high stress would prevent the net stress from being near zero without stress balancing. As previously discussed, the prosecution history makes clear that the scope of the asserted claims specifically excludes stress balancing. In light of Dr. Baker's description of stress balancing, the text of the Asserted Patent specifications, and the prosecution history it is clear that the preferred method of fabricating the structures described in the Asserted Patents is to ensure that *each* of the layers should have stress of 5×10^8 dynes/cm^2 or less. The stress here in the asserted claims refers to stresses specifically in the dielectric layers, which would not be equal to the 'net stress.' As Dr. Baker previously described very clearly stress balancing allows the 'net stress' to be near zero while the stress in individual layers, including the dielectric layers, can be 'quite high.'

IV. RESERVATION OF RIGHTS

39. The opinions expressed in this Declaration are based on the parties' contentions and my review of the evidence produced at this stage of litigation. My opinions are subject to change based on any additional opinions that Elm may present and information I may receive in

the future. With this in mind, based on the analysis I have conducted and for the reasons set forth above, I have reached the conclusions and opinions in this Declaration.

40. If I am called to testify, in connection with my anticipated testimony in this litigation, I may use as exhibits various documents produced in this case that refer or relate to the matters discussed in this Declaration. I may also rely on visual aids and may rely on analogies concerning elements of the patents discussed above, the accused products, the references cited in this Declaration, or any related technologies. In addition, I may create or assist in the creation of certain demonstrative evidence to assist me in testifying, and I reserve the right to do so.

41. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: February 1, 2019

Dr. Steven Murray

EXHIBIT E

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC, Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	C.A. No. 14-cv-1430-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, Plaintiff, v. MICRON TECHNOLOGY, INC., et al., Defendants.	C.A. No. 14-cv-1431-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, Plaintiff, v. SK HYNIX INC., et al., Defendants.	C.A. No. 14-cv-1432-LPS-CJB JURY TRIAL DEMANDED

DECLARATION OF SHEFFORD BAKER

My name is Shefford P. Baker. I am an Associate Professor in the Department of Materials Science and Engineering at Cornell University. I received my undergraduate degree in Music from the University of New Mexico before earning my M.S. and PhD (1992) in Materials Science and Engineering at Stanford University. My PhD work focuses on stresses and mechanical properties of thin metal/metal multilayer films. I also developed methods for measuring mechanical properties of thin films using nanoindentation.

Following Stanford, I worked at the Max-Planck-Institut für Metallforschung in Stuttgart Germany for five years as a member of the research staff. I supervised PhD students and conducted research. My work there focused on projects related to thin film metallizations for use in integrated circuits. In one project, I studied electromigration phenomena and developed an experiment to

relate conductor line microstructure to electromigration failure and correlated failure characteristics to line texture. In several projects, we investigated stresses and thermomechanical behavior of thin copper metallizations. The semiconductor industry was gearing up to transition to copper metallizations and did not know much about it. I supervised the design and construction of two ultra-high vacuum sputter deposition systems and a substrate curvature stress measurement system. My students and I also conducted thin film stress measurements using x-ray diffraction and mechanical property measurements using nanoindentation.

I joined the faculty at Cornell in 1998 in the Department of Material Science and Engineering (MSE). During my twenty years at Cornell, my research has focused on structure and mechanical properties in a range of materials including metal and ceramic thin films, biomineralized tissues and biogenic, geologic, and synthetic mineral crystals, silicate glasses, metallic glasses, and a number of other materials.

My research group at Cornell develops sophisticated machinery and equipment to produce and study thin films. For example, in our thin film lab, we have built (and rebuilt) a high vacuum ($\approx 10^{-7}$ Torr) evaporator system with thermal and e-beam sources, complete source and substrate shuttering, a heated and cooled sample stage and an ion gun for ion beam assisted deposition. We also designed and built an ultra-high vacuum sputter deposition system ($< 10^{-9}$ Torr) with three confocal sputter guns, a rotating heated (500˚C) sample stage, RF and DC power supplies, substrate bias. This system includes a substrate curvature stress measurement system that can detect a radius of curvature to about 60 km on a 100 mm substrate (very high stress resolution) at temperatures from liquid nitrogen to over 800˚C. In addition, we outfitted the G-2 beamline at the Cornell High Energy Synchrotron Source (CHESS), designing and building a 6-circle kappa geometry goniometer, a heated environmentally controlled stage, and other features dedicated to thin film structure and stress measurements. My group has used this machinery to study

electromigration and adhesion in thin copper films, texture and texture transformations in a variety of FCC metals films (primarily silver), phase formation, phase transformation and texture patterning in thin tantalum films, stresses in thin tungsten films, and many others. We also have a nanomechanics lab that has included several nanoindenters, an AFM and several homemade fracture and adhesion test setups. We also operate the MSE department's tensile tester where we have conducted tests on the mechanical properties of a number of samples from brazed lap joints for stainless steel heat exchangers to grafted joints in wine grape plants. Our development of and access to this equipment allows us to conduct a broad range of experiments. In particular our thin film lab allows us to produce extremely pure and clean films for model studies.

I have published extensively in the area of thin films and semiconductors. My publications have examined issues relating to stress, creep, strain hardening, structure, texture and texture transformations, phase formation and phase transformations, and many other features in thin films. A full list of my publications is attached as Exhibit A.

Much of the thin film work was motivated by the needs of the semiconductor manufacturing industry. Starting in Germany my students and I worked to understand the mechanical properties of the copper metallizations that were eventually adopted by the industry. For example, we studied the effect of tantalum barrier layers on structure and properties of copper films and worked out the relationship between interfacial oxygen concentration and adhesion between Cu films and adjacent SiO_2 layers. In another project, we studied tantalum films that were used as thin film resistors and that are now under development for Giant Spin Hall Effect devices.

During my time at Cornell, I have received several awards, including Excellence in Teaching Awards and the CAREER Award from the National Science Foundation. In addition to my research and teaching, I have been involved in developing the engineering curriculum for undergraduates, serving as the Director of Undergraduate Studies for the Department of Materials

Science and Engineering for several years. I am currently the Director of the Master of Engineering program in MSE, a program that I and several colleagues created 4 years ago to prepare MSE students for careers in industry. I am also a member of the Fields of Theoretical and Applied Mechanics, Mechanical Engineering, and Aerospace Engineering at Cornell.

Outside of Cornell, I have held many roles in the Materials Research Society, which is an international organization that promotes interdisciplinary materials research among professionals worldwide. I was the president of that organization in 2009 and am now the chair of the Publications Committee. I was also involved in the formation of the Nanoscale Informal Science Education network. The NISE is funded by the National Science Foundation and promotes public education of science (including nanoscale science) in the United States. I am also currently a member of the American Ceramics Society and TMS.

I. ASSIGNMENT, LEGAL STANDARDS, AND MATERIALS CONSIDERED

I have been asked to provide opinions about the reports offered by the experts retained by the defendants in this matter, Drs. Steven Murray and Richard B. Fair.

I understand from Elm's counsel that the terms of a patent should have their plain and ordinary meaning in the field of the invention as understood by a person having ordinary skill in the art. I also understand that the defendants argue that certain claims are indefinite. I understand that a claim is indefinite when it does not point out and distinctly claim the subject matter of the invention, which means that the claims fail to inform a person of skill in the art, with reasonable certainty, about the scope of the invention. I have conducted both inquiries as of the date of the patent, which is April 1997.

Given that understanding, my analysis has focused on how a person of skill in the art would have understood the claims and the other sections of the patent given my background with semiconductor technology and thin films, which include dielectrics. I have also focused on the

assertions regarding the patents in this lawsuit in Murray's and Fair's reports based on my knowledge of the art.

I am being compensated at my ordinary and customary consulting rate of $320 per hour for my work. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

I had one week to complete this report. So in the interests of time, I have not addressed all of those portions of the reports where Murray and Fair just quote portions of the patent, specification, or prosecution history. Instead, I discuss the technology and how a person of ordinary skill's technical knowledge would inform the reading of the patent in certain areas, including how the claims provide a reasonably certain scope of the invention.

In forming my opinions, I have read the patents at issue in this lawsuit, the reports of the defendants' experts, the articles and other materials cited in this report, and the materials cited by the defendants' experts. I have also used my background in the technology and general knowledge that I have gained in my career as a professor and practitioner. I have read Murray's and Fair's description of the level of ordinary skill in the art and use the same understanding here.

II. DISCUSSION

In preparing this report, I came to the conclusion that a person of ordinary skill in the art would find the descriptions in the patents quite straightforward to follow, and so have taken the tactic of making a tutorial presentation of the relevant state of the art at the time of the patents, with a focus on what is needed to understand both the patents, and the arguments of Defendants' expert witnesses, Fair and Murry. This information is included in section A below. Following that, relatively short technical discussions of how I would interpret two of the topics of the Claim

Construction process, namely "Low Stress Dielectrics" (and similar terms) and "Substantially Flexible Substrate" and similar terms in Sections B, C, and D.

A. STRESSES IN INTEGRATED CIRCUIT MANUFACTURING

A key feature in the patents has to do with the stresses that arise in a thin dielectric layer on a silicon substrate. The defendants' expert witnesses made a series of arguments in their explanation of their claim constructions that are based on stresses. In short, they claim that because stresses are *tensor quantities*, *inhomogeneous*, of *different "types,"* and *difficult to measure*, that a person of ordinary skill in the art would not be able to ascertain whether stresses in a dielectric were low and that therefore claims having to do with low stresses in a layer are indefinite.

In sharp contrast, I discuss that, while it is true that stress is a tensor quantity, that stress distributions are inhomogeneous, and that stresses may arise from different origins (the meaning of stress "types"), *none* of these features have any effect on the understanding or application of the patents. In addition, I explain that stresses in thin semiconductor layers can readily be measured with sufficient accuracy using methods widely known to persons of ordinary skill in the art at the time of the patents.

To make these arguments, I begin with a brief tutorial on stresses in integrated circuit manufacturing.

A.1. Stress as a tensor

` To understand what is being discussed in the patents and by the defendants' expert witnesses, it is helpful to understand the concept of "stress." (Reference for this entire section: Fung, Y.C., *A First Course in Continuum Mechanics*, (2nd ed.), Englewood Cliffs, New Jersey: Prentice-Hall Inc. 1997.) In general terms, stress describes the forces acting at a point in a

material in terms of the force per unit area. Imagine a piece of material upon which different forces are acting including pushing, pulling, twisting, *etc.* as shown in Figure 1a.

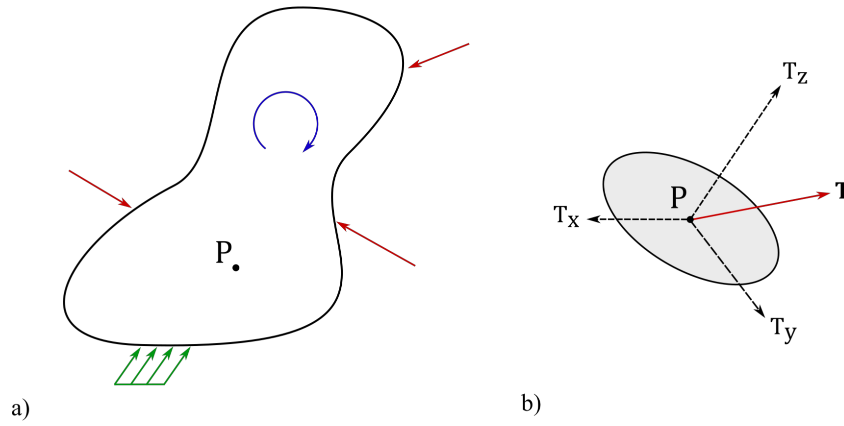


Figure 1: Forces in a body.

At any point *P* inside the material the net force is going in some direction, indicated by the arrow marked ***T*** in Figure 1b. We can pick any plane that goes through *P*. For our bookkeeping, we assign a coordinate system such that the *x* and *y* directions are perpendicular to each other and lie in the plane, while *z* is perpendicular to the plane. The force ***T*** can then be broken down into three components: the force that is perpendicular to the plane is the "normal" force component, T_x, and the parts that act in the plane are the shear components, T_y and T_z. To turn these into stresses, we divide each of these force components by the area over which it acts to get stress components σ_{xx} (normal stress), and σ_{xy}, and σ_{xz} (shear stresses). (Stress is indicated by the Greek letter σ or sigma.) To get the complete stress state at point *P*, we do the same calculations on two additional planes that are perpendicular to our first plane and to each other. It is common to show these three planes as the faces of a cube as shown in Figure 2. We see that the full stress state has 9 components, σ_{xx}, σ_{xy}, σ_{xz}, σ_{yx}, σ_{yy}, σ_{yz}, σ_{zx}, σ_{zy}, and σ_{zz}. But as it turns out, some of the shear stresses have the same values ($\sigma_{xy} = \sigma_{yx}$, $\sigma_{xz} = \sigma_{zx}$, and $\sigma_{yz} = \sigma_{zy}$). So only 3 values are needed to represent the 6 shear stress components acting at any given point *P*.

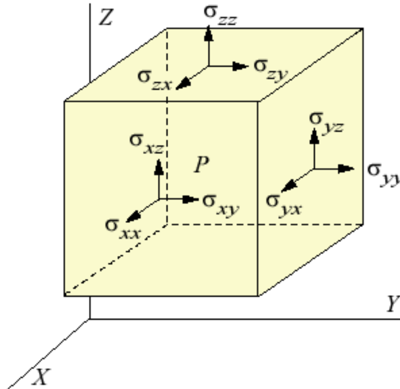


Figure 2: The 9 components of stress in an x-y-z coordinate system.

This means that, in general, 6 numbers are needed to define the stress at any point. There are three normal stress components σ_{xx}, σ_{yy}, and σ_{zz}, and there are three shear stress components σ_{xy}, σ_{xz}, and σ_{yz}. The particular set of numbers depends on the coordinate system we picked (*i.e.*, if you changed the orientation of the cube in Figure 2, you would need 6 different numbers to describe the same stress state at the same point).The fact that 6 numbers are needed at every point arises because stress is what is known as a tensor quantity (2nd rank tensor to be specific). In a loaded body such as that shown above, the stress varies from point to point and the "stress field" is the 3-D map of those values (6 values at every point).

The key facts to remember here are:

- In theory and at its most basic, stress is a tensor quantity that requires 6 different numbers (components) to fully specify it at a point.
- In a body with irregular loads (Fig. 1a) or a body that is uniformly loaded but is inhomogeneous (different properties at different points), the stress field will be inhomogeneous.

A.2. What are stress and strain?

So what *is* stress? Atoms in a material are connected to each other by bonds, which, for our purposes here, may be thought of as tiny springs connecting the atoms. At a given set of

conditions (pressure, temperature) each bond has an equilibrium length. This equilibrium length is the length the bond adopts if no external forces act on it. If the atoms are pushed closer together, the bond responds—just as a spring—with a compressive force that tries to return the atoms to their equilibrium separation. Similarly, if the atoms are pulled farther apart, the bond exerts a tensile force to return the springs to their equilibrium positions. Stress is just a measure of the forces in the bond "springs", per unit area.

The stretching of bonds (springs) discussed above, is described in terms of strain. A normal strain is just a change in length per unit length. Since materials may be both stretched and sheared, a complete description of the state of strain at any given point also requires 6 numbers (*i.e.* strain is also a second-rank tensor).

A.3 Stress in real engineering applications (not a tensor!)

While a tensor description is complicated, that is not what is being discussed in the patents. In most engineering applications, including semiconductor manufacturing, it is possible to pick coordinate systems and use well-accepted simplifying assumptions so that only a few stress and strain components are needed. Most scientists, engineers, and technologists never think of stress in its tensor form at all. For example, the most common test used to understand the mechanical properties of materials is a "uniaxial tension test." In this test a cylinder of material is stretched along its axis. If the material can be thought of as homogenous (properties are the same at all points) and isotropic (properties are the same in all directions at one point), then there is only one stress component, σ, which is just the stretching force divided by the cross sectional area of the cylinder, and there are two strains, ε, which is the change in length per unit length along the axis, and ε_T, which represents the change in diameter as the cylinder is stretched.

Deformation can be elastic or inelastic. Deformation is elastic if the deformed body returns to its original shape when the forces that caused the deformation are removed. For elastic

deformation, stress and strain are simply related by Hooke's law, $\sigma = E\varepsilon$, where E is a numerical constant called Young's modulus, and the axial and transverse strains are related by $\varepsilon_T = -\nu\varepsilon$, where ν is Poisson's ratio. This formulation would be well known by persons with ordinary skill in almost all technologies where stress is a concern, including the art of semiconductor manufacturing.

The key fact to remember here is

- In most situations we *do not need* the full stress (or strain) tensor to assess the stress in a given application. A sufficient description of the stress can be obtained with a single number.

A.4 Stress in a thin layer on a thick substrate

A similarly common and simple formulation arises in fields that involve the use of thin layers on thick substrates. This includes thin films and coatings used in optical devices, wear-resistant coatings in tools, decorative coatings, catalytic thin films, biocompatible coatings and many other applications, including dielectric layers in semiconductor manufacturing. In all of these fields of application, it is well known that the interaction between the layer and the substrate can lead to stresses in the layer, and a simple way to measure this "film stress" or "layer stress" is very widely understood (Nix, W.D., *Mechanical Properties of Thin Films.* Metallurgical Transactions A, 1989. **20A**: p. 2217-2245, Ohring, M., *Materials Science of Thin Films*. 2nd ed., 2002: Academic press., Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.).

We can understand this layer stress as follows: Imagine that a thin film is attached to a thick substrate as indicated in Figure 3a. Suppose that both the film and the substrate have uniform thickness, are homogeneous and isotropic, and are stress-free and flat. We conduct a thought experiment to see how film stresses arise (Nix, W.D., *Mechanical Properties of Thin*

Films. Metallurgical Transactions A, 1989. **20A**: p. 2217-2245): First, we imagine removing the film from the substrate (b), and then changing the film dimensions relative to the substrate (c), meaning that the width of the substrate and film are not the same. There are many ways that such a relative dimension change can occur. We can then imagine applying external forces to stretch or compress the film so that it once again fits on the substrate (d), attaching it to the substrate (e), and releasing the external forces that we used to stretch or compress the film, (f). The substrate now carries the load needed to stretch or compress the film and, because that load is applied at the film/substrate interface, it causes the substrate to bend (f). In other words, the film wants to return to its original dimensions after it is stretched and attached to the substrate, but it cannot do so because the substrate is keeping it stretched to its new dimension. The film is held in a stressed state, bending the substrate with it. The force exerted on the film must be equal in magnitude and opposite in sign to the force on the substrate (no external forces are applied) but the film is thin so that force is spread over a small area leading to a high stress while the substrate is thick so the force there is spread over a large area leading to small stresses.

In reality, the film remains on the substrate and something happens to make it want to shrink or expand relative to the substrate, but because it is forced to fit the substrate it gets stretched or compressed, *i.e.* stresses arise! We can use the thought experiment to imagine what would happen if we could take the film off of the substrate to see the relative dimension changes. This helps us to calculate the sign and the magnitude of the stresses.

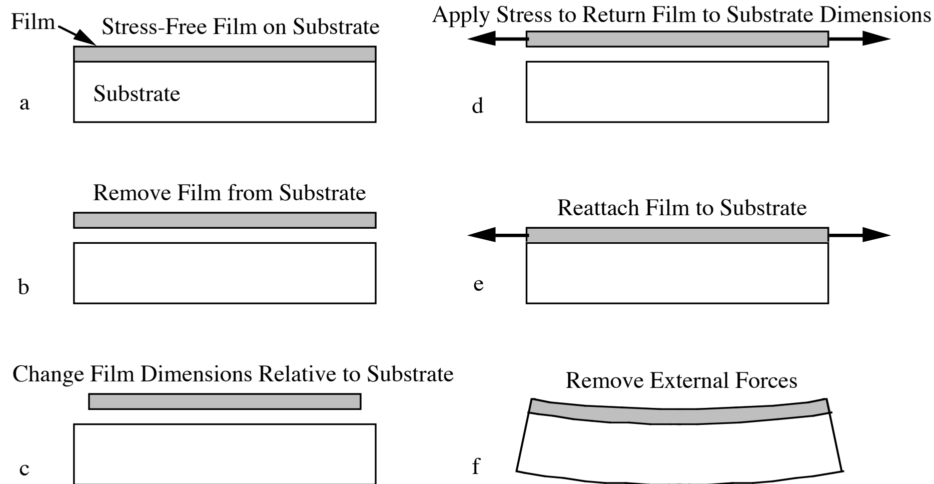


Fig. 3: Origin of film stresses

So we see that *any* process that changes the equilibrium in-plane dimension of the film relative to the substrate (Fig. 3b-c) leads to a stress in the film (Fig. 3e) and that stress leads to curvature of the film/substrate package (Fig. 3f. Note that the relaxation of the stress in the film due to curvature, Fig. 3e to Fig. 3f is very small—we'll come back to this shortly.). Two of the most common ways that these relative dimensional changes can occur are *differential thermal expansion* and *structure evolution in the film* (Nix, W.D., *Mechanical Properties of Thin Films.* Metallurgical Transactions A, 1989. **20A**: p. 2217-2245, Ohring, M., *Materials Science of Thin Films*. 2nd ed., 2002: Academic press., Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.). Differential thermal expansion occurs when the film and substrate have different thermal expansion coefficients and are subjected to a temperature change. The associated stresses are often called "thermal stresses." Structure evolution occurs when the film becomes more or less dense due to thermal processing, ion implantation, or other processes. For example, atoms arriving at the film surface with enough energy to be implanted into the film, cause the film to be denser than equilibrium, it will want to expand but will be constrained by the substrate and will be in compression. The stresses associated with structure evolution during deposition are often

called “growth stresses” (or “intrinsic stresses”). These two sources of stress are by far the most important in thin film technology. After deposition, stresses may also change due to plastic deformation or further structure evolution.

Fortunately, the stress state in the thin layer shown in Fig. 3 is *not* complicated. If we choose a coordinate system in which the x and y directions are in the plane of the film and the z direction is perpendicular to the film, the stress state in the film everywhere except very near the edges (≈ 1 or 2 film thicknesses from the edge) can be characterized by a single value, $\sigma_{xx} = \sigma_{yy}$, which is commonly referred to as the “film stress” σ_f, which is a normal stress acting in the plane of the film. This stress is also known as a “layer stress.” For a thin film on a thick substrate it is easy to show that the film stress is simply related to the radius of curvature R that this stress induces in the substrate as follows,

$$\sigma_f = \frac{E_s t_s^2}{(1-\nu_s)t_f} \frac{1}{R} \quad ,(1)$$

where E_s and ν_s are Young’s modulus and Poisson’s ratio (elastic constants) of the substrate, respectively, and t_s and t_f are the thicknesses of the substrate and film, respectively (Nix, W.D., *Mechanical Properties of Thin Films.* Metallurgical Transactions A, 1989. **20A**: p. 2217-2245, Ohring, M., *Materials Science of Thin Films*. 2nd ed., 2002: Academic press., Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.). Equation 1 is also known as the “Stoney Equation” (Stoney, G. G., "The Tension of Metallic Films Deposited by Electrolysis". Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences (1364-5021), 82 (553), p. 172 (1909))

The formulation shown in Equation 1 is very important to us for three reasons:

- (1) *This situation is very common in semiconductor manufacturing*. As we will see, an integrated circuit is formed from a series of thin layers deposited on a substrate. Each of these layers individually and all of them collectively interact with the substrate giving rise to layer stresses and substrate curvature according to Eq. 1. (Nix, W.D., *Mechanical Properties of Thin Films.* Metallurgical Transactions A, 1989. **20A**: p. 2217-2245, Ohring, M., *Materials Science of Thin Films*. 2nd ed., 2002: Academic press., Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.)
- (2) Like the uniaxial tension test described above, we again have a *simple relationship that does not require the use of tensors*. The layer stress is represented by a single number. (Nix, W.D., *Mechanical Properties of Thin Films.* Metallurgical Transactions A, 1989. **20A**: p. 2217-2245, Ohring, M., *Materials Science of Thin Films*. 2nd ed., 2002: Academic press., Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.)
- (3) Eq. 1 gives us a *very simple way to determine the layer stress*. If we can measure the radius of curvature R and know the thicknesses of the layer and the substrate, as well as Young's modulus and Poisson's ratio for the substrate, we can calculate the layer stress. In fact, this kind of measurement is very commonly used in all industries that depend on thin films (or "layers" or "coatings") (Ohring, M., *Materials Science of Thin Films*. 2nd ed., 2002: Academic press., Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.).

And here are four additional important things to know about these substrate interaction stresses:

- (4) Although a number of terms (like "thermal stress" and "intrinsic stress") are commonly used to distinguish the *origins* of stress, there are *no* physical distinctions among these stresses. Stress is stress; *there are no actual different "types" of stress*, these terms are just shorthand to refer to the stress's origin. It is more correct to think of the origin of the relative change in dimensions shown in Fig. 3c as the distinguishing feature. Thus, one would describe the stretching/compressing of the film relative to the substrate in terms of "thermal strain" or other appropriate terms (Nix, W.D., *Mechanical Properties of Thin Films.* Metallurgical Transactions A, 1989. **20A**: p. 2217-2245), and many in the industry do. The sources of strain can be identified and summed up to get the film strain ε_f. The film stress is simply related to the film strain by the appropriate version of Hooke's law, which is in this case $\sigma_f = (E_f/(1-\nu_f))\varepsilon_f$.
- (5) When the forces acting to compress or stretch an atomic bond are removed, it returns to its equilibrium length. This is the source of elastic behavior. Because stresses are associated with bond stretching, *stresses are associated with elastic strains only*. Plastic deformation occurs when atomic bonds are broken and reformed with different neighbors, permanently changing the shape of the material. The total strain is the sum of the elastic strain and the plastic strain, but the stress arises only from the elastic part.
- (6) For cases where Eq. 1 (the Stoney Equation) applies, the stress in a layer needed to produce a certain curvature (curvature $\kappa = 1/R$) is much greater than the stress that would arise in that layer if you simply took a flat stress-free film/substrate combination and bent it to the same curvature using external forces. The result of this is that a change in curvature induced by adding a second film does not significantly

affect the stress in a first film. Thus, to a good first approximation, *all films interact with the substrate independently*. (Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.)

- (7) Real films may not be homogeneous, but, as I will demonstrate below, *inhomogeneity does not necessarily affect the technologist's use of Eq. 1*.

Everything in this section would have been well known to a person of ordinary skill in the art of semiconductor manufacturing at the time of the patents.

A.5 Layer stresses in integrated circuits

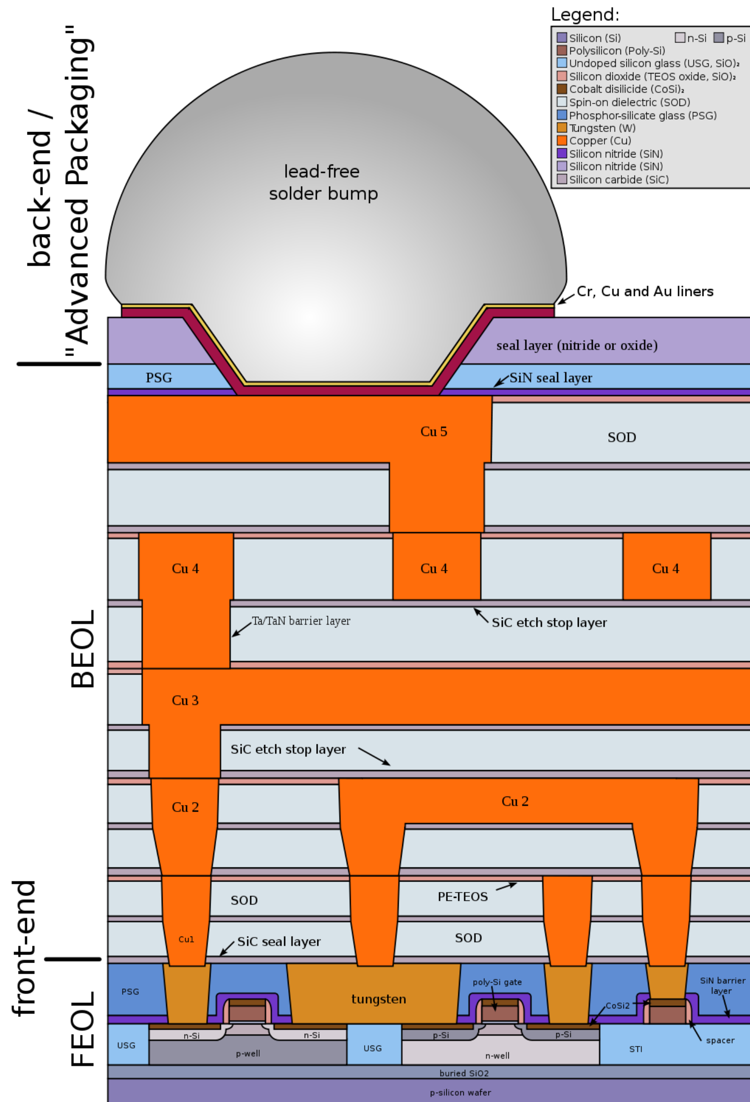
Film stresses are a major concern in semiconductor processing. As indicated in Equation 1, stresses in an attached layer can cause the substrate to curve. If the curvature of the substrate, $\kappa = 1/R$, becomes too great, it can become impossible to align photolithography masks so that the next layer can be made in registry with previous layers, impossible to successfully planarize by chemical mechanical processing, and impossible to attach a (curved) chip die to a (flat) substrate or package. (Garrou, P., C. Bower, and P. Ramm, *Handbook of 3-D Integration: Technology and Applications of 3D Integrated Circuits*, Weinheim: Wiley-VCH Verlag; 2008., Nix, W.D., *Mechanical Properties of Thin Films.* Metallurgical Transactions A, 1989. **20A**: p. 2217-2245, Clemens, B.M. and J.A. Bain, *Stress Determination in Textured Thin Films Using X-ray Diffraction,* Materials Research Society Bulletin, XVII(7): p. 46-51 (1992)) For these reasons (and others), a great deal of effort has been spent over the past five decades to reduce this curvature. One way to reduce the curvature is to make the substrate thicker. Indeed, as substrate wafer diameters have increased, the specified thickness also increased (*e.g.* in going from 100 mm to 200 mm diameter Si wafers, the standard thickness was increased from 525 µm to 725

μm). The patents at issue are concerned with a different way to reduce curvature, namely, to minimize stresses that can cause substrate deformation.

Of course, the individual layers in an integrated circuit are rarely homogeneous as shown in Fig. 3. Instead, the layers in an integrated circuit are typically inhomogeneous as shown in Figure 4. This inhomogeneity arises from the way semiconductors are made. Semiconductor manufacturing is generally divided into three broad categories, (1) "front end of line" (FEOL) and (ii) "back end of line" (BEOL) (confusingly, both part of the "front end"), and (iii) "packaging" or "back end" processing (Fig. 4a). In FEOL processing, the electrically active components (transistors, capacitors, resistors) are made on the semiconductor layer (most commonly a Si substrate but could also be a thin semiconductor layer deposited on a different substrate). In BEOL processing, electrical connections are made to the FEOL components by creating dielectric layers that contain metal "interconnect" wires. These layers are created by sequential steps in which a dielectric or metal film is deposited, patterned by lithography and etched to remove unwanted portions, a subsequent metal or dielectric film is deposited to fill in the spaces, and the unwanted parts of that layer and any surface topography are removed by chemical mechanical planarization. Additional diffusion barrier, etch stop, passivation, and other layers may be deposited as well. The result is an assembly of thin layers, consisting mostly of dielectric, but also including metals and other materials, on top of a thick substrate. (Garrou, P., C. Bower, and P. Ramm, *Handbook of 3-D Integration: Technology and Applications of 3D Integrated Circuits*, Weinheim: Wiley-VCH Verlag; 2008.)

Although the materials changed with time (e.g. the interconnect metals in Fig. 4b were aluminum, while in 4a they are copper), the layered structure is quite clear. Each individual BEOL layer includes passivation, in while metal interconnect lines are embedded.

The metal and dielectric components have different properties, so the stress within an inhomogeneous layer that arise due to interaction with the substrate will obviously be inhomogeneous. That is, the stresses will vary in the areas around every dissimilar materials interface (say metal/dielectric). As evident in Fig. 4, there are many of these. But as with the stress states near the edge, these regions with varying stresses will be quite small, extending ≈ 1-2 layer thicknesses on either side of the interface. As it turns out, under certain conditions (inhomogeneous regions small relative to the layer width and distributed across the width—conditions well met in integrated circuit layers), if we could obtain the in-plane stress values at every point in the layer and average them together, it is straightforward to show that this average stress will be very close to the value that would be obtained by measuring the substrate curvature and calculating the stress using Eq. 1.



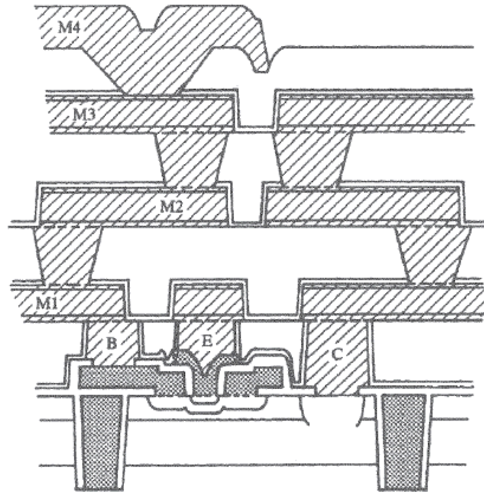


Figure 4: Schematic of a semiconductor device. (a) (Early 2000's) showing full structure, FEOL, BEOL, and packaging (image By Cepheiden https://commons.wikimedia.org/w/index.php?curid=1445444)
(b) (mid-1990's) Crosshatched areas are metal, white areas are dielectric, device components shaded, all sitting on Si (Totta, P.A., S. Khadpe, N.G. Koopan, T.C. Reiley, and M.J. Sheaffer, *CHIP-TO-PACKAGE INTERCONNECTIONS*, in *Microelectronics Packaging Handbook*, R.R. Tummala, E.J. Rymaszewski, and A.G. Klopfenstein, Editors. Springer: Boston MA. p. 129-283 (1997).)

In fact, it is very common in the semiconductor industry to refer to the "layer stress" as the stress that would be needed in a homogeneous layer of the same thickness to produce the observed curvature following Eq. 1 (Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.). This is quite a logical approach that is facilitated by the fact that the properties of the film do *not* enter Eq. 1 at all. That is, if the curvature induced in the substrate as the result of the addition or processing of a layer (or group of layers) with thickness t_f can be measured, the effective stress (also called "average stress" or "net stress") in that layer can immediately be calculated from Eq. 1. In fact, the concept of "stress balancing" is *predicated* upon this approach. If the contributions of the stresses in the different layers *to curvature* can be made to compensate each other so that the *curvature* is zero, the "net stress" (or "average stress" or "effective stress") is said to be zero, even if the stresses in the individual layers are quite high. (While neither of them use the term

"stress balancing" examples showing how to do this experimentally and theoretically are given in US 5,500,312 and in (Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.), respectively.)

Measuring the curvature is quite straightforward and can be accurate. Instruments for such measurements, such as the tools made by Flexus and marketed to the semiconductor manufacturing and research communities, were readily available and widely used. The Flexus tool calculated curvature from the deflection of laser beams reflected from the substrate surface (versions are still available from Toho Technologies). Other methods obtained curvature from capacitive displacement measurements at the wafers edge or used interferometric methods to obtain a map of the wafer shape (e.g. Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.). Any of these methods would have been suitable for obtaining layer stresses from all or some of the layers indicated in Fig. 4 (Nix, W.D., *Mechanical Properties of Thin Films.* Metallurgical Transactions A, 1989. **20A**: p. 2217-2245, Ohring, M., *Materials Science of Thin Films*. 2nd ed., 2002: Academic press., Freund, L. B., and Suresh, S. *Thin Film Materials: Stress, Defect Formation and Surface Evolution*. Cambridge University Press New York, NY, 2003.). A person of ordinary skill in the art would have been aware of these measurement methods and how they work and that the "layer stress" represented an average (in both thickness and width directions) value (also called "average stress" or "net stress"). Practically speaking, these methods have sufficient precision *by definition*.

This is not to say that the inhomogeneous stress states in semiconductors are not of interest to anybody. Since failures due to cracking, delamination, and other mechanisms occur when the peak stress, not the average stress, reaches a critical value, the characteristics of these

inhomogeneous stress states are important to researchers trying to improve device reliability. The local inhomogeneous stresses can be determined, but require more complex measurements such as x-ray diffraction (Clemens, B.M. and J.A. Bain, *Stress Determination in Textured Thin Films Using X-ray Diffraction,* Materials Research Society Bulletin, XVII(7): p. 46-51 (1992)) and Raman spectroscopy (De Wolf, Ingrid, *Stress Measurements in Si Microelectronics Devices using Raman Spectroscopy*, Journal of Raman Spectroscopy 30, 877-884 (1999)) including local probes and more complicated models (compared with Eq. 1). However, this is not within the scope of application of the patents, which focus on integrated circuit fabrication methods.

In my opinion, the average person skilled in the art at the time of the patents would have known and understood the concepts laid out in this section, including the origins of stresses in thin layers and their close tie to curvature, Eq. 1 and the meaning of the terms therein, the concepts of stress and strain both as local and averaged phenomena, and certainly the design and construction of integrated circuits. Specifically, they would have been familiar with substrate curvature stress measurements and would have understood that such measurements return a layer stress, σ_f, which is an average over the layer as described above.

B. THE SCOPE OF THE ASSERTED PATENTS

The patents refer to methods for making 3-D integrated circuit structures. It is well-known that increasing integration (more functionality in a smaller volume) drives the semiconductor industry, leading to ever greater integrated circuit capability at ever decreasing cost (*e.g.* Moore's Law). As semiconductor manufacturing is essentially a planar process (Fig. 4), one means of accomplishing this is to make the devices on the semiconductor surface smaller and smaller so that there can be more devices per unit area and to increase total capability by making the die (the individual integrated circuit "chips" that are cut from the initial large Si wafer) larger. However, this strategy is limited. As the density of wiring increases and individual

die get larger, the average length of the interconnect wires increases, the time it takes for signals to travel from one side of the chip to the other increases, and the quality of those signals is degraded. (An interconnect makes an electrical connection between different parts of an integrated circuit. *E.g.* the metal in Fig.4, shows cross sections through the different interconnect wires in the dielectric layers.) A solution to this problem, that is utilized in the asserted patents, is to stack chip die on top of each other vertically. The average wire length in a 3-D stacked circuit is shorter than that in a 2-D circuit with the same number of devices. A 3-D stacked circuit has additional advantages in that chip die with very different functions, even those made by different processes, can be stacked, creating a "system on a chip," integrating functions that would otherwise be distributed across a large printed circuit board or other large packaging. The performance of a 3-D stacked circuit could be further improved by routing some of the interconnects through the die substrates. (Garrou, P., C. Bower, and P. Ramm, *Handbook of 3-D Integration: Technology and Applications of 3D Integrated Circuits*, Weinheim: Wiley-VCH Verlag; 2008.)

The asserted patents teach about two important concepts that facilitate the manufacture of 3-D integrated circuits. The first is thinning the substrate to make the die "substantially flexible." The second is the use of "low stress" dielectrics. In my opinion, one of the problems described and solved by the patent is this: when stacking die for 3-D integration, it is critical that each die make a continuous contact covering the full area from edge to edge with the die below it. However, no surface is perfectly flat; so how can this contact be made? One way would be to make the die flexible enough that each one can easily adapt its shape to that of the die below it. That flexibility could be obtained, in part, by thinning the substrate. But thinning could lead to the problem that the curvature induced by layer stresses increases as the substrate thickness decrease (see Eq. 1!). Thus, the invention specifies that the *effective* layer stresses (that is, the

stresses that lead to curvature) must be low. Thus, the combination of a substantially flexible substrate and low stresses combine to enhance the manufacturability of 3-D integrated circuitry.

The defendants' experts, Fair and Murray, have provided their interpretations of various terms in defendants' proposed claim constructions in their declarations, dated January 18, 2019. I provide my interpretation of those terms, based on my reading of the asserted patents as well as arguments put forth by Fair and Murray in the following sections. In the interest of time, I have grouped their contentions into a smaller number of categories and have addressed them by category. Time limitations prevent me from verifying that every assertion made by these experts is supported by the cited references. In at least one case, which I noted, the assertion was not supported by the document. Elsewhere, I have treated the assertions as if they were true.

C. LOW STRESS DIELECTRIC

Plaintiff has said that a "low stress dielectric" can be interpreted as "a dielectric having a stress of less that 8×10^8 dynes/cm^2. Defendants have said that these terms are indefinite, and Micron and Samsung have said that, to the extent they are found not to be indefinite, they should be construed to mean: "having stress in the dielectric layer that is between 0 and 5×10^8 in tensile."

Fair and Murray have both responded to this topic in a style that makes the same or similar arguments repeatedly in different sections. I have organized these arguments into a more succinct form and responded to them by category as follows.

Argument C1: Stress is a term of degree which depends on context so a person of ordinary skill in the art would not know what "low stress" meant.

With very few exceptions, *all* physical quantities are terms of degree that depend on context. For example, the concepts of, say, "high" and "low" temperatures will mean very different things to technologists working on blast furnaces for steel mills and on frozen food storage facilities. This argument, as made by Fair and Murray, requires the belief that persons of

ordinary skill in the art in the manufacture of semiconductor circuits have no context within which to place the stress in a dielectric layer. In my opinion, this is not the case.

It was well known before the 1990s that different deposition methods used in different technologies can produce widely different stresses in different dielectric films (Scheuerman, Richard J., *Fabrication of Thin Dielectric Films with Low Internal Stresses*, Journal of Vacuum Science and Technology 7, 143 (1970)., Ohring, Milton *Materials Science of Thin Films: Deposition and Structure* (2nd ed.) Academic Press 2002, Cote, D.R. et al, *Low-temperature chemical vapor deposition processes and dielectrics for microelectronic circuit manufacturing at IBM*, IBM J. Res. Develop., Vol. 39 No. 4 July 1995, Cote, D.R. et al, *Low-temperature chemical vapor deposition processes and dielectrics for microelectronic circuit manufacturing at IBM*, IBM J. Res. Develop., Vol. 39 No. 4 July 1995 (IPR2016-00388 Elm Exhibit 2133), References cited by Fair at 110-112, many others). We can estimate a rough range for these values as follows: Inorganic dielectrics have failure stresses on the order of 10×10^8 to 100×10^8 dynes/cm^2 and elastic moduli on the order of $10{,}000 \times 10^8$ dynes/cm^2. This means, by Hooke's law, that the strain to failure is of order 0.1% up to 1%. Strains of this magnitude are easily generated during deposition and thermal processing, so we can expect to find films with stresses from 0 to about 100×10^8 dynes/cm^2 in order of magnitude. Figure 5 shows a compilation of stresses in a variety of films used in Si devices, as reported in the early 1990's. For the SiO_2 based dielectrics, the estimated range of about 0 to 100×10^8 dynes/cm^2 is seen to be correct. SiN_x type dielectrics typically have even higher stresses.

Residual Stress Values in Films Encountered in Si Devices[a]

Film	Process	Conditions	Stress (GPa)
SiO_2	Thermal	900–1200°C	−0.2 to −0.3
SiO_2	CVD 400°C	40 nm/min	+0.13
SiO_2	$SiH_4 + O_2$	400 nm/min	+0.38
SiO_2	CVD	450°C	+0.15
	TEOS	725°C	+0.02
SiO_2	TEOS	685°C	+0.38
	TEOS + 25% B, P		−0.02
SiO_2	Sputtered		−0.15
Si_3N_4	CVD	450–900°C	+0.7 to +1.2
Si_3N_4	Plasma	400°C	−0.7
		700°C	+0.6
Si_3N_4	Plasma 13.56 MHz	150°C	−0.3
		300°C	+0.02
Si_3N_4	Plasma 50 kHz	350°C	−1.1
Poly Si	LPCVD	560–670°C	−0.1 to −0.3
$TiSi_2$	PECVD	As-deposited	+0.4
		Annealed	+1.2
$TiSi_2$	Sputtered		+2.3
$CoSi_2$	Sputtered		+1.3
$TaSi_2$	Sputtered	800°C anneal	+3.0
$TaSi_2$	Sputtered		+1.2
W	Sputtered	200 to 400 W power	+2 to −2
W	Sputtered	5 to 15 mtorr Ar pressure	−3 to +3
Al			+0.5 to ~+1

Figure 5. Stress levels in some dielectrics used in Si manufacturing in the early 1990's (multiply by 100 to convert GPa to units of 10^8 dynes/cm^2). (Ohring, M., Materials Science of Thin Films. 2nd ed. 2002: Academic press.)

Fair (at 110-112) provides a number of references which he claims demonstrate designations of "low stress" in a variety of dielectrics that range from 0.1×10^8 dynes/cm^2 to 60×10^8 dynes/cm^2. Unfortunately, not all of the publications Fair cites even refer to stresses in dielectrics. US 55009312, for example, refers to "low stresses" obtained in Si/Mo and other multilayer films by stress balancing. But it doesn't matter. Suppose these *were* the stress levels that these practitioners found in actual dielectrics and that they referred to them as "low." The cited papers refer to widely differing materials in widely differing technologies including the average stresses obtained in Si/Mo layers used for x-ray mirrors (US 55009312), for which "low" could be any value arbitrarily close to zero, and silicon nitride dielectrics for

microelectromechanical machines (Temple-Boyer, P., C. Rossi, E. Saint-Etienne, and E. Scheid, Residual stress in low pressure chemical vapor deposition SiN_x films deposited from silane and ammonia. Journal of Vacuum Science & Technology A, 1998. 16(4): p. 2003), for which “low” is relative to conventional stresses well above 100×10^8 dynes/cm^2. To say that the stresses in these vastly disparate layers can or would be somehow inferred to provide a global metric for “low stress” in the dielectric layers used in integrated circuit manufacturing is logically equivalent to saying that the temperatures in blast furnaces and freezers can be used to provide a global metric for “low temperature”.

But a person with ordinary skill in the art of semiconductor manufacturing would not make this mistake with respect to layer stresses. Technologists working in semiconductor manufacturing are *keenly* aware that the layer stresses in the dielectrics in the devices they are building are different than the layer stresses in, for example, x-ray mirrors. They would certainly understand the basic physical concepts of the processes they were considering and what range of layer stress (and other characteristics) was available. They would not compare to “low” or “high” values in dielectrics in unrelated technologies any more than the blast furnace manufacturer would look to food storage freezer technology to determine what temperature could be considered “low”. While it is true that the values of the stresses in different dielectrics that people refer to as “high” or “low” vary significantly from technology to technology, this would not, in my opinion, lead to any confusion about what was meant by “low stress dielectric” with respect to the circuit layers in an integrated circuit on the part of a person with ordinary skill in the art when evaluating the patents in suit.

A person working in the art of semiconductor manufacturing at the time would have had several clear contexts in which to decide whether a stress qualified as “low.” Probably the most common could be described as ‘low relative to the dielectric layer stresses that were common in

conventional integrated circuit manufacturing processes in the past.' Although there is no hard line in this definition, inspection of Figure 5 suggests that, by any reasonable standard, stresses less than about 10×10^8 dynes/cm^2 would have been considered "low" at the time of the asserted patents. A more precise idea can be obtained by looking at the values obtained by research groups who were trying to develop "low stress dielectrics" specifically for these applications in integrated circuits. For example, Temple *et al.*, in 1993 reported stresses of $13 \times 10^8 – 23 \times 10^8$ dynes/cm^2 obtained in a silane-sourced PECVD (plasma-enhanced chemical vapor deposition) SiO_2, a process that could be considered more "conventional" by the time of the patents (Temple, D., A. Reisman, G.G. Fountain, M. Walters, and S.V. Hattangady, *Mechanical-Stress in SiO_2-Films Obtained by Remote Plasma-Enhanced Chemical Vapor Deposition*. Journal of the Electrochemical Society, 1993. 140(2): p. 564-567.). By contrast, Tetsuyo Homma in 1995 focused on developing new SiO_2-based dielectrics specifically designed to meet a range of integrated circuit criteria and reported stresses of 1.7×10^8 to 4.4×10^8 dynes/cm^2, clearly "low" values in his estimation (Homma, Tetsuya, *Fluorinated interlayer dielectric films in ULSI multilevel interconnections*, Jounral of Non-Crystalline Solids 187 (1995) 49-59). Homma's values would have been much lower than stresses in common use anywhere in industry at the time. Robert Wieland provides a table of "properties of different SiO_2 film types as dielectric layer for 3-D integration" listing values from 8×10^8 to 50×10^8 dynes/cm^2 as late as 2008 (Wieland, R. *Chapter 6: SiO_2* in Garrou, P., C. Bower, and P. Ramm, eds. *Handbook of 3-D Integration: Technology and Applications of 3D Integrated Circuits*, Weinheim: Wiley-VCH Verlag; 2008) but notes that the lower value $8 \times 10^8 \times 10^8$ dynes/cm^2 was only achieved by annealing at 620 to 690˚C limiting its use.

Stress is indeed a term of degree that depends on context. In my opinion, a person of ordinary skill in the art of semiconductor manufacturing would have had a very clear context for

what constituted “low stress” with respect to the dielectrics used in integrated circuits, and that stresses less than about 10×10^8 dynes/cm^2 would clearly have been thought of as “low” ca. 1997. Plaintiff’s use of 8×10^8 dynes/cm^2 is comfortably less than this.

Argument C2: Stress in a tensor quantity that requires 6 independent components to define it, and the component or components to which “low stress” applies were not specified, so a person of ordinary skill in the art would not know to which component(s) “low stress” applied.

It is true that “stress” as defined in physics is a tensor quantity. However, stress is almost never used that way in engineering and technology. As described in Section A4 above, the simple geometry of the layer-on-substrate configuration and choice of a coordinate system having two axes in the film plane and one perpendicular to the plane reduces the problem to one stress component, the film stress σ_f in Eq. 1 (also called “layer stress”). A person skilled in the art would have been well aware of this, as well as of the methods available to determine this stress from a substrate curvature measurement using Eq. 1.

Argument C3: There are many “types” of stress and the “type” is not specified so a person of ordinary skill in the art would not know to what “type” of stress to which “low stress” should be applied.

As described in Sec. A4 above, stress is stress. There is no physical distinction between the “types” of stress to which Fair and Murray refer. Terms such as “thermal stress,” “intrinsic stress,” “growth stress,” and many others are commonly used across many different industries that depend on thin film and coating technology to distinguish among different potential sources of stress. These distinctions would be of interest to a person who was interested in finding ways to modify a process to change the stress, but this is not the area of application of the asserted patents. But a person skilled in the art reading these patents would be concerned with stress primarily as it affects curvature and there is only one “layer stress” regardless of whether it arose from differential thermal strains or any other type of differential strain, and that layer stress is easily measured. A person of ordinary skill in the art would not have this confusion.

Argument C4: The stresses in an integrated circuit layer are inhomogeneous and the patent does not specify where in the layer to measure stress, so a person of ordinary skill in the art would not know where to measure to determine if stress was "low".

It is obvious from Fig. 4 that the layers in an integrated circuit are inhomogeneous. In addition to dielectrics (the main component), they also contain metallization lines and occasionally other components. It is also clear that the stresses around each dissimilar material will be inhomogeneous. However, the layer, inhomogeneous though it is, exerts a net force on the substrate, causing it to curve. Within a set of conditions that are handily met in typical integrated circuits, the curvature adopted by the substrate accurately reflects the average stress within that layer, which can be thought of as the stress in a layer of the same thickness needed to produce the measured curvature. Since it is the average stress that is correlated with the substrate curvature (via Eq. 1), the layer stress is the only value needed. A person of ordinary skill in the art of semiconductor manufacturing would be well aware of this.

The distribution of stress values in the layer, as discussed by Fair and Murray, would be of interest primarily to a person studying failure modes in the layer, which is not the area of application of the asserted patents.

This point bears emphasis. This is not just a feature of stress measurements in thin layers in semiconductors but is rather the default mode of operation in virtually all of engineering. The vast majority of materials are inhomogeneous. For example, a typical uniaxial tension test sample (as described in section A3 above) consists of many small crystallites with different sizes, shapes, and orientations, as well as a variety of different phases, and each of these entities is anisotropic. The result is that, when the sample is stretched, a very inhomogeneous stress state is created. If one had the ability to measure the stress at different points in the sample, very different values would be obtained. But in the vast majority of applications, this does not matter. What matters is how much load the sample can support at a given strain, which is accurately

represented by the average stress. As in the thin layer case, a researcher who is interested in failure modes or in a deeper interpretation of deformation mechanisms might care about the actual distribution of stresses, but this would be the exception. The fact that a person of ordinary skill in the art of semiconductor manufacturing would be interested in (and satisfied with) the layer stress (as the average or net stress) is completely consistent with the way stresses in materials are treated across science and engineering.

Argument C5: Different stress measurement methods produce different answers and the measurement method was not specified, so a person of ordinary skill in the art would not know how to measure stress.

This argument is incorrect. The concept of the stress in a layer as well as a simple method to measure it, both as described above, were both well known to persons of ordinary skill in the art of semiconductor manufacturing (and indeed in a wide swath of industries that depend on thin films, layers, and coatings). There is no reason to assume that such a person would turn to a more complex and expensive method to accomplish what would otherwise be a simple task. To the extent that different stress measurement methods measure different stress components or measure in different directions, or measure at different locations, the values they return could be different. A person of ordinary skill in the art would not attempt to compare these non-comparable values and would have known how to obtain good values. But if different methods were used to obtain the same stress components in the same direction at the same location (*e.g.* the layer stress shown in Fig. 3), the results would be the same within experimental error. A person with ordinary skill in the art would know this. For example, one could use different measures to determine the layer stress in Fig. 3, which is the subject of the asserted patents.

Argument C6: Stress balancing.

Fair at 96 writes, "No matter how interpreted, the "have stress of 5×10^8 dynes/cm^2 or less" and similar terms do not embrace stress balancing." It is frankly difficult to determine what

point he is trying to make here, as well as in 97, 98, 99, and 100. Similarly, Murray at 47 writes that "The term stress balancing" does not appear in any of the claims of the Asserted Patents…". Fair seems to be saying that "intrinsically low stress" and "stress balancing" are distinct, which is true. As to Murray's observation about what the claims say, I would defer to the patents. It is not clear what the objective of all this argumentation is, but in my opinion, the meaning of the text in the asserted patents is quite clear.

In the '239 patent at 9:7-16, the inventor writes:

> "The use of dielectrics with conventional stress levels could be used in the assembly of a 3DS DRAM circuit, however, if more than a few layers comprise the stacked assembly, each layer in the assembly will have to be stress balanced so that the net stress of the deposited films of a layer is less than 5×10^8 dynes/cm^2. The use of intrinsically low stress deposited films is the preferred method of fabrication versus the use of the method where the stress of individually deposited films are not equal but are deposited to create a net balanced lower stress."

Since the goal of the asserted patent is to assemble stacked die, the intent of the "low stress" is clear—to reduce curvature. Since the layer stress is *always* the net stress, whether it is the effects of a single layer that is measured or of all of the circuit layers simultaneously, the inventor is simply making clear that it is possible to obtain a low layer stress either by ensuring that each layer has an "intrinsically low stress" (here clearly meant to indicate the stress associated with each single layer is low), or, if "more than a few" individual layers with high ("conventional stress levels") are included, the stress will have to be balanced so that the net stress reaches the standard for "low stress" that he lays out. For these reasons, and the logic governing how stress is measured, discussed above, I understand that his use of the term "low stress" applies equally to both of these cases.

Argument C7: The concept of "low stress dielectric" is restricted to tensile stresses.

Fair and Murray both note at several points that the term "low stress" is restricted to apply only to tensile stresses. The primary motivation for this seems to come from the '239

patent at 9:4-5 where the inventor writes, "Such low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695 of the present inventor, incorporated herein by reference."

The '695 patent is about a *different* technology regarding the production of integrated circuits on free-standing membranes. In the '695 patent at 5:68–6:5, he writes (emphasis added):

> "If the **membrane** in not in tensile stress, but in compressive stress, surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing **membrane**."

He later, at 11:33, defines low stress to be less than 8×10^8 dynes/cm^2.

Stress is one of many characteristics one considers when determining how a particular dielectric is implemented in a given technology. Here, although the '695 states the value of a low stress that could be applied to the layer stress of dielectrics used in integrated circuits, it does not follow that, in the patents at issue here, this value would be restricted to tensile stress.

I understand the reference to the '695 patent to be a reference to a particular use case for a low stress dielectric as a membrane. To form the membrane in the '695 patent, he deposits the dielectric and removes a section of the substrate behind it. For a free-standing membrane, that stress has to be tensile. In compression, it would buckle and wrinkle and could not be used as a membrane.

But a person of skill in the art would not read the "tensile" stress in the membrane in the '695 patent to mean that all low stress dielectrics were in tensile stress. In most applications, including the integrated circuits in the '239 and other patents, the sign of the stress does not matter. If it's tensile it curves up, if it's compressive, it curves down, but regardless a stress of a given magnitude leads to a certain curvature (by Eq. 1). The patent is concerned with low stress to minimize curvature, whether it is up or down. It *is* logical to tie "tensile" to "membrane" however, for the reason described above. But in my opinion, a person of ordinary skill in the art

would not make an artificial link of "low stress" and "tensile" when the obvious link is "tensile" and "membrane."

D. STRESS OF 8 × 10^8 dynes/cm^2

As I pointed out above, there are clear contexts in which one could consider a stress to be "low." From the perspective of an individual layer, stresses in typical Si-based dielectrics vary from 0 to about 100 × 10^8 dynes/cm^2 (for SiO_2, considerably higher for SiN_x). Because of the large value of Young's modulus (typically a strain of only 0.1% is needed to obtain stresses of order 10 × 10^8 dynes/cm^2), and because the differential strains imposed by layer deposition and processing steps can be large, the layer stresses in dielectric layers tend towards the higher end of this spectrum rather than the lower. It takes effort to obtain a low stress film. In this sense, stresses less than about 10 × 10^8 dynes/cm^2 would have been regarded as "low" and 8 × 10^8 dynes/cm^2 fits comfortably into that range, and can be measured, as discussed above.

Another context is 'low enough to achieve a certain function,' in this case to achieve an integrated circuit chip that is simultaneously flexible enough and flat enough to be stacked. I read the specification of the patents, including the reference to the '695 patent to indicate that the inventor is suggesting that, for the example technology he is describing (DRAM on Si substrates thinned to about 50 μm and polished) a stress of 8 × 10^8 dynes/cm^2 or less would be suitable.

In either case it is clear that the inventor is referring to the stress that produces the curvature. This would be the "net stress," which could be made low either by ensuring that all (or nearly all) of the individual layers have low stress, or by stress balancing.

E. SUBSTANTIALLY FLEXIBLE

Another feature of the patents is the teaching that making a semiconductor integrated circuit die sufficiently flexible will facilitate die stacking for the purpose of making 3-D integrated circuits. As described above, one interpretation of this is that flexibility facilitates the

formation of good bonds that extend from edge to edge across the width of the die in the inevitable case that the die being stacked are not perfectly flat. This also necessitates the requirement for a sufficiently low net stress as described in detail above.

Plaintiff has said that “a substantially flexible substrate” can be interpreted following the plain and ordinary meaning as “…a substrate / semiconductor layer that is largely able to bend without breaking.” Similar arguments are made for “substantially flexible integrated circuit” and related phrasings, and for “dice that are substantially flexible” and related phrasings. Since these all clearly refer to the same thing in the patents—specifically that making a semiconductor integrated circuit die sufficiently flexible will facilitate die stacking for the purpose of making 3-D integrated circuits as described above—I treat these together.

Defendants have said that the “substantially flexible substrate” formulation should be construed as “[substrate / semiconductor layer] that has been thinned to a thickness of less than 50 microns and subsequently polished or smoothed” and that both the “substantially flexible integrated circuit” formulation and the “dice that are substantially flexible” formulation should be construed as “[integrated circuit[s] / integrated circuit layer[s] / stacked integrated circuit structure /structure] that contains a substantially flexible substrate where the dielectric material used in processing the substrate has a stress of 5×10^8 dynes/cm^2 tensile or less”.

Only Fair responded to this topic, and, as before, he did so in a style that makes the same arguments repeatedly in different sections. I have organized these arguments into a more succinct form and responded to them in categories as follows.

Argument E1: Flexibility is a term of degree which depends on context so a person of ordinary skill in the art would not know what “substantially flexible” meant.

This argument uses the same logic that was used in Argument C1 above. Here Fair’s argument requires the belief that persons of ordinary skill in the art in the manufacture of semiconductor circuits have no context within which to judge when a semiconductor integrated

circuit die was "substantially flexible". In my opinion, this is not the case. Flexibility, like *all* other physical quantities that are terms of degree depend on context. Here, the context is clear, the semiconductor integrated circuit die must be flexible enough to facilitate die stacking for the purpose of making 3-D integrated circuits. This could be viewed as being flexible enough that subsequent die can conform to the shape of the substrate or previously die on which they are to be stacked. Equivalently, one can imagine that if a stiff (*i.e.* not sufficiently flexible) die were used, it could be forced to bond across its width by applying pressure to force it to conform to the surface below it, but such die would retain bending stresses that could make them "pop off" when the bonding pressure was removed. Comparisons with use of the term "flexible" to refer to materials and/or applications other than those envisioned in the patents (*e.g.* Fair at 51, 52, 54) are spurious.

Argument E2: There are different "types" of flexibility and the "type" is not specified so a person of ordinary skill in the art would not know to what "type" of flexibility "substantially flexible" applied.

While it is true that "flexibility" could be applied to bending, tension, or torsion, as noted by Fair at 65, it is clear that the intent of the patent is to facilitate die stacking for the purpose of making 3-D integrated circuits. In this application, flexibility in bending is clearly meant.

Argument E3: 'The Elm construction changes a flexibility requirement into a non-fracture requirement' and derivative arguments.

The plain meaning of flexible, writ large, is to deform without breaking. There are two ways in which an object can be inflexible: First is can be stiff and strong enough that it doesn't deform appreciably under a relevant load (doesn't bend). Second, it can break upon application of that load. The Elm construction simply negates both of these attributes of inflexibility. Interpretation of this term in no way requires a specification of a fracture load, any more than it requires a specification of elastic constants. The concept that this "changes a flexibility requirement into a non-fracture requirement" is an artifice introduced by Fair that is not even

logical, much less a concept inferred by the patent. A flexibility requirement *is* a non-fracture requirement.

A person does *not* need to know what the fracture stress is to know that a die is flexible enough to be stacked. How much higher the fracture load is than the applied load is irrelevant. The description of fracture and the long list of fracture studies at Fair 57-59 is therefore irrelevant. Yes, it is true that fracture loads are widely statistically distributed and that different surface treatments in different technologies, even in the same material, are widely different. But there is no requirement that a manufacturer be able to predict when fracture might occur in order to understand whether an object is flexible in the context of semiconductor manufacturing described in the patent. A person of ordinary skill in the art of semiconductor manufacture would certainly not try to turn a requirement for flexibility into a fracture mechanics study.

Argument E4: General conflation of flexibility with polishing and smoothing.

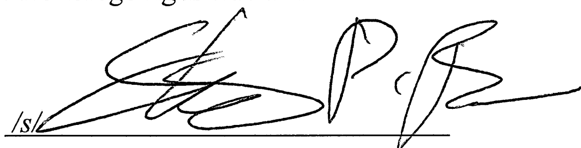
In the defendant's construction, they attempt to conflate flexibility with polishing and smoothing. I understand the inventor is providing an example of a "substantially flexible substrate" as one that has been thinned to 50 µm or below and polished and smoothed. In semiconductor manufacturing, silicon (and other) substrates are thinned using a grinding process (sometimes called "backside grind") that creates a highly damaged region. (Garrou, P., C. Bower, and P. Ramm, *Handbook of 3-D Integration: Technology and Applications of 3D Integrated Circuits*, Weinheim: Wiley-VCH Verlag; 2008.) That region is highly stressed (due to structure evolution strains in the damaged silicon) and, just like the stresses in the dielectric layers, would cause the substrate (and all attached layers) to curve. Polishing and smoothing is intended to remove this damaged layer. The inventor includes this requirement to ensure that the substrate remains flat. In addition, the damaged region contains many flaws and it is well known that these flaws facilitate fracture. In this sense, polishing and smoothing *is* intended to help ensure

flexibility by eliminating these fracture sources. However, there are many alternative methods for thinning that do not require grinding. If one of these alternative methods for thinning (for example, etching or a release layer) were used, there would be no need for subsequent polishing and smoothing, either to reduce stresses or to improve fracture resistance. A person of ordinary skill in the art would realize that polishing and smoothing are not required for flexibility, for example, in cases that do not require grinding.

Argument E5: Flexibility is undesirable.

At 60 and 61, Fair writes that "Elm's proposed construction of "substantially flexible substrate" is incorrect because it focuses on bending and bending to some extent without breaking. Both of these concepts conflict with the subject matter of the patents, which focus on the stacking of IC layers." And he goes on to explain that a person of ordinary skill in the art would know that to stack and bond circuit layers, the substrate would need to be "sufficiently planar." Fair then states, "Thus, bending a large amount without breaking would interfere with the ability of memory circuits to bond together so as to be stacked in layers." The intent of this argument is unclear. If die must remain flat as described in the patents, then, by Eq. 1, they must either have low stresses or thick substrates, and if any curvature remains, they must be separately planarized after dicing so that they can be assembled. An alternative might be to stack stiff curved substrates, but use sufficient vertical force to flatten them, creating stresses that could make them fail. Substantial flexibility allows die to bend slightly to adapt to imperfections, while taking advantage of other benefits of thin substrates. In my opinion, Fair is failing to consider ways in which the patent could be implemented, ways which I think a person of ordinary skill in the art would readily deem reasonable.

I declare under penalty of perjury that the foregoing is true and correct.

/s/ 

Shefford Baker

Dated: January 25, 2019

Exhibit A

SHEFFORD P. BAKER

CORNELL UNIVERSITY
DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING
BARD HALL 210
ITHACA, NY 14853-1501
OFFICE: 607 255 6679 FACSIMILE: 607 255 2365
ELECTRONIC MAIL: shefford.baker@cornell.edu
WEB: http://www.ccmr.cornell.edu/~baker

EDUCATION

1993 Ph.D. in Materials Science and Engineering, Stanford University
Dissertation Title: "Understanding Depth-Sensing Indentation Experiments and Mechanical Properties of Compositionally-Modulated Au-Ni Thin Films"
Dissertation Advisor: William D. Nix

1988 M.S. in Materials Science and Engineering, Stanford University

1984–1986 Mechanical Engineering coursework: University of New Mexico, Albuquerque; University of Wisconsin, Madison; and University of Wyoming, Laramie

1982 Bachelor of Music, With Distinction, Univ. of New Mexico, Albuquerque

PROFESSIONAL APPOINTMENTS

2004–present Associate Professor, Cornell University, Department of Materials Science and Engineering

1998–2003 Assistant Professor, Cornell University, Department of Materials Science and Engineering

1993–1997 Staff Scientist, Max-Planck-Institut für Metallforschung, Stuttgart, Germany

1987–1992 Research Assistant/Teaching Assistant, Department of Materials Science and Engineering, Stanford University

1985–1986 Research Assistant/Teaching Assistant, Department of Mechanical Engineering, University of New Mexico, Albuquerque

1977–1984 Professional musician and music teacher, including performance, recording, and studio, contract, and public school instruction

HONORS

- Sonny Yau '72 Excellence in Teaching Award, Cornell University College of Engineering, 2002

- Outstanding Educator, Mentor to Merrill Presidential Scholar Deborah Schorr, Cornell University, 2000
- Robert ’55 and Vanne ’57 Cowie Excellence in Teaching Award, Cornell University College of Engineering, 1999
- CAREER Award, National Science Foundation, 1999
- Graduate Student Award, Materials Research Society, 1990
- Scripta Metallurgica and Materialia Outstanding Paper Award for 1990, for the paper “On the Question of Strain Rate Continuity in Stress Rate Change Experiments” by C.-M. Kuo, K.R. Forbes, S.P. Baker, and W.D. Nix
- Kappa Mu Epsilon (mathematics honorary), University of New Mexico, 1984
- Phi Kappa Phi (honorary), University of New Mexico, 1982
- Presser Foundation Scholar (fine arts), Presser Foundation 1980-1981

PROFESSIONAL ACTIVITIES

Memberships

Materials Research Society (Publications Committee Chair 2015-present, President 2009, Vice President 2008, Board of Directors 2005-2007), The American Ceramics Society, The Minerals Metals and Materials Society

Meetings, Workshops, and Symposia Organized

- “Fifth International Conference on Materials Processing Defects,” Cornell University, Ithaca, NY, 18-20 July, 2007, with Paul Dawson, Matthew Miller, and Alan Zehnder
- “Seventh International Workshop on Stress-Induced Phenomena in Metallization,” Austin, TX, 14-16 June 2004, with Paul S. Ho, Tomoji Nakamura, and Cynthia A. Volkert
- Co-chair of the 2004 Fall Meeting of the Materials Research Society in Boston, with Julia W.P. Hsu, Bethanie J Hills Stadler, and Richard A. Vaia
- “Sixth International Workshop on Stress-Induced Phenomena in Metallization,” Cornell University, Ithaca, NY, July 25–27, 2001, with Matti A. Korhonen, Eduard Arzt, and Paul Ho
- “Dislocations and Deformation Mechanisms in Thin Films and Small Structures,” Symposium at the Materials Research Society 2001 Spring Meeting, San Francisco, CA, April 17-19, 2001, with Oliver Kraft, Klaus Schwarz, Robert Hull, and L. Ben Freund
- “Fundamentals of Nanoindentation and Nanotribology II,” Symposium at the Materials Research Society 2000 Fall Meeting, Boston, MA, November 28–30, 2000, with Robert F. Cook, Sean G. Corcoran, and Neville R. Moody

- “Fundamentals of Nanoindentation and Nanotribology,” Symposium at the Materials Research Society 1998 Spring Meeting, San Francisco, CA, April 13-17, 1998, with Neville R. Moody, William W. Gerberich, and Nancy Burnham
- “Thin Films: Stresses and Mechanical Properties VI,” Symposium at the Materials Research Society 1996 Spring Meeting, San Francisco, CA, April 8-12, 1996, with William W. Gerberich, Huajian Gao, and Jan-Eric Sundgren
- “Mechanical Characterization of Materials in Microsystems Technology/Nanoindentation Workshop” Max-Planck-Institut für Metallforschung in Stuttgart, 5-6 October, 1995, with Dietrich Munz
- “Thin Films: Stresses and Mechanical Properties V,” Symposium at the Materials Research Society 1994 Fall Meeting, Boston, MA, November 28–December 2, 1994, with Caroline A. Ross, Paul H. Townsend, Cynthia A. Volkert, and Peter Børgesen

Professional Tutorials

- “Tools and Techniques for Nanomechanical Testing of Biomaterials: The need for nanoscale mechanical testing in biomaterials” Materials Today Webinar, June 4, 2010
- “Measuring Mechanical Properties in the Nanometer Regime” (MRS webcast) taught at the Materials Research Society 2000 Fall Meeting, Boston, MA, November 26, 2000
- “Measuring Mechanical Properties in the Nanometer Regime,” taught at the Materials Research Society 1998 Spring Meeting, San Francisco, CA, April 12, 1998
- “Mechanical Properties of Thin Films” taught at the Materials Research Society 1996 Spring Meeting, San Francisco, CA, April 7, 1996
- “Mechanical Properties of Thin Films” taught at the Materials Research Society 1994 Fall Meeting, Boston, MA, November 27, 1994

Peer Reviews

Journal Publications: Nature, Scripta Materialia, Acta Materialia, Journal of Materials Research, Journal of Applied Physics, Applied Physics Letters, Materials Science and Engineering A, Thin Solid Films, Philosophical Magazine A, Philosophical Magazine Letters, Journal of the Physics and Chemistry of Solids, Modelling and Simulation in Materials Science and Engineering, Science, Journal of Orthopaedic Research, Journal of Applied Mechancis, Tribology Letters, Experimental Mechanics, Europhysics Letters, Engineering Fracture Mechanics

Proposals: National Science Foundation, Army Research Office, Department of Energy, Petroleum Research Fund, National Research Council, Swiss National Science Foundation

PUBLICATIONS

Refereed Publications

54. Elizabeth A.I. Ellis, Markus Chmielus, and Shefford P. Baker, "Effect of sputter pressure on Ta thin films: Beta phase formation, texture, and stresses" Acta Materialia **150** 317e326 (2018)
53. Yi-Yeoun. Kim, Joseph D. Carloni, Beatrice Demarchi, David Sparks, David G. Reid, Miki E. Kunitake, Chiu C. Tang, Melinda J. Duer, Colin L. Freeman, Boaz Pokroy, Kirsty Penkman, John H. Harding, Lara .A. Estroff, Shefford P. Baker, and Fiona C. Meldrum, "Tuning hardness in calcite by incorporation of amino acids" Nature Materials, **15**(8) 903-910 (2016) doi: 10.1038/nmat4631
52. Yi-Yeoun Kim, Mona Semsarilar, Joseph D. Carloni, Kang Rae Cho, Alexander N. Kulak, Iryna Polishchuk, Coit T. Hendley IV, Paul J. M. Smeets, Lee A. Fielding, Boaz Pokroy, Chiu C. Tang, Lara A. Estroff, Shefford P. Baker, Steven P. Armes, and Fiona C. Meldrum, "Structure and Properties of Nanocomposites Formed by the Occlusion of Block Copolymer Worms and Vesicles Within Calcite Crystals." *Advanced Functional Materials*, **26**(9) 1382-1392 (2016) doi: 10.1002/adfm.201504292
51. Luiz E. Ferri, Kyle C. Hoff, Shefford P. Baker, "Double torsion measurements of the brittle to ductile transition temperature in calcium aluminosilicate glasses" *International Journal of Applied Glass Science*, **7**(4) 532-544 (2106) doi: 10.1111/ijag.12188
50. Elizabeth A. Ellis, Markus Chmielus, Ming-Tzer Lin, Howie Joress, Kyle Visser, Arthur Woll, Richard P. Vinci, Walter L. Brown, and Shefford P. Baker, "Driving forces for texture transformation in thin Ag films" *Acta Materialia*, **105** 495-504 (2016) doi: 10.1016/j.actamat.2015.12.020
49. Rui-qi Song, Tobias N. Hoheisel, Hiroaki Sai, Zihui Li, Joseph D. Carloni, Suntao Wang, Randall .E. Youngman, Shefford P. Baker, Sol M. Gruner, Ulrich Wiesner, Lara A. Estroff "Formation of Periodically-Ordered Calcium Phosphate Nanostructures by Block Copolymer-Directed Self-Assembly" *Chemistry of Materials*, **28**(3) 838-847 (2016) doi: 10.1021/acs.chemmater.5b04266
48. Grace Kim, Jacqueline H. Cole, Adele L. Boskey, Shefford P. Baker, and Marjolein C. H. van der Meulen, "Reduced tissue level stiffness and mineralization in osteoporotic cancellous bone" *Calcified Tissue International* 95(2) 125-131 (2014)
47. Shefford P. Baker, Krishanu Saha, and Jonathan B. Shu, "Effect of thickness and Ti interlayers on stresses and texture transformations in thin Ag films during thermal cycling" *Applied Physics Letters* **103** 191905 (2013)
46. Shefford P. Baker, Brandon Hoffman, Lindsay Timian, Adam Silvernail, and Elizabeth A. Ellis, "Texture transformations in Ag thin films" *Acta Materialia* **61**(19) 7121-7132 (2013)
45. Miki E. Kunitake, Shefford P. Baker, and Lara A. Estroff , "The Effect of Magnesium Substitution on the Hardness of Synthetic and Biogenic Calcite" *MRS Communications* **3**(1) 79-79 (2013)
44. Miki E. Kunitake, Lauren M. Mangano, John M. Peloquin, Shefford P. Baker, and Lara A. Estroff, "Evaluation of strengthening mechanisms in calcite single crystals from mollusk shells" *Acta Biomaterialia* **9**(2) 5353-5359 (2013)

43. Jayme C Burket, Daniel J. Brooks, Jennifer M MacLeay, Shefford P. Baker, Adele L. Boskey, Marjolein C. H. van der Meulen, "Variations in nanomechanical properties and tissue composition within trabeculae from an ovine model of osteoporosis and treatment" *Bone*, **52**(1) 326-336 (2013)

42. Grace Kim, Adele L. Boskey, Shefford P. Baker, and Marjolein C. H van der Meulen, "Improved prediction of rat cortical bone mechanical behavior using composite beam theory to integrate tissue level properties" *Journal of biomechanics* 45 2784-2790 (2012)

41. Ray S. Fertig III and Shefford P. Baker, "Capture cross section of threading dislocations in thin films" *Materials Science and Engineering A* 551 67-72 (2012)

40. Ray S. Fertig III and Shefford P. Baker, "Threading dislocation interactions in an inhomogeneous stress field: A statistical model" *Scripta Materialia* **65**(5) 384-387 (2011)

39. Jayme Burket, Samuel Gourion-Arsiquaud, L.M. Havill, Shefford P. Baker, Adele L. Boskey, and Marjolein C.H. van der Meulen, "Microstructure and nanomechanical properties in osteons relate to tissue and animal age" *Journal of Biomechanics* **44**(2) 277-284 (2011)

38. Aaron M. Vodnick and Shefford P. Baker, "Strain transfer and inhomogeneous deformation in passivated thin films with mixed texture" *Acta Materialia* **59**(14) 5681-5691 (2011)

37. Eve Donnelly, Dan X. Chen, Adele L. Boskey, Shefford P. Baker, and Marjolein C. H. van der Meulen, "Contribution of mineral to bone structural behavior and tissue mechanical properties" *Calcified Tissue International* **87**(5) 450-460 (2010)

36. Ray S. Fertig III and Shefford P. Baker, "Dislocation dynamics simulations of dislocation interactions and stresses in thin films" *Acta Materialia* **58**(15) 5206-5218 (2010)

35. Aaron Vodnick, David E. Nowak, and Stephane Labatt, Olivier Thomas, and Shefford P. Baker, "Out-of-plane stresses arising from grain interactions in textured thin films,"Acta Materialia **58**(7) 2452-2463 (2010)

34. Eve Donnelly, Adele L. Boskey, Shefford P. Baker, Marjolein C. H. van der Meulen, "Effects of tissue age on bone tissue material composition and nanomechanical properties in the rat cortex" *Journal of Biomedical Materials Research A* **92A**(3) 1048-1056 (2010)

33. Ray S. Fertig and Shefford P. Baker, "Simulation of dislocations and strength in thin films: A review" *Progress in Materials Science*, **54**(6) 874-908 (2009)

32. Catherine M. Oertel, Shefford P. Baker, Annika Niklasson, Lars-Gunnar Johansson, and Jan-Erik Svensson "Acetic Acid Vapor Corrosion of Lead--Tin Alloys Containing 3.4 and 15% Tin" *Journal of The Electrochemical Society* **156**(12) C414-C421 (2009)

31. Jon F. Ihlefeld, Aaron M. Vodnick, Shefford P. Baker, William J. Borland, and Jon-Paul Maria, "Extrinsic scaling effects on the dielectric response of ferroelectric thin films" *Journal of Applied Physics* **103**(7) 074112 (2008)

30. Robert Knepper and Shefford P. Baker, "Coefficient of thermal expansion and biaxial elastic modulus of β phase tantalum thin films" *Applied Physics Letters,* **90**, 181908 (2007)

29. Cormac J. Byrne, Aaron M. Kueck, Shefford P. Baker, and Paul H. Steen "In-situ manipulation of cooling rates during planar-flow melt-spinning processing" *Materials Science and Engineering A* 459 172-181 (2007)

28. Robert Knepper, Blake Stevens, and Shefford P. Baker, "Effect of oxygen on the thermomechanical behavior of tantalum thin films during the β–α phase transformation" *Journal of Applied Physics* **100**(12) 123508 (2006)

27. D. E. Nowak, D. R. Blasini, A. M. Vodnick, B. Blank, M. W. Tate, A. Deyhim, D.-M. Smilgies, H. Abruña, S. M. Gruner, and S. P. Baker, "A six-circle diffractometer with atmosphere- and temperature-controlled sample stage and area and line detectors for use in the G2 experimental station at CHESS" *Review of Scientific Instruments,* **77** (11) 113301 (2006)

26. Eve Donnelly, Rebecca M. Williams, Seth A. Downs, Michelle E. Dickinson, Shefford P. Baker, and Marjolein C.H. van der Meulen, "Quasistatic and dynamic nanomechanical properties of cancellous bone tissue relate to collagen content and organization" *Journal of Materials Research*, **21**(8) 2106-2117 (2006)

25. Eve Donnnelly, Shefford P. Baker, Adele L. Boskey, and Marjolein C.H. van der Meulen, "Effects of surface roughness and maximum load on the mechanical properties of cancellous bone measured by nanoindentation*" Journal of Biomedical Materials Research*, **77A** 426-435 (2006)

24. Mengzhi Pang and Shefford P. Baker, "Quantitative Measurements of Subcritical Debonding of Cu Films from Glass Substrates" *Journal of Materials Research,* 20(9) 2420-2431 (2005)

23. J.B. Shu, S.Clyburn, T.E. Mates, and S.P. Baker, "Effect of Oxygen on the Thermomechanical Behavior of Passivated Cu Thin Films" *Journal of Materials Research,* **18**(9) 2122-2134 (2003)

22. P. Pant, K.W. Schwarz, and S.P. Baker, "Dislocation Interactions in Thin FCC Metal Films" *Acta Materialia,* **51**(11) 3243-3258 (2003)

21. S.P. Baker, R.-M. Keller-Flaig, and J.B. Shu, "Bauschinger Effect and Anomalous Deformation Induced by Oxygen in Passivated Thin Cu Films on Substrates" *Acta Materialia,* **51**(10) 3019-3036 (2003)

20. H.T. Hesemann, P. Müllner, O. Kraft, D.E. Nowak, K. Finkelstein, S.P. Baker, and E. Arzt, "Texture Dependence of the Martensitic Transformation in Cobalt Thin Films," *Scripta Materialia,* **48**(8) 1129-1133 (2003)

19. S.P. Baker, L. Zhang, and H. Gao "Effect of Dislocation Core Spreading on the Strength of Thin Films" *Journal of Materials Research* **17**(7) 1808-1813 (2002)

18. H. Gao, L. Zhang, and S.P. Baker, "Dislocation Core Spreading at Interfaces Between Metal Films and Amorphous Substrates" *Journal of the Mechanics and Physics of Solids* **50**(10) 2169-2202 (2002)

17. S.P. Baker, X. Wang, and C.-Y. Hui, "Effect of Non-Linear Elastic Behavior on Bilayer Decohesion of Thin Metal Films from Nonmetal Substrates" *Journal of Applied Mechanics*, **69**(4) 407 (2002)

16. S.P. Baker, A. Kretschmann, and E. Arzt, "Thermomechanical Behavior of Different Texture Components in Cu Thin Films" *Acta Materialia* **49** 2145-2160 (2001)
15. M. Kunert, O. Kienzle, B. Baretzky, S.P. Baker, and E.J. Mittemeijer, "Hardness-Depth Profile of a Carbon-Implanted Ti-6Al-4V Alloy and its Relation to Hardness and Microstructure" *Journal of Materials Research* **16**(8) 2321-2335 (2001)
14. M. Kunert, B. Baretzky, S.P. Baker, and E.J. Mittemeijer, "Hardness-Depth Profiling on Nanometer Scale" *Materials Transactions A*, **32A** 1201-1209 (2001)
13. S.P. Baker, "Plastic Deformation and Strength of Materials in Small Dimensions" *Materials Science and Engineering A,* **A319-32***,* 16-23 (2001)
12. S.P. Baker, "Nanoindentation Techniques" in *The Encyclopedia of Materials Science and Technology* (Pergamon, Oxford, 2001)
11. N. Burnham, S.P. Baker, and H. Pollack, "Model for Mechanical Property Nanoprobes" *Journal of Materials Research* **15**(9) 2006-2014 (2000)
10. S.P. Baker, Y.-C. Joo, M.P. Knauß, and E. Arzt, "Electromigration Damage in Mechanically Deformed Al Conductor Lines: Dislocations as Fast Diffusion Paths" *Acta Materialia* **48** 2199-2208 (2000)
9. Y.-C. Joo, C.V. Thompson, S.P. Baker, and E. Arzt, "Electromigration Proximity Effects of Two Neighboring Fast-Diffusion Segments in Single-Crystal Aluminum Lines" *Journal of Applied Physics* **85**(4) 2108-2113 (1999)
8. R.-M. Keller, S.P. Baker, and E. Arzt. "Stress-Temperature Behavior of Unpassivated Thin Copper Films" *Acta Materialia* **47**(2) 415-426 (1999)
7. Y.-C. Joo, S.P. Baker, and E. Arzt, "Electromigration in Single-crystal Aluminum Lines with Fast Diffusion Paths made by Nanoindentation" *Acta Materialia*, **46**(6) 1969-1979 (1998)
6. R.-M. Keller, S.P. Baker, and E. Arzt, "Quantitative Analysis of Strengthening Mechanisms in Thin Cu Films: Effects of Film Thickness, Grain Size, and Passivation" *Journal of Materials Research* **13**(5) 1307-1317 (1998)
5. S.P. Baker, "Between Nanoindentation and Scanning Force Microscopy: Measuring Mechanical Properties in the Nanometer Regime" *Thin Solid Films* **308-309** 289-296 (1997)
4. S.P. Baker and W.D. Nix, "Intrinsic Stresses in Compositionally Modulated Au-Ni Thin Films and the Supermodulus Effect," *Journal of Materials Research* **9**(12) 3145 (1994)
3. S.P. Baker and W.D. Nix, "Mechanical Properties of Compositionally Modulated Au-Ni Thin Films: Nanoindentation and Microcantilever Deflection Experiments," *Journal of Materials Research* **9**(12) 3131 (1994)
2. S. Bader, S.P. Baker, W.-M. Kuschke and E. Arzt, "Mechanische Eigenschaften und Zuverlässigkeit von Materialien in Mikrodimensionen" ("Mechanical Properties and Reliability of Materials in Microdimensions," in German), *Metall* **48**(3) 370 (1994)
1. C.-M. Kuo, K.R. Forbes, S.P. Baker and W.D. Nix, "On the Question of Strain Rate Continuity in Stress Rate Change Experiments," *Scripta Metall.* **24** 1623 (1990)

Other Publications

17. David S. Ginley, Shefford P. Baker and James J. De Yoreo "Diversity in MRS and in MRS leadership: Use your vote" *Materials Research Society Bulletin* 35(9) 638 – 639 (2010)

16. Shefford P. Baker, "Make the MRS "House" your home," *Materials Research Society Bulletin* 34(12) 891 (2009)

15. Shefford P. Baker "What is MRS All About, Really?" *Materials Research Society Bulletin* **34**(11) 781 (2009)

14. Shefford P. Baker "Advocacy: Why and How" *Materials Research Society Bulletin*, **34**(4) 227-228 (2009)

13. Shefford P. Baker "MRS/MRS-Mexico Hold Inaugural Joint Meeting" *Materials Research Society Bulletin* **34**(3) 149 (2009)

12. Shefford P. Baker "Change is Good: The Past and Future of MRS" *Materials Research Society Bulletin* **34**(1) 3 (2009)

11. P.S. Ho, C.A. Volkert, T. Nakamura, S.P. Baker, "Stress-Induced Phenomena in Metallization," proceedings of the *Seventh International Workshop on Stress-Induced Phenomena in Metallization*, held at the University of Texas, Austin, Texas, 14-16 June 2004 (AIP Conference Proceedings volume **742**, American Institute of Physics, Melville, NY 2004)

10. S.P. Baker, R.P. Vinci, and T. Arias, "Elastic and Anelastic Behavior of Materials in Small Dimensions" in *Materials Research Society Bulletin*, **27**(1) 26-29 (2002)

9. R.P. Vinci and S.P. Baker, guest editors: "Mechanical Properties of Materials in Small Dimensions" *Materials Research Society Bulletin* Volume **27**, Issue 1, January, 2002 (Materials Research Society, Warrendale PA)

8. S.P. Baker, M.A. Korhonen, E. Arzt, and P. Ho, "Stress-Induced Phenomena in Metallization," proceedings of the *Sixth International Workshop on Stress-Induced Phenomena in Metallization*, held at Cornell University, Ithaca, NY, July 25–27, 2001 (AIP Conference Proceedings volume **612**, American Institute of Physics, Melville, NY 2002)

7. O. Kraft, K.W. Schwarz, S.P. Baker, R. Hull, and L.B. Freund, proceedings of the symposium, *Dislocations and Deformation Mechanisms in Thin Films and Small Structures*, held at the 2001 Spring Meeting of the Materials Research Society in San Francisco, CA, USA (Proceedings volume **673**, Materials Research Society, Warrendale, PA, 2001)

6. S.P. Baker, R.F. Cook, S.G. Corcoran, and N.R. Moody, proceedings of the symposium, *Fundamentals of Nanoindentation and Nanotribology II*, held at the 2000 Fall Meeting of the Materials Research Society in Boston, MA, USA, (Proceedings volume **649**, Materials Research Society, Warrendale, PA, 2001)

5. N.R. Moody, W.W. Gerberich, N. Burnham, and S.P. Baker, proceedings of the symposium, *Fundamentals of Nanoindentation and Nanotribology*, held at the 1998 Spring Meeting of the Materials Research Society in San Francisco, CA, USA, (Proceedings volume **522**, Materials Research Society, Warrendale, PA, 1998) 491 pages

4. S.P. Baker, "Besonderheiten bei der Nanohärteprüfung an Silizium" (Special Considerations for Nanohardness testing of Silicon – in German) Deutsches Institut für Normung e.V. DIN Fachbericht 65 (Beuth Verlag GmbH, Berlin 1997)

3. W.W. Gerberich, H. Gao, J.-E. Sundgren, and S.P. Baker, proceedings of the symposium, *Thin Films: Stresses and Mechanical Properties VI,* held at the 1996 Spring Meeting of the Materials Research Society in Boston, MA, USA. (Proceedings volume **436**, Materials Research Society, Pittsburgh, PA, 1996) 542 pages

2. S.P. Baker, C.A. Ross, P.H. Townsend, C.A. Volkert and P. Børgesen, proceedings of the symposium, *Thin Films: Stresses and Mechanical Properties V,* held at the 1994 Fall Meeting of the Materials Research Society in Boston USA. (Proceedings volume **356**, Materials Research Society, Pittsburgh, PA, 1995) 901 pages

1. S.P. Baker and E. Arzt, "Elastic Stiffness Constants of SiGe," in *Properties of Strained and Relaxed Silicon Germanium*, edited by Erich Kasper, (INSPEC, the Institution of Electrical Engineers, Electronic Materials Infomation Service Datareviews Series No. 12, London, 1995) p. 67-69

Conference Proceedings

45. Jayme C. Burket, Samuel Gourion-Arsiquaud, L.M. Havill, Shefford P. Baker, Adele M. Boskey, Marjolein C.M. van der Meulen (2009) "Variations in cortical bone nano-mechanical properties with osteon tissue age and animal age" *Transactions of the Orthopaedic Research Society* **34** (2009)

44. Lara A. Estroff, Hanying Li, Miki Kunitake, Huolin L. Xin, Aaron Vodnick, Shefford P. Baker, and David A. Muller "Biogenic and synthetic polymer-reinforced single crystals: Formation and properties" in *Abstracts of papers of the American Chemical Society* **237** 1153-CHED (2009)

43. Catherine Oertel, Shefford P. Baker, Annika Niklasson, Lars-Gunnar Johansson and Jan-Erik Svensson "Focused-Ion Beam and Electron Microscopy Analysis of Corrosion of Lead-Tin Alloys: Applications to Conservation of Organ Pipes" in Mater Res Soc Symp. Proc. Vol 1047, Materials Research Society, 1047-Y05-01 (2008)

42. Aaron Vodnick, Michael Lawrence, Bethany Little, Derek Worden and Shefford Baker "Synchrotron Characterization of Texture and Stress Evolution in Ag Films" in Mater. Res. Soc. Symp. Proc. Vol. 1027, Materials Research Society, 1027-D01-01 (2008)

41. Fertig RS, Baker SP. "Relationship between film stress and dislocation microstructure evolution in thin films," in: LaVan D, Spearing M, Vengallatore S, Silva Md, editors. Microelectromechanical Systems -- Materials and Devices, vol. 1052. Boston, MA: Mater. Res. Soc., 2007. p.DD07.

40. Eve Donnelly, Shefford P. Baker, Marjolein C.H. van der Meulen, "Mature Tissue Modulus achieved in the cortex within days of bone formation" *Transactions of the Orthopaedic Research Society* **31** 153 (2006)

39. Eve Donnelly, X. Xiao, Shefford P. Baker, R. Mendelsohn, Adele L. Boskey, and Marjolein C.H. van der Meulen, "Systematic variations in bone tissue micromechanical properties relate to composition*" Transactions of the Orthopaedic Research Society* **30** 672 (2005)

38. Eve Donnelly, Rebecca M. Williams, Shefford P. Baker, and Marjolein C. H. van der Meulen, "Collagen content and organization relate to bone nanomechanical properties" in *Structure and Mechanical Behavior of Biological Materials*, edited by Peter Fratzl, William J. Landis, Rizhi Wang, and Fred H. Silver, (Mat. Res. Soc. Symp. Proc. 874E, Materials Research Society, Warrendale, PA, 2005) p. L7.5

37. Robert Knepper, Katherine Jackson, Blake Stevens, and Shefford P. Baker, "Thermomechanical behavior and microstructure evolution in tantalum thin films" in *Stability of Thin Films and Nanostructures*, edited by Richard P. Vinci, Ruth Schwaiger, Alamgir Karim, and Vivek Shenoy (Mat. Res. Soc. Symp. Proc. 854E, Materials Research Society, Warrendale, PA, 2004) p. U6.8

36. D.E. Nowak and S.P. Baker, "Early yielding and stress recovery in (111) and (100) texture components in Cu thin films determined using synchrotron x-ray diffraction", in *Thin Films—Stresses and Mechanical Properties X*, edited by S.G. Corcoran, Y-C. Joo, N.R. Moody, Z. Suo , (Mat. Res. Soc. Symp. Proc. 795, Materials Research Society, Warrendale, PA, 2003) U10.5

35. Eve Donnelly, Shefford P. Baker, Adele Boskey, and Marjolein C.H. van der Meulen, "Effects of Surface Roughness and Maximum Load on the Mechanical Properties of Cancellous Bone Measured by Nanoindentation" *in Biological and Bio-Inspired Materials and Devices*, edited by J. Aizenberg, W.J. Landis, C. Orme, and R. Wang, (Mat. Res. Soc. Symp. Proc. 823, Materials Research Society, Warrendale, PA, 2004) W8.5

34. Mengzhi Pang, Monika Backhaus-Ricoult, and Shefford P. Baker, "The Effect of Oxygen on Adhesion of Thin Copper Films to Silicon Nitride," in *Thin Films—Stresses and Mechanical Properties X*, edited by S.G. Corcoran, Y-C. Joo, N.R. Moody, Z. Suo , (Mat. Res. Soc. Symp. Proc. **795**, Materials Research Society, Warrendale, PA, 2003) U3.6

33. Robert Knepper, Blake Stevens, and Shefford P. Baker, "Thermomechanical Behavior of Tantalum Thin Films: The Effect of Oxygen and the β to α Phase Transition," in *Thin Films—Stresses and Mechanical Properties X*, edited by S.G. Corcoran, Y-C. Joo, N.R. Moody, Z. Suo , (Mat. Res. Soc. Symp. Proc. **795**, Materials Research Society, Warrendale, PA, 2003) U11.27

32. Eve Donnelly, Thorsten Staedler, Shefford P. Baker, and Marjolein C.H. van der Meulen, "Assessment of intralamellar property variations by nanoindentation" in *transactions of the 49th annual meeting of the Orthopaedic Research Society*, New Orleans, LA 2003

31. D.E. Nowak, B. Blank, A. Deyhim, and S.P. Baker, "Development of an Ultra-High Vacuum Oven for High Temperature X-ray Studies," *in Proceedings of the Eighth International Conference on Synchrotron Radiation Instrumentation*, AIP Conference Proceedings, n 708 1146-9 (2004)

30. T. Staedler, E. Donnelly, M.C.H. van der Meulen, and S.P. Baker, "Quasi-static and Dynamic Nanoindentation Testing of Lamellar and Inter-lamellar Trabecular Bone," in *Mechanical Properties Derived from Nanostructuring Materials* edited by D.F. Bahr, N.R. Moody, H.H. Kung, K.J. Wahl, (Mat. Res. Soc. Symp. Proc. **778**, Materials Research Society, Warrendale, PA, 2003) U.3.14

29. M. Pang and S.P. Baker, "Quantitative Measurements of Subcritical Debonding of Cu Films from Dielectric Substrates," in *Materials, Technology, and Reliability for Advanced Interconnects and Low-k Dielectrics*, edited by J. Leu, A. McKerrow, O. Kraft, and T. Kikkawa, (Mat. Res. Soc. Symp. Proc. **766**, Materials Research Society, Warrendale, PA, 2003) E2.8

28. P. Pant and S.P. Baker, "Strain Relaxation by Dislocation Arrays in Thin Films," in *Multiscale Phenomena in Materials—Experiments and Modeling Related to Mechanical Behavior*, edited by K.J. Hemker, D.H. Lassila, L.E. Levine, and H.M. Zbib, (Mat. Res. Soc. Symp. Proc. **779**, Materials Research Society, Warrendale, PA, 2003) W5.25

27. J.B. Shu and S.P. Baker, "Plastic Relaxation in Thin Copper Films," in: *Thin Films: Stresses and Mechanical Properties IX*, edited by C.S. Ozkan, L.B. Freund, R.C. Cammarata, and H. Gao, (Mat. Res. Soc. Symp. Proc. **695**, Materials Research Society, Warrendale, PA, 2002) p. 15-20

26. D.E. Nowak, O. Thomas, E. Stach, and S.P. Baker, "X-Ray Diffraction Analysis and Modeling of Strain Induced by Thermal Cycling in a Thin Aluminum (011) Bicrystal Film" in *Thin Films: Stresses and Mechanical Properties IX*, edited by C.S. Ozkan, L. B. Freund, R.C. Cammarata, and H. Gao, (Mat. Res. Soc. Symp. Proc. **695**, Materials Research Society, Warrendale, PA, 2002) p. 3-8

25. P. Pant, K.W. Schwarz, and S.P. Baker,"Dislocation Dynamics Simulations of Dislocation Interactions in Thin FCC Metal Films" in *Dislocations and Deformation Mechanisms in Thin Films and Small Structures*, edited by O. Kraft, K.W. Schwarz, S.P. Baker, R.Hull, and L.B. Freund (Mat. Res. Soc. Symp. Proc. **673**, Materials Research Society, Warrendale, PA, 2001) p. P2.2.1-6

24. H. Gao, L. Zhang, and S.P. Baker,"Dislocation Core Spreading at Interfaces between Crystalline and Amorphous Solids" in *Dislocations and Deformation Mechanisms in Thin Films and Small Structures*, edited by O. Kraft, K.W. Schwarz, S.P. Baker, R.Hull, and L.B. Freund (Mat. Res. Soc. Symp. Proc. **673**, Materials Research Society, Warrendale, PA, 2001) p. P2.6.1-6

23. M. Kunert, B. Baretzky, E.J. Mittemeijer, and S.P. Baker, "Sub-Micrometer Spatially Resolved Measurements of Mechanical Properties and Correlation to Microstructure and Composition," in *Fundamentals of Nanoindentation and Nanotribology*, edited by S.P. Baker, R.F. Cook, S.G. Corcoran, and N.R. Moody, (Mat. Res. Soc. Symp. Proc. **649**, Materials Research Society, Warrendale, PA, 2001) p. Q3.2.1-Q3.2.6

22. Y.-C. Joo, S.P. Baker, E. Arzt, and C.V. Thompson “Model Studies of Electromigration using Indented Single-Crystal Aluminum Lines,” in *Proceedings of the Fifth International Workshop on Stress Induced Phenomena in Metallization* (AIP Conf. Proc. **491**, American Institute of Physics, New York, 1999) p. 100-111

21. J. Shu, S. Clyburn, T. Mates, and S.P. Baker “Effects of Thickness and Oxygen Content on Thermomechanical Behavior of Thin Cu Films Passivated with AlN” in *Materials Reliability in Microelectronics IX,”* edited by D.D. Brown, Ad.H. Verbruggen, and C.A. Volkert, (Mat. Res. Soc. Symp. Proc. **563**, Materials Research Society, Warrendale, PA, 1999) p. 707-712

20. M. Hommel, O. Kraft, S.P. Baker, and E. Arzt, “Micro-tensile and Fatigue Testing of Copper Thin Films on Substrates” in *Materials Science of Microelectromechanical System (MEMS) Devices*, edited by A.H. Heuer, and S.J. Jacobs, (Mat. Res. Soc. Symp. Proc. **546**, Materials Research Society, Warrendale, PA, 1999)

19. M. Kunert, B. Baretzky, S.P. Baker, and E.J. Mittemeijer, “Nanometer-scale Measurements of Mechanical Properties and Composition in an Ion Implanted Titanium-based Alloy” in *Fundamentals of Nanoindentation and Nanotribology*, edited by N.R. Moody, W.W. Gerberich, N. Burnham, and S.P. Baker, (Mat. Res. Soc. Symp. Proc. **522**, Materials Research Society, Warrendale, PA, 1998) p. 95-100

18. S.P. Baker, R.-M. Keller, A. Kretschmann, and E. Arzt, “ Deformation Mechanisms in Thin Cu Films” in *Materials Reliability in Microelectronics VIII,* edited J.C. Bravman, T.N. Marieb, J.R. Lloyd, and M.A. Korhonen, (Mat. Res. Soc. Symp. Proc. **516**, Materials Research Society, Warrendale, PA, 1998) p. 287-298

17. S.P. Baker, R.-M. Keller, and E. Arzt, “Energy Storage and Recovery in Thin Metal Films on Substrates,” in *Thin Films: Stresses and Mechanical Properties VII,* edited by R.C. Cammarata, M. Nastasi, E.P. Busso, and W.C. Oliver, (Mat. Res. Soc. Symp. Proc. **505**, Materials Research Society, Warrendale, PA, 1998) p. 605-610

16. S.P. Baker, M.P. Knauß, and E. Arzt, “Measuring Mechanical Properties in Small Dimensions via Deflection of Micrometer Scale Cantilever Beams” in *Abstract Proceedings of the 1997 SEM Spring Conference on Experimental Mechanics*, Society for Experimental Mechanics, Bethel, CN, 1997) p. 110-111

15. Y.-C. Joo, P. Müllner, S.P. Baker, and E. Arzt, “Mechanical Properties of Al-Cu Films with Various Heat Treatments,” in *Materials Reliability in Microelectronics VII,* edited J.J. Clement, R.R. Keller, K.S. Krish, J.E. Sanchez, Jr., and Z. Suo, (Mat. Res. Soc. Symp. Proc. **473**, Materials Research Society, Pittsburgh, PA, 1997) p. 409-414

14. S.P. Baker, C.R. Ottermann, M. Laube, F. Rauch, and K. Bange, “Dependence of Hardness and Stiffness on Density of TiO_2 and Ta_2O_5 Layers,” in *Thin Films: Stresses and Mechanical Properties VI,* edited by W.W. Gerberich, H. Gao, J.-E. Sundgren, and S.P. Baker, (Mat. Res. Soc. Symp. Proc. **436**, Materials Research Society, Pittsburgh, PA, 1996) p. 71-76

13. S. Kirchner, O. Kraft, S.P. Baker, and E. Arzt, “Microstructure and Mechanical Properties of Thin Al-0.6%Si-0.6%Ge Films,” in *Thin Films: Stresses and Mechanical*

Properties VI, edited by W.W. Gerberich, H. Gao, J.-E. Sundgren, and S.P. Baker, (Mat. Res. Soc. Symp. Proc. **436**, Materials Research Society, Pittsburgh, PA, 1996) p. 21-26

12. A. Kretschmann, W.-M. Kuschke, S.P. Baker, and E. Arzt, "Plastic Deformation in Thin Cu Films Determined by X-ray Microtensile Tests," in *Thin Films: Stresses and Mechanical Properties VI,* edited by W.W. Gerberich, H. Gao, J.-E. Sundgren, and S.P. Baker, (Mat. Res. Soc. Symp. Proc. **436**, Materials Research Society, Pittsburgh, PA, 1996) p. 59-64

11. R.-M. Keller, W. Sigle, S.P. Baker, O. Kraft, and E. Arzt, "In-Situ TEM Investigation During Thermal Cycling of Thin Copper Films," in *Thin Films: Stresses and Mechanical Properties VI,* edited by W.W. Gerberich, H. Gao, J.-E. Sundgren, and S.P. Baker, (Mat. Res. Soc. Symp. Proc. **436**, Materials Research Society, Pittsburgh, PA, 1996) p. 221-226

10. Y.-C. Joo, S.P. Baker, M.P. Knauß, and E. Arzt, "Electromigration in Single-Crystal Aluminum Lines Pre-Damaged by Nanoindentation," in *Materials Reliability in Microelectronics VI,* edited by W.F. Filter, J.J. Clement, A.S. Oates, and R. Rosenberg, (Mat. Res. Soc. Symp. Proc. **428**, Materials Research Society, Pittsburgh, PA, 1996) p. 225-230

9. M.P. Knauss, S.P. Baker and E. Arzt, "Biegeexperimente an Mikrobalken zur Bestimmung Mechanischer Eigenschaften von Dünnen Schichten" ("Microbeam Bending Experiments for Determination of the Mechanical Properties of Thin Films," in German), in *Micro Materials '95* (Deutsher Verband für Materialforschung und -prüfung e.V, Berlin 1996) p. 653-658

8. S.P. Baker, M.P. Knauss, U.E. Möckl and E. Arzt, "Electroplasticity and Electromigration" in *Thin Films: Stresses and Mechanical Properties V,* edited by S.P. Baker, C.A. Ross, P.H. Townsend, C.A. Volkert and P. Børgesen, (Mat. Res. Soc. Symp. Proc. **356**, Materials Research Society, Pittsburgh, PA, 1995) p. 483

7. S.P. Baker, J.A. Bain, B.M. Clemens and W.D. Nix, "Interfacial Structure and Mechanical Properties of Compositionally-Modulated Au-Ni Thin Films" in *Polycrystalline Thin Films: Structure, Texture, Properties and Applications,* edited by M. Parker, K. Barmak, R. Sinclair, D.A. Smith and J Floro, (Mat. Res. Soc. Symp. Proc. **343**, Materials Research Society, Pittsburgh, PA, 1994) p. 555

6. S.P. Baker, "The Analysis of Depth-Sensing Indentation Data," in *Thin Films: Stresses and Mechanical Properties IV*, edited by P.H. Townsend, J.E. Sanchez, T.P. Weihs and P. Børgesen, (Mat. Res. Soc. Symp. Proc. **308**, Materials Research Society, Pittsburgh, PA, 1993) p. 209

5. S.P. Baker, M.K. Small, J.J. Vlassak, B.J. Daniels and W.D. Nix, "The Search for the Supermodulus Effect," in the proceedings of the NATO Advanced Study Institute: *Mechanical Properties and Deformation Behavior of Materials Having Ultra-Fine Microstructures*, (NATO ASI Series E, Applied Sciences, **233**, Kluwer Academic Publishers, Dordrecht, 1993) p. 165

4. S.P. Baker, T.W. Barbee Jr. and W.D. Nix, "Time-Dependent Deformation in Room-Temperature Indentation Experiments using a Nanoindenter," in *Thin Films: Stresses and Mechanical Properties III*, edited by W.D. Nix, J.C. Bravman, E. Arzt and L.B. Freund,

(Mat. Res. Soc. Symp. Proc. **239**, Materials Research Society, Pittsburgh, PA, 1989) p. 319

3. S.P. Baker and W.D. Nix, "Mechanical Properties of Thin Films on Substrates," in *Optical Thin Films III: New Developments,* edited by R. Ian Seddon, *Proc. SPIE* **1323**, 263 (1990)

2. S.P. Baker, A.F. Jankowski, S. Hong and W.D. Nix, "Mechanical Properties of Compositionally-Modulated Au-Ni Thin Films Using Indentation and Microbeam Deflection Techniques", in *Thin Films: Stresses and Mechanical Properties II*, edited by M.F. Doerner, W.C. Oliver, G.M. Pharr, and F.R. Brotzen, (Mat. Res. Soc. Symp. Proc. **188**, Materials Research Society, Pittsburgh, PA, 1989) p. 289

1. S.R. Nutt, K.A. Green, S.P. Baker, W.D. Nix and A.F. Jankowski, "Gold-Nickel Multilayer Films: Structure-Property Correlations," in *Thin Films: Stresses and Mechanical Properties*, edited by J.C. Bravman, W.D. Nix, D.M. Barnett and D.A. Smith, (Mat. Res. Soc. Symp. Proc. **130**, Materials Research Society, Pittsburgh, PA, 1989) p. 129

INVITED TALKS

111. "Topological Constraint Theory as a Predictor of Hardness in Glass" Glass and Optical Materials Division of the American Ceramic Society Annual Meeting , San Antonio, TX, May 24, 2018

110. "Plastic Deformation of Silica Glass Studied by Indentation and Micropillar Compression with In-Situ Raman" TMS Symposium on Thermo-mechanical Response of Materials with Special Emphasis on In-situ Techniques, Phoenix, AZ, March 15, 2018

109. "Plastic Deformation and Hardness in Silicate Glasses" Rutgers University, Department of Materials Science and Engineering, Piscataway, New Jersey September 27, 2016

108. "Plastic deformation and hardness of glass—calcium aluminosilicate, magnesium aluminosilicate, and calcium galliosilicate glasses" at the Corning Glass Summit 2016 in Corning, New York, June 3, 2016

107. "Texture transformations in thin films" University of Wyoming, October 1, 2015

106. "Plastic deformation and the hardness of glasses" in the symposium "From Structural to Mechanical Properties of Disordered Solids" at the International Materials Research Conference 2015 in Cancun, Mexico, August 19, 2015

105. "Driving forces for texture transformations in thin Ag films" in the symposium "Micro and Nanomechanical Testing of Materials" at the International Materials Research Conference 2015 in Cancun, Mexico, August 17, 2015

104. "Nanotwins and stability of physical-vapor-deposited thin films" Meijo University, Nagoya, Japan, March 2, 2014

103. "Texture and texture transformations in thin metal films" National Chung Hsing University, Taiwan October 9, 2013
102. "What stops threads?: Dislocation structure, stress distributions, and strength in thin films" Instrument Technology Research Center, National Applied Research Laboratories, Hsinchu, Taiwan, October 8, 2013
101. "Texture and texture transformations in thin films" TACT2013 International Thin Films Conference, The Grand Hotel, Taipei, Taiwan, October 8, 2013 (Keynote Lecture)
100. "Texture transformations and anomalous grain growth in thin metal films" Texas A&M University, May 23, 2013
95. "Texture transformations and anomalous grain growth in thin metal films" International Conference on Metallurgical Coatings and Thin Films, April 18, 2013
94. "Strong Materials Made From Sea Water: Nanoscale Structure and Mechanical Properties of Calcite Single Crystals From the Mollusk *Atrina Rigida*" Hysitron Inc Open House, June 15, 2012
93. "What stops threads?: Dislocation structure, stress distributions, and strength in thin films," Alfred University, March 29, 2012
92. "Mechanical Properties of Biomineralized Tissues Studied by Nanoindentation," Workshop on Mechanical Behaviour of Systems at Small Length Scales – 3, Trivandrum, India, September 18-21, 2011
91. "Continuous Orientation Gradients, Discontinuous Boundary Structure, and Dislocations in Phase-Transformed Ta Thin Films," Cornell Mechanics of Solids Seminar, October 13, 2010
90. "Tools and Techniques for Nanomechanical Testing of Biomaterials" Webinar presented in partnership with Materials Today, Thursday, June 17th, 2010.
89. "Innovation: Some roles for professional societies" Innovation Workshop on Advanced Materials and Devices, ICAM 2009, Rio de Janeiro, September 20-25, 2009
88. "What stops threads?: Dislocation structure, stress distributions, and strength in thin films," University of Texas at Austin, July 7, 2009
87. "The globalization of science: Funding, practice, and communications," Fifth Annual Micro Nano Breakthrough Conference, Vancouver, Washington, September 8-10, 2008
86. "Continuous Orientation Gradients, Discontinuous Boundary Structure, and Dislocations in Phase-Transformed Ta Thin Films," University of Virginia, October 13, 2008
85. "Dislocation Structure and the Strength of Thin Films," Materials Research Society 2008 Spring Meeting, San Francisco Symposium Z: Materials Structures—The Nabarro Legacy, March 25 2008
84. "Surprising threads in the story of thin film strength," Lehigh University, November 12, 2007
83. "Surprising threads in the story of thin film strength," Brown University, October 29 2007

82. "Continuous Orientation Gradients, Discontinuous Boundary Structure, and Dislocations in Phase-Transformed Ta Thin Films," Thin Air Philosophical Society Symposium, University of Colorado, Boulder, August 6-9, 2007
81. "Mechanical Properties, Microstructure, and the β–α Phase Transformation in Ta Thin Films," Symposium in Honor of Carl Koch, TMS Annual Meeting, February 26-March 1, 2007
80. "Mechanical Behavior of Nanoscale Materials," Shanghai Jiao Tong University/Cornell University Joint Symposium, October 12-13, 2006
79. "Mechanical Behavior of Nanoscale Materials," Tsinghua-Foxconn Nanotechnology Research Center, Tsinghua University, Beijing, China, October 9-10, 2006
78. "Mechanical Behavior of Thin Films," Max-Planck-Institut für Metallforschung, 4 July 2006
77. "Dislocation Dynamics Simulations of Deformation in Metal Thin Films" TECSEN–CNRS–Université Paul Cézanne, Faculté des Sciences de St Jérôme, Marseille, 29 June 2006
76. "Thermomechanical Behavior of (011) Aluminum Thin Films," TECSEN Lab seminar, Université Paul Cézanne, Faculté des Sciences de St Jérôme, Marseille, France, 13 June 2006
75. "Stresses, Phase Transformations, and Microstructure in Ta Thin Films," Institute Seminar, Faculté St. Jérôme, Université Paul Cézanne, Marseille, France, 7 June 2006
74. "Stresses, Phase Transformations, and Microstructure in Ta Thin Films," Department of Materials Science and Engineering Seminar, North Carolina State University, April 7, 2006
73. "Mechanical Behavior of Thin Films and Patterned Structures," Intel Technology Forum (worldwide electronic web/telecast), 22 September 2005
72. "Is there still something interesting to learn about thin metal films?—the odd case of Ta" at the National Institutes for Standards and Technology, Boulder CO, 11 August, 2005
71. "Is there still something interesting to learn about thin metal films? — The odd case of Ta" at the NSF-sponsored *Thin Air Philosophical Society Symposium*—Current Challenges in Mechanics and Materials, Laramie, WY, 8 August, 2005
70. "Are there Dislocations in my Film? Critical Thickness, Dislocation Introduction, and Propagation in Heteroepitaxy," 16th American Conference on Crystal Growth and Epitaxy, Big Sky Resort, MT, July 10 - 15, 2005
69. "Mechanical Behavior of Thin Films," ASM International, Rochester Chapter, Rochester, NY, 3 May 2005
68. "Effect of Oxygen on Subcritical Delamination of Thin Cu Films from Ceramic Substrate Layers," 11th International Conference on Fracture, Turin, Italy, March 20-25, 2005
67. "Mechanics and Materials and Experiments: Open Questions," at the *Thin Air Philosophical Society Inaugural Meeting*, Laramie, WY, 3 August, 2003

66. “Themomechanical Behavior of Different Texture Components in Thin FCC Metal Films,” in the symposium *Mechanical Properties Derived from Nanostructuring Materials* at the Materials Research Society 2003 Spring Meeting, San Francisco, CA, 22-25 April, 2003
65. “Channeling Dislocations in Thin Films: A Robust Concept for Understanding Mechanical Behavior of Thin Films,” Department of Chemical Engineering and Materials Science, University of Minnesota, 14 October, 2002
64. “Dynamic Nanocontact Measurements of Trabecular Bone and Silicate Glasses,” Hysitron Inc. Minneapolis, MN, 11 October, 2002
63. “Effects of Adhesion on Deformation Behavior of Thin Metal Films on Substrates,” in *EuroConference on Structure and Composition of Interfaces in Solids*, Kloster Irsee, Germany, 18-23 August, 2002
62. “Effect of Interface Chemistry on the Thermomechanical Behavior of Thin Films,” Institut für Metallkunde der Universität Stuttgart, 15 August, 2002
61. “The Thermomechanical Behavior of Thin Metal Films,” *Gordon Conference on Thin Film Mechanical Behavior*, Colby College, Waterville, ME, July 14-19 2002
60. “Effects of Adhesion on Deformation Behavior of Thin Metal Films on Substrates,” in the symposium *Mechanics of Thin Films and other Small Structures* at the 14th US National Congress of Theoretical and Applied Mechanics, Blacksburg, VA, 23-28 June 2002
59. “Mechanical Behavior of Thin Metal Films,” Dept. of Mechanical and Aerospace Engineering, Cornell University, 19 February 2002
58. “Thermomechanical Behavior of Thin Ag Films on Substrates,” in the symposium *Thin Films, Stresses and Mechanical Properties IX* at the Materials Research Society 2001 Fall Meeting, Boston, MA, 26-30 November 2001
57. “Mechanical Properties of Materials in Small Dimensions: Multiscale Modeling”, at the Engineering Foundation Conference on *Integrating Materials Science into Engineering Structures and Devices*, Lake Arrowhead, CA, Nov 11-15, 2001,
56. “Can you remind me what you’re working on?” Stanford University, Seminar in honor of W.D. Nix’s 60th Birthday, 6 October, 2001,
55. “Nanocontact Measurements of Mechanical Properties” Polymer Outreach Program, Cornell Center for Materials Research, 21 May, 2001
54. “Anomalous Mechanical Behavior in Small Dimensions” Cornell University, Dept. of Materials Science and Engineering, 15 March 2001,
53. “Anomalous Mechanical Behavior in Small Dimensions,” Dept. of Materials Science and Engineering, Rensselaer Polytechnic Institute, 22 February 2001
52. “Mechanical Properties in Small Dimensions,” Sandia National Laboratories, Albuquerque, NM, 1 August, 2000

51. “Bilayer Modeling and Measurements of Adhesion of Thin Metal Films to Glass,” in the symposium *Nanomechanics of Surfaces and Interfaces*, ASME International Mechanical Engineering Congress and Exposition, Orlando FL, 5-10 November, 2000

50. “Nanoindentation of Surface Layers,” European Science Foundation Conference on *Surface Engineering for Protection of Metals and Alloys*, Acquafredda di Maratea, Italy, 1-4 October 2000

49. “Plastic Deformation and Strength of Materials in Small Dimensions,” Plenary Speaker, *Twelfth International Conference on the Strength of Materials*, Asilomar, CA, August 27–Sept 1, 2000

48. “Plasticity in Thin Metal Films: Beyond the “Oxygen Effect” in the seminar *Vom Powerteam zum Bambuswald* celebrating 10 years of the Arzt division at the Max-Planck-Institut für Metallforschung, Stuttgart, 7 July, 2000

47. “Mechanical Properties of Thin Metal Films,” Dept. of Materials Science and Engineering, Johns Hopkins University, 15 March, 2000

46. “Mechanical Properties of Thin Metal Films,” Department of Materials Science and Engineering, Lehigh University, 8 February, 2000

45. “Plastic Deformation in Thin Metal Films” in the symposium *Thin Films: Stresses and Mechanical Properties VIII* at the Materials Research Society 1999 Fall Meeting, Boston MA, 29 November-3 December, 1999

44. “Measuring Mechanical Properties in The Nanometer Regime” Xerox Corp, Webster, NY, 10 November 1999

43. “Remarkable Plastic Deformation Effects During Thermal Cycling of Thin Metal Films” in the symposium *Nanomechanics of Surfaces and Interfaces* at the 36th Annual Technical Meeting of the Society of Engineering Science, Austin, TX, 25-27 October, 1999

42. “Mechanical Behavior of Thin Cu Metallizations” Motorola Semiconductor Products, Austin TX, 25 October 1999

41. “Plastic Deformation in Different Texture Components in Copper Thin Films” at the Engineering Foundation Conference on *Mechanical Properties of Films, Coating and Interfacial Materials* Il Ciocco Italy June 27-July 2, 1999

40. “Anomalous Mechanical Behavior in Thin Cu Metallizations” IBM TJ Watson Reseach Center, 14 June 1999

39. “Mechanical Behavior of Thin Metal Films,” Martin-Luther-Universität, Halle, Germany, 10 December, 1998

38. “Measuring the Mechanical Properties of Thin Films using Depth-Sensing Indentation Methods,” *Nanoindentation Workshop*, Hückelhoven, Germany, 9 December, 1998

37. “Plasticity and Dislocation Behavior in Thin Metal Films,” *Special Workshop on Dislocation Dynamics* held in conjunction with the Materials Research Society 1998 Fall Meeting, 4 December, 1998

36. "Deformation Mechanisms in Thin Metal Films on Substrates," Department of Theoretical and Applied Mechanics, Cornell University, 16 September, 1998
35. "Deformation Mechanisms in Thin Cu Films," in the symposium *Materials Reliability in Microelectronics VII* at the Materials Research Society 1998 Spring Meeting, 13-18 April, 1998
34. "Mechanical Behavior of Thin Cu Films," Department of Materials Science and Engineering, Cornell University, 19 March 1998
33. "Nanoindentation: The State of the Art," Ecole Polytechnique Federale de Lausanne, 10 November 1997
32. "Measuring Mechanical Properties in the Nanometer Regime Using Nanoindentation Methods," Hysitron Inc. Minneapolis, MN, 5 July, 1997
31. "Effects of Energy Storage and Recovery During Plastic Deformation of Thin Films on Substrates", McNU 97 Conference, Northwestern University, 2 July, 1997
30. "Measuring Mechanical Properties in Small Dimensions via Deflection of Micrometer-scale Cantilever Beams," in the *1997 Spring Conference on Experimental Mechanics*, Society for Experimental Mechanics, Bellevue WA, June 1997
29. "Between Nanoindentation and Atomic Force Microscopy: Measuring Mechanical Properties in the Nanometer Regime" in the symposium *Micro- and Nanoscale Mechanical Testing, Modelling and Analysis* at the International Conference on Metallurgical Coatings and Thin Films, San Diego, CA 21-25 April, 1997
28. "Mechanical Properties in Small Dimensions" Department of Materials Science and Engineering, Cornell University, 13 February, 1997
27. "Mechanical Properties of Thin Films" Institut für Festkörper- und Werkstofforschung, Dresden, 16 December, 1996
26. "Electroplasticity and Electromigration," Department of Chemical Engineering and Materials Science, University of Minnesota, 18 July, 1996
25. "Mechanical Properties in Small Dimensions," Department of Materials Science and Engineering, Northwestern University, 7 March, 1996
24. "Electroplasticity and Electromigration", Materials Department, University of California-Santa Barbara, 4 December, 1995
23. "Mechanical Properties of Thin Films," Department of Chemical Engineering and Materials Science, University of Minnesota, 25 August, 1995
22. "Electroplasticity and Electromigration," Department of Materials Science and Engineering, University of Texas at Austin, 17 August, 1995
21. "Mechanical Properties of Thin Films," Physics Department, Linköping University 27 April, 1995
20. "Working with the Nanoindenter," Departement Physik, ETH- Hönggerberg, Zürich, 8 February, 1994

19. "Submicrometer Depth-Sensing Indentation: The State of the Art," Institut für Physik der Universität Augsburg, 4 February, 1994
18. "Mechanical Properties of Thin Films," Max-Planck-Institut für Metallforschung, Stuttgart, 22 November 1993
17. "Mechanical Properties of Polycrystalline Thin Films," at the International Union of Vacuum Science, Technique and Applications (IUVSTA) Workshop: *Polycrystalline Thin Films: Microstructure Evolution and Structure-Property Relationships*, Balatonaliga, Hungary, 5-9 October, 1992
16. "The Search for the Supermodulus Effect," at the NATO Advanced Study Institute: *Mechanical Properties and Deformation Behavior of Materials Having Ultra-Fine Microstructures*, Porto Novo, Portugal, June 28 - July 10, 1992
15 "Mechanical Properties and Structure of Compositionally-Modulated Au-Ni Thin Films," Materials Division, Lawrence Livermore National Laboratory, 31 July 1992
14. "Mechanical Properties and Structure of Compositionally-Modulated Au-Ni Thin Films," Sandia National Laboratory, Livermore, CA, 5 April 1992
13. "Mechanical Properties and Structure of Compositionally-Modulated Au-Ni Thin Films," Los Alamos National Laboratory, Los Alamos, NM, 30 March, 1992
12. "Nanoindentation, the State of the Art," National Physical Laboratory, Teddington, UK, 16 December, 1991
11. "Thermal Drift Effects in the Nanoindenter" Department of Materials, Oxford University, 12 Dec 1991
10. "Mechanical Testing of Thin Films," presentation in the symposium *Advanced Mechanical/Materials Testing* at 1991 ASM International Materials Week, Cincinnati, Ohio, 21-24 October, 1991
9. "The Supermodulus Effect" and "Thermal Drift Effects in the Nanoindenter" IBM Almaden Research Center, 20 August 1991
8. "The Supermodulus Effect: New Developments," Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland, 31 May 1991
7. "The Supermodulus Effect: New Developments," Max-Planck-Institut für Metallforschung, Stuttgart, Germany, 28 May 1991
6. "The Supermodulus Effect: New Developments," Royal Institute of Technology, Stockholm, Sweden, 23 May 1991
5. "Mechanical Properties of Thin Films," Materials Science Division, Uppsala University, Uppsala, Sweden, 22 May 1991
4. "The Supermodulus Effect: New Developments," Oxford University, Oxford UK, 20 May 1991
3. "Measuring the Hardness of Hard Materials Using the Nanoindenter" Los Alamos National Laboratory, 1 June 1990

2. "Characterization of Thin Films by Deflection of Cantilever Beams and Membranes," Oak Ridge National Laboratory, 5 January 1990
1. "Mechanical Properties of Thin Films on Substrates," in the symposium *Optical Thin Films III: New Developments* at the International Society for Optical Engineering meeting, San Diego, CA 9-11 July 1990

EXHIBIT F

Trials@uspto.gov
Tel: 571-272-7822

Paper 66
Entered: June 23, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX, INC.,
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00389
Patent 8,035,233 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and
FRANCES L. IPPOLITO, *Administrative Patent Judges*.

IPPOLITO, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively "Petitioner") filed a Petition on December 28, 2015, requesting an *inter partes* review of claims 22, 31, 33, and 34 of U.S. Patent No. 8,035,233 B2 (Ex. 1001, "the '233 patent"). (Paper 4, "Pet."). On April 2, 2016, Patent Owner, Elm 3DS Innovations, LLC statutorily disclaimed claims 22 and 31 (Ex. 2138), thus, we did not consider Petitioner's unpatentability challenges of claims 22 and 31. *See* 37 C.F.R. § 107(e). Subsequently, Patent Owner filed a Preliminary Response to the Petition on April 4, 2016 (Paper 11, "Prelim. Resp.").

Based on these submissions, we instituted an *inter partes* review of claims 33 and 34 of the '233 patent on the following grounds:

Reference(s)	Basis	Claim(s) Challenged
Leedy '695[1] and Hitachi[2]	§ 103	33 and 34
Matsumoto[3], Bower[4], and Leedy '695	§ 103	33 and 34

Paper 14 ("Dec. on Inst.").

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[1] US Patent No. 5,354,695, issued Oct. 11, 1994 (Ex. 1006, "Leedy '695").
[2] JP Patent Application Publication No. H8-125120, published May 17, 1996 (Ex. 1015, "Hitachi"). Petitioner has provided a certified English translation. Ex. 1015, 17.
[3] T. Matsumoto, *Three-Dimensional Integration Technology Based on Wafer Bonding Technique Using Micro-Bumps*, in International Conference on Solid State Devices and Materials 1073–1074 (1995) (Ex. 1013, "Matsumoto").
[4] US Patent No. 5,503,704, issued Apr. 2, 1996 (Ex. 1014, "Bower").

After institution, Patent Owner filed its Patent Owner Response on October 14, 2016 (Paper 53, "PO Resp.") and Petitioner filed a Reply (Paper 59, "Reply"). A consolidated oral hearing was held on April 6, 2017, and a transcript of the oral hearing is of record. Paper 65 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims. For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 33 and 34 of the '233 patent are unpatentable.

A. Related Proceedings

Petitioner indicates that the '233 patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

Additionally, patents related to the '233 patent are the subject of petitions filed in IPR2016-00386 (US Patent No. 8,653,672); IPR2016-00387 (US Patent No. 8,841,778); IPR2016-00388 and IPR2016-00393 (US Patent No. 7,193,239); IPR2016-00390 (US Patent No. 8,629,542); IPR2016-00391 (US Patent No. 8,796,862); IPR2016-00394 (US Patent No. 8,410,617); IPR2016-00395 (US Patent No. 7,504,732); IPR2016-00687 (US Patent No. 8,928,119); IPR2016-00691 (US Patent No. 7,474,004); IPR 2016-00708 (US Patent No. 8,907,499); IPR 2016-00786 (US Patent No. 8,933,570); and IPR 2016-00770 (US Patent No. 8,907,499). Dec. on Inst. 3.

We also note that Petitioner filed two additional petitions requesting *inter partes* review of U.S. Patent No. 8,791,581 (IPR2016-00703 and IPR2016-00706) for which we did not institute a review.

B. Time Bar under 35 U.S.C. § 315(b)

In our Decision to Institute, we did not agree with Patent Owner that the Petition was barred under 35 U.S.C. § 315(b) because, according to Patent Owner, the Office lacked authority to treat certain days, on which the Office experienced an emergency situation such that many of its online and information technology systems were shut down, as federal holidays. Dec. on Inst. 3–5. Patent Owner has not raised this issue subsequent to institution in this proceeding.

C. The ’233 Patent

The ’233 patent is directed generally to a “[t]hree-[d]imensional [s]tructure (3DS)” for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1a is reproduced below.

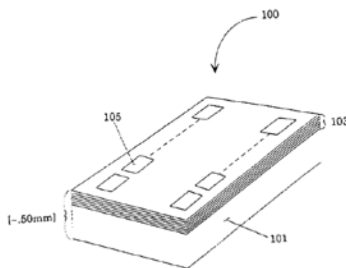

Figure 1a

Figure 1a shows 3DS memory device 100 having a stack of integrated circuit layers with a “fine-grain inter-layer vertical interconnect” between all

circuit layers. *Id.* at 4:13–17. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:33–35. The ’233 patent discloses that “each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness.” *Id.* at 4:38–40. The ’233 patent further discloses that the “thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication.” *Id.* at 8:61–66.

Figure 1b is reproduced below.

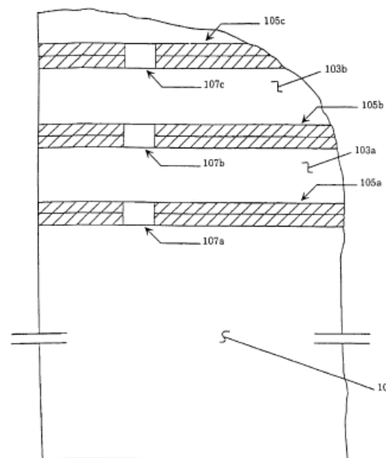

Figure 1b

Referring to Figure 1b, the ’233 patent shows a cross-section of a 3DS DRAM integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:53–56. Bond and interconnect layers 105a, 105b, etc. are shown between circuit layers 103a and 103b. *Id.* at Fig. 1b. The ’233 patent discloses that pattern 107a, 107b, etc. in the bond and interconnect layers 105a, 105b, etc. defines the vertical interconnect contacts between the

integrated circuit layers and serves to electrically isolate these contacts from each other and the remaining bond material. *Id.* at 4: 27–31. Additionally, the ’233 patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:31–32.

Further, the ’233 patent teaches that the “term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 μm.” *Id.* at 4:16–21. The fine-grained inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:21–23.

D. Illustrative Claim

Dependent claims 33 and 34 are the challenged claims in this proceeding. Claims 33 and 34 depend from disclaimed independent claim 22, and, as such, include the limitations recited in claim 22. Thus, claims 22 and 33 are reproduced below to illustrate the subject matter of the ’233 patent:

> 22. An integrated circuit structure comprising:
>
> first, second, and third substrates each having integrated circuits formed thereon;
>
> at least one of metal and non-polymeric first bonding layers on the first and second substrates, wherein the first bonding layers comprise bond-forming material on a majority of first surfaces of the first and second substrates that bonds the first and second substrates to each other; and
>
> at least one of metal and non-polymeric second bonding layers on the second and third substrates, wherein the second bonding layers comprise bond-forming material on a majority of a second surface of the second substrate and a first surface of the third substrate that bonds the second and third substrates to each other.

33. The apparatus of claim 22, wherein the circuitry are formed with a low stress dielectric.

II. ANALYSIS

A. *Claim Construction*

Following institution, the parties submitted briefing regarding the claim construction standard applicable in this proceeding. Papers 21, 24, 26. Patent Owner further filed a Notice of Patent Expiration, representing that the '233 patent will not expire prior to the deadline for issuing a final written decision in this matter. Paper 22, 2.

In our Decision regarding claim construction, we determined that the broadest reasonable construction standard continues to apply to the claims at issue in the unexpired '233 patent. Paper 29, 6. Accordingly, here, we interpret claims of an unexpired patent using the "broadest reasonable construction in light of the specification of the patent in which [the claims] appear[]." 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee,* 136 S. Ct. 2131, 2144 (2016) (concluding the broadest reasonable construction "regulation represents a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office").

Under this standard, we note that the Board may not "construe claims during IPR so broadly that its constructions are *unreasonable* under general claim construction principles. . . . '[T]he protocol of giving claims their broadest reasonable interpretation . . . does not include giving claims a legally incorrect interpretation.'" *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2016). "Rather, 'claims should always be read in light of the specification and teachings in the underlying patent'" and "[e]ven under the broadest reasonable interpretation, the Board's

construction 'cannot be divorced from the specification and the record evidence.'" *Id.* (citations omitted).

1. "low stress dielectric" (claims 33 and 34)

In the Decision on Institution, we construed "low stress dielectric" to mean a dielectric having a stress of less than 8×10^8 dynes/cm^2. The parties have not challenged this construction. Further, based on the complete record before us, we discern no reason to deviate from our previous determination here. For example, we note that the disclosure in the Specification of the '233 patent is consistent with our construction, and teaches that dielectrics in low stress include those that have a stress of less than 5×10^8 dynes/cm^2 and "low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695." Ex. 1001, 8:60–9:2. Looking to the disclosure of Leedy '695, U.S. Patent No. 5,354,695, the reference teaches "[l]ow stress is defined relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being *less than 8×10^8 dynes/cm^2 (preferably 1×10^7 dynes/cm^2) in tension*." Ex. 1006, 11:33–37 (emphasis added).

2. "substrate" (claims 33 and 34)

Patent Owner asserts that the plain and ordinary meaning of the term "substrate" is "the underlying material upon which a device, circuit, or epitaxial layer is fabricated." PO Resp. 44. According to Patent Owner, this proposed construction is consistent with the '233 patent because the claim language recites "first, second and third substrates each having integrated circuits formed thereon." *Id.* (citing Ex. 1001, claim 22).

In its Reply, Petitioner responds that the term "substrate" includes "all forms of structural support for integrated circuits" and should not be limited to an "underlying" structure because the embodiments disclosed in the '233

patent include circuits formed vertically through a substrate. Reply 4–6 (citing Ex. 1001, Fig. 4, 10:11–14). Additionally, Petitioner refers to Patent Owner's Exhibit 2146 as describing circuit components embedded within or buried under the epitaxial substrate, not just on its surface. *Id.* at 6 (citing Ex. 2146, 414, 632, 636–37, 640). Further, Petitioner asserts that Patent Owner conceded during prosecution that the term "substrate" includes the circuit membranes disclosed in Leedy '695 (e.g., circuit membrane 160a, 160b, 160c). Reply 6. We understand Petitioner's argument to be that Patent Owner's statements or actions during prosecution constitute an admission that the meaning of "substrate" includes the circuit membrane described in Leedy '695.

Based on the complete record, we adopt Patent Owner's construction with the modification that the term "substrate" is not restricted to *underlying* structures. At the Oral Hearing, Patent Owner clarified that its proposed construction included fabricating below, above, or through a "substrate." Tr. 65, 53:22–54:7. Patent Owner's clarification is consistent with the disclosure in the '233 patent, which teaches forming vertical components of circuits through substrates. Ex. 1001, 11–15.

Accordingly, under the broadest reasonable interpretation, we construe the term "substrate" to mean the "material on or in which a device, circuit, or epitaxial layer is fabricated."

B. Grounds Under 35 U.S.C. § 103

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a

person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). 35 U.S.C. § 103. The ultimate determination of obviousness under § 103 is a question of law based on underlying factual findings. *In re Baxter Int'l, Inc.,* 678 F.3d 1357, 1362 (Fed. Cir. 2012) (citing *Graham v. John Deere Co*., 383 U.S. 1, 17–18 (1966)). These underlying factual considerations consist of: (1) the "level of ordinary skill in the pertinent art," (2) the "scope and content of the prior art," (3) the "differences between the prior art and the claims at issue," and (4) "secondary considerations" of non-obviousness such as "commercial success, long-felt but unsolved needs, failure of others, etc." *KSR*, 550 U.S. at 406 (quoting *Graham,* 383 U.S. at 17–18).

We analyze the asserted grounds based on obviousness with the principles identified above in mind.

2. Level of Skill in the Art

Petitioner's declarant, Dr. Paul D. Franzon, testifies that a person of ordinary skill in the art at the time of the invention would have had at least a bachelor's degree in electrical engineering, material science, or equivalent thereof, and at least 3–5 years of experience in the relevant field, e.g., semiconductor processing. Ex. 1002 ¶¶ 53–54; Pet. 12. Patent Owner does not dispute Petitioner's assessment. *See* Tr. 161:21–25, 112:5–14. We adopt Petitioner's proposed level of skill in the art, which is consistent with the '233 patent and the asserted prior art. For example, the '233 patent is directed to stacked integrated circuits and Leedy '695 is directed to methods for fabricating integrated circuits from membranes formed of low stress dielectic materials. Ex. 1001, 1:23–24; Ex. 1006, Abstract.

3. Claims 33 and 34 – Obvious over Matsumoto, Bower, and Leedy ’695

i. Summary of Leedy ’695 (Ex. 1006)

Leedy ’695 relates to the fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and semiconductor materials. Ex. 1006, 1:38–41. In the Abstract, Leedy ’695 indicates that the disclosed integrated circuits are fabricated from flexible membranes “formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers.” *Id.* at Abstract. Leedy ’695 also discloses forming a “tensile low stress dielectric membrane” on a semiconductor layer as part of its integrated circuit structure. *Id.* at 1:53–58. Leedy ’695 further defines “[l]ow stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8 x 10^8 dynes/cm^2 (preferably 1 x 10^7 dynes/cm^2) in tension.” *Id.* at 11:33–37. Additionally, Leedy ’695 discloses two chemical vapor deposition (CVD) process recipes for manufacturing “structurally enhanced low stress dielectric circuit membranes.” *Id*. at 11:51–65. Referring to Figure 8, Leedy ’695 discloses a three dimensional circuit membrane. *Id.* at 4:43. Figure 8 is reproduced below.

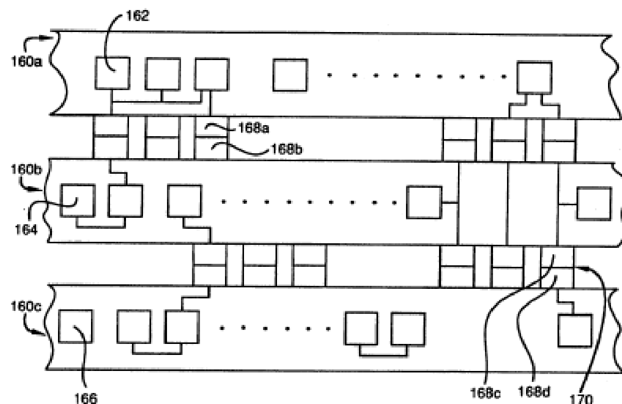

Fig_8

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three dimensional circuit structure. *Id.* at 16:38–40. Interconnection between circuit membranes 160a, 160b, 160c including SDs 162, 164, 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between 4 µm and 25 µm in diameter) on the surface of two circuit membranes 160b, 160c and using a mechanical or gas pressure source to press bond pads 168c, 168d together. *Id.* at 16:43–49.

ii. Summary of Matsumoto (Ex. 1013)

Matsumoto relates to three-dimensional LSI (Large Scale Integration) technology based on a wafer bonding technique using micro-bumps. Ex. 1013, 3. Figure 2 is reproduced below.

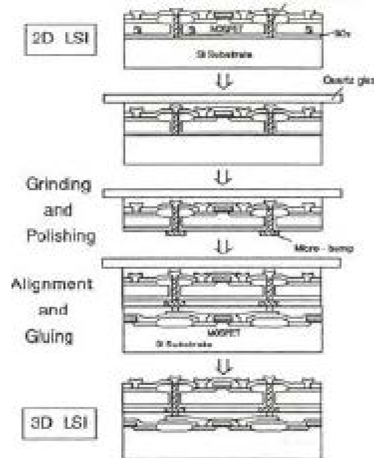

Fig.2 Fabrication sequence of 3D LSI.

Figure 2 illustrates the fabrication process sequence for fabrication of a three dimensional image processing LSI. Ex. 1013, 3. As shown in Figure 2, a 2D LSI wafer with buried interconnections is used as a starting wafer for the 3D LSI. *Id.* The buried interconnections are formed by depositing n+ poly-

Si into trenches. *Id.* The 2D LSI wafer is then glued to a quartz glass and thinned by grinding and polishing. *Id.* The thinned wafer is bonded to a thick wafer through micro-bumps and a UV hardening adhesive layer is inserted between the two wafers to enhance bonding. According to Matsumoto, "3D LSI can be fabricated by repeating such sequence." *Id.*

iii. Summary of Bower (Ex. 1014)

Bower describes a process for direct bonding similar or dissimilar materials at low temperatures in which a material surface is rendered hydrophilic and reactive by creating nitrogen based radicals on the surface, the surface is direct bonded to a second surface. Ex. 1014, Abstract. Bower discloses bonding two surfaces by "combining a nitrogen based constituent with an activator to render a surface both hydrophilic and reactive at low temperatures." Ex. 1014, 2:12–15. In one example, Bower discloses that "pure silicon or titanium can be rendered hydrophilic and reactive by subjecting the material to a plasma of NH_3 . . . . Once the materials are rendered hydrophilic and reactive in this manner, the materials can be brought into physical contact at room temperature to form an initial bond, and thereafter annealed at a temperature below approximately 500° C …." *Id.* at 2:15–26. Bower further teaches that the described process "can be applied to planarized surfaces of 'completed' integrated circuit chips and wafers." *Id.* at 3:11–12. Bower also teaches that "organic glues and indium bumps have been used" previously, but that both have "limitations" compared to low temperature nitride bonding. *Id.* at 3:17–20.

iv. Analysis

Petitioner argues that claims 33 and 34 are obvious over the combination of Matsumoto, Bower, and Leedy '695. *See* Pet. 3. For this

challenge, Petitioner argues that Matsumoto discloses first, second, and third substrates each having integrated circuits formed thereon. Pet. 43. Referring to Figure 1 of Matsumoto, Petitioner argues Matsumoto discloses stacking four integrated circuit wafers to form a 3D integrated circuit structure. *Id.* (citing Ex. 1013, 1073; Ex. 1002 ¶ 124). Petitioner argues that each "2D wafer" is a substrate having integrated circuits formed thereon. *Id.*

Petitioner further argues that one of ordinary skill in the art would have been motivated to apply the direct bonding method disclosed in *Bower* to the three-dimensional image sensor device disclosed by *Matsumoto* by modifying Matsumoto's stack "such that titanium-nitride ('TiN') bond pads are used to form the vertical interconnection (in place of micro-bumps), and silicon nitride bonds are used to bond the remaining surfaces (in place of an adhesive layer)." Pet. 47; *see id.* at 40–41 (citing Ex. 1014, 3:11–13; 3:17–20; Ex. 1002 ¶ 109). Petitioner further notes that Bower discloses the "benefits of applying its direct bonding technique—the formation of a strong bond at low temperature—to the integration of electronic circuitry." Pet. 41 (citing Ex. 1014, 1:64–67).

Additionally, Petitioner argues that the combination of Matsumoto, Bower, and Leedy '695 discloses that "the circuitry are formed with a low stress dielectric" limitation recited in claim 33, and "the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have a stress of about 5×10^8 dynes/cm^2 or less" limitation recited in claim 34 (which depends from claim 33). Pet. 52–57. With respect to these limitations, Petitioner acknowledges that neither Matsumoto nor Bower discloses a low stress dielectric. Pet. 56. However, Petitioner argues

Matsumoto discloses the use of a dielectric layer in forming its

> integrated circuit. *See* Ex. 1013 at 1073 ("The buried interconnections are formed by depositing n+ poly-Si into trenches which are formed through the field oxide."); Fig. 2; Ex. 1002 at ¶127. This is one of two types of "low stress dielectric" described in the '233 Patent. *See* Ex. 1001 at 8:61-9:2 (describing silicon dioxide). Similarly, Bower also discloses the use of a silicon nitride dielectric layer overlying at least the first substrate. *See* Ex. 1014 at 3:21-28; Ex. 1002 at ¶127. This is the second of the two types of "low stress dielectric" described in the '233 Patent. *See* Ex. 1001 at 8:61-9:2 (silicon nitride).

Id. Further, Petitioner argues that there are several reasons one of ordinary skill in the art would have combined the references with a reasonable expectation of success of achieving the claimed inventions recited in claims 33 and 34. *Id.* at 52–57.

For the reasons that follow, we determine that Petitioner has not demonstrated by a preponderance of the evidence that one of ordinary skill in the art would have had a reason to combine the references in the manner proposed by Petitioner to arrive at the claimed invention, or would have had a reasonable expectation of success.

1. Reason to Substitute

To start, Petitioner contends that the Office has previously found that Leedy '695 discloses the subject matter of claims 33 and 34, and that Patent Owner (Applicant at the time) did not dispute the Examiner's findings. Pet. 56–57 (citing Ex. 1017, 690, 709–712, 728, 739–760, 782–784, 979–980). Petitioner, however, does not acknowledge, much less address adequately, the significant difference in the record before the Office, which lacked the testimonial evidence of the Petitioner's expert, Paul D. Franzon, Ph.D. (Ex. 1002 (declaration); Ex. 2164 (deposition transcript)) and testimonial evidence of Patent Owner's expert, Alexander D. Glew, Ph.D. (Ex. 2166

(declaration)). Thus, we are not persuaded that the relied upon sections of the prosecution history are controlling in this instance.

Next, Petitioner refers to many general benefits and advantages of Leedy ’695’s disclosed dielectric, but does not explain how these advantages apply to the specific dielectric materials of Matsumoto or Bower. For example, Petitioner asserts that

> having a low tensile stress dielectric layer in a stacked integrated circuit device allows the layer “to withstand a wide range of IC processing techniques and processing temperatures … without noticeable deficiency in performance.” Ex. 1006 at 2:37-40. *Leedy ’695* explains the alleged importance of having low tensile stress as follows: “If the membrane is not in tensile stress, but in compressive stress, surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane.” *Id*. at 5:63-6:5; Ex. 1002 at ¶95. Thus, in light of the potential benefits disclosed by *Leedy ’695*— including improved surface flatness, improved ability to cope with subsequent high-temperature processing steps, lower dielectric film stress, and improved structural integrity—a person of ordinary skill in the art would have been motivated to apply the low-stress dielectric deposition techniques disclosed in *Leedy ’695* to manufacture the stacked integrated circuit structures disclosed in *Matsumoto* and *Bower*. *See* Ex. 1002 at ¶95.

Pet. 53.

We first observe that Petitioner incorrectly attributes benefits of the entire Membrane Dielectric Isolation (MDI) process to the single low stress dielectric component. Pet. 53 (citing Ex. 1006, 2:37–40, 5:63–6:5). Column 2, lines 37 through 40 of Leedy ’695, which is cited on page 53 of Petition, provides the “[flexible thin film free standing dielectric] *membrane* is able to withstand a wide range of IC processing techniques and processing

temperatures (of at least 400° C.) without noticeable deficiency in performance." Emphasis added. Further, column 5, line 63 through column 6, line 5 states that

> [t]here are many established methods for forming thin semiconductor substrates or membranes. The MDI process requires that the semiconductor membrane forming process (thinning process) produce a highly uniform membrane typically less than 2 μm thick and that the surface tension of the semiconductor membrane be in low tensile stress. If the *membrane* is not in tensile stress, but in compressive stress, surface flatness and *membrane* structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing *membrane*.

Emphasis Added. Here, Leedy '695 indicates explicitly that the ability to withstand high temperature processes is attributed to the *membrane* and not solely to the dielectric that is a component of the membrane. Ex. 1006, 2:37–40. Similarly, Leedy '695 advises that if the *membrane* is in compressive stress, surface flatness and *membrane* structural integrity will be inadequate. Thus, the probative value of Petitioner's argument is diminished because these cited sections of Leedy '695 do not support Petitioner's position that the low stress dielectric imparts the advantages attributed to the membrane structure or membrane isolation techniques.

We further observe that paragraph 95 of Dr. Franzon's testimony largely mirrors the Petition, but adds the following:

> It is worth noting that Matsumoto shows that the ID-VD characteristics of MOS transistor were slightly different after stacking compared with before stacking. *See id.* at Fig. 8. Although the authors do not discuss why, one possible reason is the changed transistor channel strain caused by the stress being different after bonding as compared with before. One possible solution might have been to implement the low-stress dielectric

> deposition technique disclosed by Leedy ’695 to the stacked integrated circuit structures disclosed in Matsumoto.

Ex. 1002 ¶ 95. Here, Dr. Franzon’s testimony does not cite to Matsumoto or any other source that supports this opinion. Even in referring to Figure 8 in Matsumoto, Dr. Franzon acknowledges that Matsumoto does not disclose why the ID-VD characteristics of MOS transistors were shown to be slightly different, or that this is a problem. Dr. Franzon speculates that the difference could be attributed to strain that possibly could be resolved by a low stress dielectric, but does not explain how strain contributes to the ID-VD difference, and, more importantly, why and how one of ordinary skill in the art would have viewed the low stress dielectric deposition technique in Leedy ’695 as a solution to this potential problem. Thus, in this regard, we determine Dr. Franzon’s testimony is entitled little weight. *See In re Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) (“[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.”); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Further, even assuming that Dr. Franzon is correct in his assessment, we note that Petitioner did not present these arguments in its Petition, and we decline to adopt these arguments on behalf of the Petitioner. *In re Magnum Oil*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (indicating that the Board is not free “to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR. Instead, the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.”).

Additionally, Petitioner's reliance on express reasons that low tensile stress is important for Leedy '695's process for constructing Leedy '695's low tensile stress dielectric membranes (e.g., surface flatness) has minimal probative value in supporting Petitioner's proposed substitution with Matsumoto, which is fabricated in a different process relying on a conventional, rigid substrate. *See* Ex. 1013, Figure 2. This is because Petitioner does not explain sufficiently why or how the importance of low tensile stress for Leedy '695's process for constructing low tensile stress dielectric membranes bears on why one of ordinary skill in the art would have substituted Leedy '695's dielectric material for the purported dielectric layer in Matsumoto. For example, Petitioner does not argue that Matsumoto's dielectric layer experiences surface flatness or other structural problems that would be improved by the use of a low stress dielectric, or how this substitution would be accomplished in light of the fabrication processes disclosed in Leedy '695. *See* Pet. 53–57.

Petitioner also does not explain why or how the importance of low tensile stress in Leedy '695's process bears on why one of ordinary skill in the art would have substituted a low stress dielectric for the bonding material in Bower. *See* Pet. 55 ("Bower also discloses the use of a silicon nitride dielectric layer overlying at least the first substrate. *See* Ex. 1014 at 3:21-28; Ex. 1002 at ¶127."). Indeed, other than relying on the '233 patent's mention of a silicon nitride dielectric, (Pet. 55), Petitioner does not explain how the Bower bonding layer performs as a dielectric material. According to Petitioner:

> *Bower* discloses methods of directly bonding two wafers by "combining a nitrogen based constituent with an activator to render a surface both hydrophilic and reactive at low

> temperatures." Ex. 1014 at 2:12-15. Under this approach, a non-polymeric bond-forming material would cover the entire surface of an integrated circuit chip or wafer. *See id.;* Ex. 1002 at ¶¶102, 124. Specifically, *Bower* discloses that its direct bonding method that "can be applied to planarized surfaces of 'completed' integrated circuit chips and wafers" to replace conventional bonding through "organic glues and indium bumps" to produce a "clean, low temperature" bond that is superior to the bond formed by conventional processes. *See* Ex. 1014 at 3:11-20; Ex. 1002 at ¶109.

Pet. 49.

Nonetheless, turning to column 3, lines 21 through 28, we observe that Bower teaches that TiN complements Si_3N_4 to provide both insulating and conducting surfaces which can be bonded at low temperatures. Even assuming the silicon nitride disclosed has insulating or dielectric properties, Petitioner has failed to explain why one of ordinary skill in the art would have replaced the silicon nitride insulating bonding material described in Bower with Leedy '695's low stress dielectric. For example, Petitioner does not point to any evidence in the record that demonstrates Leedy '695's low stress dielectric material performs any bonding, or that Bower's bonding layer exhibits structural problems that would be improved by the use of a low stress dielectric such as one fabricated by the MDI processes disclosed in Leedy '695.

Petitioner further argues that replacement of one dielectric for another is a matter of simple substitution because the deposition processes disclosed in Bower and Leedy '695 are compatible with each other. Pet. 54 (citing Ex. 1002 ¶ 98). Petitioner additionally asserts that

> each of *Matsumoto*, *Bower*, and *Leedy '695* discloses a stacked integrated circuit device. *See* Ex. 1013 at 1073; Ex. 1014 at 3:11-20; Ex. 1006 at 45:49-53; Ex. 1002 at ¶97. Thus, a person of ordinary skill in the art would have found it obvious to

> combine *Leedy '695* with *Matsumoto* and *Bower* because they are in the same field of technology and attempt to address the same problem of vertically integrating integrated circuit devices. *See* Ex. 1002 at ¶97.

Pet. 54. Dr. Franzon adds that a person of skill in the art would have been motivated to combine Leedy '695 and Bower because Leedy '695 uses anodic bonding to form a 3D structure and Bower discloses bonding of Nitride at a lower temperature. Ex. 1002 ¶ 98.

On this point, Petitioner essentially argues that Matsumoto, Bower, and Leedy '695 were directed generally to similar structures and problems in the semiconductor fabrication arts, and a skilled artisan could have looked at both references to improve upon fabrication processes that are *compatible*. In this regard, we find that Petitioner's "reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they *could* be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention." *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017). While the references need not explicitly provide a reason for the asserted substitution, Petitioner, nevertheless, must explain why a person of ordinary skill in the art would have substituted Leedy '695's low stress dielectric for the specific dielectrics in Matsumoto and Bower. "[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention." *Belden Inc. v. Berk–Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015).

We recognize that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill" (*KSR*, 550 U.S. at 417). Here, however, Petitioner's testimony is conclusory without explaining what types of problems or improvements in "vertically integrating integrated circuit devices" would have motivated one of ordinary skill in the art to make Petitioner's proposed substitution of Leedy '695's dielectric in Matsumoto or Bower's devices. *In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) ("The factual inquiry whether to combine references must be thorough and searching.")). Further, Petitioner does not explain in the Petition what aspects of Leedy '695's process and Bower's process lends support to the conclusion that these processes are compatible, and how that alleged compatibility would have motivated a substitution of Leedy '695 low stress dielectric for the bonding material in Bower.

Moreover, here, too, the probative value of Petitioner's argument is diminished by Petitioner's reliance on Dr. Franzon's testimony in paragraphs 97 and 98 of his declaration. Petitioner cites to paragraph 97 of Dr. Franzon's declaration testimony without further discussing or explaining the relevance of the testimony. Pet. 54 (citing Ex. 1002 ¶ 97). In paragraph 97, Dr. Franzon asserts that

> Leedy '695, Matsumoto, and Bower each discloses a stacked integrated circuit structure, and are all in the same technology field of three-dimensional integration and address similar challenges relating to the stacking of integrated circuit devices.

> Accordingly, applying the process methods disclosed by Leedy '695 to Matsumoto and Bower merely involves the substitution of the Leedy '695 low-stress dielectric film for the dielectric films disclosed by Matsumoto and Bower, which would have yielded predictable results.

Ex. 1002 ¶ 97. Although "any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed" (*KSR*, 550 U.S. at 420), Dr. Franzon's two sentence conclusory assertions lack specifics as to what those similar challenges are, and fail to provide any citations to the references themselves or explanation and analysis as to how these references support his assertions. Thus, we weigh Dr. Franzon's testimony accordingly. *See In re Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); *see also* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

Further, in paragraph 68, Dr. Franzon testifies that "[g]iven that Bower discloses bonding of Nitride at lower temperatures than Leedy '695 and that Leedy '695 discloses a low-stress Silicon Nitride recipe, a person of skill in the art would have been motivated to combine their teachings." Ex. 1002 ¶ 98. Here, essentially Dr. Franzon asserts that Bower's nitride layer to nitride layer bonding process occurs at a lower temperature than Leedy '695's silicon nitride deposition process. *Id.* Even assuming that to be the case, we do not see where in this cited testimony that Dr. Franzon explains why one of skill in the art would have substituted Leedy '695's low stress silicon nitride dielectric for the bonding material in Bower. Rather, Dr.

Franzon argues, as Petitioner does, that Leedy ’695 discloses a “recipe” that could be used in Bower to form a nitride layer in Bower. *Id.* Again, testimony that one of ordinary skill in the art *could have used* the techniques is not sufficient to support Petitioner’s contention that one of ordinary skill in the art would have had a reason to combine the references as proposed by Petitioner in the manner of the claimed invention. *In re Giannelli*, 739 F.3d 1375, 1380 (Fed. Cir. 2014) (indicating that the Board should have determined whether it would have been obvious to modify the prior art apparatus to arrive at the claimed invention and finding the mere capability to do so insufficient).

In Reply, Petitioner contends, without support of expert or citation to law, that “the lack of disclosure of ‘tensile’ dielectrics or how to make a [low tensile stress dielectric, aside from incorporating a § 102(b) reference, indicates that it was trivial to substitute Leedy ’695’s [low tensile stress dielectrics] in place of other dielectrics. Reply 2. We disagree with Petitioner—one does not necessarily follow from the other.

Similarly, we disagree that the record supports Petitioner’s assertions in its Reply that the specific benefits of (1) enhancing structural integrity and surface flatness of stacked circuit structures (Pet. 53; Ex. 1002 ¶¶ 95, 121[5]; (2) reducing likelihood of heat damage (Pet. 53; Ex. 1002 ¶¶ 95–96); and (3) providing a dielectric that can withstand heat from subsequent processing (Pet. 53; Ex. 1002 ¶¶ 95–96) would have motivated the proposed substitution. As discussed above, Petitioner relies on benefits that Leedy ’695 attributes to the entire *membrane* or membrane fabrication process, not

[5] Paragraph 121 of Dr. Franzon is directed to the combination of Leedy ’695 and Hitachi.

to the dielectric alone. *See* Ex. 1002 ¶ 95; *see also* Ex. 1006, 2:9–31, 2:37–40 ("This *membrane* is able to withstand a wide range of IC processing techniques and processing temperatures (of at least 400° C.) without noticeable deficiency in performance."), 3:56–4:13 ((Listing benefits to fabricating an IC with the MDI process), 5:63–6:5 ("If the *membrane* is not in tensile stress, but in compressive stress, surface flatness and *membrane* structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane."), 6:48–58 ("The ability to form large durable temperature tolerant low tensile stress films of both semiconductor and dielectric materials as components or layers of a substrate for the fabrication of integrated circuits and interconnect structures is unique to the *MDI process*. The large free standing semiconductor and dielectric *membrane* substrates of the *MDI process* provide unique structural advantages to lower the cost and complexity of circuit fabrication and enhance the performance of circuit operation."). Accordingly, we determine Petitioner's conclusory assertions in its Reply are insufficient to overcome Patent Owner's well-reasoned and supported arguments.

2. *Expected Success*

In addition, it is Petitioner's burden to demonstrate both "that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so." *Intelligent Bio-Systems, Inc. v. Illumina Cambridge LTD.*, 821 F.3d 1359, 1368–1369 (Fed. Cir. 2016) (citing *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.* 688 F.3d 1342, 1360 (Fed. Cir. 2012).

In considering the record before us, we take into account the complexity of integrated circuit fabrication. Without question, fabrication of integrated circuits is complex technology. No less than four prior art text books, ranging from 600 pages to nearly 850 pages and describing the fabrication of integrated circuits, have been provided as background references, principally in support of the declaration testimony of Alexander D. Glew, Ph.D., Patent Owner's expert. Ex. 1040 (Wolf et al., *Processing for the VLSI Era, Volume 1–Process Technology* (1986)); Ex. 2146 (Wolf, Silicon Processing for the VLSI Era, Volume 2 – Process Integration (1990)); Ex. 2159 (W. R. Runyan & K. E. Bean, Semiconductor Integrated Circuit Processing Technology (1990)); Ex. 2162 (Multi-Chip Module Technologies and Alternatives: The Basics (Daryl Ann Doane & Paul D. Franzon eds., 1993)). Also of record are two other background references of around 100 pages and 650 pages. Ex. 2169 (Handbook of Semiconductor Manufacturing Technology (Robert Doering & Yoshio Nishi eds., 2nd ed. 2008); Ex. 2158 (Peter van Zant, Microchip Fabrication (4th ed., 2000)).

Patent Owner, with liberal citations to those references, other prior art references, and declaration testimony of its expert explaining the same, explains how integrated circuits are fabricated to illustrate the complexity of the process and the detailed planning and decisions required for fabrication. PO Resp. 2–29. According to Dr. Glew, integrated circuit fabrication is a "complex manufacturing process . . . that can be generally divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer

fabrication; and (4) packaging. Ex. 2166 ¶ 23 (citing Ex. 2158, 13[6,7]); *see also* PO Resp. 5 (citing Ex. 2166 ¶ 23; Ex. 2158, 13). In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and then sliced into thin disks called "wafers." PO Resp. 4 (citing Ex. 2166 ¶ 25; Ex. 2158, 13–14). Most helpful is the explanation of different techniques for producing and layering dielectrics (PO Resp. 15–29), including growing dielectrics using thermal oxidation (PO Resp. 17–18), depositing dielectrics (PO Resp. 18–19), and a comparison of thermal chemical vapor deposition (PO Resp. 19) with plasma-enhanced chemical vapor deposition (PO Resp. 20–21).

We understand from the testimony of Dr. Glew and reference citations that a typical fabrication of a semiconductor integrated circuit may include thousands of process steps (Ex. 2166 ¶ ¶ 29–30 (citing Ex. 2158, 14, 29–31, 71)). Explaining different techniques for producing and layering dielectrics, Dr. Glew explains that "different dielectric materials are layered throughout the fabrication process, with each dielectric layer having a different location, each being created at a different stage, and each serving a different specific

[6] We follow Patent Owner's practice of citing to page numbers of the text, rather than the pagination of Exhibit 2158.
[7] We recognize that the text cited by Dr. Glew (Ex. 2158) is the fourth edition and has publication dates of 1984, 1997, and 2000. Dr. Glew relies on this text as supporting his testimony and recognizes the earliest effective filing date claimed by the challenged patent of April 4, 1997. Ex. 2166 ¶ 104. Petitioner does not contend that Dr. Glew's reliance on this text is in error or that Dr. Glew's summary of integrated circuit fabrication is faulty. Nor does Petitioner contend that the general explanation of integrated circuit fabrication found in the text, and used by Dr. Glew to support his testimony, changed between the 1997 edition of the text and the later editions.

purpose." Ex. 2166 ¶ 61 (citing Ex. 2158, 72–73, 79, 81–82); *see generally* PO Resp. 15–29 (discussing different techniques for producing and layering dielectrics). Dr. Glew continues:

> These dielectrics can be produced and layered using a large number of techniques, and the particular technique used will greatly impact the properties of the resulting dielectric (and, therefore, its usefulness for any particular dielectric layer and purpose). For example, dielectric silicon dioxide layers can be produced and applied in hundreds of different ways, each resulting in a silicon dioxide with different properties (and potential uses). (Ex. 2158 at 154; Ex. 2146 at 225, 306; Ex. 2159 at 55).

Ex. 2166 ¶ 62. Thus, selecting a dielectric material involves choosing particular fabrication techniques that are part of an overall fabrication process for a particular integrated circuit.

Turning again to the Petition, Petitioner asserts that

> *Leedy '695* discloses fabrication techniques for low-stress dielectric films that are compatible with "most of the established integrated processing methods for the fabrication of circuit devices and interconnect metallization." Ex. 1006 at 1:50-52. *Leedy '695* provides two process recipes for depositing low stress silicon dioxide and silicon nitride films using Novellus deposition equipment, a common tool in the semiconductor fabrication industry around the priority date of the '233 patent. *See id.* at 11:51-65; Ex. 1002 at ¶96. Thus, a person of ordinary skill in the art would have reasonably expected success from applying the known deposition recipes disclosed in *Leedy '695* to manufacture the stacked integrated circuit structure disclosed in *Matsumoto* and *Bower*. *See id.*

Pet. 54.

Based on the complete record, we determine that Petitioner's arguments and conclusion are insufficiently supported. The fact that Leedy '695 discloses fabrication for low stress dielectric films using Novellus

deposition equipment does not sufficiently support Petitioner's conclusion in view of the complexities of integrated circuit fabrication. Furthermore, Petitioner's assertion that a person of ordinary skill in the art "would have reasonably expected success from applying the known deposition recipes disclosed in *Leedy '695* to manufacture the stacked integrated circuit structure disclosed in Matsumoto and Bower" is not supported by the record. Petitioner's citations to Leedy '695 (Ex. 1006, 1:50–52, 11:51–65) do not on their face, without explanation, support Petitioner's position.

Petitioner's citation to column 1 indicates: "[t]hese membranes permit the application (continued use) of most of the established integrated processing methods for the fabrication of circuit devices and interconnect metallization." Ex. 1006, 1:50–52. In the preceding sentence, Leedy '695 refers to "these membranes," discussed in lines 50 through 52, as "large area free standing membranes . . . [fabricated] from low stress dielectric and/or semiconductor films." *Id.* at 1:44–49. As such, Leedy '695's statements apply to the *free standing membrane*, not solely to the dielectric layer within the *membrane*. At a minimum, Petitioner's reliance on this cited passage requires additional explanation on how this teaching demonstrates one of ordinary skill in the art would have reasonably expected success from the substitution of only the dielectric material from Leedy '695's membrane in Matsumoto's and Bower's structures (e.g., nitride bonding layer).

Petitioner's citation to column 11 similarly requires further explanation regarding how it supports Petitioner's position. Column 11, lines 51 through 65 teach "recipes" for silicon dioxide and silicon nitride. In doing so, Leedy '695 cautions that "[s]mall variations in the parameters of the recipes can produce changes in the material structure, etch rate,

refractive index, surface stress, or other characteristics of the deposited dielectric material.”). Ex. 1006, 11:46–50. Thus, while Leedy ’695 provides recipes for dielectric material for use in its MDI process, Leedy ’695 acknowledges that even small changes to these recipes will change the character of the resulting dielectric. *Id.* This teaching is consistent with the testimony provided by both experts, which weighs against Petitioner’s conclusion that replacing dielectrics in integrated circuit fabrication is a matter of simple substitution.

Specifically, both Dr. Franzon and Dr. Glew agree that dielectrics have different properties and different methods of forming dielectrics in integrated circuit fabrication result in dielectrics having different properties. *See, e.g.,* Ex. 2164 (Dr. Franzon deposition transcript), 69:17–19 (Q. Do the different methods result in different properties of the dielectrics? A. Yes.”); Ex. 2166 (Dr. Glew’s declaration) ¶ 139 (Identifying eighteen properties[8] of dielectrics; testifying that one of ordinary skill in the art would consider many of those factors when choosing a dielectric); *see also* PO Resp. 60–63 (discussing Dr. Franzon’s and Dr. Glew’s testimony); *see also* Ex. 2146 (Wolf Volume 2), 195 (Table 4.4 listing eighteen desired properties of interlevel dielectrics); PO Resp. 28 (citing Ex. 2146, 195); Tr. 125:12–17

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[8] Dr. Glew identifies the following properties of dielectrics: dielectric constant, breakdown of field strength, leakage, surface conductance, moisture absorption or permeability to moisture, stress, adhesion to aluminum, adhesion to other dielectric layers, stability, etch rate, permeability to hydrogen, amount of incorporated electrical charge or dipoles, amount of impurities, quality of step coverage, thickness and uniformity of the film, ability to provide good doped uniformity across a wafer, defect density, and amount of residual constituents that “outgas” during later processing. Ex. 2166 ¶ 139.

(Patent Owner's counsel referencing Ex. 2146, 195 (table of eighteen properties). Dr. Franzon acknowledges dielectric properties should be considered when selecting a dielectric. Ex. 2164 (Dr. Franzon deposition transcript), 59:25–60:2, 61:10–13, 79:25–80:3, 91:8–12); Ex. 2164, 78:23–79:1 (Dr. Franzon testifies that "[t]here is likely quite a long list of factors that go into choosing between them [dielectrics], and an engineer would weigh those using his knowledge and skills."). This weighs against a finding that one of ordinary skill in the art would have had expected success substituting Leedy '695's low tensile stress dielectric material for Matsumoto's or Bower's dielectric materials.

In reviewing Dr. Franzon's testimony, we are mindful of the sentiment that "[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton." *KSR*, 550 U.S. at 421. However, in his deposition, Dr. Franzon responded to many questions about dielectrics by indicating research would be needed to answer the particular question and he did not consider how the different processes would affect dielectric properties, which weighs against a finding that one of ordinary skill would have a reasonable expectation of success in substituting Leedy '695's dielectric. *See* Ex. 2164, 133:5–135:5. For example, an excerpt of Dr. Franzon's testimony is provided below:

> Q. What are some of the differences in the properties of a silicon dioxide grown through plasma-enhanced CVD as opposed to grown through oxidation?
>
> A. I haven't researched a detailed answer to that question. There is many variations on the formulas for these CVDs.
>
> Q. But you understand that there is a difference. Right?

> THE WITNESS: There may be differences, depending on the details of the formulations and the processing parameters and so forth.
>
> Q. What are some of the details of the formulation parameters that you would need to know in order to answer that question?
>
> A. I haven't researched the answer to that question in general, so I would need a variety of references that I can't anticipate in order to properly answer that question.

Ex. 2164, 133:8–134:3; *see, e.g.,* Ex. 2164, 71:9–73:17 ("Q. Do you consider oxidation to be a growth or a deposition? A. I haven't researched that answer to the question. Thermal oxidation [requires] oxygen atoms in contact with the surface, at least, in order to grow the thermal oxide. But there's a lot of variance on thermal oxide techniques that I haven't researched. Q. And can you give me an example of some variants in thermal oxide techniques? A. One example that comes to mind is a wet oxide deposition versus a dryer one. Q: And does a wet oxide deposition versus a drier one cause different arrangements of the bonds in silicon dioxide? A: I haven't researched the answer to that question. . . . Q: Do you know if wet oxide versus dry oxide would affect the dielectric constant of silicon dioxide? A. I haven't researched the answer to that question. Q. Do you know if PDCVD [sic] would result in a different dielectric constant than thermal oxide? A. I haven't researched the answer to that question.").

We are not suggesting that a reasonable expectation of success in the complex field of integrated circuit fabrication would preclude one of ordinary skill in the art from researching aspects of making the combination. Rather, we find the number of Dr. Franzon's responses that research is required weighs against Petitioner's conclusory assertions in this regard,

which were discussed previously. *See, e.g.,* Ex. 2164, 71:9–73:17, 73:18–74:4, 24:6–22, 65:10–14, 129:7–9, 130:17–25, 134:20–25; Pet. 52– 55. Thus, considering the complex field of integrated circuit fabrication and taking into account the level of ordinary skill in that art as set forth by Petitioner, there is insufficient evidence of record to conclude that ordinary creativity would support a conclusion that one of ordinary skill in the art would have reasonably expected success in substituting Leedy '695's dielectric material for Matsumoto's or Bower's purported dielectrics.

3. Expert Testimony

In general, we weigh Dr. Glew's testimony concerning the reasons why one of ordinary skill in the art would not have had reason to combine these references in the manner proposed by Petitioner more heavily than Dr. Franzon's declaration testimony that one of ordinary skill in the art would have done so and would have had an expectation of success.

Dr. Franzon's testimony, in large measure, is that Leedy '695 identifies advantages of "the disclosed dielectric deposition techniques (Ex. 1002 ¶ 95); that Leedy '695 discloses dielectric deposition processes that are compatible with conventional integrated circuit fabrication methods (*id.* at ¶¶ 96, 98); and all three references are in the same technological field and "address similar challenges relating to the stacking of integrated circuit devices" (*id.* at ¶ 97). Pet. 52–55. Dr. Franzon's testimony, however, does not adequately address why one of ordinary skill in the art would have specifically used Leedy '695's fabrication process to make Matsumoto or Bower's structures with Leedy '695's low tensile stress dielectric as a dielectric layer or bonding nitride layer, which is the combination on which

Petitioner relies for the recited dielectric material characterized by the particular tensile stress claimed. *See id.*

Notably, too, Dr. Franzon does not specify or otherwise explain the "similar challenges relating to the stacking of integrated circuit devices" he refers to in his testimony. Ex. 1002 ¶ 97. We, however, recognize that "any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *KSR*, 550 U.S. at 420. Noting, however, that references are in the same general field and address similar unnamed challenges in the circumstances of this case—involving complex technology of integrated circuit fabrication, we conclude that Dr. Franzon's testimony about the benefits of Leedy '695's general process is insufficient to support Petitioner's position regarding dielectric substitution of particular structures in Matsumoto and Bower. *See In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) ("The factual inquiry whether to combine references must be thorough and searching.")); *InTouch Techs., Inc. v. VGO Commc'ns, Inc.,* 751 F.3d 1327, 1347 (Fed. Cir. 2014) ("While an analysis of any teaching, suggestion, or motivation to combine elements from different prior art references is useful in an obviousness analysis, the overall inquiry must be expansive and flexible.").

In contrast, Patent Owner relies on Dr. Glew's testimony, which is specific as to reasons why one of ordinary skill in the art would not have combined Leedy '695's fabrication process to modify Matsumoto's or Bower's structures. Specifically, for example, Patent Owner relies on

Dr. Glew's testimony that Matsumoto's silicon dioxide field oxide is grown directly on the Si Substrate at high temperatures using thermal oxidation and could not be produced using plasma-enhanced chemical vapor deposition used by Leedy '695. PO Resp. 49–52; Ex. 2166 ¶¶ 127–128. Dr. Glew further testified that one of ordinary skill in the art would understand that Matsumoto's silicon dioxide dielectric could not be deposited using plasma-enhanced chemical vapor deposition described by Leedy '695 "because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining . . . steps[9] without changing its form." Ex. 2166 ¶ 130 (citing Ex. 2169, 29–30). Notably, Dr. Glew testifies that plasma-enhanced chemical vapor deposition (a known technique used by Leedy '695) cannot be used with Matsumoto's techniques because "positive ions present in the plasma can strike and damage the wafer and the exposed active components in and on its surface." Ex. 2166 ¶ 140 (citing Ex. 2159, 139).

We also note the absence of further declaration testimony by Dr. Franzon opposing Dr. Glew's position or otherwise supporting Petitioner's Reply to Patent Owner's Response. For the reasons noted previously, because of the complexity of integrated circuit fabrication, expert testimony is critical to explaining why a reason one of ordinary skill

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[9] Petitioner and Patent Owner dispute what is meant by front-end and back-end processing steps, we are not persuaded that resolving this issue is necessary to determine whether a skilled artisan would have had reason to combine the asserted references in the manner proposed by Petitioner to arrive at the claimed invention, and whether one of ordinary skill in the art would have had a reasonable expectation of success of doing so.

in the art would have had a reason to combine the references as the claims require. *Kinetic Concepts*, 688 F.3d at 1369. This is particularly true in view of Dr. Glew's well-reasoned and supported testimony. Petitioner's attorney-argument in its Reply consists of conclusory statements with insufficiently explained citations to Leedy '695 and other references and is insufficient to establish that one of ordinary skill in the art would have had reason to combine the references in the manner proposed by Petitioner. *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (a petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements").

For example, in Reply to Dr. Glew's testimony supporting Patent Owner Response, Petitioner's attorneys assert that plasma-enhanced chemical vapor deposition dielectrics are compatible with silicon substrates and high temperature processes. Reply 18–23 (citing Ex. 1082, 1006, 1088)). We recognize that sometimes expert testimony is not always necessary. *See, e.g., Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1369 (Fed. Cir. 2012) (indicating expert technology is not always required) (citing *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1240 n.5 (Fed. Cir. 2010) ("However, as we [have] noted . . . 'expert testimony regarding matters beyond the comprehension of layperson is sometimes essential,' particularly in cases involving complex technology. In such cases, expert testimony may be critical, for example, to establish . . . the existence (or lack thereof) of a motivation to combine references." (internal citations omitted)) (alteration in original)). Accordingly, because of the complexity of integrated circuit fabrication discussed above, however, attorney-argument addressing Dr. Glew's well-reasoned and supported testimony does not

persuade us that one of ordinary skill in the art would have had reason to combine the references in the manner proposed by Petitioner or would have had a reasonable expectation of success.

4. Conclusion

As described above, Petitioner in its Petition made arguments as to why one of ordinary skill in the art would be motivated to combine Matsumoto, Bower, with Leedy ’695 to achieve the purported claimed invention and would have had a reasonable expectation of success. Patent Owner provided well-reasoned argument based on testimonial evidence, background references, and prior art references identifying shortcomings in Petitioner’s position. There is evidence from both sides regarding the presence or absence of a reason to combine Matsumoto, Bower, and Leedy ’695 in the manner proposed by Petitioner to arrive at the claimed invention and regarding whether one of ordinary skill in the art would have had a reasonable expectation of success.

Here, Petitioner has the burden to show, by a preponderance of the evidence, a reason why one of ordinary skill in the art would have combined the prior art references to arrive at the invention and why one of ordinary skill in the art would have reasonable expectation of success of combining the references to meet the limitations of the claimed invention. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.,* 821 F.3d 1359, 1367 (Fed. Cir. 2016) (“The reasonable expectation of success requirement refers to the likelihood of success in combining the references to meet the limitations of the claimed invention. . . . [O]ne must have a motivation to combine [the references] accompanied by a reasonable expectation of achieving what is claimed in the

patent-at-issue."). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")).

It is well-settled that identifying a reason to combine references is not confined to a "rigid or mandatory formula[]." *KSR*, 550 U.S. at 419; *see In re Nuvasive,* 842 F.3d 1376, 1383(Fed. Cir. 2016). Moreover, "[w]hile an analysis of any teaching, suggestion, or motivation to combine elements from different prior art references is useful in an obviousness analysis, the overall inquiry must be expansive and flexible." *InTouch Techns., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014). Furthermore, the inquiry cannot be met by conclusory statements but rather must be "thorough and searching." *See In re Nuvasive,* 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee,* 277 F.3d 1338, 1342 (Fed. Cir. 2002) ("The factual inquiry whether to combine references must be thorough and searching.")). Additionally, we must be careful not to allow hindsight reconstruction of references to reach the claimed invention without adequate explanation as to how or why the references would be combined to produce the claimed invention. *See, e.g., Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1368 (Fed. Cir. 2012) (quoting *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 n.3 ("We must still be careful not to allow hindsight reconstruction of the references to reach the claimed

invention without any explanation as to how or why the references would be combined to produce the claimed invention.”)).

We find Petitioner’s arguments regarding its proposed combination to be incomplete. In the context of these cases, it is insufficient to propose incorporating “the material” of Leedy ’695 without providing sufficient detail as to the combined process to produce the claimed combination. We recognize that it is axiomatic that bodily incorporation is not required. *See, e.g., In re Mouttet,* 686 F.3d 1322, 1332 (Fed. Cir. 2012) (“It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of the elements.”). To be clear, we are not suggesting that Petitioner must explain how Leedy ’695’s entire membrane dielectric isolation process would or could be included with Matsumoto’s or Bower’s integrated circuit fabrication process. Rather, we find Petitioner’s explanation to be incomplete because it does not adequately explain how Matsumoto’s (or Bower’s) fabrication process would be changed to use Leedy ’695’s dielectric material, which is formed in a different manner than Leedy ’695’s MDI (membrane dielectric isolation) process. This is necessary, at least, to support a conclusion that one of ordinary skill in the art would have had a reasonable expectation of success of using Leedy ’695’s dielectric material in place of purported dielectric material in Matsumoto or Bower.

For these reasons above, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the challenged claims 33 and 34 are unpatentable over the combination of Matsumoto, Bower, and Leedy ’695.

4. Claims 33 and 34 – Obvious over Leedy '695 and Hitachi

i. Summary of Hitachi (Ex. 1015)

Hitachi "pertains to a semiconductor device suitable to achieve a highly reliable three-dimensional LSI having extremely high integration density." Ex. 1007 ¶ 1. As an example of a "LSI," Hitachi refers to Figure 5 (reproduced below) as showing three-dimensional LSI 21 with eight layers of thin film 19 laminated via connection surface terminals 20. *Id.* ¶ 35.

[FIG. 5]

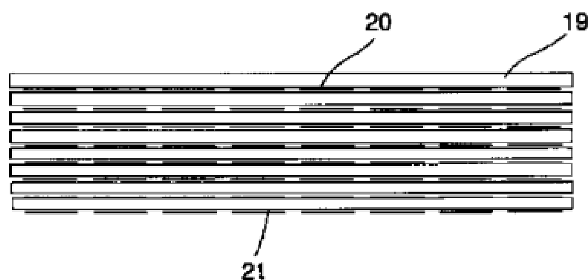
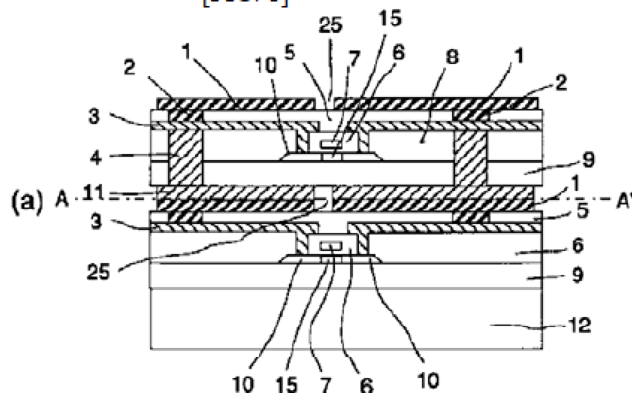


Figure 1 (reproduced below) is a cross sectional view showing an example of embodiment in which two layers of LSIs were laminated.

[FIG. 1]



In Figure 1, front connection surface terminal 1, consisting of a gold (Au) film formed on the upper surface, of the first transistor arranged below was connected to back connection surface terminal 11, consisting of a gold film formed on the back surface, of the second transistor arranged above. Front

connection surface terminal 1 and back connection surface terminal 11 were all planar; both connection became a surface connection, so the contact area was very large. *Id.* ¶ 14. Wirings 3 of the first and the second LSI were connected to front connection surface terminal 1 via a conductive film filled in surface through-hole 2 formed in surface insulating film 5, and wiring 3 of the second LSI arranged on the upper part was connected to back connection surface terminal 11 via a conductive film that further fills the inside of the back surface through-hole 4. *Id.* ¶ 17. Hitachi further discloses that "a highly reliable connection will be achieved as long as the front connection surface terminal 1 and the back connection surface terminal 11 are arranged as densely as possible and the gap between the adjoining connection surface terminals is made small." *Id.* ¶ 20.

ii. Analysis

Petitioner argues that claims 33 and 34 are obvious over the combination of Leedy '695 and Hitachi. *See* Pet. 3. Although Patent Owner has statutorily disclaimed claims 22 and 31 (Ex. 2138), claims 33 and 34 depend from claim 22 and require all the limitations recited in disclaimed claim 22. Thus, we will include the limitations recited in claim 22 in our discussion of claims 33 and 34 below.

Claim 33 is directed to an integrated circuit structure that includes "first, second, and third substrates each having integrated circuits formed thereon" recited in independent claim 22. For this limitation, Petitioner argues that Leedy '695's Figure 8 teaches first (160a), second (160b), and third (160c) substrates. Pet. 27 (citing Ex. 1006 at 16:38–40; Fig. 8; Abstract). Petitioner further asserts that Leedy '695 teaches that each substrate includes active circuit devices (e.g., "SDs 162, 164, 166") formed

thereon. *Id.* (citing Ex. 1006 at 16:40–43, 26:3, Ex. 1002 ¶ 119). Additionally, Petitioner argues that Hitachi also discloses stacking up to eight integrated circuit substrates to form a 3D integrated circuit structure. Pet. 27–28 (citing Ex. 1015 ¶ 35, Fig. 5).

Patent Owner argues that Leedy '695's Figure 8 depicts the vertical bonding of circuit membranes, which Patent Owner argues are not "substrates." PO Resp. 45–46. Patent Owner further asserts that Leedy '233 teaches "fabricating the IC devices on a standard silicon substrate, which is then, in turn, processed, trenched and thinned until all that is left are the discrete, individual transistor-sized islands." *Id.* at 46 (citing Ex. 1006, 3:23–33, 24:20–32, 7:1–28, 9:65–10:40).

In its Reply, Petitioner responds, among other things, that even under Patent Owner's construction, Leedy '695's discloses "substrates." Reply 8. Petitioner first refers to Leedy '695's "Method #2" for fabricating semiconductor devices 24, 26, 28 on a substrate membrane 20. *Id.* (citing Ex. 10:14–30; Figs. 3a–b). Petitioner asserts that substrate membrane 20 remains in the final structure and may be oxidized into a dielectric through an optional isolation process. Reply 8 (citing 8:40–58; 10:4–5, 10:26–30; Figs. 3a–b). Petitioner argues that Figure 3b "is an inverted figure with substrate 20 on top and dielectric layer 36 on the bottom." Reply 9 n.6.

Based on the complete record, we agree with Petitioner that Leedy '695 teaches that a substrate may remain in the integrated circuit, and further may include a dielectric layer. In particular, Leedy '695 describes a Membrane Dielectric Isolation (MDI) process "as two methods, depending on which method of forming the semiconductor substrate thin film is selected." Ex. 1006, 6:59–61.

With respect to "Method #2" of MDI, Leedy '695 generally describes the steps as:

> 1. Form a free standing low stress semiconductor substrate membrane.
>
> 2. Optionally grow the desired epitaxial device layers.
>
> 3. Complete all desired top side IC processing steps including deposition of a low stress dielectric membrane.
>
> 4. Optionally trench isolate the semiconductor device areas from the back side.
>
> 5. Complete IC processing steps on the back side of substrate and remaining top side of substrate.
>
> IC processing steps used on the top side and backside of the semiconductor membrane substrate are well known and not unique in application to the semiconductor substrate membrane; nearly any semiconductor process technique can be applied.

Ex. 1006, 9:64–10:13. Leedy '695 adds that a thin low stress semiconductor substrate membrane 20, such as the one shown in Figure 2, is fabricated prior to deposition of the low stress dielectric membrane and fabrication of semiconductor devices. Ex. 1006, 10:14–17. Leedy '695 further teaches that "[a]fter the semiconductor substrate membrane 20 is fabricated (*see* FIG. 3*a*), semiconductor devices 24, 26, 28, . . . , 30 are fabricated and interconnected on the substrate 20 with the use of low stress dielectric material." Ex. 1006, 10: 26–30. Additionally, we note that Figure 3b shows an enlarged view of the portion of Figure 3a, which includes the presence of "substrate membrane 20," semiconductors 24, 26, 28, and a dielectric layer 36 covering the semiconductor devices. Ex. 1006, 9:27–28, Fig. 3b.

In the case of a vertical three dimensional circuit structure, as shown in Figure 8 of Leedy '695, we understand Petitioner to argue that each circuit membrane (e.g., circuit membranes 160a, 160b, 160c) is a substrate

structure that may include substrate membrane 20 and dielectric layer 36 formed from a MDI method (e.g., Method #2). *See* Pet. 27 (annotated Fig. 8 from Leedy '695) (citing Ex. 1006, 16:40–43, 26:3; Ex. 1002 ¶ 119).

In this regard, applying our construction of "substrate," we determine that each of Leedy '695's circuit membranes serves as a "material on or in which a device, circuit, or epitaxial layer is fabricated" because the three dimensional vertical circuit, described in Figure 8 of Leedy '695, is formed by interconnecting the circuit membranes through compression bonding of surface electrodes 168a, 168b, 168c, 168d (bond pads) on the circuit membranes. Ex. 1006, 16:38–49; *see also id.* at 1:8–10 ("[t]his invention relates to methods for fabricating integrated circuits on and in flexible membranes, and to structures fabricated using such methods."). Leedy '695, teaches that the vertically bonded circuit membrane structure disclosed in Figure 8 is an example of "MDI Circuit Membrane Advantages" in which "[t]he fabrication of circuit membranes provides the capability to fabricate and use integrated circuits in novel ways." Ex. 1006, 15:61–64. To fabricate the three dimensional integrated circuit structure, the circuit membranes are bonded via surface electrodes 168a–d. Our reading of Leedy '695 is consistent with Leedy '695's additional teaching of a method for forming a MOSFET transistor. *See* Ex. 1006, Fig. 10a–d. In this regard, Leedy '695 teaches the use of a "starting *substrate* structure" that is "a combination of silicon and dielectric 204 film forming a membrane 202." Ex. 1006, 16:1–3. Leedy '695 further teaches that "membrane 202 is formed by one of the methods disclosed above," *id.* at 16:3–4, which we understand to include "Method #2." Thus, Leedy '695 itself refers to described membranes as substrates.

Furthermore, our determination that Leedy ’695’s “circuit membrane” is a “substrate” is consistent with the ’233 patent use of the term “substrate,” which does not exclude the material used for a “substrate.” Specifically, the ’233 patent teaches

> The two 3DS memory fabrication methods, however, have a common objective which is the thermal diffusion metal bonding (also referred to as thermal compression bonding) of a number of circuit substrates onto a rigid supporting or common substrate which itself may optionally also be a circuit component layer.
>
> The supporting or common substrate can be a standard semiconductor wafer, a quartz wafer or *a substrate of any material composition that is compatible with the processing steps of the 3DS circuit, the operation of the circuit and the processing equipment used*.

Ex. 1001, 7:35–45 (emphasis added).

In sum, having considered Leedy ’695’s disclosure, the parties’ arguments and evidence, and our construction of the term “substrate,” we determine that Petitioner has demonstrated sufficiently how Leedy ’695’s circuit membranes 160a, 160b, 160c teach substrates, i.e., material in or on which the three dimensional circuit is fabricated/formed through the interconnection and bonding of the bond pads on the surface of the circuit membranes.

We note that we need not determine whether the statements and actions by Patent Owner in the prosecution of the ’233 patent constitute admissions, acquiesce, or disclaimers. We have adopted Patent Owner’s proposed claim construction of “substrate,” and even under this construction, we have determined that Petitioner has presented persuasive arguments and evidence supporting its position that Leedy ’695 discloses first, second, and

third substrates as recited in claim 22 and required in claim 33 (and claim 34). *See* Reply 9–10 ("The '233 Patent is not limited to semiconductor substrates, but describes using 'a substrate of *any material composition*,' including a dielectric 'quartz wafer.' Ex. 1001, 7:41–45.").

Claim 33 further requires through its dependence from disclaimed 22:

> at least one of metal and non-polymeric first bonding layers on the first and second substrates, wherein the first bonding layers comprise bond-forming material on a majority of first surfaces of the first and second substrates that bonds the first and second substrates to each other; and
>
> at least one of metal and non-polymeric second bonding layers on the second and third substrates, wherein the second bonding layers comprise bond-forming material on a majority of a second surface of the second substrate and a first surface of the third substrate that bonds the second and third substrates to each other.

For these limitations, Petitioner argues that Leedy '695 performs "compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads)." Pet. 28 (citing Ex. 1006, 16:40–43). For example, Petitioner provides annotated Figure 8 (reproduced below) to show bond pads between circuit membranes 160a, 160b, 160c.

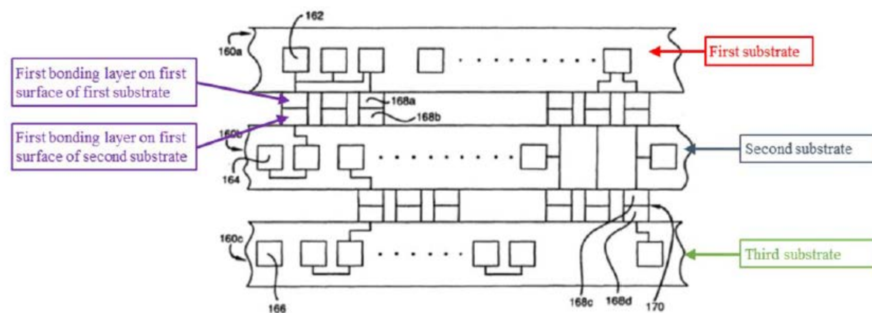
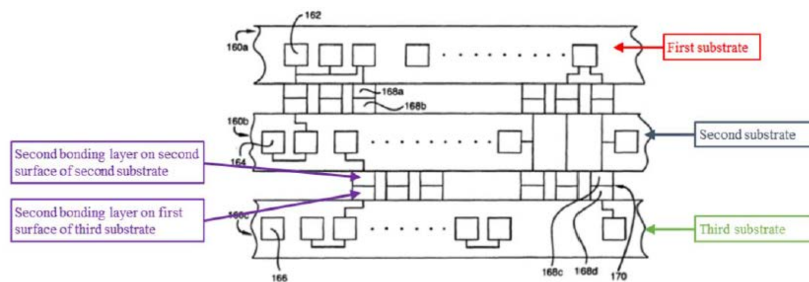


Fig_8



Id. at 28, 33–34. According to Petitioner, Leedy '695 teaches "[b]onding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between 4 µm and 25 µm in diameter) on the surface of two MDI circuit membranes 160b, 160c and using a mechanical or gas pressure source to press the bond pads 168c, 168d together." Pet. 28 (citing Ex. 1006, 16:43–49).

Petitioner adds that Leedy '695 teaches bonding multiple substrates by welding metal solder pads or through thermal compression bonding. Pet. 28 (citing Ex. 1006, 16:51–56). According to Petitioner, "bonding layers 168a and 168b are metal first bonding layers on the first and second substrates (160a and 160b), wherein the first bonding layers comprise bond-forming material that bonds the first and second substrates to each other." Pet. 29 (citing Ex. 1006, Fig. 8; Ex. 1002 ¶ 119). Petitioner further argues that "bonding layers 168c and 168d are metal second bonding layers on the second (160b) and third (160c) substrates." Pet. 32.

Petitioner acknowledges that Leedy '695 does not teach bond-forming material on the *majority* of the first surfaces. Pet. 29. However, Petitioner argues that Hitachi discloses that bond pads 1 and 11 (i.e. "connection surface terminals") form "very large contact areas" and are arranged "as densely as possible" to minimize the gaps between the bonding surfaces.

Pet. 29 (citing Ex. 1015 ¶ 14). Petitioner further relies on the testimony of Dr. Franzon, for the proposition that "[b]y arranging the bond pads 'as densely as possible' with small gaps between, the bond-forming materials would cover more than half of the surface area of the chip." Pet. 30 (citing Ex. 1002 ¶¶ 84–85).

Additionally, Petitioner argues that "a person of ordinary skill in the art would have found it obvious to enlarge the bond pads in the *Leedy '695* structure based on the motivation provided by *Hitachi*." Pet. 31–32 (citing Ex. 1002 ¶¶ 86–88). Petitioner argues that Hitachi teaches maximizing the size of bond pads improves reliability and performance by decreasing thermal and electrical resistance. *Id.* (citing Ex. 1015 ¶¶ 7, 13; Ex. 1002 ¶ 87). Petitioner further asserts that "[i]n light of these benefits, a person of ordinary skill in the art would have been motivated to modify the bond pad design of *Leedy '695* such that the bond-forming material cover a majority of first surfaces of the first and second substrates, and would have reasonably expected success from making this change." *Id.*

Based on the entire record, we determine that Petitioner has explained persuasively how and why a person of ordinary skill in the art would have modified Leedy '695's disclosure of "compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads)," (Pet. 28 (citing Ex. 1006, 16:40–43)) with the enlarged pads shown in Hitachi (Pet. 30–32). Specifically, we determine that Leedy '695 teaches metal bond pads 168a, 168b, 168c, 168d between surfaces of circuit membranes 160a, 160b, 160c (i.e., surfaces of substrates). Ex. 1006, 16:40–43. Additionally, we determine that Hitachi teaches the benefits of enlarged bond pads, which include improving the electrical and thermal conductivity of the

interconnections in a stacked circuit structure. Ex. 1015 ¶ 14. For example, in Hitachi's Figure 1(a) (reproduced below), Hitachi discloses vertically bonding two substrates through two pads – "back connection surface terminal 11" and "front connection surface terminal 1." Ex. 1015 ¶ 14; Fig. 1(a). Hitachi indicates that the contact area between front connection surface terminal 1 and back connection surface terminal 11 "was very large," and that "a highly reliable connection will be achieved as long as the front connection surface terminal 1 and the back connection surface terminal 11 are arranged as densely as possible and the gap between the adjoining connection surface terminals is made small." *Id.* at ¶¶ 14, 20.

With respect to this disclosure, we further credit the testimony of Dr. Franzon, who testifies that

> *Hitachi* explains that its enlarged bond pad design provides multiple benefits, such as improving the electrical and thermal conductivity of the interconnections. Ex. 1015 at [0007], [0013]. In view of the benefits taught by *Hitachi*—such as minimizing contact resistance and improving thermal resistance—a person of ordinary skill in the art would have been motivated to enlarge the bond pad design of *Leedy '695* such that they occupy a majority of the bonding surface, as illustrated in Figure 1(b) of *Hitachi*. *See id.*

Ex. 1002 ¶ 87. In this regard, Dr. Franzon's testimony is persuasive because it comports with and is supported by citations to Hitachi's disclosure of arranging the connection surface terminals "as densely as possible" and to minimize the "gap between the adjoining connection surface terminals." *See Id.* For example, Dr. Franzon cites to paragraph 7 of Hitachi, which teaches the prior art structure disclosed in Figure 2 employs a small connection area between connecting pin 14 and pad 13. Ex. 1015 ¶ 7. With regard to Figure 2, Hitachi teaches that the prior art structures utilized a high bump 14 with a

large gap between adjoining pins 14. *Id.* at ¶ 6. As Dr. Franzon notes, Hitachi explains that an enlarged pad design provides benefits over the prior art (e.g., Figure 2) because "there have been many problems many problems such as increased contact resistance due to a small contact area, causing an unstable operation, increased thermal resistance due to the presence of a gap, and raising temperature, causing difficult high integration." *See* Ex. 1002 ¶ 87; Ex. 1015 ¶ 7. Further, in paragraph 13, also cited by Dr. Franzon, Hitachi teaches that its improved structure has a larger connection area "not only cracks hardly occur due to the generation of local stress in thermal cycles after connection formation, but the contact resistance is also small, eliminating the possibility of unstable contact resistance. The gap between connecting pins does not exist." We further note that the Petition cites to paragraph 20 of Hitachi, which is consistent with the disclosure discussed above and Dr. Franzon's testimony. Pet. 30. Paragraph 20 provides that "a highly reliable connection will be achieved as long as the front connection surface terminal 1 and the back connection surface terminal 11 [(*see* Ex. 1015, Figs. 1a–1b)] are arranged as densely as possible and the gap between the adjoining connection surface terminals is made small".

In weighing Dr. Franzon's testimony, we observe, that in this particular instance and for this specific asserted combination of references, Dr. Franzon has provided and explained the underlying basis for his opinions as well as provided citations to the references to support his testimony. *See* Ex. 1002 ¶ 87. Based on the complete record, this aspect of Dr. Franzon's testimony is consistent with the arguments provided by Petitioner and the citations to the references. Further, while we are cognizant that it is ultimately Petitioner's burden to demonstrate by a

preponderance of the evidence that the challenged claims are unpatentable over this asserted combination, we also recognize that in considering the weight to give to Dr. Franzon's expert testimony, we review the arguments provided by both of the parties, the evidence cited, and the teachings in the references relied upon by Hitachi. We have not been made aware of any reason to doubt Dr. Franzon's testimony with respect to these bonding layer(s) limitations, nor have we determined otherwise that these particular portions of Dr. Franzon's opinion, directed to these limitations, are suspect. Thus, we weigh Dr. Franzon's testimony accordingly and credit his testimony in this regard.

Moreover, we note that while the IC fabrication process is a complex one, it does not follow that the complexity with respect to another obviousness challenge (i.e., obviousness challenge based on the combination of Matsumoto, Bower, and Leedy '695) binds the separate and distinct challenge based on Leedy '695 and Hitachi. For example, unlike Petitioner's other challenge, Petitioner does not assert that a dielectric substitution must be made, with its attendant complexities of fabrication that must be accounted for, into Matsumoto or Bower. Rather, here, in this particular challenge, Petitioner relies on Leedy '695 for its primary integrated circuit structure (e.g., Ex. 1006, Fig. 8) and cites Hitachi for a design change, i.e., enlargement of Leedy '695's existing metal bond pads, that Petitioner argues would have been obvious based on the benefits of enlarged bond pads described in Hitachi. Pet. 22–26. Given the difference in the challenges presented, we do not ascribe the arguments made by either party in one obviousness challenge to another completely separate challenge when the record does not indicate the parties' intentions of doing so. *See In*

re Magnum Oil, 829 F.3d 1364, 1381 (Fed. Cir. 2016) (indicating that the Board is not free "to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR. Instead, the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.").

Additionally, as discussed above, Petitioner relies on Figure 8 of Leedy '695 to show a stacked circuit structure with bond pads between circuit substrate membranes 160a, 160b, 160c. *See* Pet. 29. With regard to Figure 8, Leedy '695 teaches that after the circuit substrate membranes have been formed (e.g., through Method #2), the vertical bonding of two or more circuit membranes form a three dimensional circuit structure. *See* Ex. 1006, 38–40. In other words, the bonding of the circuit membranes is subsequent fabrication processing (i.e., interconnection) that occurs after the circuit membranes have been formed by the MDI fabrication process. *Id.* at 15:63–65 ("The fabrication of circuit membranes provide the capability to fabricate and use integrated circuits in novel ways."). With respect to interconnection, such as that shown between bond pads in Figure 8 of Leedy '695, Leedy '695 further teaches that "[t]hese [circuit] membranes permit the application (continued use) of most of the established integrated processing methods for the fabrication of circuit devices and *interconnect metallization*. Ex. 1006, 1:49:52 (emphasis added). Thus, Leedy '695 indicates that established interconnection metallization processes may be used with the circuit membranes after the circuit membranes are made from MDI fabrication process. *Id.*

Based on the complete record, we determine that Petitioner has demonstrated by a preponderance of the evidence how the asserted

combination of Leedy ’695 and Hitachi teach or suggest the “bonding layer” limitations recited in claim 33 (and claim 34).

Claim 33 further recites “the circuitry are formed with a low stress dielectric.” Petitioner argues that Leedy ’695 discloses “‘methods for fabricating integrated circuits … formed of very thin low stress dielectric materials,’ and applying such methods to ‘3D IC fabrication.’” Pet. 37 (citing Ex. 1006, Abstract). Petitioner further asserts Leedy ’695 discloses forming a “tensile low stress dielectric membrane” on a semiconductor substrate and that low stress dielectric may include “silicon dioxide” or “silicon nitride” formed by deposition. *Id.* at 37–38 (citing Ex. 1006, 1:53–58, 11:33–36; Ex. 1002 ¶¶ 75–77).

Based on the complete record, Petitioner’s position is persuasive and consistent with the disclosure in Leedy ’695, which we determine discloses *low stress* silicon dioxide and silicon nitride deposition recipes for the MDI process. Ex. 1006, 11:25–64 (emphasis added). Accordingly, based on the complete record, we determine that Petitioner has demonstrated by a preponderance of the evidence that the combination of Leedy ’695 and Hitachi would have conveyed to one of ordinary skill in the art the invention recited claim 33.

With respect to claim 34, claim 34 depends from claim 33 and further recites “the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have a stress of about 5×10^8 dynes/cm^2 or less.” Petitioner argues that Leedy ’695 discloses forming a “silicon dioxide” dielectric film that is caused to have a stress of preferably $1 \text{ x } 10^7$ dynes/cm^2. Pet. 38 (citing Ex. 1006, 11:33–37.

Based on the complete record, we determine that Petitioner’s

arguments are persuasive and consistent with Leedy ’695’s disclosure. *See* Ex. 1006, 11:33–37. As discussed above, our construction of a “low stress dielectric” as “a dielectric having a stress of less than 8 x 10^8 dynes/cm^2” takes into account the teaching in the Specification of the ’233 patent that dielectrics in low stress include those that have a stress of less than 5×10^8 dynes/cm^2 and “low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695.” Ex. 1001, 8:60–9:2. Thus, we determine that Leedy ’695 discloses low stress dielectrics with a stress of 1 x 10^7 dynes/cm^2, and teaches that “[l]ow stress is defined relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8×10^8 dynes/cm^2 (preferably 1×10^7 dynes/cm^2) in tension.” Ex. 1006, 11:33–37.

Accordingly, based on a review of the complete record, we determine that Petitioner has demonstrated by a preponderance of the evidence claims 33 and 34 of the ’233 patent are unpatentable over the combination of Leedy ’695 and Hitachi.

III. CONCLUSION

Having considered the parties’ arguments and evidence, we conclude that Petitioner has satisfied its burden of demonstrating, by a preponderance of the evidence, that the subject matter of claims 33 and 34 of the ’233 patent would have been obvious over the combination of Leedy ’695 and Hitachi. Separately, we determine that Petitioner has not met its burden of demonstrating, by a preponderance of the evidence, that the combination of Matsumoto, Bower, and Leedy ’695 would have conveyed to one of skill in the art the claimed inventions recited in claims 33 and 24.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 33 and 34 of the ’233 patent have been shown by a preponderance of the evidence to be unpatentable; and

FURTHER ORDERED that this is a Final Written Decision under 35 U.S.C. § 318(a), and that parties to the proceeding seeking judicial review of the decision under 35 U.S.C. § 319 must comply with the notice and service requirements of 37 C.F.R. § 90.2.

FOR PETITIONER:

John Kappos
Xin-Yi (Vincent) Zhou
Brian Cook
O'MELVENY & MYERS LLP
jkappos@omm.com
PTABMICRONELM@omm.com
PTABMICRONELM@omm.com

Naveen Modi
Allan Soobert
Phillip Citroen
PAUL HASTINGS LLP
PH Samsung ELM IPR@paulhastings.com
PH-Samsung-ELM-IPR@paulhastings.com
PH-Samsung-ELM-IPR@paulhastings.com

Jason Engel
Benjamin Weed
K&L GATES LLP
jason.engel.PTAB@klgates.com
Skhynix-Elm@klgates.com

FOR PATENT OWNER:

Cyrus A. Morton
Kelsey Thorkelson
ROBINS KAPLAN LLP
cmorton@robinskaplan.com
kthorkelson@robinskaplan.com

William A. Meunier
Michael T. Renaud
MINTZ, LEVIN, COHN, FERRIS, GLOVSKY AND POPEO, P.C.
wameunier@mintz.com
mtrenaud@mintz.com

James Carmichael
CARMICHAEL IP, PLLC
jim@carmichaelip.com