IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; AND MICRON CONSUMER PRODUCTS GROUP, INC., DEFENDANTS.	C.A. No. 14-01431-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG ELECTRONICS AMERICA, INC., AND SAMSUNG AUSTIN SEMICONDUCTOR, LLC, DEFENDANTS.	C.A. No. 14-01430-LPS-CJB JURY TRIAL DEMANDED
ELM 3DS INNOVATIONS, LLC, PLAINTIFF, V. SK HYNIX INC., SK HYNIX AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC., AND SK HYNIX MEMORY SOLUTIONS INC., DEFENDANTS.	C.A. No. 14-01432-LPS-CJB JURY TRIAL DEMANDED

DEFENDANTS' OBJECTIONS AND RESPONSES
TO PLAINTIFF'S TECHNOLOGY TUTORIAL

I. INTRODUCTION

Pursuant to Paragraph 10 of the Amended Scheduling Order (D.I. 176 in 14-01430-LPS, D.I. 152 in 14-01431-LPS, D.I. 179 in 14-01432-LPS), Defendants submit these objections and responses to the technology tutorial (D.I. 200 in 14-01430-LPS, D.I. 172 in 14-01431-LPS, and D.I. 201 in 14-01432-LPS) submitted by Plaintiff Elm 3DS Innovations, LLC ("Elm"). Elm's tutorial violates the Court's Order that the "tutorial should focus on the technology in issue and should not be used for argument," not only by arguing the meaning and scope of disputed claim language, but doing so in a misleading manner. Defendants respectfully request that the Court disregard certain passages of Elm's tutorial as set forth below.

II. OBJECTIONS TO ELM'S TUTORIAL

Elm improperly uses its tutorial to argue an overly broad interpretation for the disputed claim term "vertical interconnect" and its variants which appear as follows in the Joint Claim Construction Chart (JCCC) (D.I. 194 in 14-01430-LPS, D.I. 166 in 14-01431-LPS, and D.I. 193 in 14-01432-LPS):

> JCCC Term 6."**vertically interconnected** circuit block stacks" / "**vertically interconnected** circuit blocks";
> JCCC Term 7."a plurality of **vertical interconnect** segments interconnecting the first and second integrated circuit layers, wherein each **vertical interconnect** segment forms an interconnection only between a pair of adjacent integrated circuits";
> JCCC Term 8."said plurality of first interconnection and said plurality of second interconnections are substantially aligned with each other, and said plurality of first interconnections and said plurality of second interconnections are electrically coupled together to form a plurality of **vertical interconnections**, including redundant **vertical interconnections**."

In its tutorial, Elm repeatedly uses the disputed claim term "vertical interconnect" and its variants in a manner inconsistent with the use of that term in the asserted patents. *See*, *e.g.*, U.S. Patent No. 7,193,239 (D.I. 1-1) ("'239 Patent") at 4:13-19 ("The term fine-grain inter-layer ***vertical interconnect*** is used to ***mean electrical interconnect conductors that pass through a***

circuit layer with or without an intervening device element and have a pitch of nominally less than 100 µm and more typically less than 10 µm, but not limited to a pitch of less than 2 µm ….") (emphasis added).[1]

First, as shown below in tutorial slides 47 and 48, Elm depicts prior art 3D structure interconnects, which do not pass through a circuit layer, as "vertical interconnects." *See also* Elm's Tutorial at 8:48-9:02. Elm's characterization thus contradicts the definition of "vertical interconnects" in the asserted patents. *See* '239 Patent at 4:13-19. Thus, Elm's tutorial slides 47-48 and accompanying narration should be disregarded by the Court.

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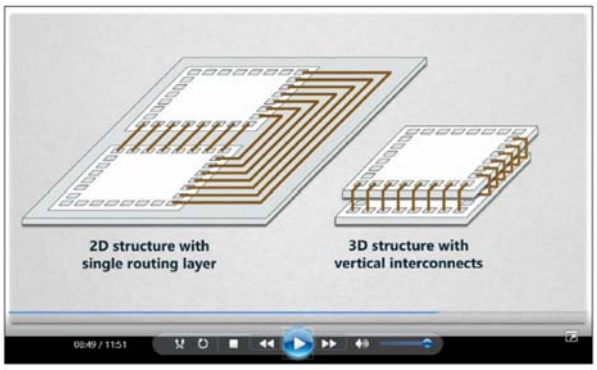
<td> 
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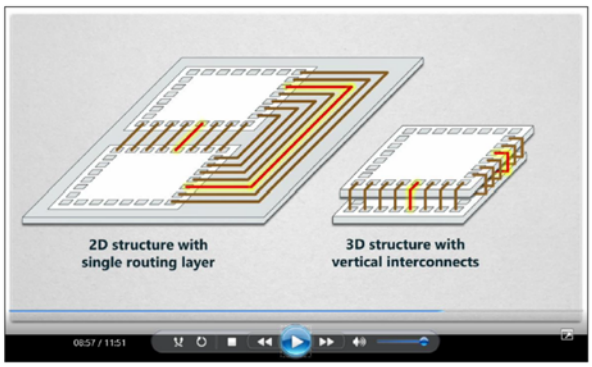
<td> 
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<td>Elm's Tutorial at Slide 47.</td>
<td>Elm's Tutorial at Slide 48.</td>
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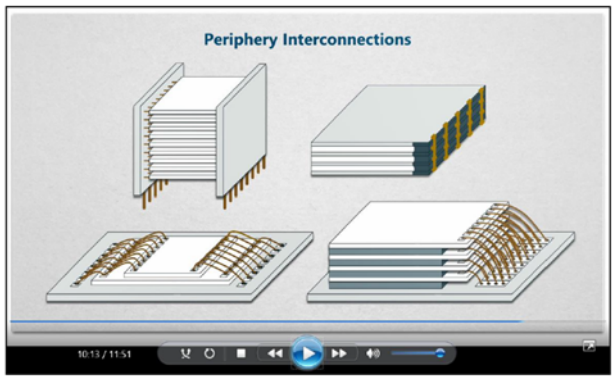
Second, in tutorial slides 51-53 and accompanying narration (*see* Elm's Tutorial at 9:54-10:37) provided below, Elm again uses the claim term "vertical interconnect" in an argumentative and misleading manner to convey a meaning that is inconsistent with that term's use in the asserted patents. For example, in the narration accompanying slide 51, Plaintiff argues for a general interpretation of the disputed claim term untethered to the asserted patents:

> When stacking chips, designers have dozens of **vertical connection** methods at their disposal. These **vertical connection** methods generally fit into two categories.

[1] "Fine-grain" refers to the conductors' pitch, namely "nominally less than 100 µm and more typically less than 10 µm, but not limited to a pitch of less than 2 µm." '239 Patent at 4:13-19.

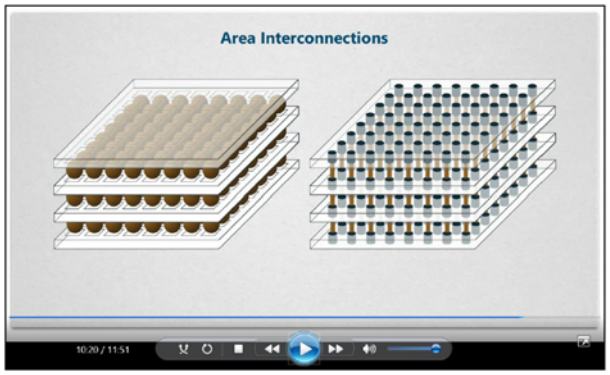
Elm's Tutorial at 9:54-10:04 (narration accompanying slide 51) (emphasis added).

In tutorial slide 52 and accompanying narration, Elm states that "vertical connections" encompass a first category of prior art interconnections which it refers to as "periphery interconnections." But, here again, Elm misleadingly depicts the supposed "vertical interconnections" as electrical conductors that do not pass through a circuit layer, thus contradicting the asserted patents' definition of "vertical interconnect." *See* '239 Patent at 4:13-19. The asserted patents never refer to these prior art interconnects as "vertical interconnects." In fact, the asserted patents distinguish these same prior art interconnects—"interconnect[s] … formed along the outside surface of the circuit stack"—from the claimed "vertical interconnects." *See*, *e.g.*,'239 Patent at 2:34-48 (explaining that these prior art interconnects are "too expensive" in contrast to the "vertical interconnects" in the claimed invention); 3:10-40; 1:66-67; 6:7-9; 6:15-22.

	"Periphery interconnections, such as soldered vertical PC boards, metal films patterned and deposited on the face of a chip stack, and wire bonded stacked chips."
Elm's Tutorial at Slide 52.	Narration at 10:04-10:14 (narration accompanying Elm's Tutorial at Slide 52).

In tutorial slide 53 and accompanying narration, Elm asserts that the disputed term's meaning encompasses a second category of prior art interconnections which it refers to as "area interconnections." In addition to being argumentative, Elm's characterization is misleading because Elm identifies connections which are merely between two layers but do not pass through

a layer, as "vertical interconnects," thus contradicting that term's definition in the asserted patents. *See* '239 Patent at 4:13-19.

	"The second category of **vertical interconnects** are known as area interconnections. Two examples of area interconnections are shown here. The illustration on the left depicts solder ball arrays while the illustration on the right depicts stacked silicon wafers with filled vias. As area interconnections are not restricted to the edges of a substrate, more connections can be made."
Elm's Tutorial at Slide 53.	Narration at 10:14-10:37 (narration accompanying Elm's Tutorial at Slide 53) (emphasis added).

Thus, Elm's tutorial slides 51-53 and their accompanying narration should be disregarded by the Court as being argumentative and misleading.

Elm also improperly uses its tutorial in a subtle yet unmistakable attempt to fill gaps in the disclosure of the asserted patents and rehabilitate the indefinite "stress" terms. These terms appear in the JCCC as:

> JCCC Term 4."have **stress** of about 5×10^8 dynes/cm^2 or less" and variants
> JCCC Term 5."**low stress** dielectric" and variants

As Defendants explain in their claim construction briefing, the "stress" terms are indefinite because, among other things, there are many types of stresses in the context of semiconductor devices and a person of ordinary skill in the art (POSA) would not know with reasonable certainty, from the intrinsic evidence or otherwise, which type of stress is claimed. Defendants' Opening Br. at 11-12. Elm's tutorial (and specifically tutorial slide 57 and accompanying narration) improperly and misleadingly implies that the patents express concern about "curvature caused by the stress of the dielectric" and propose addressing that specific

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